RH850/U2B Group

R01AN6437EJ0100
Rev.1.00

DS-ADC & DFE Application Note

Introduction

This application note summaries the operation example that uses ΔΣAD convertor (hereinafter referred to DS-ADC) and digital filter (hereinafter referred to DFE).

The task the example and application example described in this application note has been confirmed, but please sure to confirm the operation before using it.

Target Device

This document applies to RH850/U2Bx.

【Note 1】When using other than U2B16

Change the microcontroller when using the sample program in this application for other than U2B16. Update the header file and reset the number of the clock frequency.

(1) Select “*****(build tool)” from the project tree

(2) Execute “I/O header file generation”

(3) Select “*****(debag tool)” from the project tree

(4) Select the tab of “Setting for connection”

Set “main clock frequency” of “clock” = “20MHz”

Contents

1. ΔΣAD Convertor － Digital Filter Operation Example

1.1 Specifications

In this application example, A/D converts the voltage injected to DSAN000P pin at a fixed sampling rate to use DS-ADC (DSADC00). The A/D conversion value performs the FIR filtering in DFE ch0 and transfers the filtering result to the local RAM by DTS ch32.

The specifications of this application example are shown below.

- DS-ADC (DSADC00) performs the A/D conversion of analog input voltage continually by the single end inputting and the common voltage “ADSVREFL”.
- A/D conversion value of DS-ADC (DSADC00) entry to DFE automatically.
- DFE filters the input data by the band pass filter constructed by internal FIR filter.
- The filter coefficient and data used for the FIR filter setting are stored RAM in DFE (coefficient memory and data memory).
- The DFE filtering result is not performed decimation processing (thinning).
- DTS ch32 performs DMA transfer the DFE output result to the local RAM.
- DS-ADC startup trigger: Software trigger
- DS-ADC sampling rate: 200ksps
- DFE processing result output rate: 200kHz (No decimation)
- Number of DMA transfers: 200 times
- Input voltage range: 0 ~ ADSVCC (ADSVC: Analog power volage 0 ~ + 5.5V)
- Output data format: 32 bit 32signed fixed-point number

Table 1-1 shows the filter specification example in this application example. The sampling frequency “fs” in this table indicates the data inputted speed to DFE and it means the sampling rate of DS-ADC (200ksps).

Table1-1 Filter Specification Example

Items	Detail
Configuration filter	Band pass filter
Sampling frequency fs	200ksps
Low-pass cutoff frequency f_L	5kHz
High-pass cutoff frequency f_H	15kHz
Passed band ripple R_p	1dB
Stop band attenuation quantity A_p	25dB

Figure 1-1 shows the system configuration.

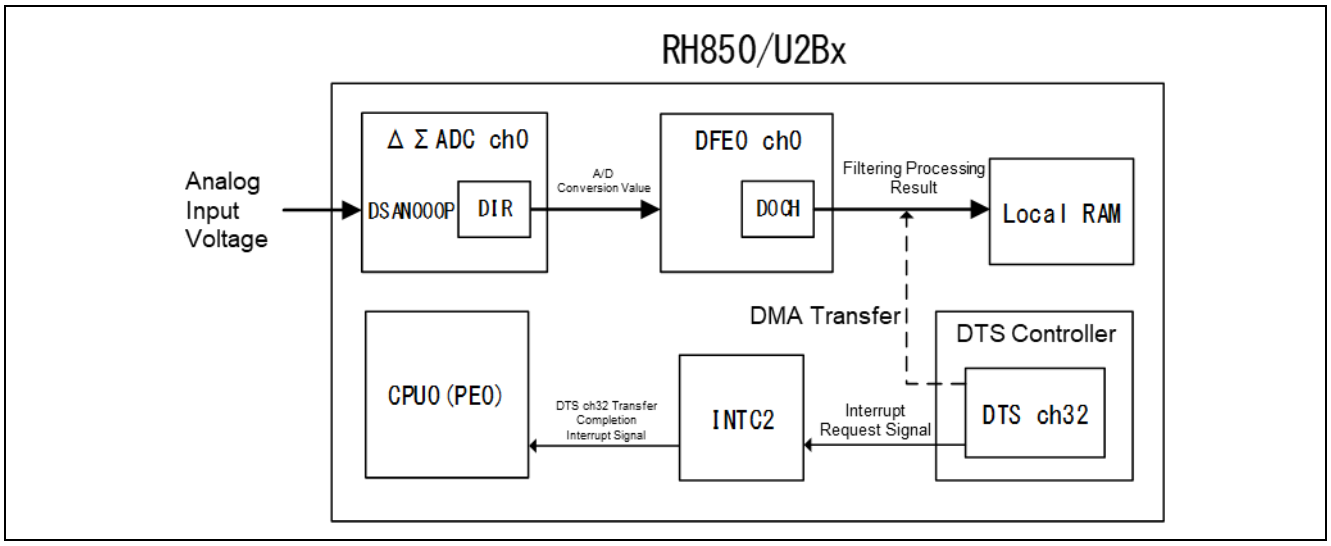

Figure 1-1 System Configuration

1.1.1 Use Function

The used hardware functions of RH/850/U2Bx in this application are shown below.

・ΔΣAD convertor (DS-ADC)	Performs the A/D conversion of analog input voltage.
・Digital Filter (DFE)	Configures the band pass filter by internal FIR filter and performs filtering to the A/D conversion value of DS-ADC.
・DTS controller	DMA transfers the DFE output result to the local RAM.
・Interrupt controller (INTC2)	Controls the DTS ch63-32 interrupt to CPU for transfer complete interrupt request.

1.2 Explanation of Application Example

1.2.1 Operation Explanation

Figure 1-2 shows the operation explanation in this application example. This series of operations is explained separately for hardware processing and software processing.

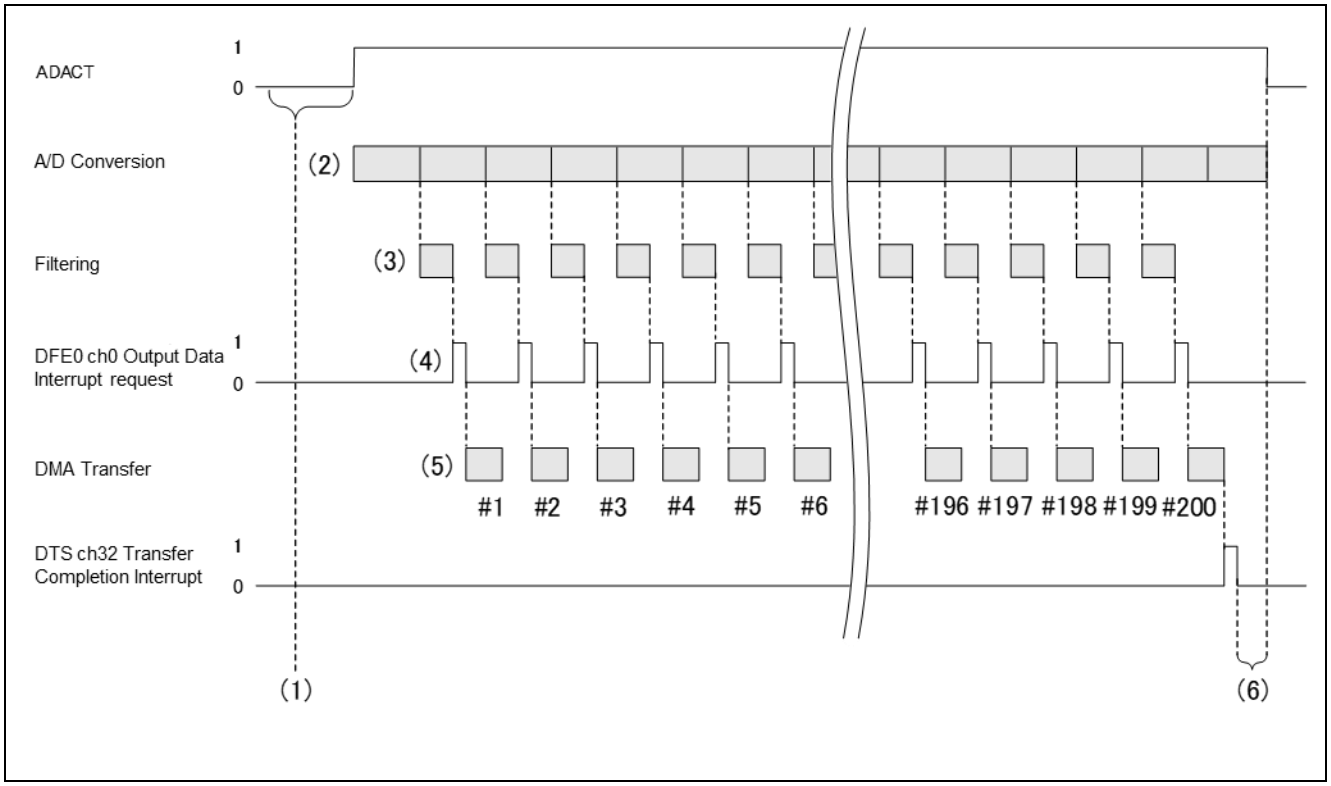

Figure 1-1 Operation Explanation

(1) Software Operation

①Interrupt prohibition

②DS-ADC function initialization

③DFE function initialization

④DTS function initialization

⑤Interrupt function initialization

⑥Interrupt enable

⑦A/D conversion starting of DS-ADC (DSADC00)

(2) DS-ADC (DSADC00) Processing

①DS-ADC (DSADC00) performs the sampling of analog input voltage with 200ksps.

②Entries A/D conversion value to DFE each time A/D conversion ends.

(3) DFE0 ch0 Processing

①The filtering is started by sending the data from DS-ADC (DSADC00) to DFE0 ch0.

(4) DFE0 ch0 Processing

①The filter processing result is outputted and the DFE0 ch0 output data interrupt request is occurred.(*)

*: In this operation example, for occurring the output data interrupt request, the decimation processing is set as execution in the PRCSA bit of control register B and the decimation is not performed by setting the decimation count to "0" in the accumulation/decimation count setting register.

(5) DTS ch32 Processing

①DTS ch32 performs the DMA transmission of filter processing result to the local RAM to trigger the DMA DFE0 ch0 output data interrupt request.

(6) DTS ch32 Processing

①DTS ch63-32 transfers complementation is occurred after completing 200 DMA transfers.

Software Processing (DTS ch63-32 transfer complementation interrupt)

②Stop the A/D transmission of DS-ADC (DSADC00).

③Clears the transfer complementation interrupt of DTS ch32.

1.2.2 Operation Condition of Use Function

Table 1-2 shows the operation condition of used DS-ADC in this application example.

Table1-2 DS-ADC Operation Example

Items	Details
Use channel	DSADC00
Analog input pin	DSAN000P
Sampling rate	200ksps
Over sampling rate	8Msps
DFE entry	Performs
DFE-TAG	0
Gain	×1
Conversion type	Single end input
Common voltage	ADSVREFL
A/D conversion data format	16bit signed fixed-point number
Valid bit	12bit

Table 1-3 shows the operation condition of used DFE in this application example.

Table1-3 DFE Operation Example

Items	Details
Use channel	DFE0 ch0
Channel tag	0
Use filter	FIR
Number of taps	32
Input data format	16bit signed fixed-point number
Coefficient data format	16bit signed fixed-point number
Output data format	32bit signed fixed-point number
Number of decimations	No decimation processing

Table 1-4 shows the operation condition of used DTS in this application example

Table1-4 DTS Operation Example

Items	Details
DTS channel	32
Channel master “SPID”	0
Channel maser ”UM”	Supervisor mode
DTS trigger factor	DFE0 ch0 output data interrupt request
Transmission mode	Single transmission
Source address	DFE0 ch0 output data register (DFDOCH0)
Destination address	Local RAM
Number of transmissions	200 times
Source address count direction	Fixed
Destination address count direction	Increment
Transmission unit	32bit

1.3 Module Setting

1.3.1 DFE Setting

Internal RH850/U2Bx DFE incorporates the FIR filters up to 64taps and IIR filter up to 6th order.

In this operation example, the FIR filter configures the band pass filter. The setting methods of register setting and coefficient memory are shown below.

(1) Coefficient Memory

Stores the filter coefficient of FIR filter to the coefficient memory (CMEM) in DFE. Refers to “1.3.2 Coefficient Memory Setting” for details.

(2) Control Register Settings (Refers to “1.4.4 Register Explanation” for register setting details.)

CTLACH0 Register Setting

- Channel tag: 0
- Filter processing selection: FIR 32tap
- Input data format selection: 16bit fixed point
- Output data interrupt request enable

CTLBCH0 Register setting

- Accumulation circuit processing selection: Selects decimation processing

CTLCCH0 Register Setting

- Input Selection: Selects DS-ADC

ACA Register Setting

- Number of decimation setting: No decimation processing

(3) Channel Activation

CTLACH0.EN is ”1”.

1.3.2 Coefficient Memory Setting

The CMEM data format stores filter coefficient is selectable from the 16bit signed fixed-point format and 16bit integer format. In this application example, the signed fixed-point format is used. The point position of signed fixed-point format is between the 16th and 15th bits. Execute the write access to CMEM with the 32bits. The 16bits access and 8bits access is prohibited.

Table 1-5 shows the filter coefficient calculated from the filter specification example of Table 1-1. In this application example, the filter coefficient is calculated by window method. In Table 1-5, the filter coefficient is mentioned as the 32,768 times integer value (Shift the decimal point position 15 bits to the left) for treating as the 16bit signed fixed-point format.

Table1-5 Filter Coefficient Example

TAP Number (n)	Filter Coefficient (16bit signed fixed-point format)
0	15
1	-13
2	-200
3	-535
4	-965
5	-1405
6	-1747
7	-1889
8	-1752
9	-1304
10	-569
11	373
12	1397
13	2350
14	3085
15	3486
16	3486
17	3085
18	2350
19	1397
20	373
21	-569
22	-1304
23	-1752
24	-1889
25	-1747
26	-1405
27	-965
28	-535
29	-200
30	-13
31	15

1.3.3 Interrupt Setting

In this application example, DTS ch63-32 transfer completion interrupt is used at the completion of DTS ch32 DMA transfer. This interrupt includes the 32 interrupts requests of DTS ch32 to ch63. When the multiple interrupts are occurred to this 32 interrupt request factors, DTS ch63-32 transfer complementation interrupt requests are occurred to the high priority interrupt request. The priority setting of each DTS channels is set by the DTS channel priority setting (DTSPRn). In this application example, “0” is set as the DTS ch32 priority.

1.4 Software Explanation

1.4.1 Function Explanation

Table 1-6 shows the used function in this application example.

Table1-6 Function Explanation

Function Name	Label Name	Processing Detail
Maine function	main_pe0	Performs each function calling and interrupt waiting.
Function for DTS ch63-32 transfer completion interrupts	dst_end_int	Transfer completion interrupt function for DTS ch63-32.
Function for DS-ADC function initialization	ds_adc_init	Performs the initial setting of DS-ADC (DSADC00).
Function for DFE function initialization	dfe_init	Performs the initial setting of DFE0 ch0.
Function for DTS function initialization	dts_init	Performs the initial setting of DTS ch32.
Function for interrupt function initialization	intc_init	Performs the transfer completion interrupt setting of DTS ch63-32.

1.4.2 Use Define Declaration Explanation

Table 1-7 shows the explanation of the used define declaration in this application explanation.

Table1-7 Explanation of Use Define Declaration

Label Name	Function	Setting Value	Use Function Name
TAP_NUM	Number of taps of FIR filter.	32	dfe_init

1.4.3 Use Variable Explanation

Table 1-8 shows the explanation of used variable.

Table1-8 Explanation of Use Variable

Label Name	Function	Data Length	Use Function Name
*cmem0[TAP_NUM/2]	Pointer variable that indicates the coefficient memory of DFE0 ch0.	signed long	dfe_init
smp_data[200]	Stores the output result of DFE.	signed long	dts_Init

1.4.4 Register Explanation

Table 1-9 shows the register setting example of DS-ADC (DSADC00).

Table1-9 Register Setting Example of DS-ADC (DSADC00)

Register Name	Setting Value	Bit Name	Function	Setting Detail
■DS-ADC Common Register				
AD global control register (DSADCADGCR)	0x00	ODDE	Disconnection detective function self-diagnostic	Disable
		ODE	Disconnection detective	Disable
		UNSND	Conversion result output	Signed
Pin level self-diagnostic Control register (DSADCTDCR)	0x00	TDE	Pin level self-diagnostic function	Disable
■DS-ADC Fixed Register				
Unit control register (DSADC00UCR)	0x04000000	VPRSTE	Virtual channel pointer reset	None
		RDMA	Read gate DMA mode	Outputs DMA transfer request for all of A/D conversion result.
		RESO0	High accurate mode	High impedance mode
		DFES	DFE channel selection	Selects DFE0.
		DFMT[3:0]	Data format	No mask
		VCEP[2:0]	End virtual channel pointer	0
Virtual channel control register (DSADC00VCR0)	0x00101000	FSELEXTE	Extension Fs switching bit	No extension
		GAIN[1:0]	Gain	×1
		VCULME	Upper-limit threshold notification	No notification
		VCLLME	Lower-limit threshold notification	No notification
		VCULLMTBS[1:0]	Threshold table selection	DSADCnULTBR0 (Unused)
		ORT	Post filter 2nd stage output rate selection	1/2
		TPVSL[2:0]	TAP coefficient selection	Coefficient 1
		DSDFTYP[3:0]	Post filter type	Depends on ORT and TPVSL setting.
		ADIE	Conversion completion interrupt	Disable

		ULEIE	Upper-limit/Lower-limit interrupt	Disable
		DFENT	DFE Entry	Entry.
		DFTAG[3:0]	DFE-TAG	0
		CNVCLS[1:0]	Conversion classification	Single mode input Common voltage=ADSVREFL
		GCTRL[3:0]	Input pin setting	DSAN000P

Register Name	Setting Value	Bit Name	Function	Setting Detail
AD start control register (DSADC00ADSTCR)	0x01	ADST	Starts A/D conversion.	Conversion starts
AD stop control register (DSADC00 ADENDCR)	0x01	ADEND	Stops A/D conversion.	Conversion stops
AD conversion trigger control register (DSADC00ADTCR)	0x00	ADSTTE	AD synchronization start enable	ADSTART disable
		ENDTRGE	AD end trigger enable	AD end trigger disable
		STTRGE	AD start trigger enable	AD start trigger disable
Virtual channel pointer register (DSADC00VCPTRR)	0x00	VCPTR[2:0]	Virtual channel number during A/D conversion	Clears as 0.
Safety control register (DSADC00SFTCR)	0x00	RDCLRE	Read & clear enable	No clearing
		OWEIE	Overwrite error interrupt	Prohibit
		PEIE	Parity error interrupt	Prohibit
		IDEIE	ID error interrupt	Prohibit
Upper-limit/Lower-limit table register (DSADC00ULTBR0 ～3)	0x7FFF8000	ULMTB[15:0]	Upper-limit table	Unused (Initial value)
		LLMTB[15:0]	Lower-limit table	Unused (Initial value)
Pin level self-diagnostic level register (DSADC00TDLVR)	0x00	AN3NLV	Pin level self-diagnostic specification	Unused (Initial value)
		AN3PLV	Pin level self-diagnostic specification	Unused (Initial value)
		AN2NLV	Pin level self-diagnostic specification	Unused (Initial value)
		AN2PLV	Pin level self-diagnostic specification	Unused (Initial value)
		AN1NLV	Pin level self-diagnostic specification	Unused (Initial value)
		AN1PLV	Pin level self-diagnostic specification	Unused (Initial value)
		AN0NLV	Pin level self-diagnostic specification	Unused (Initial value)
		AN0PLV	Pin level self-diagnostic specification	Unused (Initial value)

Table 1-10 shows the DFE0 register setting example.

Table1-10 Setting Example of DFE0 Register

Register Name	Setting Value	Bit Name	Function	Setting Detail
Control register A (DFE0CTLACH0)	0x00003010 ↓ 0x00003011	CATAG	Tag value for cascade input	0 (Unused)
		CAEN	Cascade enable	No cascade
		CAENL	Cascade enable	No cascade
		TAG	Channel tag	0 (Set value same with AD tag value inputted from AD.)
		CMD	Filter processing selection	FIR 32TAP
		IEF	Filter end interrupt	Prohibit
		FMT	FIR input data format	16bit fixed-point
		IEP	PH end interrupt	Prohibit
		IEE	Error interrupt	Prohibit
		IEC	Matching condition interrupt	Prohibit
		IEO	Output data interrupt	Enable
		CNSL	Matching condition interrupt 0/1 function selection	INT_DFE_CND0 : Selects compare match interrupt request. (Unused) INT_DFE_CND1 : Selects PH end interrupt request. (Unused)
		CNSLE	CNSL enable	Setting prohibition of CNSL
		AIME	Automatic initialization	Prohibit
		EN	Channel enable	Channel enable
Control register C （DFE0CTLCCH0）	0x00000100	CA0E	C-ADC selection	No use
		DAyE	DS-ADC selection	Uses channel0.
		SAyE	SAR-ADC selection	No use

Register Name	Setting Value	Bit Name	Function	Setting Detail
Control register B (DFE0CTLBCH0)	0x01000002	SELB1U	Selection of compare target register	Selects CPA register value as value of compare calculation target value. (Unused)
		SELAU	Selection of calculation/decimation register	Selects ACA value.
		OFSL	Compare offset value “α” selection	Selects DFEjCPOFST0 register value. (Unused)
		DISB	PH processing prohibition	Prohibits PH processing.
		PHPS	PH peak type selection	PH processing detects upper limit peak. (Unused)
		CPCS	Compare value type selection	DFEjCPA～DFEjCPD are selected by DFEjCTLBCHn.SELB1. (Unused)
		PHSLB2	PH initial value register selection	DFEjPHIA register value is selected as initial value of PH processing. (Unused)
		DISA	Calculation /decimation processing prohibition	Calculation/decimation processing prohibition
		PRCSC	Output data register floating-point conversion	Not execute floating-point conversion.
		SELB2	PH initial value register selection	Selects PHIA register value to initial value of PH processing. (Unused)
		SELB1	Compare target register selection	Selects CPA register value to compare calculation target value. (Unused)
		PRCSB	PH circuit processing selection	Not perform PH processing and compare calculation processing.
		HOFS	Middle value output register floating-point conversion	Not execute floating-point conversion.
		PICS	PH index register control selection	PH index update mode
		SELA	calculation/decimation count register selection	Selects ACA value.
		PFMT	PH result register	Not execute

			floating-point selection	floating-point conversion. (Unused)
		ABS	Absolute value calculation	Not calculate absolute value.
		PRCSA	Calculation circuit processing selection	Execute decimation processing.
Output data register (DFE0DOCH0)	-	DO	Output data	Stores calculation result after completing DFE processing.
Calculation/decimation count setting register A (DFE0ACA)	0x0000	AC	Calculation/decimation times	Not calculate and decimate.

Table 1-11 shows the register setting example of DTS ch32.

Table1-11 Register Setting Example of DTS ch32

Register Name	Setting Value	Bit Name	Function	Setting Detail
■Global Register				
DTS channel priority setting 2 (DTSPR2)	0xFFFFFFFC	DTSnPR[1:0] (n=32 to 63)	Priority setting of DTS channel	Set “0” (highest priority) to DTS channel 32 priority.
DTS channel 32 channel master setting (DTS032CM)	0x00000000	CHAIN_ RESTRICT	Chain function limit setting	No limit
		CHAIN_SPID [4:0]	Chain enable SPID setting	0 (Unused)
		CHAIN_UM	Chain enable UM setting	(Unused)
		SPID[4:0]	Channel master SPID setting	Set SPID = 0.
		UM	Channel master UM setting	Supervisor mode
		CMC[15:0]	Transmission time compare	(Unused)
■DTS Channel Register				
DTS Source Address (DTSA032)	(unsigned long)&DFE0.DOCH0	SA[31:0]	Source address	Sets source address to DFE0 ch0 output data register.
DTS Destination Address (DTDA032)	(unsigned long)&smp_data[0]	DA[31:0]	Destination address	Sets destination address to header address of array for sampling data.
DTS Transmission Time (DTTC032)	0x000000C8	ARC[15:0]	Address reload count	(Unused)
		TRC[15:0]	Transition times	Set 200 times to transition times.

Register Name	Setting Value	Bit Name	Function	Setting Detail
DTS transfer control (DTTCT032)	0x00004048	ESE	DMA transfer stop setting when error transfer	Continues DMA transfers.
		CHNSEL[6:0]	Chain destination selection	(Unused)
		CHNE[1:0]	Chain enable	Disable
		CCE	Transfer times match interrupt	Prohibit
		TCE	Transfer completion interrupt	Enable
		RLD2M[1:0]	Reload function 2 setting	Disables reload function 2.
		RLD1M[1:0]	Reload function 1 setting	Disables reload function 1.
		DACM[1:0]	Destination address count direction	Increment
		SACM[1:0]	Source address count direction	Fixed
		DS[2:0]	Transfer data size	32bits
		TRM[1:0]	Transfer mode	Single transition
DTSFSL Operation Setting (DTFSL032)	0x00000001	REQEN	DTS transfer request enable	Set enables to DTS transfer request.
DTS transfer request clear (DTFSC032)	0x000000B1	ERC	Transfer error flag (ER) clear	Clear
		CCC	Transfer count compare flag (CC) clear	Clear
		TCC	Transfer completion flag (TC) clear	Clear
		DRQC	DMA transfer request clear	Clear

Table 1-12 shows the register setting of INTC2.

Table1-12 Register Setting Example of INTC2

Register Name	Setting Value	Bit Name	Function	Setting Detail
EI level interrupt bind register (EIBD63)	0x00000000	CST	Broadcast interrupt port number setting	Prohibit
		BCP[1:0]	Broadcast interrupt port number setting	(Unused)
		PEID[2:0]	Specification of destination binds (request) the interrupt	PE0 (CPU0)
EI level control register (EIC63)	0x0040	EICTn	Interrupt channel type bit	(Possible to read only.)
		EIRFn	Interrupt request flag	(Possible to read only.)
		EIMKn	Interrupt mask bit	Enables interrupt processing.
		EITBn	Interrupt vector method selection	Table reference method
		EIPn	Specification of interrupt priority	0 (Highest priority)

1.4.5 Operation Flow

Figure 1-3 shows the software operation flow in this application example.

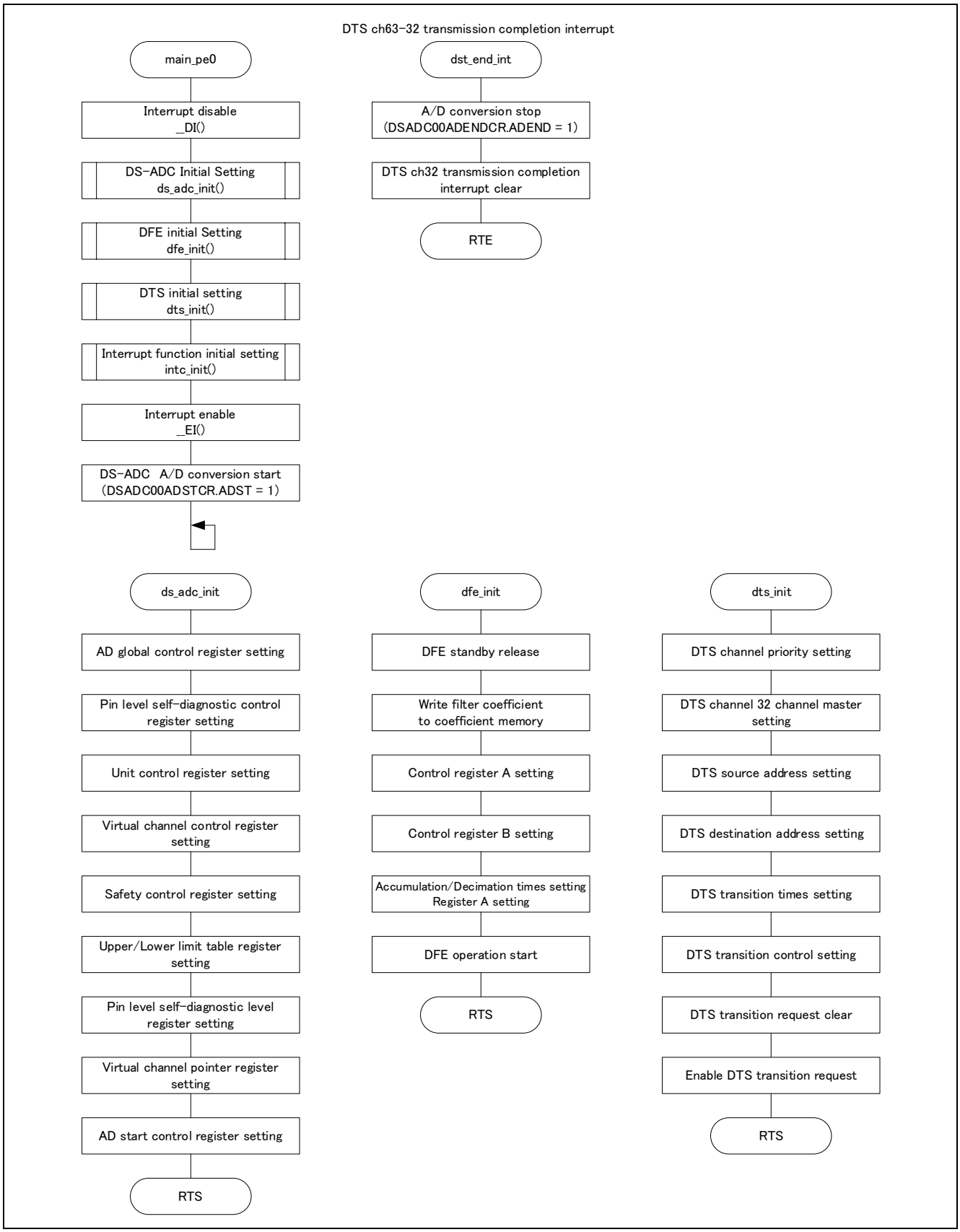

Figure1-2 Software Operation Flow

2. Operation Example of PH23 Processing

2.1 Specifications

In this application example, DS-ADC (DSADC00) is used and the applied voltage to a DSAN000P pin is A/D converted with the constant sampling rate. A/D conversion value applies the filtering by the FIR filter in DFE ch0, performs the peak-hold23 processing to the filtering result, and detects the upper-limit/lower-limit of the filtering result. Store the detected upper-limit PH1/PH3 and lower-limit PH2 to the local RAM. (This application example is the operation added the peak-hold 23 processing to the operation example 1.)

The specifications of this application examples are shown below.

- DS-ADC (DSADC00) A/D-converts the single end inputs and the common voltage ADSVREFL continuously.
- The A/D conversion value of DS-ADC (DSADC00) entries to DFE automatically.
- DFE performs the filtering the input data by the configured band pass filter by the internal FILR filter.
- The filter coefficient and data used for FIR filter setting are stored to RAM in DFE (coefficient memory and data memory).
- The DFE filtering result is not performed the decimation processing.
- DFE output result performs the PH23 processing started the upper-limit detection on PH circuit.
- Regards the timer trigger of timer D treat as the initialization flag and end flag of PH23 processing.
- Captures the count value of timer D by the update of pick hold value.
- Reads the PH23 processing result from the register by CPU and saves it to the local RAM.
- DS-ADC startup trigger: Software trigger
- DS-ADC sampling rate: 200ksps
- DFE processing result output rate: 200kHz (No decimation processing)
- Input voltage range: 0 ～ ADSVCC (ADSVC: Analog power voltage 0 ～ + 5.5V)
- Output data format: 32bits signed fixed-point number

Table 2-1 shows the filter specification example in this application example. The sampling frequency “fs” in the table indicates the inputted data speed to DFE and it means DS-ADC sampling rate (200ksps) in this application example.

Table2-1 Filter Specification Example

Items	Description
Configuration filte	Bandpass filter
Sampling frequency “fs”	200ksps
High-range cutoff frequency “f_L”	5kHz
Low-range cutoff frequency “f_H”	15kHz
Bandpass ripple R_p	1dB
Stopband attenuation A_p	25dB

In this operation example, A/D-converts the applied voltage to DSAN000P pin. Table 2-2 and figure 2-1 shows the specification of the A/D-converted input signal.

Table2-2 Specification of Input Signal

Items	Description
Presumptive input wave	Sine wave
Maximum voltage	5V
Minimum frequency	5kHz
Maximum frequency	15kHz

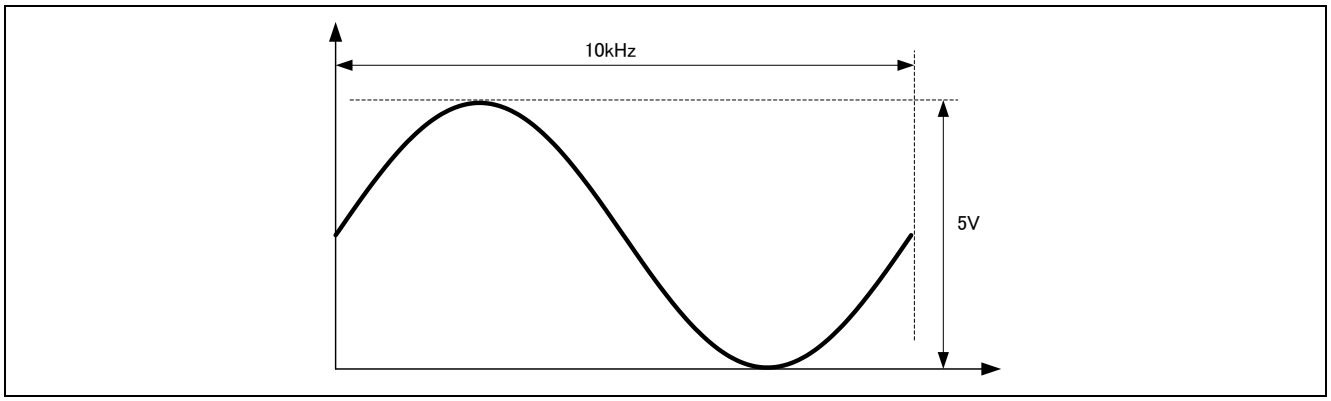

Figure2-1 Input Wave Example

Figure 2-2 shows the system configuration.

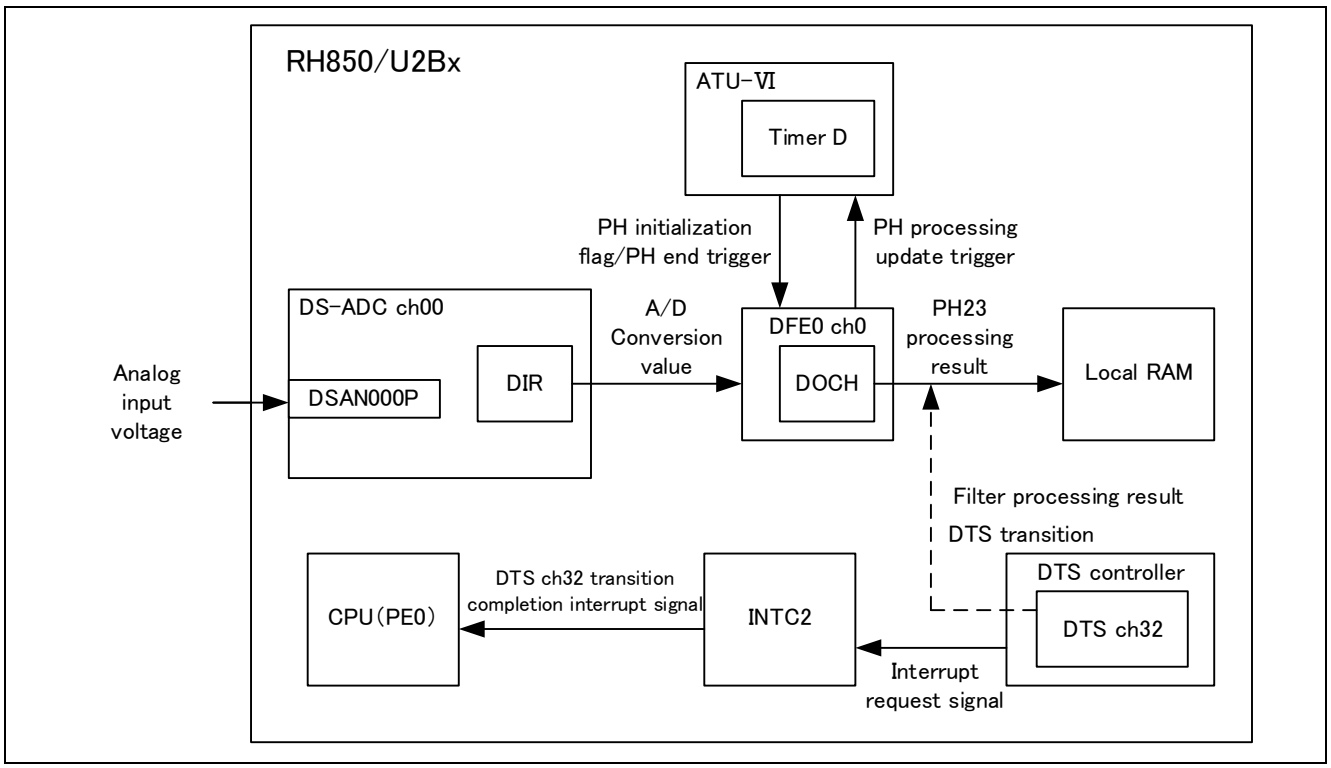

Figure2-2 System Configuration

2.1.1 Use Function

The used RH850/U2Bx hardware functions in this application note are show below.

・ΔΣAD convertor (DS-ADC)	A/D-converts analog input voltage.
・Digital filter (DFE)	Configures bandpass filter by internal FIR filter and applied filtering to A/D conversion value. The filtering result performs PH23 processing and calculates upper-limit/lower-limit.
・ATU-Ⅵ	Supplies the PH23 processing start/end trigger for timer D Synchronizes the peak hold value updates and captures the counter value of timer D.
・DTS controller	DMA-transfers the DFE output result to local RAM.
・Interrupt controller (INTC2)	Controls the DTS ch63-32 transfer completion request and the timer D compere match interrupt to CPU.

2.2 Application Explanation

2.2.1 Operation Explanation

Figure 2-3 shows the operation explanation in this application example. This series of operations is explained separately for hardware processing and software processing.

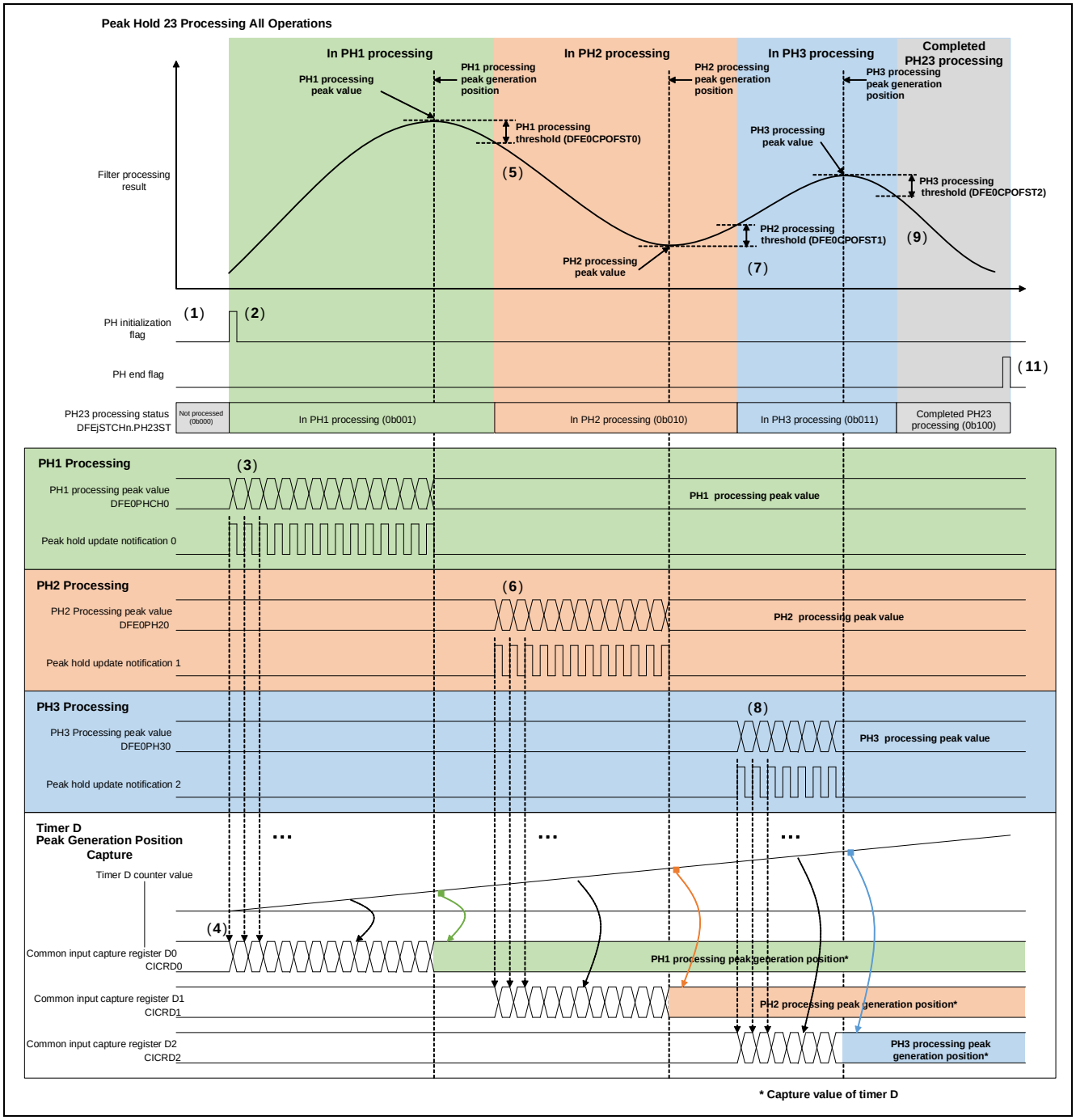

Figure2-3 Operation Explanation

(1) Software Processing

①Interrupt prohibit

②DS-ADC function initialization

③DFE function initialization

④ATU-VI timer D initialization

⑤DTS function initialization

⑥Interrupt function initialization

⑦Interrupt enable

⑧A/D conversion start of DS-ADC (DSADC00)

⑨Starts timer D count-up

(2) DFE Processing

①Stars the PH23 processing for the DFE filter processing result when the PH initialization flag rises.

(3) DFE Processing

①Performs the peak hold processing of upper-limit peak for the filtering result.

②Issues the PH update notification when the peak hold value updating of PH result register.

(4) DFE Processing

①When the peak hold value updating, captures the counter value of timer D
to the capturing result register of timer D.

(5) DFE Processing

①Ends the PH1 processing when the following condition is established.

"Value of PH circuit input data < Value of PH result register n ＋ Comparing offset value (*)"

②Starts the PH2 processing.

(6) DFE Processing

①Performs the peak hold processing of lower-limit peak for the filtering result.

②Issues the PH update notification when the peak hold value updating of PH result register.

(7) DFE Processing

①Ends the PH2 processing when the following condition is established.

"Value of PH circuit input data > Value of PH2 result register 0 + Comparing offset value (*)"

②Starts the PH3 processing.

(8) DFE Processing

①Performs the peak hold processing of upper-limit peak for the filtering result.

②Issues the PH update notification when the peak hold value updating of PH result register.

(9) DFE Processing

①Ends the PH3 processing when the following condition is established.

"Value of PH circuit input data > Value of PH3 result register 0 + Comparing offset value (*)"

(10) Software Processing

①Stores the following value to the local RAM.

- Peak hold value of PH1 processing, Capturing result resister value of timer D
- Peak hold value of PH2 processing, Capturing result resister value of timer D
- Peak hold value of PH3 processing, Capturing result resister value of timer D

(11) DFE Processing

①Ends the PH23 processing by the PH end flag.

*: Sets the comparing offset value by "Comparing offset value register nDFEjCPOFSTn (n=0~2)"

2.2.2 Operation Condition of Use Function

Table 2-3 shows the used DS-ADC operation condition in this application example.

Table2-3 DS-ADC Operation Condition

Items	Descriptions
Use channel	DSADC00
Analog input pin	DSAN000P
Sampling plate	200ksps
Over sampling rate	8Msps
DFE entry	Yes
DFE-TAG	0
Gain	×1
Conversion type	Single end input
Common voltage	ADSVREFL
A/D conversion data format	16bit signed fixed-point number
Enable bit	12bit

Table 2-4 shows the used DFE operation condition in this application example.

Table2-4 DFE Operation Condition

Items	Descriptions
Use channel	DFE0 ch0
Channel tag	0
Use filter	FIR
Number of taps	32
Input data format	16bit signed fixed-point number
Coefficient data format	16bit signed fixed-point number
Output data format	32bit signed fixed-point number
Decimation times	No decimation processing
Peak-Hold processing	Performs the PH processing and comparison simultaneously.
PH initialization flag and end flag	Set to compare match A0/B0 of timer D.

Table 2-5 shows the used ATU-VI(timer D) operation condition in this application example.

Table2-5 ATU-Ⅵ (Timer D) Operation Condition

Contents	Descriptions
Prescaler division ration	1/10（40MHz / 10 = 4MHz）
Clock source	Clock bus 0
Compare match interrupt	Use OCR2D00
Compare match A (OCR1D00)	500us
Compare match B (OCR2D00)	700us

2.3 Module Setting

2.3.1 DFE Setting

Internal RH850/U2Bx DFE incorporates the FIR filters up to 64taps and IIR filter up to 6th order.

In this operation example, the FIR filter configures the band pass filter. The setting methods of register setting and coefficient memory are shown below.

(1) Coefficient Memory

Stores the filter coefficient of FIR filter to the coefficient memory (CMEM) in DFE. Refers to “1.3.2 Coefficient Memory Setting” for details.

(2) Control Register Settings (Refers to “2.4.4 Register Explanation” for register setting details.)

CTLACH0 Register Setting

- Channel tag：0
- Filter processing selection：FIR 32TAP
- Input data format selection: 16bit fixed point
- Output data interrupt request enable

CTLBCH0 Register Setting

- Calculation circuit processing selection: Selects decimation processing.
- Set to perform PH processing and comparison simultaneously.
- Comparison specification: Selects less-than mark (<).

CTLCCH0 Register Setting

- Input selection: Selects DS-ADC.

ACA Register Setting

- Decimation count setting: No decimation processing

CPOFST0～2 Register Setting

- Sets “0x03000000” to threshold.

PH2CTL0 Register Setting

- Comparison specification: Selects more-than mark (>).

PH3CTL0 Register Setting

- Comparison specification: Selects less-than mark (<).

PHUPDC0～3 Register Setting

- Enables the update notification of PH1～3.

TRGCH0, PITRG Register Setting

- Set the PH initialization flag and end flag to the compare match A0/B0 of timer D.

PH23CCTL0 Register Setting

- PH23 processing performs

(3) Channel Activation

Set ”1” to CTLACH0.EN bit.

2.4 Software Explanation

2.4.1 Function Explanation

Table 2-6 shows the used function in this application example.

Table2-6 Function Explanation

Function Name	Label Name	Description
Maine Function	main_pe0	Performs the calling and interrupting of each function.
Initialization function of DS-ADC function	ds_adc_init	Performs the DS-ADC (DSADC00) initialization function.
Initialization function of DFE function	dfe_init	Preforms the DFE0 ch0 initialization setting.
Initialization function of ATU function	atu_init	Preforms the ATU-Ⅵ timer D initialization setting.
Initialization function of DTS function	dts_init	Preforms the DTS ch32 initialization setting.
Initialization function of interrupt function	intc_init	Performs the setting of DTS ch63-32 transfer completion interrupts and timer D compare match interrupt.
Compare match interrupt function	atu6_td_int	Stores the PH23 processing result to the Local RAM.
DTS ch63-32 transfer completion interrupt function	dst_end_int	The transfer completion interrupt function of DTS ch63-32.

2.4.2 Use Define Declaration Explanation

Table 2-7 shows the explanation of the used define declaration in this application explanation.

Table2-7 Explanation of Use Define Declaration

Label Name	Function	Setting Value	Use Function Name
TAP_NUM	Number of taps of FIR filter.	32	dfe_init

2.4.3 Use Variable Explanation

Table 2-8 shows the explanation of used variable.

Table2-8 Explanation of Use Variable

Label Name	Function	Data Length	Use Function Name
*cmem0[TAP_NUM/2]	The pointer variable indicates the coefficient memory of DFE0 ch0.	signed long	dfe_init
smp_data[200]	Stores the DFE output result.	signed long	dts_Init
cap_data_ph1	Stores the timer D counter value when completing the PH1 processing.	unsigned long	atu6_td_int
cap_data_ph2	Stores the timer D counter value when completing the PH2 processing.	unsigned long	atu6_td_int
cap_data_ph3	Stores the timer D counter value when completing the PH3 processing.	unsigned long	atu6_td_int
smp_data_ph1	Stores the peak hold value of PH1 processing.	signed long	atu6_td_int
smp_data_ph2	Stores the peak hold value of PH2 processing.	signed long	atu6_td_int
smp_data_ph3	Stores the peak hold value of PH3 processing.	signed long	atu6_td_int

2.4.4 Register Explanation

Table 2-9 shows the register setting example of DS-ADC (DSADC00).

Table2-9 Register Setting Example of DS-ADC (DSADC00)

Register Name	Setting Value	Bit Name	Function	Setting Detail
■DS-ADC Common Register				
AD global control register (DSADCADGCR)	0x00	ODDE	Disconnection detective function self-diagnostic	Disable
		ODE	Disconnection detective	Disable
		UNSND	Conversion result output	Signed
Pin level self-diagnostic Control register (DSADCTDCR)	0x00	TDE	Pin level self-diagnostic function	Disable
■DS-ADC Fixed Register				
Unit control register (DSADC00UCR)	0x04000000	VPRSTE	Virtual channel pointer reset	Outputs DMA transfer request for all of A/D conversion result.
		RDMA	Read gate DMA mode	High impedance mode
		RESO0	High accurate mode	Selects DFE0.
		DFES	DFE channel selection	No mask
		DFMT[3:0]	Data Format	0
		VCEP[2:0]	End virtual channel Pointer	Outputs DMA transfer request for all of A/D conversion result.
Virtual channel control register (DSADC00VCR0)	0x00101000	FSELEXTE	Extension Fs switching bit	No extension
		GAIN[1:0]	Gain	×1
		VCULME	Upper-limit threshold notification	No notification
		VCLLME	Lower-limit threshold notification	No notification
		VCULLMTBS[1:0]	Threshold table selection	DSADCnULTBR0 (Unused)
		ORT	Post filter 2nd stage output rate selection	1/2
		TPVSL[2:0]	TAP coefficient selection	Coefficient 1
		DSDFTYP[3:0]	Post filter type	Depends on ORT and TPVSL setting.
		ADIE	Conversion completion interrupt	Disable

		ULEIE	Upper-limit/Lower-limit interrupt	Disable
		DFENT	DFE Entry	Entry.
		DFTAG[3:0]	DFE-TAG	0
		CNVCLS[1:0]	Conversion classification	Single mode input Common voltage=ADSVREFL
		GCTRL[3:0]	Input pin setting	DSAN000P

Register Name	Setting Value	Bit Name	Function	Setting Detail
AD start control register (DSADC00ADSTCR)	0x01	ADST	Starts A/D conversion.	Conversion starts
AD stop control register (DSADC00 ADENDCR)	0x01	ADEND	Stops A/D conversion.	Conversion stops
AD conversion trigger control register (DSADC00ADTCR)	0x00	ADSTTE	AD synchronization start enable	ADSTART disable
		ENDTRGE	AD end trigger enable	AD end trigger disable
		STTRGE	AD start trigger enable	AD start trigger disable
Virtual channel pointer register (DSADC00VCPTRR)	0x00	VCPTR[2:0]	Virtual channel number during A/D conversion	Clears as 0.
Safety control register (DSADC00SFTCR)	0x00	RDCLRE	Read & clear enable	No clearing
		OWEIE	Overwrite error interrupt	Prohibit
		PEIE	Parity error interrupt	Prohibit
		IDEIE	ID error interrupt	Prohibit
Upper-limit/Lower-limit table register (DSADC00ULTBR0 ～3)	0x7FFF8000	ULMTB[15:0]	Upper-limit table	Unused (Initial value)
		LLMTB[15:0]	Lower-limit table	Unused (Initial value)
Pin level self-diagnostic level register (DSADC00TDLVR)	0x00	AN3NLV	Pin level self-diagnostic specification	Unused (Initial value)
		AN3PLV	Pin level self-diagnostic specification	Unused (Initial value)
		AN2NLV	Pin level self-diagnostic specification	Unused (Initial value)
		AN2PLV	Pin level self-diagnostic specification	Unused (Initial value)
		AN1NLV	Pin level self-diagnostic specification	Unused (Initial value)
		AN1PLV	Pin level self-diagnostic specification	Unused (Initial value)
		AN0NLV	Pin level self-diagnostic specification	Unused (Initial value)
		AN0PLV	Pin level self-diagnostic specification	Unused (Initial value)

Table 2-10 shows the DFE0 register setting example.

Table2-10 Setting Example of DFE0 Register

Register Name	Setting Value	Bit Name	Function	Setting Detail
Control register A (DFE0CTLACH0)	0x00003010 ↓ 0x00003011	CATAG	Tag value for cascade input	0 (Unused)
		CAEN	Cascade enable	No cascade
		CAENL	Cascade enable	No cascade
		TAG	Channel tag	0 (Set value same with AD tag value inputted from AD.)
		CMD	Filter processing selection	FIR 32TAP
		IEF	Filter end interrupt	Prohibit
		FMT	FIR input data format	16bit fixed-point
		IEP	PH end interrupt	Prohibit
		IEE	Error interrupt	Prohibit
		IEC	Matching condition interrupt	Prohibit
		IEO	Output data interrupt	Enable
		CNSL	Matching condition interrupt 0/1 function selection	INT_DFE_CND0 : Selects compare match interrupt request. (Unused) INT_DFE_CND1 : Selects PH end interrupt request. (Unused)
		CNSLE	CNSL enable	Setting prohibition of CNSL
		AIME	Automatic initialization	Prohibit
		EN	Channel enable	Channel enable

Register Name	Setting Value	Bit Name	Function	Setting Detail
Control register B (DFE0CTLBCH0)	0x01403302	OFSL	Compare offset value “α” selection	Selects DFEjCPOFST0 register value.
		DISB	PH processing prohibition	Prohibits PH processing.
		PHPS	PH peak type selection	PH processing detects upper limit peak.
		CPCS	Compare value type selection	DFEjPHCHn is selected by DFEjCTLBCHn.SELB1.
		PHSLB2	PH initial value register selection	DFEjPHIA register value is selected as initial value of PH processing.
		DISA	Calculation /Decimation processing prohibition	Calculation/decimation processing prohibition
		PRCSC	Output data register floating-point conversion	Not execute floating-point conversion.
		SELB2	Comparing calculation selection	Selects less-than mark (<).
		SELB1	Compare target register selection	Register (DFEjPHCHn) + Compare offset value setting register (DFEjCPOFSTn)
		PRCSB	PH circuit processing selection	Set to perform PH processing and comparison simultaneously.
		HOFS	Middle value output register floating-point conversion	Not execute floating-point conversion.
		PICS	PH index register control selection	PH index update mode
		SELA	calculation/decimation count register selection	Selects ACA value.
		PFMT	PH result register floating-point selection	Not execute floating-point conversion. (Unused)
		ABS	Absolute value calculation	Not calculate absolute value.
		PRCSA	Calculation circuit processing selection	Execute decimation processing.
Control register C (DFE0CTLCCH0)	0x00000100	CA0E	C-ADC selection	No use
		DAyE	DS-ADC selection	Uses channel0.
		SAyE	SAR-ADC	No use

			selection	
Output data register (DFE0DOCH0)	-	DO	Output data	Stores calculation result after completing DFE processing.
Calculation/decimation count setting register A (DFE0ACA)	0x0000	AC	Calculation/decimation times	Not calculate and decimate.

Register Name	Setting Value	Bit Name	Function	Setting Detail
Compare offset value setting register (DFE0CPOFST0) (DFE0CPOFST1) (DFE0CPOFST2)	0x03000000	CPOFST	Sets compare offset value α,	Sets α=0x03000000.
Peak hold 2 control register 0 (DFE0PH2CTL0)	0x0000010C	OFSL	Compare offset value α selection of peak hold 2 processing	Selects DFE0CPOFST1 register value.
		PHPS	Peak hold 2 peak type selection	Detects lower-limit peak.
		CN2SLB2	Peak hold 2 Compare calculation selection	Selects more-than mark (>).
Peak hold 3 Control register 0 (DFE0PH3CTL0)	0x00000203	OFSL	Compare offset value α selection of peak hold 3 processing	Selects DFEjCPOFST2 register value.
		PHPS	Peak hold 3 peak type selection	Detects lower-limit peak.
		CN3SLB2	Peak hold 3 Compare calculation selection	Selects less-than mark (<).
PH initial value setting register (DFE0PHIA)	0x80000000	PHI	Sets PH initial value.	Sets minimum negative value.
PH initial value setting register (DFE0PHIB)	0x7FFFFFFF	PHI	Sets PH initial value.	Sets maximum integer value.

Register Name	Setting Value	Bit Name	Function	Setting Detail
Peak hold updates notification setting register 0 (DFE0PHUPDC0)	0x01	PHUPDCH	PH result register updates notification channel selection	The PH result register updating of channel 0 is notification target.
		PH23SL	PH2/PH3 result register updates notification selection	Notifies when the PH2 is updated. (Unused)
		PH23E	PH2/PH3 result register updates notification enable	Prohibits the notification.
		OEPHUPD	PH result register updates notification enable	Enables the notification.
Peak hold updates notification setting register 1 (DFE0PHUPDC1)	0x03	PHUPDCH	PH result register updates notification channel selection	The PH result register updating of channel 0 is notification target.
		PH23SL	PH2/PH3 result register updates notification selection	Notifies when the PH2 is updated.
		PH23E	PH2/PH3 result register updates notification enable	Enables the notification.
		OEPHUPD	PH result register updates notification enable	Enables the notification.
Peak hold updates notification setting register 2 (DFE0PHUPDC2)	0x07	PHUPDCH	PH result register updates notification channel selection	The PH result register updating of channel 0 is notification target.
		PH23SL	PH2/PH3 result register updates notification selection	Notifies when the PH3 is updated. (Unused)
		PH23E	PH2/PH3 result register updates notification enable	Enables the notification.
		OEPHUPD	PH result register updates notification enable	Enables the notification.

Register Name	Setting Value	Bit Name	Function	Setting Detail
Trigger setting register (DFE0TRGCH0)	0x00040400	PMFE	Peak hold mask ending flag trigger setting	Not generate the peak hold ending flag.
		PME	Peak hold mask starting flag trigger setting	Not generate the Peak hold mask starting flag
		PFE	Peak hold ending flag trigger setting	Generates the Peak hold ending flag by the timer trigger.
		AFE	Integration/decimation prohibition flag trigger setting	Not generate the integration/decimation prohibition flag
		PE	Peak hold initialization flag trigger setting	Generates the Peak hold initialization flag by the timer trigger.
		PT	Peak hold initialization flag and peak hold ending flag timer trigger selection	Uses the timer trigger 0.
		AE	Integration/decimation initialization flag trigger setting	Not generates the Integration/decimation initialization flag
		AT	Integration/decimation initialization flag trigger setting	Uses the timer trigger 0. (Unused)
		FE	Trigger setting of filter initialization flag	Not generates the filter initialization flag.
		FT	Filter initialization flag timer trigger selection	Uses the timer trigger 0. (Unused)

Register Name	Setting Value	Bit Name	Function	Setting Detail
Peak hold initialization/end timer trigger selection register (DFE0PITRG)	0x00000000	PITMTRG3	Timer trigger 3 for Peak hold initialization/end timer trigger	Uses timer D compare match A0/B0. (Unused)
		PITMTRG2	Timer trigger 2 for Peak hold initialization/end timer trigger	Uses timer D compare match A0/B0. (Unused)
		PITMTRG1	Timer trigger 1 for Peak hold initialization/end timer trigger	Uses timer D compare match A0/B0. (Unused)
		PITMTRG0	Timer trigger 0 for Peak hold initialization/end timer trigger	Uses timer D compare match A0/B0.
Peak hold 23 common control register 0 (DFE0PH23CCTL0)	0x00000001	CHS	Peak hold 23 target channel selection	Uses channel 0.
		PFMT	Peak hold 23 result register floating-point conversion	Not floating-point convert.
		PEN	Peak hold 23 enable	Enables peak hold 23.

Table 2-11 shows the register setting example of ATU-Ⅵ (Timer D).

Table2-11 register setting example of ATU-Ⅵ (Timer D)

Register Name	Setting Value	Bit Name	Function	Setting Detail
Prescaler register 0 (PSCR0)	0x0009	PSCx[9:0]	Sets prescaler division ration.	Sets “1/10”. (40MHz / 10)
Timer control register D0 (TCRD0)	0x4000	OBREDx	Offset base register enable	Prohibits input capture operation of OSBRDx.
		C2CEDx	Counter 2 clear enable	Prohibits TCNT2Dx counter clearing request from timer B.
		C1CEDx	Counter 1 clearing enable	Prohibits TCNT1Dx counter clearing request from timer B.
		CLR2Dx	TCNT2Dx clearing setting bit	Not use CUCR2Dx compare match for TCNT2DX clearing.
		CKSEL2Dx[2:0]	TCNT2Dx clock selects	Up-counts TCNT2Dx by clock bus 0.
		CLR1Dx	TCNT1Dx clearing setting bit	Not use CUCR1Dx compare match for TCNT1DX clearing.
		CKSEL1Dx[2:0]	TCNT1Dx clock selects	Up-counts TCNT1Dx by clock bus 0.
		DCSELDx[2:0]	TCNTDxy clock selects	Up-counts TCNTDxy by clock bus 0.

Register Name	Setting Value	Bit Name	Function	Setting Detail
Timer I/O control register 1D0 (TIOR1D0)	0x0002	OSSDx3[1:0]	Compare match output factor selection bit	No TODxyA pin output
		OSSDx2[1:0]	Compare match output factor selection bit	No TODxyA pin output
		OSSDx1[1:0]	Compare match output factor selection bit	No TODxyA pin output
		OSSDx0[1:0]	Compare match output factor selection bit	No TODxyA pin output
		IOADx3[1:0]	I/O control A	Compare match A prohibition
		IOADx2[1:0]	I/O control A	Compare match A prohibition
		IOADx1[1:0]	I/O control A	Compare match A prohibition
		IOADx0[1:0]	I/O control A	1 output by compare match A
Timer I/O control register 2D0 (TIOR2D0)	0x0001	IOBDx3[2:0]	I/O control B	Compare match B prohibition
		IOBDx2[2:0]	I/O control B	Compare match B prohibition
		IOBDx1[2:0]	I/O control B	Compare match B prohibition
		IOBDx0[2:0]	I/O control B	0 output by compare match A
Timer D Interrupt selection control register 0 (ATUINTSELD0)	0x00000001	ATU_INTSEL_ D13[2:0]	Interrupt request selection	Selects OCR1Dxy compare match interrupt.
		ATU_INTSEL_ D12[2:0]	Interrupt request selection	Selects OCR1Dxy compare match interrupt.
		ATU_INTSEL_ D11[2:0]	Interrupt request selection	Selects OCR1Dxy compare match interrupt.
		ATU_INTSEL_ D10[2:0]	Interrupt request selection	Selects OCR1Dxy compare match interrupt.
		ATU_INTSEL_ D03[2:0]	Interrupt request selection	Selects OCR1Dxy compare match interrupt.
		ATU_INTSEL_ D02[2:0]	Interrupt request selection	Selects OCR1Dxy compare match interrupt.
		ATU_INTSEL_ D01[2:0]	Interrupt request selection	Selects OCR1Dxy compare match interrupt.
		ATU_INTSEL_ D00[2:0]	Interrupt request selection	Selects OCR2Dxy compare match interrupt.

Register Name	Setting Value	Bit Name	Function	Setting Detail
DFE compare A timer trigger A1 (ATUDFEENA1)	0x00000001	ATU_DFEEN_A7[3:0]	Timer trigger	Prohibits
		ATU_DFEEN_A6[3:0]	Timer trigger	Prohibits
		ATU_DFEEN_A5[3:0]	Timer trigger	Prohibits
		ATU_DFEEN_A4[3:0]	Timer trigger	Prohibits
		ATU_DFEEN_A3[3:0]	Timer trigger	Prohibits
		ATU_DFEEN_A2[3:0]	Timer trigger	Prohibits
		ATU_DFEEN_A1[3:0]	Timer trigger	Prohibits
		ATU_DFEEN_A0[3:0]	Timer trigger	Selects D00A compare match interrupt.
Timer interrupt enable register 2D0 (TIER2D0)	0x00000101	UNDEDx3	Under flow interrupt enable	Prohibits
		UNDEDx2	Under flow interrupt enable	Prohibits
		UNDEDx1	Under flow interrupt enable	Prohibits
		UNDEDx0	Under flow interrupt enable	Prohibits
		CMPBEDx3	Compare match B interrupt enable	Prohibits
		CMPBEDx2	Compare match B interrupt enable	Prohibits
		CMPBEDx1	Compare match B interrupt enable	Prohibits
		CMPBEDx0	Compare match B interrupt enable	Enable
		CMPAEDx3	Compare match A interrupt enable	Prohibits
		CMPAEDx2	Compare match A interrupt enable	Prohibits
		CMPAEDx1	Compare match A interrupt enable	Prohibits
		CMPAEDx0	Compare match A interrupt enable	Enable

Register Name	Setting Value	Bit Name	Function	Setting Detail
Timer status clear register (TSCRD0)	0x3FFF	OVFC2Dx	Overflow flag clear enable 2Dx	Flag clears
		OVFC1Dx	Overflow flag clear enable 1Dx	Flag clears
		UDFCDx3	Underflow flag clear enable Dx3	Flag clears
		UDFCDx2	Underflow flag clear enable Dx2	Flag clears
		UDFCDx1	Underflow flag clear enable Dx1	Flag clears
		UDFCDx0	Underflow flag clear enable Dx0	Flag clears
		CMFCADx3	Compare A flag clear enable Dx3	Flag clears
		CMFCADx2	Compare A flag clear enable Dx2	Flag clears
		CMFCADx1	Compare A flag clear enable Dx1	Flag clears
		CMFCADx0	Compare A flag clear enable Dx0	Flag clears
		CMFCBDx3	Compare B flag clear enable Dx3	Flag clears
		CMFCBDx2	Compare B flag clear enable Dx2	Flag clears
		CMFCBDx1	Compare B flag clear enable Dx1	Flag clears
		CMFCBDx0	Compare B flag clear enable Dx0	Flag clears

Register Name	Setting Value	Bit Name	Function	Setting Detail
Output compare register 1D00 (OCR1D00)	0x000007D0	OC1D[31:0]	Compare value setting	0x000007D0（500us）
Output compare register 2D00 (OCR2D00)	0x00000AF0	OC2D[31:0]	Compare value setting	0x00000AF0（700us）
Common input capture selection register D (CCAPSELD)	0x01	CCAPSEL	Input capture selection	Captures TCNT2D0 value.
Timer start register D (TSTRD)	0x0001	STRD8	Counter D8 start bit	Stops counting operation.
		STRD7	Counter D7 start bit	Stops counting operation.
		STRD6	Counter D6 start bit	Stops counting operation.
		STRD5	Counter D5 start bit	Stops counting operation.
		STRD4	Counter D4 start bit	Stops counting operation.
		STRD3	Counter D3 start bit	Stops counting operation.
		STRD2	Counter D2 start bit	Stops counting operation.
		STRD1	Counter D1 start bit	Stops counting operation.
		STRD0	Counter D0 start bit	Enables counting operation.
ATU master enable register (ATUENR)	0x11	TGE	Timer G enable bit	Stops counting operation.
		TFE	Timer F enable bit	Stops counting operation.
		TEE	Timer E enable bit	Stops counting operation.
		TDE	Timer D enable bit	Enables counting operation.
		TCE	Timer C enable bit	Stops counting operation.
		TBE	Timer B enable bit	Stops counting operation.
		TAE	Timer A enable bit	Stops counting operation.
		PSCE	Prescaler enable bit	Enables clock generation.

Table 2-12 shows the register setting example of DTS ch32.

Table2-12 Register Setting of DTS Ch32

Register Name	Setting Value	Bit Name	Function	Setting Detail
■Global Register				
DTS channel priority setting 2 (DTSPR2)	0xFFFFFFFC	DTSnPR[1:0] (n=32 to 63)	Priority setting of DTS channel	Set “0” (highest priority) to DTS channel 32 priority.
DTS channel 32 channel master setting (DTS032CM)	0x00000000	CHAIN_ RESTRICT	Chain function limit setting	No limit
		CHAIN_SPID [4:0]	Chain enable SPID setting	0 (Unused)
		CHAIN_UM	Chain enable UM setting	(Unused)
		SPID[4:0]	Channel master SPID setting	Set SPID = 0.
		UM	Channel master UM setting	Supervisor mode
		CMC[15:0]	Transmission time compare	(Unused)
■DTS Channel Register				
DTS Source Address (DTSA032)	(unsigned long)&DFE0.DOCH0	SA[31:0]	Source address	Sets source address to DFE0 ch0 output data register.
DTS Destination Address (DTDA032)	(unsigned long)&smp_data[0]	DA[31:0]	Destination address	Sets destination address to header address of array for sampling data.
DTS Transmission Time (DTTC032)	0x000000C8	ARC[15:0]	Address reload count	(Unused)
		TRC[15:0]	Transition times	Set 200 times to transition times.

Register Name	Setting Value	Bit Name	Function	Setting Detail
DTS transfer control (DTTCT032)	0x00004048	ESE	DMA transfer stop setting when error transfer	Continues DMA transfers.
		CHNSEL[6:0]	Chain destination selection	(Unused)
		CHNE[1:0]	Chain enable	Disables
		CCE	Transfer times match interrupt	Prohibits
		TCE	Transfer completion interrupt	Enables
		RLD2M[1:0]	Reload function 2 setting	Disables reload function 2.
		RLD1M[1:0]	Reload function 1 setting	Disables reload function 1.
		DACM[1:0]	Destination address count direction	Increments
		SACM[1:0]	Source address count direction	Fixed
		DS[2:0]	Transfer data size	32bits
		TRM[1:0]	Transfer mode	Single transition
DTSFSL Operation Setting (DTFSL032)	0x00000001	REQEN	DTS transfer request enable	Set enables to DTS transfer request.
DTS transfer request clear (DTFSC032)	0x000000B1	ERC	Transfer error flag (ER) clear	Clears
		CCC	Transfer count compare flag (CC) clear	Clears
		TCC	Transfer completion flag (TC) clear	Clears
		DRQC	DMA transfer request clear	Clears

Table 2-13 shows the register setting of INTC2.

Table 2-13 Register Setting Example of INTC2

Register Name	Setting Value	Bit Name	Function	Setting Detail
EI level interrupt bind register (EIBD63) (EIBD164)	0x00000000	CST	Broadcast interrupt port number setting	Prohibits
		BCP[1:0]	Broadcast interrupt port number setting	(Unused)
		PEID[2:0]	Specification of destination binds (request) the interrupt	PE0 (CPU0)
EI level control register (EIC63) (EIC164)	0x0040	EICTn	Interrupt channel type bit	(Possible to read only.)
		EIRFn	Interrupt request flag	(Possible to read only.)
		EIMKn	Interrupt mask bit	Enables interrupt processing.
		EITBn	Interrupt vector method selection	Table reference method
		EIPn	Specification of interrupt priority	0 (Highest priority)

2.4.5 Operation flow

Figure 2-4 shows the software operation flow of in this application example.

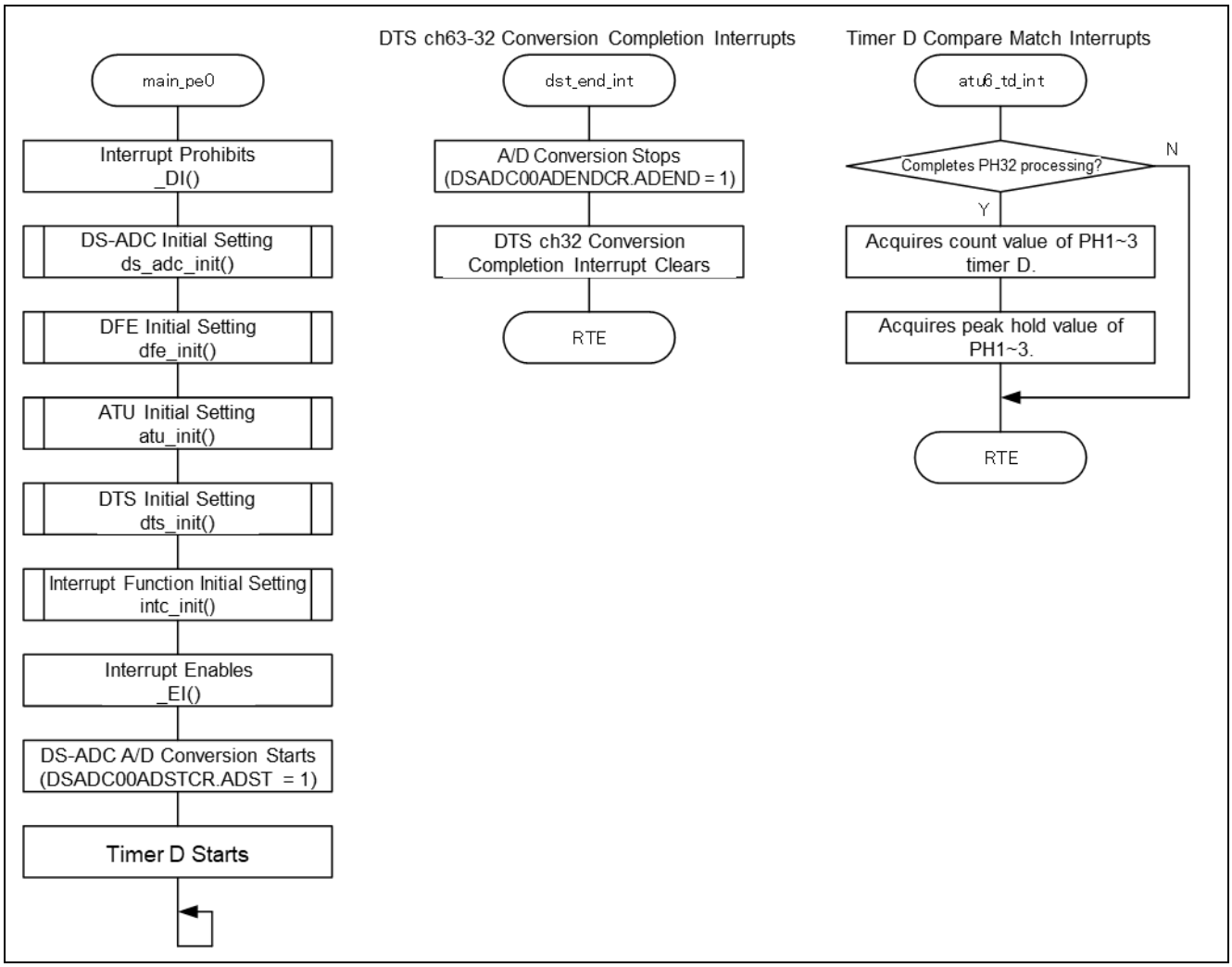

Figure 2-4 Software Operation Flow

3. FIFO Functions (Combination with DS-ADC, sDMAC, ATU-Ⅵ Timer G)

3.1 Specifications

In this application example, A/D-converts the applied voltage with fixed sampling rate to the DSAN000P, DSAN100P, and DSAN210P pins to use the DS-ADC (DSADC00, DSADC10, DSADC21*). The A/D conversion value performs the filtering with the FIR filters in DFE ch0/ch1/ch2, and stores the output data register of DFE0 ch0/ch1/ch2 values to the DFE_FIFO Buffer A ch0/ch1/ch2 in a lump by the FIFO capture trigger from timer G. The filtering result is distributed for each system and transferred to the local RAM by the DMA transfer (uses scatter function) triggered by the capture end interrupt.

The specifications in this application example are shown below.

- A/D-converts the analog input voltage by the DS-ADC (DSADC00, DSADC10, DSADC21) single end inputs and the common voltage ADSVREFL continuously.
- The A/D conversion value of DS-ADC (DSADC00, DSADC10, DSADC21) entries to DFE automatically.
- DFE performs the filtering the input data by the configured band pass filter by the internal FILR filter.
- The filter coefficient and data used for FIR filter setting are stored to RAM in DFE (coefficient memory and data memory).
- The DFE filtering result is not performed the decimation processing.
- Generates the FIFO capture trigger by the timer G.
- Stores the output data register value of DFE0 ch0/ch1/ch2 to DFE_FIFO Buffer A ch0/ch1/ch2.
- Regards the buffer A capture end interrupt as the transfer request factor of sDMAC.
- The values captured by DFE due to sDMAC scatter operation are tributed to each system and transferred to RAM
- DS-ADC startup trigger: Software trigger
- DS-ADC sampling plate: 200ksps
- DFE processing result output late: 200kHz (No decimation)
- Input voltage range: 0 ~ ADSVCC (ADSVCC: Analog power voltage 0 ~ + 5.5V）
- Output data format: 32bits signed fixed-point number

Table 3-1 shows the filter specification example in this application example. The sampling frequency “fs” in the table indicates the inputted data speed to DFE and it means DS-ADC sampling rate (200ksps) in this application example.

Table3-1 Filter Specification Example

Items	Description
Configuration filter	Bandpass filter
Sampling frequency “fs”	200ksps
High-range cutoff frequency “f_L”	5kHz
Low-range cutoff frequency “f_H”	15kHz
Bandpass ripple R_p	1dB
Stopband attenuation A_p	25dB

*: Changes to DSADC20 when using 292pin version (U2B10, U2B6) that does not have DCADC21.

Figure 3-1 shows the system configuration.

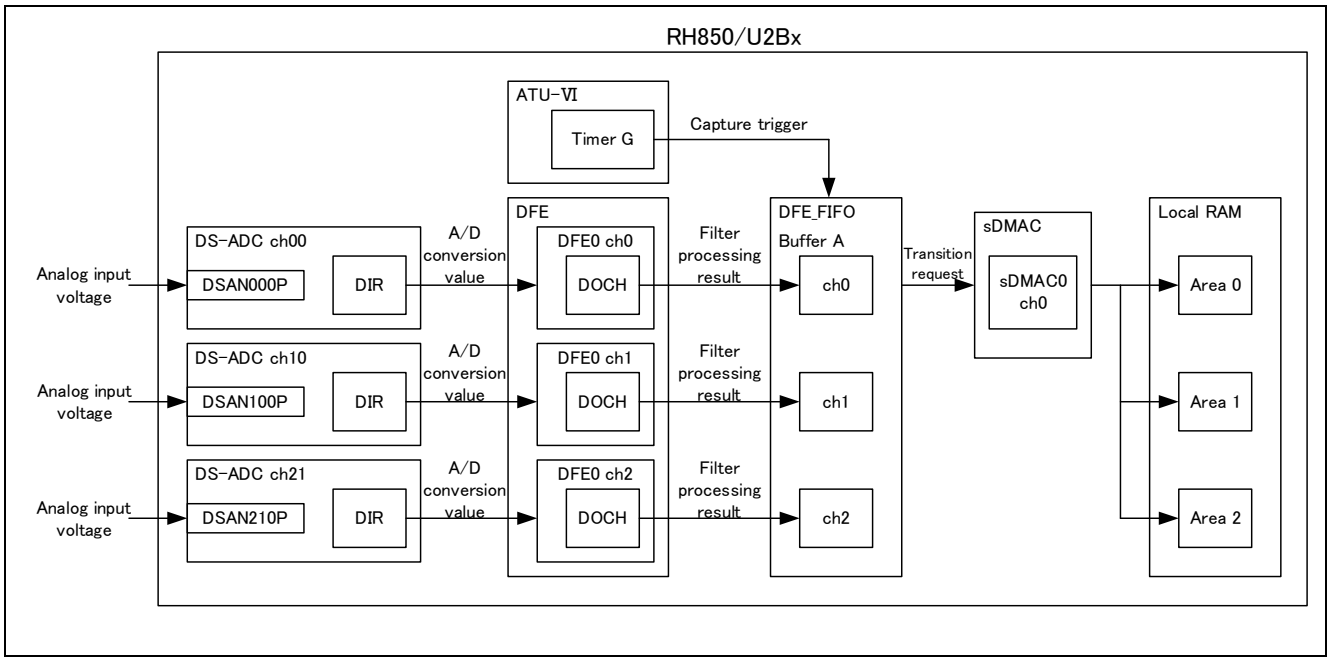

Figure3-1 System Configuration

3.1.1 Use Function

The used hardware functions in this application note of RH850/U2Bx are shown below.

・ΔΣAD convertor (DS-ADC)	A/D-converts analog input voltage.
・Digital filter (DFE)	Configures bandpass filter by internal FIR filter and applied filtering to A/D conversion value.
・DFE_FIFO	Using buffer A, stores the three values of DFE0 output data register by FIFO capture trigger from the timer G.
・sDMAC	The values captured by DFE due to scatter operation are tributed to each system and transferred to RAM
・ATU-VI	Applies the timer FIFO capture trigger to DFE_FIFO to use timer G.
・Interrupt controller (INTC2)	Controls the interrupts to CPU of sDMAC transfer completion interrupt request.

3.2 Explanation of Application Example

3.2.1 Operation Explanation

Figure 3-2 shows the operation explanation in this application example and figure 3-3 shows the scatter transfer overview.

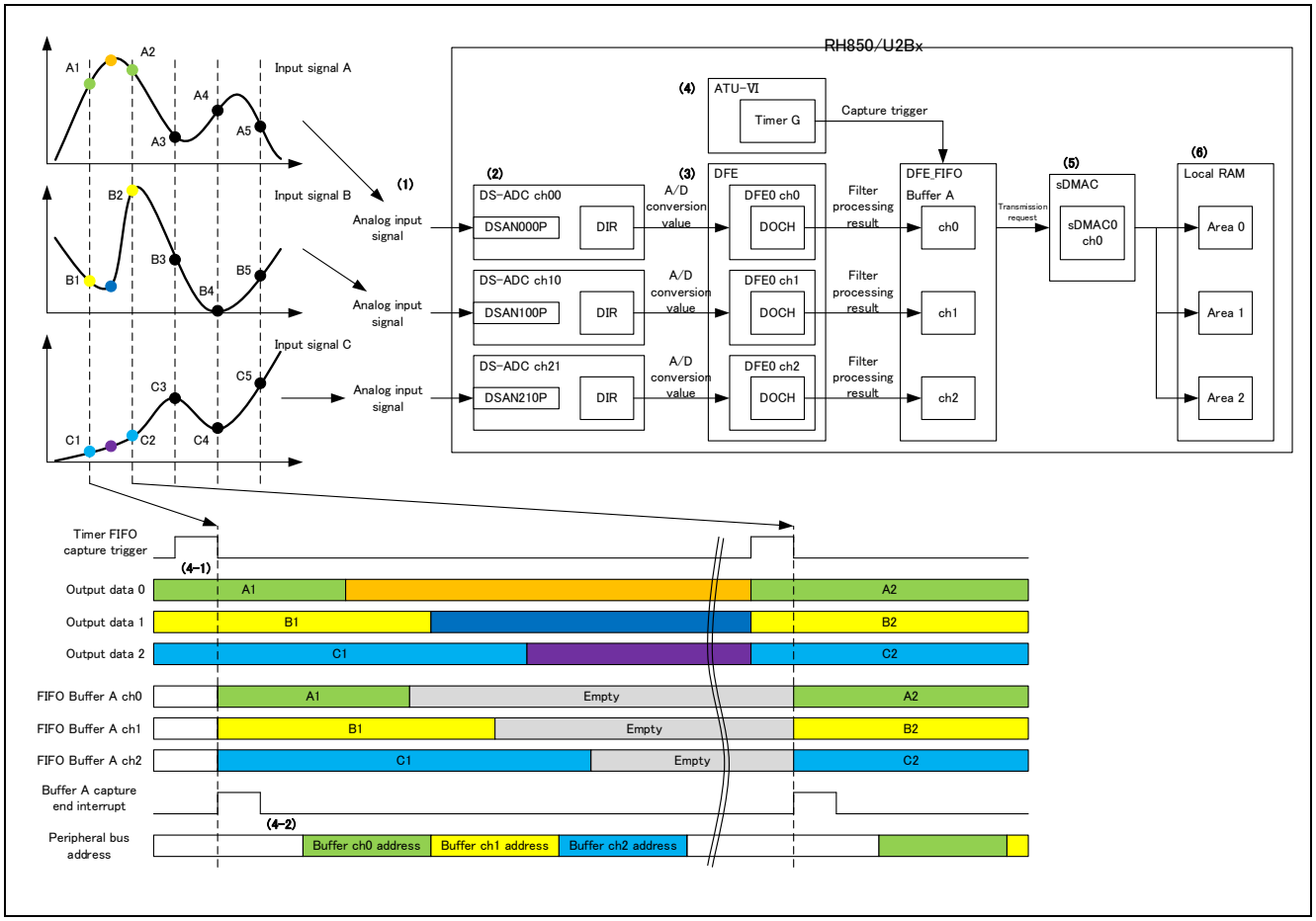

Figure3-2 Operation Explanation

(1) Inputs the analog signal to DS-ADC ch00, ch10, and ch21 from each analog input pin.

(2) Each DS-ADC performs the A/D conversion at a fixed sampling period.

(3) Entries the A/D conversion result of DS-ADC to DFE and performs filtering.

(4) Stores the output data register value of DFE collectively by the FIFO capture trigger from timer G.

(5) Using the scatter transfer of sDMAC, transfers the value stored to buffer A ch0~2 to the local RAM.

(6) It is tributed for each input system of DS-ADC ch0~2 and stored to the local RAM.

The scatter function can transfer the filtering results to each array variable with sDMAC 1 channel.

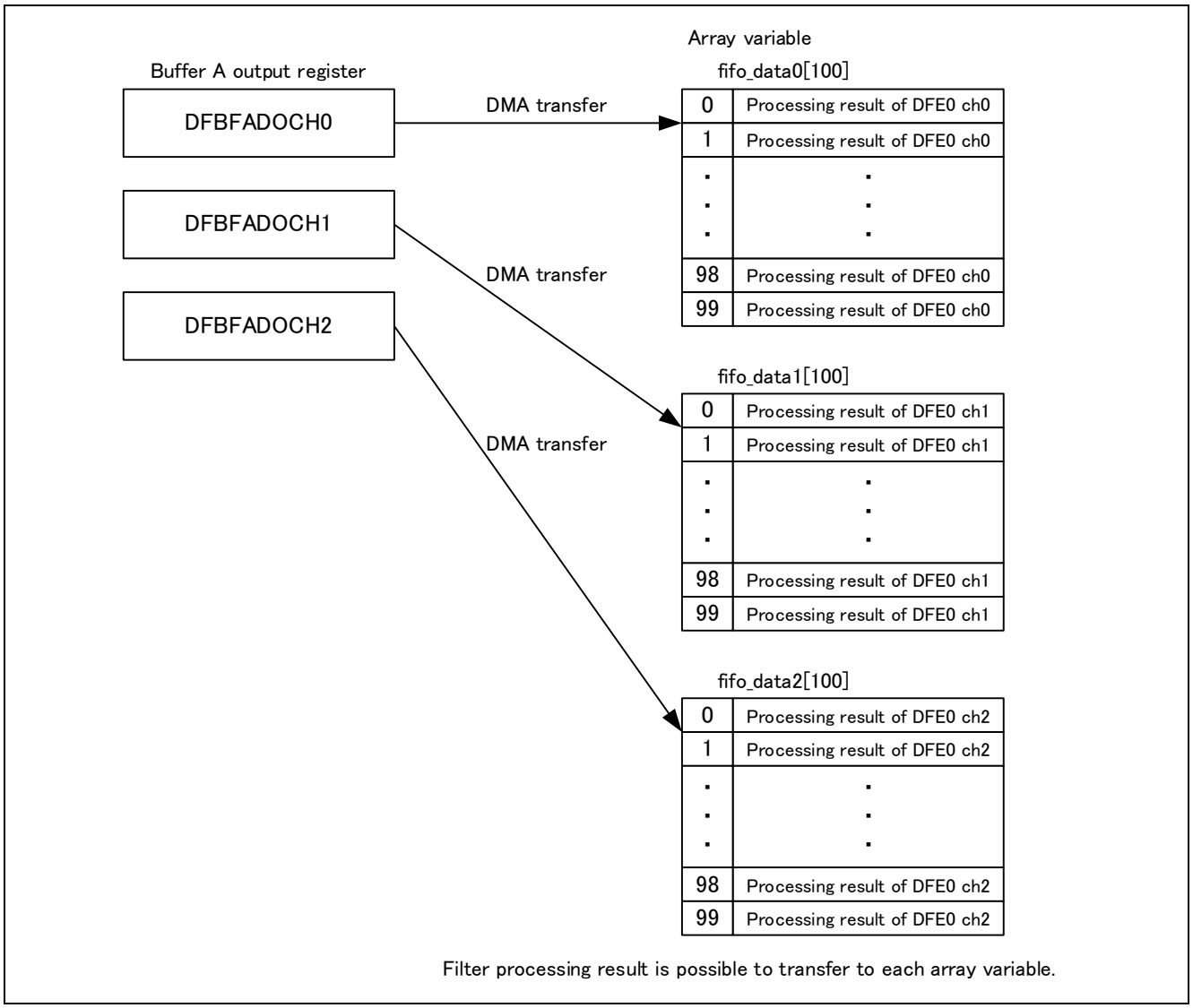

Figure3-3 Scatter Transfer Overview of sDMAC

3.2.2 Operating Conditions of Usage Functions

Table 3-2 shows the operating conditions of DS-ADC used in this application example.

Table 3-2 Operating Conditions of DS-ADC

Item	Description
Use channel	DSADC00, DSADC10, DSADC21
Analog input pin	DSAN000P, DSAN100P, DSAN210P
Sampling rate	200ksps
Over sampling rate	8Msps
DFE entry	Not entry
DFE-TAG	0, 7, F
Gain	×1
Conversion type	Single end input
Common voltage	ADSVREFL
A/D conversion data format	Number of 16-bits signed fixed-points
Effective bit	12 bits

Table 3-3 shows the operating conditions of DFE used in this application example.

Table 3-3 Operating Conditions of DFE

Item	Description
Used channel	DFE0 ch0, ch1, ch2
Channel tag	0, 7, F
Used filter	FIR
Number of taps	32
Input data format	Number of 16-bits signed fixed-points
Coefficient data format	Number of 16-bits signed fixed-points
Output data format	Number of 32-bits signed fixed-points
Decimation times	Not decimation processing
Peak-Hold processing	Not PH processing

Table 3-4 shows the operating conditions of ATU-IV (Timer G) used in this application example.

Table 3-4 Operating Conditions of ATU-IV (Timer G)

Item	Description
Division ration of prescaler	1/10 (40MHz / 10 = 4MHz)
Clock source	Clock bus 1
Compare match value	0x20 (8us)
Compare match interrupt	Use G1 compare match interrupt.
FIFO capture trigger	Use G1 compare match interrupt.

Table 3-5 shows the operating conditions of sDMAC used in this application example.

Table 3-5 Operating Conditions of sDMAC

Item	Description
sDMAC channel	sDMAC0 ch0
Channel master SPID	0
Channel master UM	Supervisor mode
sDMAC trigger source	Buffer A capture trigger end interrupt
Source address	Buffer A output register (DFBFADOCH0)
Destination address	Local RAM
Source address / count direction	Increment
Destination address count direction	Fixed
Scatter transmission internal loop Address increment value	Address of fifo_data1[0] to address of fifo_data0[0]
Repetition times of internal DMA loop	2 times
Transmission mode	Scatter conversion enable
Transmission size	12 bytes
Unit of transmission	4 bytes

3.3 Module Setting

3.3.1 DFE Setting

The DFE incorporating RH850/U2Bx incorporates the FIR filter with up to 64 taps and the IIR filter up to 6th.

In this application example, the FIR filter configures the bandpass filter. The follows explain the register setting and the setting method of the coefficient memory for this time.

(1) Coefficient Memory Setting

The setting for storing the filter coefficient of the FIR filter to the coefficient memory internal DFE. Refer to “1.3.2 Coefficient Memory Setting” for the details.

(2) Control Register Setting (Refer to “3.4.4 Explanation for Registers” for the details of the register setting.)

CTLACH0 Register Setting

- Channel tag: 0
- Filter processing selection: FIR 32 TAP
- Input data format selection: 16-bits fixed signed fixed point
- Output data interrupt request disable

CTLACH1 Register Setting

- Channel tag: 7
- Filter processing selection: FIR 32 TAP
- Input data format selection: 16-bits fixed signed fixed point
- Output data interrupt request disable

CTLACH2 Register Setting

- Channel tag: F
- Filter processing selection: FIR 32 TAP
- Input data format selection: 16-bits fixed signed fixed point
- Output data interrupt request disable

CTLBCH0 to 2 Register Setting

- Accumulation circuit processing selection: Select decimation processing

CTLCCH0 to 2 Register Setting

- Input selection: Select DS-ADC

ACA Register Setting

- Decimation times setting: No decimation processing

(3) Chanel Enabling

Set CTLACH0 to 2.EN bits to ”1”.

(4)DFE_FIFO setting

DFBFACCTL Register Setting

- Buffer A circuit: Use

DFBFACTLCH0 Register Setting

- Buffer A_ch0 enable
- Capture target channel: DFE0_ch0

DFBFACTLCH1 Register Setting

- Buffer A_ch1 enable
- Capture target channel: DFE0_ch1

DFBFACTLCH1 Register Setting

- Buffer A_ch1 enable
- Capture target channel: DFE0_ch2

3.4 Explanation of software

3.4.1 Explanation of functions

Table 3-6 shows the used functions in this application example.

Table 3-6 Explanation of functions

Function Name	Label Name	Processing
Maine function	main_pe0	It performs the calling of each function and the waiting of interrupt.
sDMAC transmitting completion interrupt function	sdmac_end_int	It is transferring completion interrupt function of sDMAC.
Initialize function for DS-ADC function	ds_adc_init	It performs the initial setting of DS-ADC (DSADC00、DSADC10, DSADC21).
Initialize function for DFE function	dfe_init	It performs the initial setting of DFE0 ch0, ch1, and ch2.
Initialize function for ATU function	atu_init	It performs the initial setting of ATU-VI Timer G.
Initialize function for sDMAC function	sdmac_init	It performs the initial setting of sDMAC0 ch0.
Initialize function for interrupt function	intc_init	It sets the transferring completion interrupt of sDMAC.

3.4.2 Explanation of Used Define Declaration

Table 3-7 shows the explanation of used define declaration in this application example.

Table 3-7 Explanation of Used Define Declaration

Label Name	Function	Setting Value	Used Function Name
TAP_NUM	It shows the number of TAP of FIR filter.	32	dfe_init

3.4.3 Explanation of Used Variable

Table 3-8 shows the explanation of the variable used in in this application example.

Table 3-8 Explanation of Used Variable

Label Name	Function	Data Length	Used Function Name
*cmem0[TAP_NUM/2]	The pointer variable that shows the coefficient memory of DFE0 ch0.	signed long	dfe_init
*cmem1[TAP_NUM/2]	The pointer variable that shows the coefficient memory of DFE0 ch1.	signed long	dfe_init
*cmem2[TAP_NUM/2]	The pointer variable that shows the coefficient memory of DFE0 ch2.	signed long	dfe_init
fifo_data0 [100]	It stores the output result of DFE0 ch0.	signed long	sdmac_init
fifo_data1 [100]	It stores the output result of DFE0 ch1.	signed long	sdmac_init
fifo_data2 [100]	It stores the output result of DFE0 ch2.	signed long	sdmac_init

3.4.4 Explanation for Registers

Table 3-9 shows the register setting example of DS-ADC (DSADC00, DSADC10, DSADC21).

Table 3-9 Register Setting Example of DS-ADC (DSADC00, DSADC10, DSADC21)

Register Name	Setting Value	Bit Name	Function	Setting
■DS-ADC Common Register				
AD global control register （DSADCADGCR）	0x00	ODDE	Disconnecting detection function self-diagnosis	Disable
		ODE	Disconnecting detection	Disable
		UNSND	Conversion result output	Signed
Pin level self-diagnosis control register (DSADCTDCR)	0x00	TDE	Pin level self-diagnosis function	Disable
■DS-ADC characteristic register				
Unit control register (DSADC00UCR)	0x04000000	VPRSTE	Virtual channel pointer reset	None
		RDMA	Read gate DMA mode	Outputs DMA conversion request against entire A/D conversion result.
		RESO0	High-accuracy mode	High-impedance mode
		DFES	DFE channel selection	Select DFE0
		DFMT[3:0]	Data format	No mask
		VCEP[2:0]	End virtual channel pointer	0
Virtual channel control register (DSADC00VCR0)	0x00101000	GAIN[1:0]	Gain	×1
		VCULME	Upper-limit threshold notification	No notification
		VCLLME	Lower-limit threshold notification	No notification
		VCULLMTBS[1:0]	Threshold table selection	DSADCnULTBR0 (Unused)
		ORT	Rear filter 2nd stage output rate selection	1/2
		TPVSL[2:0]	TAP coefficient selection	Coefficient 1
		DSDFTYP[3:0]	Post filter type	Depending on setting of ORT and TPVSL
		ADIE	Conversion completion interrupt	Disable
		ULEIE	Upper/Lower limit error interrupt	Disable
		DFENT	DFE entry	Entry.

		DFTAG[3:0]	DFE-TAG	0
		CNVCLS[1:0]	Conversion type	Single-end input, high-voltage=ADSVREFL
		GCTRL[3:0]	Input pin setting	DSAN000P

Register Name	Setting Value	Bit Name	Function	Setting
Virtual channel control register (DSADC10VCR0)	0x00101700	FSELEXTE	Extension Fs switching bit	No extension
		GAIN[1:0]	Gain	×1
		VCULME	Upper-limit threshold notification	No notification
		VCLLME	Lower-limit threshold notification	No notification
		VCULLMTBS[1:0]	Threshold table selection	DSADCnULTBR0 (Unused)
		ORT	Rear filter 2nd stage output rate selection	1/2
		TPVSL[2:0]	TAP coefficient selection	Coefficient 1
		DSDFTYP[3:0]	Post filter type	Depending on setting of ORT and TPVSL
		ADIE	Conversion completion interrupt	Disable
		ULEIE	Upper/Lower limit error interrupt	Disable
		DFENT	DFE entry	Entry.
		DFTAG[3:0]	DFE-TAG	7
		CNVCLS[1:0]	Conversion type	Single-end input, high-voltage=ADSVREFL
		GCTRL[3:0]	Input pin setting	DSAN100P
Virtual channel control register (DSADC21VCR0)	0x00101F00	GAIN[1:0]	Gain	×1
		VCULME	Upper-limit threshold notification	No notification
		VCLLME	Lower-limit threshold notification	No notification
		VCULLMTBS[1:0]	Threshold table selection	DSADCnULTBR0 (Unused)
		ORT	Rear filter 2nd stage output rate selection	1/2
		TPVSL[2:0]	TAP coefficient selection	Coefficient 1
		DSDFTYP[3:0]	Post filter type	Depending on setting of ORT and TPVSL
		ADIE	Conversion completion interrupt	Disable
		ULEIE	Upper/Lower limit error interrupt	Disable
		DFENT	DFE entry	Entry.

		DFTAG[3:0]	DFE-TAG	F
		CNVCLS[1:0]	Conversion type	Single-end input, high-voltage =ADSVREFL
		GCTRL[3:0]	Input pin setting	DSAN210P

Register Name	Setting Value	Bit Name	Function	Setting
Safety control register (DSADC00SFTCR) (DSADC10SFTCR) (DSADC21SFTCR)	0x00	RDCLRE	Read & clear enable	No clear
		OWEIE	Overwrite error interrupt	Prohibition
		PEIE	Parity error interrupt	Prohibition
		IDEIE	ID error interrupt	Prohibition
Upper/Lower limit table register (DSADC00ULTBR0 ~3)	0x7FFF8000	ULMTB[15:0]	Upper limit table	Unused (initial value)
		LLMTB[15:0]	Lower limit table	Unused (initial value)
Upper/Lower limit table register (DSADC10ULTBR0 ~1)	0x7FFF8000	ULMTB[15:0]	Upper limit table	Unused (initial value)
		LLMTB[15:0]	Lower limit table	Unused (initial value)
Pin level self-diagnosis control register (DSADC00TDLVR) (DSADC10TDLVR) (DSADC21TDLVR)	0x00	AN3NLV	Pin level self-diagnosis level specification	Unused (initial value)
		AN3PLV	Pin level self-diagnosis level specification	Unused (initial value)
		AN2NLV	Pin level self-diagnosis level specification	Unused (initial value)
		AN2PLV	Pin level self-diagnosis level specification	Unused (initial value)
		AN1NLV	Pin level self-diagnosis level specification	Unused (initial value)
		AN1PLV	Pin level self-diagnosis level specification	Unused (initial value)
		AN0NLV	Pin level self-diagnosis level specification	Unused (initial value)
		AN0PLV	Pin level self-diagnosis level specification	Unused (initial value)
Virtual channel pointer register (DSADC00 VCPTRR) (DSADC10 VCPTRR) (DSADC21 VCPTRR)	0x00	VCPTR[2:0]	Virtual channel number in A/D conversion progressing	Clear to 0.

Register Name	Setting Value	Bit name	Function	Setting
AD conversion trigger control register (DSADC00ADTCR) (DSADC10ADTCR) (DSADC21ADTCR)	0x40	ADSTTE	AD synchronization starting enable	ADSTART enable
		ENDTRGE	AD end trigger enable	AD end trigger disable
		STTRGE	AD start trigger enable	AD start trigger disable
AD synchronization starting control register (DSADCSYNSTCR)	0x01	ADSTART	A/D conversion start of each ΔΣADC	A/D conversion start

Table 3-10 shows the register setting example of DFE0.

Table 3-10 Register Setting Example of DFE

Register Name	Setting Value	Bit Name	Function	Setting
Control register A (DFE0CTLACH0)	0x00003000 ↓ 0x00003001	CATAG	Tag value for cascade input	0 (Unused)
		CAEN	Cascade enable	No cascade
		TAG	Channel tag	0 (set with the same AD tag value inputted from AD)
		CMD	Filter processing selection	FIR 32TAP
		IEF	Filter end interrupt	Prohibition
		FMT	FIR input data format	16-bits signed fixed-points
		IEP	PH end interrupt	Prohibition
		IEE	Error interrupt	Prohibition
		IEC	Condition matching interrupt	Prohibition
		IEO	Data output interrupt	Prohibition
		CNSL	Condition matching interrupt 0/1 function selection	INT_DFE_CND0: Select the comparison matching interrupt request. (Unused) INT_DFE_CND1: Select the PH end interrupt request. (Unused)
		CNSLE	CNSL enable	CNSL bit setting disable
		AIME	Automatic initialization	Prohibition
		EN	Channel enable	Channel enable

Register Name	Setting Value	Bit Name	Function	Setting
Control register A （DFE0CTLACH1）	0x00073000 ↓ 0x00073001	CATAG	Tag value for cascade input	0 (Unused)
		CAEN	Cascade enable	No cascade
		CAENL	Cascade enable	No cascade
		TAG	Channel Tag	7 (set with the same AD tag value inputted from AD)
		CMD	Filter processing selection	FIR 32TAP
		FMT	Filter end interrupt	16-bits signed fixed-points
		IEF	FIR input data format	Prohibition
		IEP	PH end interrupt	Prohibition
		IEE	Error interrupt	Prohibition
		IEC	Condition matching interrupt	Prohibition
		IEO	Data output interrupt	Prohibition
		CNSL	Condition matching interrupt 0/1 function selection	INT_DFE_CND0: Select the comparison matching interrupt request. (Unused) INT_DFE_CND1: Select the PH end interrupt request. (Unused)
		CNSLE	CNSL enable	CNSL bit setting disable
		AIME	Automatic initialization	Prohibition
		EN	Channel enable	Channel enable

Register Name	Setting Value	Bit Name	Function	Setting
Control register A (DFE0CTLACH2)	0x000F3000 ↓ 0x000F3001	CATAG	Tag value for cascade input	0 (Unused)
		CAEN	Cascade enable	No cascade
		TAG	Channel tag	F (set with the same AD tag value inputted from AD)
		CMD	Filter processing selection	FIR 32TAP
		FMT	FIR input data format	16-bits signed fixed-points
		IEP	PH end interrupt	Prohibition
		IEE	Error interrupt	Prohibition
		IEC	Condition matching interrupt	Prohibition
		IEO	Data output interrupt	Prohibition
		CNSL	Condition matching interrupt 0/1 function selection	INT_DFE_CND0: Select the comparison matching interrupt request. (Unused) INT_DFE_CND1: Select the PH end interrupt request. (Unused)
		CNSLE	CNSL enable	CNSL bit setting disable
		AIME	Automatic initialization	Prohibition
		EN	Channel enable	Channel enable

Register Name	Setting Value	Bit Name	Function	Setting
Control register B (DFE0CTLBCH0) (DFE0CTLBCH1) (DFE0CTLBCH2)	0x01000002	OFSL	Compare offset value α selection	DFEjCPOFST0 register value selection (Unused)
		DISB	PH processing prohibition	PH processing prohibition
		PHPS	PH peak type selection	PH processing detects the upper limit peak. (Unused)
		CPCS	Compare value type selection	DFEjCPA to DFEjCPD are selected by DFEjCTLBCHn.SELB1. (Unused)
		PHSLB2	PH initial value register selection	DFEjPHIA register value is selected as the initial value of PH processing. (Unused)
		DISA	Accumulation/Decimation processing prohibition	Accumulation/Decimation processing prohibition
		PRCSC	Output data register floating point conversion	Not execute the floating-point conversion.
		SELB2	PH initial value register selection	Select PHIA register value to the initial value of PH processing.
		SELB1	Compare target register selection	Select CPA register value to the value of the compare calculation target. (Unused)
		PRCSB	PH circuit processing selection	Not PH processing and compare calculation processing.
		HOFS	Intermediate value output register floating-point conversion	Not execute the floating-point conversion.
		PICS	PH index register control selection	PH index update mode
		SELA	Accumulation/Decimation times register selection	Select ACA value
		PFMT	PH result register floating-point conversion	Not execute the floating-point conversion. ()Unused
		ABS	Absolute value calculation	Do not the absolute value calculation.
		PRCSA	Accumulation circuit processing selection	Execute the decimation processing
Control register C (DFE0CTLCCH0)	0x00000100	CA0E	C-ADC selection	Not use
		DAyE	DS-ADC selection	Channle0 is used.
		SAyE	SAR-ADC	Not use

			selection	
Control register C (DFE0CTLCCH1)	0x00000200	CA0E	C-ADC selection	Not use
		DAyE	DS-ADC selection	Channle1 is used.
		SAyE	SAR-ADC selection	Not use
Control register C (DFE0CTLCCH2)	0x00020000	CA0E	C-ADC selection	Not use
		DAyE	DS-ADC selection	Channle9 is used.
		SAyE	SAR-ADC selection	Not use
Accumulation/decimation times setting register A (DFE0ACA)	0x0000	AC	Accumulation/Decimation times	Not Accumulation/Decimation

Table 3-11 shows the register setting example of DFE_FIFO (Buffer A).

Table 3-11 Register setting example of DFE_FIFO (Buffer A).

Register Name	Setting Value	Bit Name	Function	Setting
Buffer A Common control register (DFBFACCTL)	0x00000003	AUNE	Buffer A data update flag enable	Not use the buffer A data update flag
		AIEE	Buffer A error Interrupt request enable	Disable
		AIEO	Buffer A output data update interrupt request enable	Enable
		AEN	Buffer A enable	Processing execution of buffer A
Buffer A control register (DFBFACTLCH0)	0x00000001	BFACH	Capture target channel selection	Set DFE0 ch0
		ADSL	Buffer A DFE selection	Select DFE0
		CHEN	Buffer A channel enable	Enable buffer A channel 0
Buffer A control register (DFBFACTLCH1)	0x00000101	BFACH	Capture target channel selection	Set DFE0 ch1
		ADSL	Buffer A DFE selection	Select DFE0
		CHEN	Buffer A channel enable	Enable buffer A channel 1
Buffer A control register (DFBFACTLCH2)	0x00000201	BFACH	Capture target channel selection	Set DFE0 ch2
		ADSL	Buffer A DFE selection	Select DFE0
		CHEN	Buffer A channel enable	Enable buffer A channel 2
Buffer A clear register (DFBFACLR)	0x00000001	CLRA	Buffer A clear	Buffer A FIFO clear

Table 3-12 shows the register setting example of ATU-VI (Timer G).

Table 3-12 Register Setting Example of ATU-VI (Timer G)

Register Name	Setting Value	Bit Name	Function	Setting
Prescaler register 1 (PSCR1)	0x0009	PSCx[9:0]	Set division ratio of prescaler	Set 1/10 (40MHz / 10)
Timer control register G1 (TCRG1)	0x10	CKSELGx[2:0]	Clock select	Use clock bus 1
		EVSYMGx	External event synchronization mode set	Standard count mode
Compare match register G1 (OCRG1)	0x00000020	OCRGx[31:0]	Specify compare match value	Set 8us
Timer interrupt enable register G (TIERG)	0x0002	CMPIEG9	Compare match interrupt enable G9	Disable
		CMPIEG8	Compare match interrupt enable G8	Disable
		CMPIEG7	Compare match interrupt enable G7	Disable
		CMPIEG6	Compare match interrupt enable G6	Disable
		CMPIEG5	Compare match interrupt enable G5	Disable
		CMPIEG4	Compare match interrupt enable G4	Disable
		CMPIEG3	Compare match interrupt enable G3	Disable
		CMPIEG2	Compare match interrupt enable G2	Disable
		CMPIEG1	Compare match interrupt enable G1	Disable
		CMPIEG0	Compare match interrupt enable G0	Disable
Timer status clear register G1 (TSCRG1)	0x03	OVFCGx	Overflow flag clear G1 enable	Flag clear
		CMFCGx	Overflow flag clear G1 enable	Flag clear
Timer FIFO Capture trigger selection (ATUDFESELD1T)	0x00000001	ATU_DFESEL_D1T[2:0]	Select timer FIFO capture trigger input	Set OCRG1 compare match interrupt

Register Name	Setting Value	Bit Name	Function	Setting
Timer start register G (TSTRG)	0x0002	STRG9	Counter G start bit	TCNTG9: Operating stop
		STRG8	Counter G start bit	TCNTG8: Operating stop
		STRG7	Counter G start bit	TCNTG7: Operating stop
		STRG6	Counter G start bit	TCNTG6: Operating stop
		STRG5	Counter G start bit	TCNTG5: Operating stop
		STRG4	Counter G start bit	TCNTG4: Operating stop
		STRG3	Counter G start bit	TCNTG3: Operating stop
		STRG2	Counter G start bit	TCNTG2: Operating stop
		STRG1	Counter G start bit	TCNTG1: Operating enable
		STRG0	Counter G start bit	TCNTG0: Operating stop
ATU master enable register (ATUENR)	0x81	TGE	Timer G enable bit	Timer G: Operating enable
		TFE	Timer F enable bit	Timer F: Operating stop
		TEE	Timer E enable bit	Timer E: Operating stop
		TDE	Timer D enable bit	Timer D: Operating stop
		TCE	Timer C enable bit	Timer C: Operating stop
		TBE	Timer B enable bit	Timer B: Operating stop
		TAE	Timer A enable bit	Timer A: Operating stop
		PSCE	Prescaler enable bit	Enable clock generation of prescaler

Table 3-13 shows the register setting example of sDMAC0.

Table 3-13 Register Setting Example of sDMAC0

Register Name	Setting Value	Bit Name	Function	Setting
DMA channel master setting register (DMA0CM_0)	0x00001C00	SPID[4:0]	Setting of channel master	SPID=0x1C(sDMAC0)
		UM	UM setting of channel master	Supervisor mode
DMA channel control register (DMA0CHCR_0)	0x0000 ↓ 0x0003	DPE	Descriptor enable bit	Descriptor disable
		DPB	Descriptor start bit	Start DMA transfer by register setting
		CAEE	Channel address error notification enable	Address error notification disable
		CAIE	Channel address error interrupt enable	Disable
		DSIE	Descriptor step end interrupt master enable	Disable
		IE	Transfer end interrupt enable	Disable ↓ Enable
		DE	DMA enable	DMA transfer disable ↓ DMA transfer enable
DMA source address register (DMA0SAR_0)	(unsigned long) &DFEFIFO.DFBFADOCH0.UINT32	SAR[31:0]	DMA transfer source address setting	Address of DFBFADOCH0 register
DMA destination address register (DMA0DAR_0)	(unsigned long) & fifo_data0[0]	DAR[31:0]	DMA transfer destination Address setting	Address of arrangement variable fifo_data0[0] for storing DFE processing result
DMA transfer size register (DMA0TSR_0)	0x0000000C	TSR[31:0]	Setting of DMA transfer size	12byte(=4byte×3 times)

Register Name	Setting Value	Bit Name	Function	Setting
DMA transfer mode register (DMA0TMR_0)	0x00001122	SLM[3:0]	DMA transfer low-speed mode	Normal mode
		PRI[3:0]	Channel request priority setting	Priority enable of channel request
		TRS	Transfer request source	Hardware request
		DM[1:0]	Destination address count direction	Fixed
		SM[1:0]	Source address count destination	Increment
		DTS[3:0]	DMA destination transaction size	4byte transfer
		STS[3:0]	DMA source transaction size	4byte transfer
DMA resource selection register (DMA0RS_0)	0x0003001E	TC[15:0]	Transfer times for each hardware request	3 times
		TL[2:0]	Transfer limitation for each hardware request	DMAjTMR_n.STS × DMAjRS_n.TC
		FPT	First preload trigger	(Unused)
		PLE	Preload Enable	Disable
		DRQI	Initialization of DMA request	DRQ(Hardware request status)initialization disable
		RS[7:0]	Hardware DMA transfer source selection	Buffer A capture end interrupt INTDFEFIFOOUTA (group 0-30)
DMA Scatter Internal address increment register (DMA0SIAI_0)	(unsigned long)&fifo_data1[0] – (unsigned long)&fifo_data0[0]	SIAI[31:0]	Destination address increment value of scatter internal loop	Arrangement variable, address of fifo_data1[0] to address of fifo_data0[0] for storing DFE processing results

Register Name	Setting Value	Bit Name	Function	Setting
DMA scatter gathering control register (DMA0SGCR_0)	0x80020000	SEN	Scatter enable	Scatter enable
		ZF	Zero fill	Disable
		SIRPT[13:0]	Repetition times of scatter internal DMA loop	2 times
		GEN	Gather Enable	Gather disable
		GIRPT[13:0]	Repetition times of gather internal DMA loop	(Unused)
DMA channel flag clear register (DMA0CHFCR_0)	0x0000320F	OVFC	Hardware transfer request overflow flag clear	Clear
		DRQC	Clearing of hardware transfer request	Clear
		DPEC	Descriptor enabling clear	Clear
		CAEC	Address error flag clear	Clear
		DSEC	Descriptor step end flag clear	Clear
		TEC	Transfer completion flag Clear	Clear
		DEC	DMA enabling clear	Clear
DMA operation register (DMA0OR)	0x0001	PR[1:0]	Priority between channels	CH0> CH1> ... > CH14> CH15
		DME	DMA master enable	DMA transfer enable for all channels

Table 3-14 shows the register setting example of INTC2.

Table 3-14 Register Setting Example of INTC2

Register Name	Setting Value	Bit Name	Function	Setting
EI level interrupt bind register (EIBD70)	0x00000000	CST	Broadcast interrupt enable	Disable
		BCP[1:0]	Setting for broad cast interrupt port number	(Unused)
		PEID[2:0]	Specify destination bound interrupt	PE0(CPU0)
EI level interrupt control register (EIC70)	0x0040	EICTn	Interrupt channel type bit	(Possible only read)
		EIRFn	Interrupt request flag	(Possible only read)
		EIMKn	Interrupt mask bit	Enable interrupt processing
		EITBn	Interrupt vector method selection	Table reference method
		EIPn	Specify interrupt priority	0 (Highest-priority)

3.4.5 Operation Flow

Figure 3-4 shows the software operation flow in this application example.

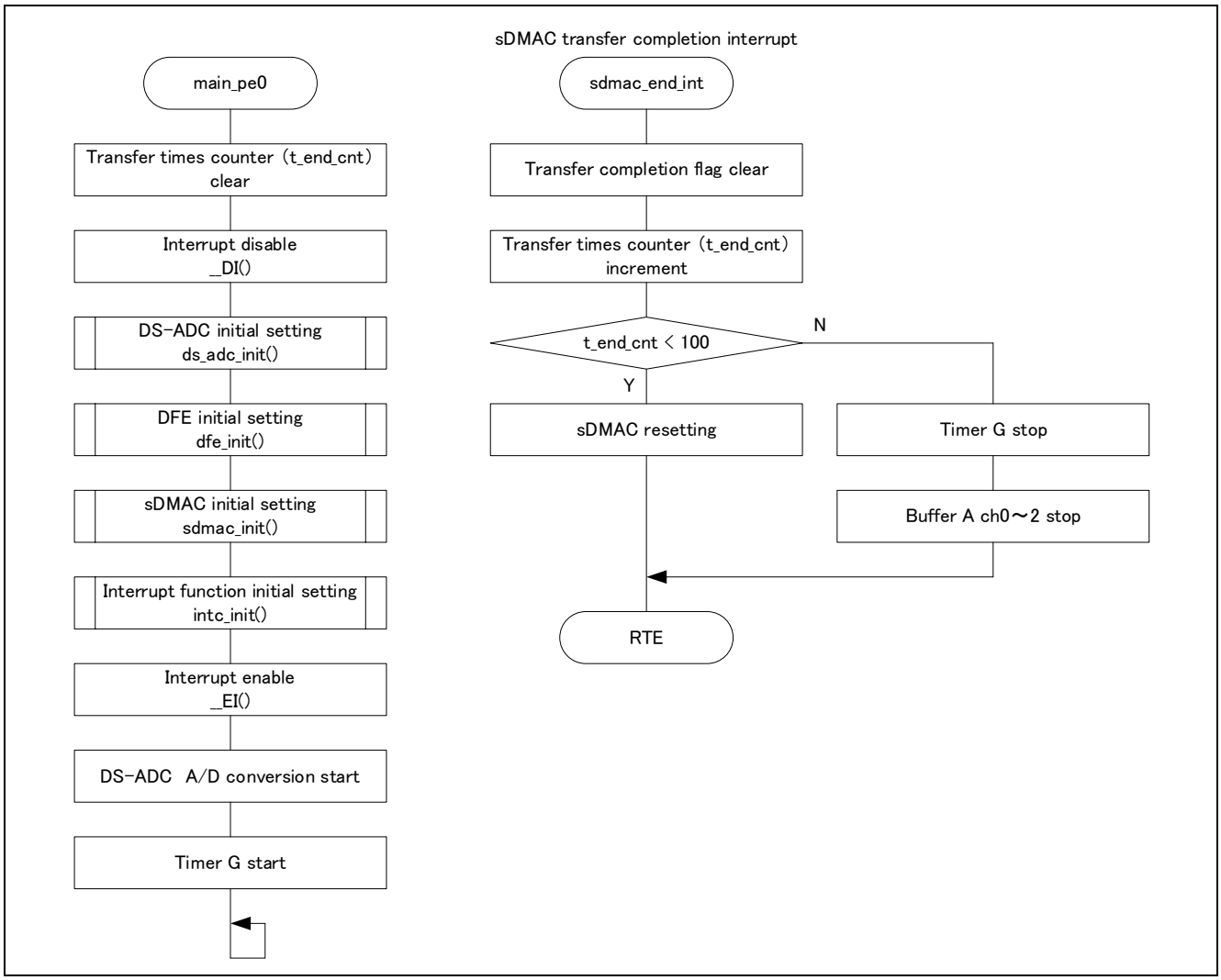

Figure 3-4 Software Operation Flow

4. Calculation between Channels by Subtraction Circuit

4.1 Specification

In this operation example, the applied voltage is A/D-converted to the DSAN000P and DSAN100P pins with the constant sampling rate by using DS-ADC (DSADC00 and DSADC10). The A/D conversion value is applied the filtering by the FIR filter in DFE0 ch0 and ch1. When the filtering is completed, the filtering result is subtracted in the subtraction circuit by the software trigger, and the subtraction result is stored to the local RAM by the DMA-conversion of sDMAC.

The specifications in this application example are shown below.

- DS-ADC (DSADC00 and DSADC10) continuously A/D-converts the analog input voltage by the single end input and the common voltage ADSVREFL.
- The A/D conversion value of DS-ADC (DSADC00 and DSADC10) automatically entries to DFE.
- The DFE filters the input data by the bandpass filter configured by the built-in FIR filter.
- The filter coefficient and data used for the FIR filter setting are stored to the RAM in DFE (coefficient memory and data memory).
- The filtering result of DFE does not perform the decimation processing (thinning).
- The filtering result of two channels are subtracted to use the subtraction circuit.
- The subtraction result is stored to the local RAM in sDMAC.
- Subtraction start trigger: Software trigger
- DS-ADC start trigger: Software trigger
- DS-ADC sampling rate: 200ksps
- DFE processing result output rate: 200kHz (No decimation processing)
- Input voltage range: 0 to ADSVCC (ADSVCC: analog power voltage 0 to + 5.5V)
- Output data format: number of 32 bits signed fixed point

Table 4-1 shows the filter specification example in this application example. The sampling frequency “fs” indicates the data inputting speed to DFE, and it means the sampling rate (200ksps) of DS-ADC in this application example.

Table 4-1 Filter Specification Example

Items	Description
Configuring filter	Bandpass filter
Sampling frequency fs	200ksps
Low-pass cut-offed frequency f_L	5kHz
High-pass cut-offed frequency f_H	15kHz
Bandpass ripple R_p	1dB
Bandstop attuation A_p	25dB

Figure 4-1 shows the system configuration diagram.

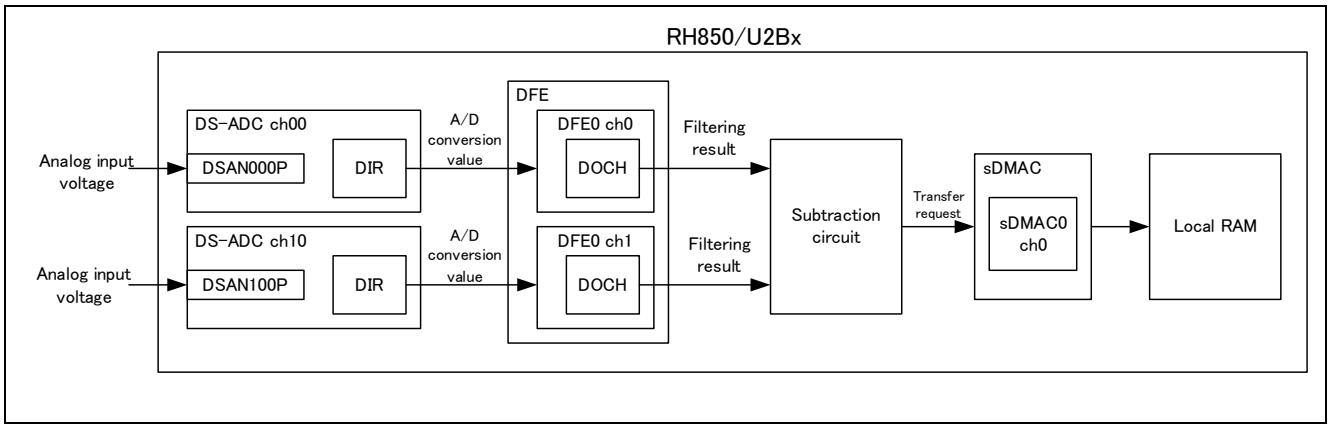

Figure 4-1 System Configuration Diagram

4.1.1 Use Function

The hardware functions of RH850/U2Bx using in this application note are shown below.

・ΔΣAD convertor (DS-ADC)	A/D convert the analog input signal.
・Digital filter (DFE)	Configure the bandpass filter by internal FIR filter and apply the filtering to the A/D conversion value of DS-ADC.
・Subtraction Circuit	Subtract the filtering result of the two channels.
・sDMAC	Transfer the subtraction result to the local RAM.
・Interrupt controller (INTC2)	Control the DFE output interrupt and the interrupt to CPU of the sDMAC transfer completion interrupt.

4.2 Explanation for Application Example

4.2.1 Operation Explanation

Figure 4-2 shows the operation explanation for this application example.

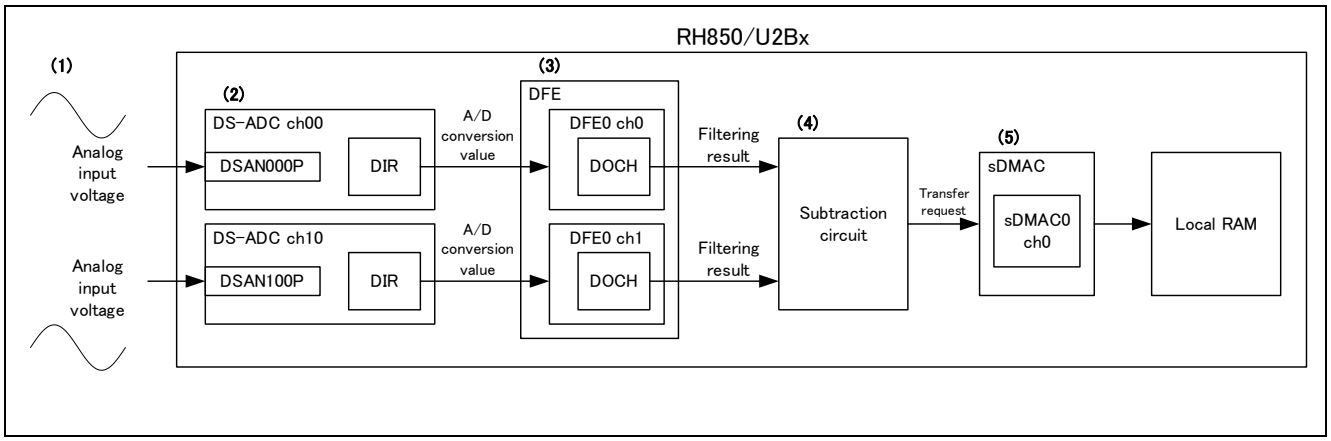

Figure 4-2 Operation Explanation

(1) Input each analog signal to DS-ADC ch00 and ch10 from the analog input signal.

(2) A/D-convert with the constant sampling cycle in each DS-ADC.

(3) Entry the A/D conversion result of DS-ADC to DFE and perform the filtering.

(4) For the filtering result of two channels, perform the subtraction in the subtraction circuit.

(5) Transfer the subtraction result to local RAM in sDMAC.

4.2.2 Operation Condition of Use Function

Table 4-2 shows the operation condition of DS-ADC used in this application example.

Table 4-2 DS-ADC Operation Condition

Items	Contents
Use channel	DSADC00, DSADC10
Analog input pin	DSAN000P, DSAN100P
Sampling rate	200ksps
Over sampling rate	8Msps
DFE entry	Entry
DFE-TAG	0, F
Gain	×1
Conversion type	Single end input
Common voltage	ADSVREFL
A/D conversion data format	Number of 16 bits signed fixed point
Effective bit	12bit

Table 4-3 the operation condition of DFE used in this application example.

Table 4-3 DFE Operation Condition

Items	Contents
Use channel	DFE0 ch0, ch1
Channel tag	0, F
Use filter	FIR
Taps	32
Input data format	Number of 16 bits signed fixed point
Coefficient data format	Number of 16 bits signed fixed point
Output data format	Number of 32 bits signed fixed point
Decimation times	No decimation processing
Peak-Hold processing	No PH processing

Table 4-4 shows the operation condition of sDMAC used in this application example.

Table 4-4 sDMAC Operation Condition

Items	Contents
sDMAC channel	sDMAC0 ch0
Channel master SPID	0
Channel master UM	Supervisor mode
sDMAC trigger source	Subtraction data output interrupt
Source address	Subtraction result register (SUBDOCH0)
Destination address	Local RAM
Source address count direction	Fixed
Destination address count direction	Increment
Transfer size	400byte
Transfer unit	4byte

4.3 Module Setting

4.3.1 DFE Setting

The DFE with built in RH850/U2Bx incorporates up to 64 taps FIR filter and up to sixth IIR filter.

In this operation example, the bandpass filter is configured by the FIR filer. The setting method of the register setting and the coefficient memory are explained below.

(1) Coefficient Memory Setting

Store the filter coefficient of FIR filter to the coefficient memory in DFE (CMEM). Refer to “1.3.2 Coefficient Memory Setting” for the details.

(2) Control Register Setting (Refer to “4.4.4 Explanation for Register” for the details of the register settings.)

CTLACH0 Register Setting

- Channel tag: 0
- Filter processing selection: FIR 32TAP
- Input data format selection: 16 bits signed fixed point
- Output data interrupt request disable

CTLACH1 Register Setting

- Channel tag: F
- Filter processing selection: FIR 32TAP
- Input data format selection: 16 bits signed fixed point
- Output data interrupt request disable

CTLBCH0 to 1 Register Setting

- Subtraction circuit processing selection: Select decimation processing

CTLCCH0 Register Setting

- Input selection: Select DS-ADC

ACA Register Setting

- Decimation times setting: No decimation processing

(3) Channel Enabling

Set CTLACH0 to 1.EN bit to “1”.

(4) Setting for Subtraction Circuit

SUBTRGCH0 Register Setting

- Subtraction start trigger: Soft trigger

SUBCTLCH0 Register Setting

- Subtraction setting: DFE0 ch0 to DFE0 ch1
- Subtraction data output interrupt: Enable
- Subtraction circuit: Enable

4.4 Software Explanation

4.4.1 Explanation for Function

Table 4-5 shows the used function in this application example.

Table 4-5 Explanation for Function

Function Name	Label Name	Contents
Main function	main_pe0	Perform the calling and the interrupt waiting of each function.
DFE output data interrupt function	dfe_end_int	Start subtraction. (Software trigger)
sDMAC transfer completion interrupt function	sdmac_end_int	Transfer completion interrupt function of sDMAC
DS-ADC feature initialize function	ds_adc_init	Perform the initial setting of DS-ADC(DSADC00, DSADC10).
DFE function initialize function	dfe_init	Perform the initial setting of DFE0 ch0 and ch1.
sDMAC feature initialize function	sdmac_init	Perform the initial setting of sDMAC0 ch0.
Interrupt features initialize function	intc_init	Perform the setting of the DFE data output interrupt and the transfer completion interrupt of sDMAC.

4.4.2 Explanation for Use Define Declaration

Table 4-6 shows the explanation of the define declaration used in this application example.

Table 4-6 Explanation for Used Define Declaration

Label Name	Function	Setting Value	Used Function Name
TAP_NUM	Indicate the number of the taps of FIR filter.	32	dfe_init

4.4.3 Explanation for Use Variable

Table 4-7 shows the explanation of the variable used in this application example.

Table 4-7 Explanation for Used Variable

Label Name	Function	Data length	Used Function Name
*cmem0[TAP_NUM/2]	Pointer variable that indicates the coefficient memory of DFE0 ch0.	signed long	dfe_init
*cmem1[TAP_NUM/2]	Pointer variable that indicates the coefficient memory of DFE0 ch1.	signed long	dfe_init
sub_data [100]	Store the subtraction result.	signed long	sdmac_init

4.4.4 Explanation for Register

Table 4-8 shows the register setting example of DS-ADC (DSADC00, DSADC10).

Table 4-8 Register Setting Example of DS-ADC (DSADC00, DSADC10)

Register Name	Setting Value	Bit Name	Function	Contents
■DS-ADC Common Register				
AD global control register (DSADCADGCR)	0x00	ODDE	Disconnecting detection function self-diagnosis	Disable
		ODE	Disconnecting detection	Disable
		UNSND	Conversion result output	Signed
Pin level self-diagnosis control register (DSADCTDCR)	0x00	TDE	Pin level self-diagnosis function	Disable
■DS-ADC Specific Register				
Unit control register (DSADC00UCR)	0x04000000	VPRSTE	Virtual channel pointer reset	None
		RDMA	Read gate DMA mode	Output the DMA conversion request for all A/D conversion result
		RESO0	High-accuracy mode	High impedance mode
		DFES	DFE channel selection	Select DFE0
		DFMT[3:0]	Data format	No mask
		VCEP[2:0]	End virtual channel pointer	0
Virtual channel control register (DSADC00VCR0)	0x00101000	GAIN[1:0]	Gain	×1
		VCULME	Upper slash hold notification	No notification
		VCLLME	Lower slash hold notification	No notification
		VCULLMTBS[1:0]	Threshold table selection	DSADCnULTBR0 (Unused)
		ORT	Rear filter 2nd stage output rate selection	1/2
		TPVSL[2:0]	TAP coefficient selection	Coefficient 1
		DSDFTYP[3:0]	Post filter type	Dependent on the setting of ORT and TPVSL.
		ADIE	Conversion completion interrupt	Disable
		ULEIE	Upper/Lower error interrupt	Disable
		DFENT	DFE entry	Entry
		DFTAG[3:0]	DFE-TAG	0
		CNVCLS[1:0]	Conversion type	Single end input,

				Common voltage=ADSVREFL
		GCTRL[3:0]	Input pin setting	DSAN000P

Register Name	Setting Value	Bit Name	Function	Contents
Virtual channel control register (DSADC10VCR0)	0x00101F00	FSELEXTE	Expansion Fs switching bit	No expansion
		GAIN[1:0]	Gain	×1
		VCULME	Upper limit threshold notification	No notification
		VCLLME	Lower limit threshold notification	No notification
		VCULLMTBS[1:0]	Threshold table selection	DSADCnULTBR0 (Unused)
		ORT	Rear filter 2nd stage output rate selection	1/2
		TPVSL[2:0]	TAP coefficient selection	Coefficient 1
		DSDFTYP[3:0]	Post filter type	Depend on ORT and TPVSL
		ADIE	Conversion completion interrupt	Disable
		ULEIE	Upper/Lower error interrupt	Disable
		DFENT	DFE entry	Entry
		DFTAG[3:0]	DFE-TAG	F
		CNVCLS[1:0]	Conversion type	Sigle end input, common voltage=ADSVREFL
		GCTRL[3:0]	Input pin setting	DSAN100P
Safety control register (DSADC00SFTCR) (DSADC10SFTCR)	0x00	RDCLRE	Lead & clear enable	Not clear
		OWEIE	Overwrite error interrupt	Prohibit
		PEIE	Parity error interrupt	Prohibit
		IDEIE	ID error interrupt	Prohibit
Upper/Lower limit table register (DSADC00ULTBR0 to 3)	0x7FFF8000	ULMTB[15:0]	Upper limit table	Unused (initial value)
		LLMTB[15:0]	Lower limit table	Unused (initial value)
Upper/Lower table register (DSADC10ULTBR0 to 1)	0x7FFF8000	ULMTB[15:0]	Upper limit table	Unused (initial value)
		LLMTB[15:0]	Upper limit table	Unused (initial value)

Register Name	Setting Value	Bit Name	Function	Contents
Pin level self-diagnosis level register (DSADC00TDLVR) (DSADC10TDLVR)	0x00	AN3NLV	Pin level self-diagnosis level specification	Unused (initial value)
		AN3PLV	Pin level self-diagnosis level specification	Unused (initial value)
		AN2NLV	Pin level self-diagnosis level specification	Unused (initial value)
		AN2PLV	Pin level self-diagnosis level specification	Unused (initial value)
		AN1NLV	Pin level self-diagnosis level specification	Unused (initial value)
		AN1PLV	Pin level self-diagnosis level specification	Unused (initial value)
		AN0NLV	Pin level self-diagnosis level specification	Unused (initial value)
		AN0PLV	Pin level self-diagnosis level specification	Unused (initial value)
Virtual channel pointer register (DSADC10 VCPTRR) (DSADC21 VCPTRR)	0x00	VCPTR[2:0]	Virtual channel number of A/D converting	Clear to 0
AD conversion trigger control register (DSADC00ADTCR) (DSADC10ADTCR)	0x40	ADSTTE	AD synchronization start enable	ADSTART enable
		ENDTRGE	AD end trigger enable	AD end trigger disable
		STTRGE	AD start trigger enable	AD start trigger disable
AD synchronization start control register AD (DSADCSYNSTCR)	0x01	ADSTART	A/D conversion start of each ΔΣADC	A/D conversion start

Table 4-9 shows the register setting example of DFE0.

Table 4-9 Register Setting Example of DFE0

Register Name	Setting Value	Bit Name	Function	Contents
Control register A (DFE0CTLACH0)	0x00003000 ↓ 0x00003001	CATAG	Tag value for cascade input	0 (Unused)
		CAEN	Cascade enable	No cascade
		CAENL	Cascade enable	No cascade
		TAG	Channel tag	0 (Set same value with the AD tag value inputted by AD.)
		CMD	Filter processing selection	FIR 32TAP
		IEF	Filter end interrupt	Disabled
		FMT	FIR input data format	16 bits signed fixed point
		IEP	PH end interrupt	Prohibit
		IEE	Error interrupt	Prohibit
		IEC	Condition match interrupt	Prohibit
		IEO	Data output interrupt	Prohibit
		CNSL	Condition matching interrupt 0/1 function selection	INT_DFE_CND0: Select the compare matching interrupt request. (Unused) INT_DFE_CND1: Select the PH end interrupt request. (Unused)
		CNSLE	CNSL enable	Disable CNSL nit disable
		AIME	Automatic initialization	Prohibit
		EN	Channel enable	Channel enable

Register Name	Setting Value	Bit Name	Function	Contents
Control register A （DFE0CTLACH1）	0x000F3010 ↓ 0x000F3011	CATAG	Tag value for cascade input	0 (Unused)
		CAEN	Cascade enable	No cascade
		TAG	Channel tag	F (Set same value with the AD tag value inputted by AD.)
		CMD	Filter processing selection	FIR 32TAP
		FMT	FIR input data format	16 bits signed fixed point
		IEP	PH end interrupt	Prohibit
		IEE	Error interrupt	Prohibit
		IEC	Condition match interrupt	Prohibit
		IEO	Output data interrupt	Enable
		CNSL	Condition matching interrupt 0/1 function selection	INT_DFE_CND0: Select the compare matching interrupt request. (Unused) INT_DFE_CND1: Select the PH end interrupt request. (Unused)
		CNSLE	CNSL enable	Disable CNSL nit disable
		AIME	Automatic initialization	Prohibit
		EN	Channel enable	Channel enable

Register Name	Setting Value	Bit Name	Function	Contents
Control register B (DFE0CTLBCH0) (DFE0CTLBCH1)	0x01000002	OFSL	Comparison offset value α selection	DFEjCPOFST0 register value selection (Unused)
		DISB	PH processing prohibition	PH processing prohibition
		PHPS	PH peak type selection	PH processing detects upper limit peak (unused).
		CPCS	Comparison value type selection	Select DFEjCPA to DFEjCPD by DFEjCTLBCHn.SELB1(unused).
		PHSLB2	PH initial value register selection	DFEjPHIA register value is selected as initial value of PH processing (unused).
		DISA	Accumulation /Decimation processing prohibition	Accumulation /Decimation processing prohibition
		PRCSC	Output data register floating-point conversion	Not execute floating-point conversion
		SELB2	PH initial value register selection	Select PHIA register value to initial value of PH processing (unused).
		SELB1	Comparison target register selection	Select CPA register value to value of comparison calculation target (unused).
		PRCSB	PH circuit processing selection	Not perform PH processing and comparison calculation processing.
		HOFS	Intermediate value output register floating-point conversion	Not execute floating-point conversion
		PICS	PH index register control selection	PH index update mode
		SELA	Accumulation /Decimation times register selection	Select value of ACA
		PFMT	PH result register floating-point conversion	Not execute floating-point conversion (unused).
		ABS	Absolute value calculation	Not calculate absolute value
		PRCSA	Accumulation circuit processing selection	Execute decimation processing

Control register C (DFE0CTLCCH0)	0x00000100	CA0E	C-ADC selection	Not use
		DAyE	DS-ADC selection	Use channel 0
		SAyE	SAR-ADC selection	Not use
Control register C (DFE0CTLCCH1)	0x00000200	CA0E	C-ADC selection	Not use
		DAyE	DS-ADC selection	Use channel 1
		SAyE	SAR-ADC selection	Not use
Accumulation/Decimation times setting register A (DFE0ACA)	0x0000	AC	Accumulation /Decimation times	Not calculate/ decimate

Table 4-10 shows the register setting of the subtraction circuit.

Table 4-10 Setting Example of Subtraction Register

Register Name	Setting Value	Bit Name	Function	Contents
Subtraction trigger register (SUBTRGCH0)	0x00000080	SBFE	Subtraction end flag trigger setting	Not generate
		SBE	Subtraction start flag trigger setting	Generate by software trigger
		SBT	Timer trigger selection of subtraction start flag and subtraction end flag	(Not use timer)
Subtraction control register （SUBCTLCH0）	0x00000013	CATAG	Cascade tag	(Unused)
		CAEN	Cascade enable	Prohibition
		MINCH	Minuend channel selection	Channel 0
		SUBCH	Subtrahend channel selection	Channel 1
		SFMT	Subtrahend result floating-point conversion	Not convert floating-point
		SIEE	Subtrahend error interrupt request	Prohibit
		SIEO	Subtrahend data output interrupt	Enable
		SEN	Subtrahend channel enable	Execute subtraction processing

Table 4-1 shows the register setting example of sDMAC0.

Table 4-11 Register Setting Example of sDMAC0

Register Name	Setting Value	Bit Name	Function	Contents
DMA channel master setting register (DMA0CM_0)	0x00001C00	SPID[4:0]	Setting of channel master SPID	SPID=0x1C(sDMAC0)
		UM	UM setting of channel master	Supervisor mode
DMA channel control register (DMA0CHCR_0)	0x0000 ↓ 0x0003	DPE	Descriptor enable bit	Descriptor mode
		DPB	Descriptor start bit	Start DMA transfer by register setting
		CAEE	Channel address error notification enable	Address error notification disable
		CAIE	Channel address error interrupt enable	Prohibit
		DSIE	Descriptor step end interrupt master enable	Prohibit
		IE	Transfer end interrupt enable	Prohibit ↓ Permit
		DE	DMA enable	DMA transfer prohibit ↓ DMA transfer permit
DMA source address register (DMA0SAR_0)	(unsigned long) &DFE0.SUBDOCH0.UINT32	SAR[31:0]	DMA transfer source address setting	Address of SUBDOCH0 register
DMA destination address register (DMA0DAR_0)	(unsigned long) &sub_data[0]	DAR[31:0]	DMA transfer source address setting	Address of array variable sub_data [0] for subtraction result storing
DMA transfer size register (DMA0TSR_0)	0x00000190	TSR[31:0]	Setting of DMA transfer size	400byte (=4byte×100 times)

Register Name	Setting Value	Bit Name	Function	Contents
DMA transfer mode register (DMA0TMR_0)	0x00001422	SLM[3:0]	DMA transfer low-speed mode	Normal mode
		PRI[3:0]	Channel request priority setting	Priority disable of channel request
		TRS	Transfer request source	Hardware request
		DM[1:0]	Destination address count direction	Increment
		SM[1:0]	Source address count direction	Fixed
		DTS[3:0]	DMA destination transaction size	4byte transfer
		STS[3:0]	DMA source transaction size	4byte transfer
DMA resource selection register (DMA0RS_0)	0x00010014	TC[15:0]	Transfer times for each hardware request	1 time
		TL[2:0]	Transfer limitation for each hardware request	DMAjTMR_n.STS × DMAjRS_n.TC
		FPT	First preload trigger	(Unused)
		PLE	Preload enable	Prohibit
		DRQI	Initialization of DMA request	DRQ (Hardware request Status) initialization prohibition
		RS[7:0]	Hardware DMA transfer source selection	Subtraction data output interrupt INTDFE0SUBOUT0 (group 0-20)
DMA channel flag clear register (DMA0CHFCR_0)	0x0000320F	OVFC	Hardware transfer request overflow flag clear	Clear
		DRQC	Clear of hardware transfer request	Clear
		DPEC	Descriptor enable clear	Clear
		CAEC	Address error flag clear	Clear
		DSEC	Descriptor step end flag clear	Clear
		TEC	Transfer completion flag clear	Clear
		DEC	DMA enable clear	Clear

Register Name	Setting Value	Bit Name	Function	Contents
DMA operation register （DMA0OR）	0x0001	PR[1:0]	Priority between channels	CH0> CH1> ... > CH14> CH15
		DME	DMA master enable	DMA transfer enable for all channels

Table 4-12 shows the register setting example of INTC2.

Table 4-12 Register Setting Example of INTC2

Register Name	Setting Value	Bit Name	Function	Contents
EI level interrupt bind register (EIBD506) (EIBD70)	0x00000000	CST	Broadcast interrupt enable	Disable
		BCP[1:0]	Setting of broad cast interrupt port number	(Unused)
		PEID[2:0]	Specify the destination bound (requested) the interrupt	PE0(CPU0)
EI level interrupt control register (EIC506) (EIC70)	0x0040	EICTn	Interrupt channel type bit	(Possible only lead)
		EIRFn	Interrupt request flag	(Possible only lead)
		EIMKn	Interrupt mask bit	Enable interrupt processing
		EITBn	Interrupt vector method selection	Table reference method
		EIPn	Specify the interrupt priority	0 (High-priority)

4.4.5 Operation Flow

Figure 4-3 shows the software operation flow in this allocation example.

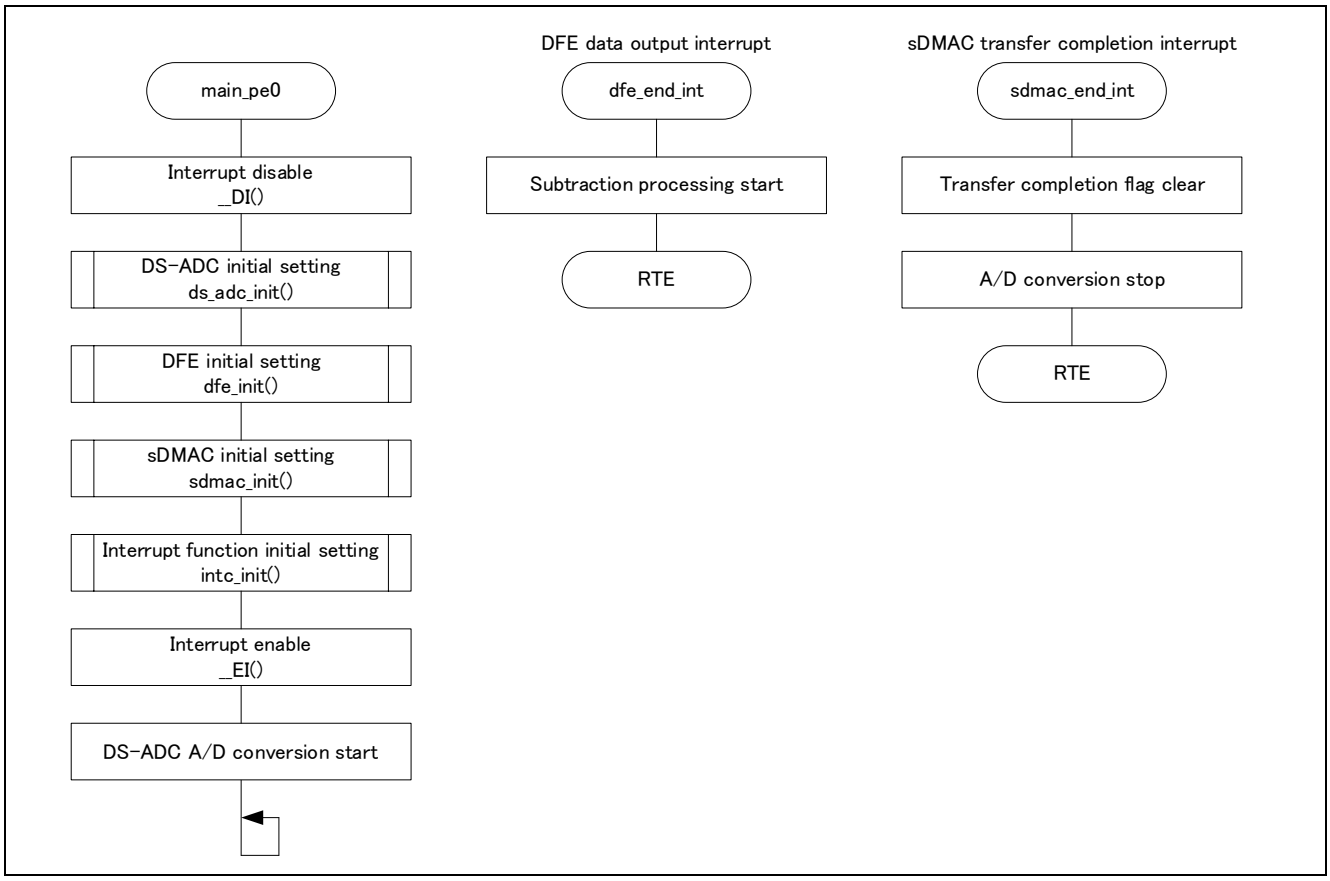

Figure 4-3 Software Operation Flow

5. Diagnosis Example for Digital Filter

5.1 Specification

In this self-diagnosis, the sim waveform generated by the software is inputted to DFE and the output result is stored to the local RAM. The diagnosis for DFE is performed to compare the result with the expected value of DFE conversion result and check if the expected result is obtained.

The specifications in this diagnosis example are shown below.

- DFE performs the filtering processing for the input data by the bandpass filter configured by the internal FIR filter (Taps: 32).
- The filter coefficient and the data used for the FIR filter setting are stored to the RAM (coefficient memory and data memory) in DFE.
- As the data example for the diagnosis inputted to DFE, the data that the 30khz sin waveform sampled 300 times by the sampling rate 100khz is used.
- The filter processing result for DFE is not performed the decimation processing.
- The input data for DFE is written to the software input register (DI) in CPU. Whether the next input data can be written to DI is determined by the VALID bit in the status register (STCH0).
- The output result for DFE is read from the output data register (DOCH0) in CPU and stored to the local RAM. Whether the next output data is written to DOCH0 is determined by the DOEN bit in the status register (STCH0).
- The DFE output result stored to the local RAM area and the previously prepared expected value are compared. Refer to “5.5 DFE Output Result Expected Value” for the data to be compared.
- Output data format: Number of 32 bits signed fixed-point

Table 5-1 shows the filter specification example to be the diagnosis target in this diagnosis example.

Table 5-1 Filter Specification Example

Item	Content
Configuration filter	Bandpass filter
Sampling waveform fs	100ksps
Low-pass cutoff frequency f_L	5kHz
High-pass cutoff frequency f_H	15kHz
Bandpass ripple R_p	1dB
Bandstop attenuation A_p	25dB

Figure 5-1 shows the system configuration diagram.

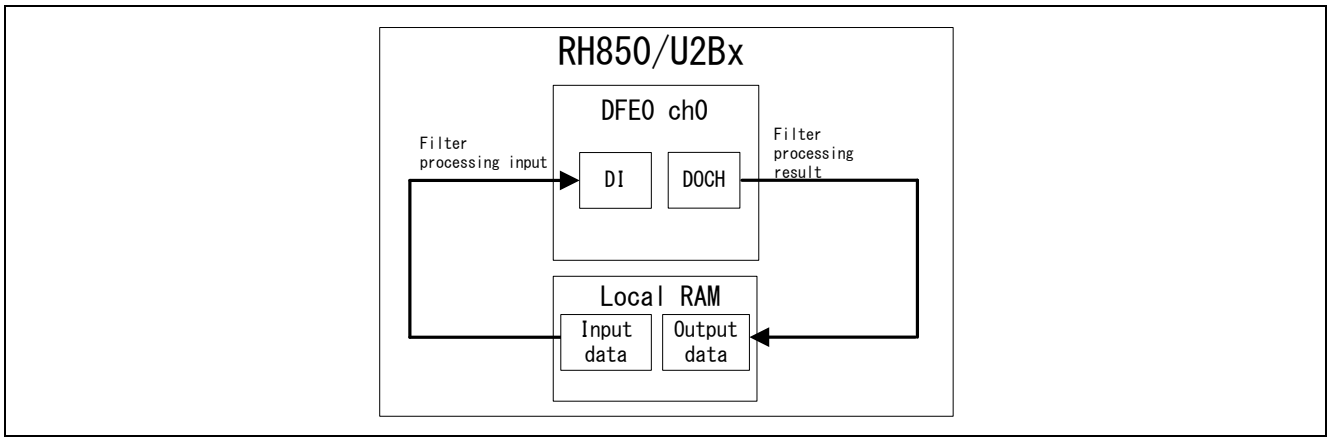

Figure 5-1 System Configuration Diagram

5.1.1 Use Function

The hardware function for RH850/U2Bx used in this application note is shown below.

・Digital filter (DFE) It configure the bandpass filter by the internal FIR filter and applies the filter processing to the software input value.

5.2 Explanation for Application Example

5.2.1 Operation Explanation

A sequence of the operation is explained separately as the hardware processing and the software processing.

(1) Software Processing

①Interrupt disable

②DFE function initialization

③Interrupt enable

④DFE input data generation

⑤Write the DFE input data to software input data register

⑥Read the data in the output data register

⑦Repeat the above ⑤⑥ processing 300 times

⑧Compare the DFE output data with the expected value data

(2) DFE0 ch0 Processing

①The filter processing is started to feed the data from the software input data register to DFE0 ch0

②If the processing of DFE0 ch0, the output result is read form the output data register

5.2.2 Operation Condition of Use Function

Refer to Table3-1 in “1.2.2 Operation Condition of Use Function” for the operation condition of DFE.

5.3 Module Setting

5.3.1 DFE Setting

Refer to “1.3.1 DFE Setting” for DFE setting.

Coefficient Memory Setting

Table 5-2 shows the filter coefficient of the filter (Table 5-1) for the diagnosis target.

Table 5-2 Filter Coefficient Example

TAP number(n)	Filter coefficient (16 bits fixed point format notation)
0	1184
1	710
2	674
3	106
4	-826
5	-1391
6	-1051
7	-194
8	90
9	-916
10	-2706
11	-3798
12	-2888
13	76
14	3770
15	6288
16	6288
17	3770
18	76
19	-2888
20	-3798
21	-2706
22	-916
23	90
24	-194
25	-1051
26	-1391
27	-826
28	-106
29	674
30	-710
31	1184

5.4 Software Explanation

5.4.1 Explanation for Function

Table 5-3 shows the used function in this application example.

Table 5-3 Explanation for Function

Function Name	Label Name	Description
Maine function	main_pe0	Write the DFE input data for each function and read the output data. Add, compare the output data with the expected value data.
DFE feature initialization function	dfe_init	Perform the initial setting of DFE0 ch0.
DFE input data making function	DFE_Input_data	Make the data inputted to DFE0.

5.4.2 Explanation for Used Define Declaration

Table 5-4 shows the explanation for the used define declaration in this application example.

Table 5-4 Explanation for Used Define Declaration

Label Name	Function	Setting Value	Used Function Name
TAP_NUM	Indicate the taps of FIR filter.	32	dfe_Init
PLOT_NUM	Indicate the times sampled in the frequency (30khz).	300	main_pe0、DFE_Input_data
DI_TIMEOUT_CNT	Indicate the software input data register writing timeout or the reading timeout of the output data register.	32	main_pe0
DFE_CHECK_INDEX_TOP	Indicate the comparison start index of the frequency (30kHz) to be the data comparison target.	31	main_pe0
DFE_CHECK_INDEX_LAST	Indicate the comparison end index of the frequency (30kHz) to be the data comparison target.	300	main_pe0

5.4.3 Explanation for Used Variable

Table 5-5 shows the explanation for the variables used in this application note.

Table 5-5 Explanation for Used Variable

Label Name	Function	Data Length	Used Function Name
*cmem0[TAP_NUM/2]	The pointer variable that indicates the coefficient memory of DFE ch0.	unsigned long	dfe_Init
input_data[PLOT_NUM]	Store the input data of DFE.	signed short	main_pe0、DFE_Input_data
smp_data[PLOT_NUM]	Store the output result of DFE.	signed long	main_pe0
DFE_TimeoutFlag	Indicates whether the software input data register write timeout or the output data register read timeout has generated. 0=Not generated timeout 1=Generated timeout	int	main_pe0
DFE_TestNgFlag	Compare the DFE output data with the expected value data and indicate whether they are matched. 0=Matched the result 1=Not matched	int	main_pe0
DfeCompCheckData[PLOT_NUM]	Expected value of DFE output data	signed long	main_pe0

5.4.4 Register Explanation

Table 5-6 shows the register setting example of DFE0.

Table 5-6 Register Setting Example of DFE0

Register Name	Setting Value	Bit Name	Function	Contents
Control register A (DFE0CTLACH0)	0x00003000 ↓ 0x00003001	CATAG	Tag value for cascade input	0 (unused)
		CAEN	Cascade enable	Not cascade
		CAENL	Cascade enable	Not cascade
		TAG	Channel tag	0 (Set the same value with the AD tag value inputted form AD)
		CMD	Filter processing selection	FIR 32TAP
		IEF	Filter end interrupt	Prohibit
		FMT	FIR input data format	16 bits fixed point
		IEP	PH end interrupt	Prohibit
		IEE	Error interrupt	Prohibit
		IEC	Condition match interrupt	Prohibit
		IEO	Data output interrupt	Prohibit
		CNSL	Condition match interrupt 0/1 function selection	INT_DFE_CND0: Select comparison matching interrupt request (unused) INT_DFE_CND1: Select PH end interrupt request (unused)
		CNSLE	CNSL enable	Setting disable of CNSL bit
		AIME	Automatic initialization	Prohibit
		EN	Channel enable	Channel enable

Register Name	Setting Value	Bit Name	Function	Contents
Control register B (DFE0CTLBCH0)	0x01000002	OFSL	Comparison offset value α selection	DFEjCPOFST0 register value selection (unused)
		DISB	PH processing disable	PH processing prohibition
		PHPS	PH peak type selection	PH processing detects the upper peak (unused)
		CPCS	Comparison value type selection	DFEjCPA to DFEjCPD are selected by DFEjCTLBCHn.SELB1 (unused)
		PHSLB2	PH initial value register selection	DFEjPHIA register value is selected as the initial value of PH processing.
		DISA	Accumulation/Decimation processing disable	Accumulation/Decimation processing prohibition
		PRCSC	Output data register floating-point conversion	Not execute the floating-point conversion
		SELB2	PH initial value register selection	Select PHIA register value as the initial value of PH processing (unused)
		SELB1	Comparison target register selection	Select CPA register value to comparison calculation target value (unused)
		PRCSB	PH circuit processing selection	Not perform PH processing and comparison calculation processing
		HOFS	Intermediate value output register floating-point conversion	Not execute floating-point conversion
		PICS	PH index register control selection	PH index update mode
		SELA	Accumulation/Decimation times register selection	Select value of ACA
		PFMT	PH result register floating-point conversion	Not execute floating-point conversion (unused)
		ABS	Absolute value calculation	Not calculate the absolute value
		PRCSA	Accumulation circuit processing selection	Execute decimation processing
Accumulation/Decimat	0x0000	AC	Accumulation/Dec	Not

ion times setting register A (DFE0ACA)			imation times	accumulation/decimation

5.4.5 Operation Flow

Table 5-2 shows the software operation flow in this application example.

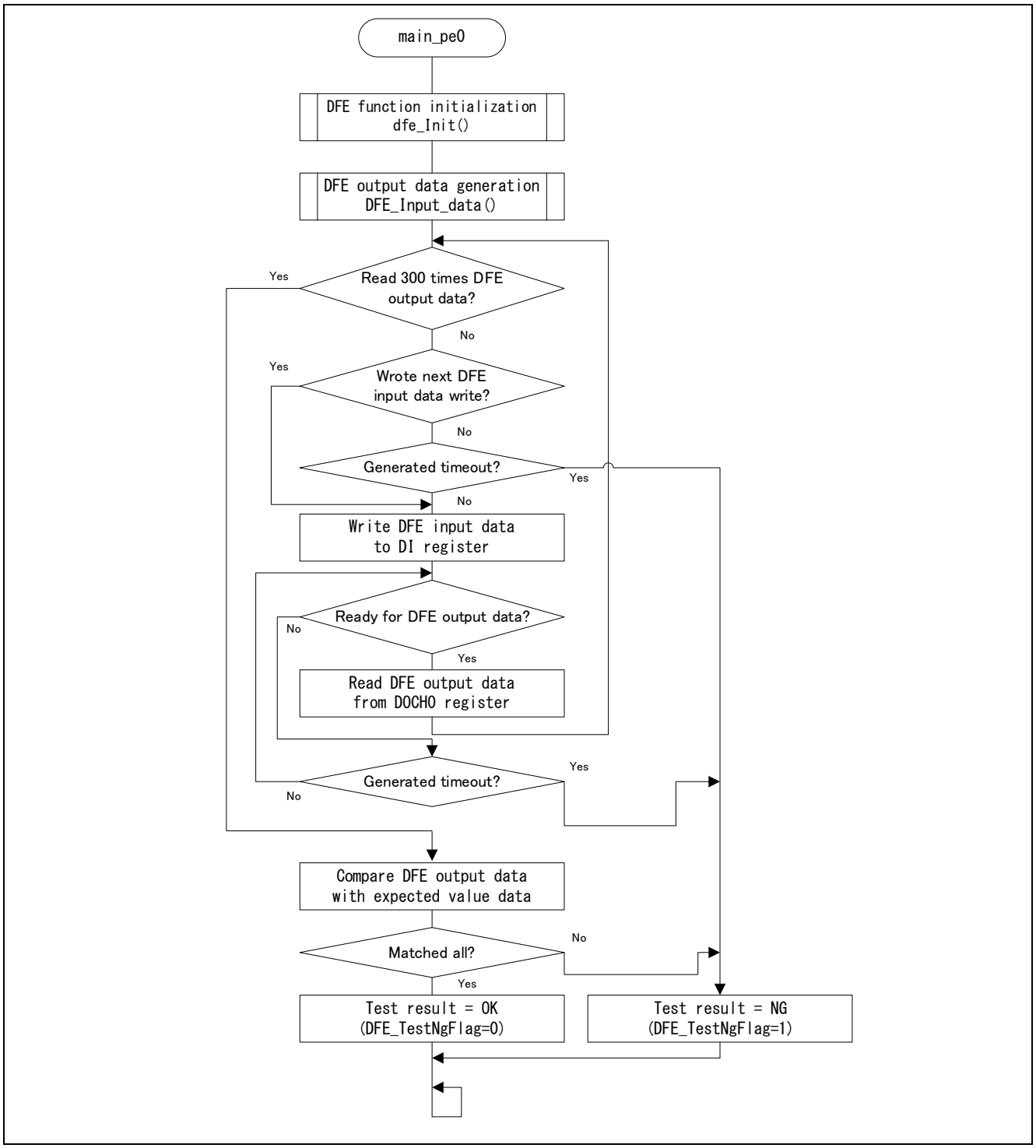

Figure 5-2 Software Operation Flow

5.5 DFE Output Result Expected Value

Table 5-7 shows the expected value data (300) compared with the DFE output result. The 31 data from the beginning (gray part) is out of comparison since the DFE processing is performed in 32Tap.

Table 5-7 DFE Output Result Expected Value

Sampling No	Value	Sampling No	Value	Sampling No	Value
0	-72131792	100	-57788148	200	-57783856
1	-94494326	101	-14393204	201	-14444528
2	-67542428	102	66676232	202	66667424
3	107083196	103	-26816292	203	-26789104
4	31568164	104	-50104504	204	-50118068
5	-123687902	105	57784480	205	57788324
6	-35078956	106	14393704	206	14454672
7	15502210	107	-66679606	207	-66664670
8	-30376402	108	26812996	208	26788012
9	102890254	109	50102362	209	50121550
10	92405796	110	-57793976	210	-57788742
11	30779454	111	-14411952	211	-14457930
12	46637858	112	66666368	212	66659772
13	-136766916	113	-26820578	213	-26793460
14	-181851058	114	-50107112	214	-50135232
15	-28606986	115	57796882	215	57778998
16	-46252040	116	14419948	216	14447346
17	-39636494	117	-66662572	217	-66665016
18	154673508	118	26824344	218	26793884
19	108498900	119	50113204	219	50137212
20	-71152772	120	-57792066	220	-57768366
21	26230710	121	-14415226	221	-14438598
22	57034702	122	66665164	222	66674510
23	-94346820	123	-26818664	223	-26783392
24	23584550	124	-50107912	224	-50133078
25	144115084	125	57790842	225	57770046
26	-66333764	126	14410950	226	14444530
27	-82141448	127	-66672168	227	-66673744
28	118596606	128	26808220	228	26780680
29	-42429198	129	50105700	229	50137996
30	-36290204	130	-57788396	230	-57766528
31	-14401328	131	-14411484	231	-14445736
32	66655384	132	66675256	232	66670738
33	-26832700	133	-26812804	233	-26791546
34	-50115698	134	-50114174	234	-50149444
35	57774654	135	57784786	235	57759404
36	14401060	136	14417556	236	14443396
37	-66660020	137	-66665002	237	-66673654
38	26819750	138	26820096	238	26780784
39	50102092	139	50118078	239	50136990
40	-57787154	140	-57784280	240	-57765824
41	-14408216	141	-14421456	241	-14444136
42	66660920	142	66662458	242	66681580
43	-26814080	143	-26816484	243	-26761508
44	-50087148	144	-50118506	244	-50124068

45	57800180	145	57781924	245	57775864
46	14415932	146	14415364	246	14456144
47	-66659600	147	-66670384	247	-66679830
48	26806348	148	26804040	248	26769184
49	50085912	149	50116728	249	50132346
50	-57799344	150	-57778134	250	-57768206
51	-14412200	151	-14417454	251	-14457650
52	66658912	152	66675230	252	66665380
53	-26812914	153	-26806492	253	-26779854
54	-50099836	154	-50120454	254	-50151942
55	57784162	155	57779292	255	57745396
56	14404480	156	14419024	256	14447856
57	-66654662	157	-66669068	257	-66666028
58	26827552	158	26812332	258	26769934
59	50113996	159	50130956	259	50147096
60	-57770786	160	-57773540	260	-57729256
61	-14400968	161	-14418404	261	-14444078
62	66652354	162	66670904	262	66664952
63	-26832144	163	-26813552	263	-26760130
64	-50118694	164	-50125468	264	-50139292
65	57765876	165	57774348	265	57733074
66	14394928	166	14420368	266	14462120
67	-66661310	167	-66671620	267	-66644942
68	26826764	168	26802944	268	26756008
69	50118058	169	50117200	269	50133068
70	-57765428	170	-57786560	270	-57732542
71	-14387468	171	-14437008	271	-14473880
72	66672792	172	66665332	272	66635342
73	-26818510	173	-26800348	273	-26748346
74	-50116178	174	-50115972	274	-50124044
75	57767492	175	57790430	275	57728004
76	14388500	176	14438890	276	14475760
77	-66670104	177	-66666336	277	-66634908
78	26827026	178	26807556	278	26733178
79	50115804	179	50128204	279	50116110
80	-57774728	180	-57777594	280	-57718896
81	-14399622	181	-14426332	281	-14470824
82	66661296	182	66671862	282	66639798
83	-26837572	183	-26806100	283	-26729490
84	-50113274	184	-50133016	284	-50114890
85	57786426	185	57766942	285	57717240
86	14410326	186	14422494	286	14455408
87	-66656156	187	-66671768	287	-66644066
88	26837856	188	26801292	288	26735284
89	50108096	189	50134212	289	50115036
90	-57793716	190	-57773064	290	-57720684
91	-14413484	191	-14437436	291	-14444212
92	66658782	192	66662932	292	66636046
93	-26833590	193	-26802472	293	-26746750
94	-50105532	194	-50131482	294	-50111774
95	57794478	195	57782002	295	57727084
96	14407182	196	14445676	296	14456188

97	-66668414	197	-66663280	297	-66619834
98	26822438	198	26800548	298	26766346
99	50107684	199	50126300	299	50108932

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Revision History

Rev.	Date	Description	
		Page	Description
1.00	2023.10.5	—	Initial edition

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2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

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(Rev.5.0-1 October 2020)

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