RH850/U2B6

R/D Converter (RDC3AL)

Introduction

This application note describes the examples of operation using the R/D (resolver/digital) converter (RDC3AL) of RH850/U2B6.

Examples of tasks and applications described in this application note have been verified. However, before using this R/D converter, be sure to check operating environment.

Target Device

This application note applies to RH850/U2B6.

Contents

1. Introduction

This application note describes how to use the R/D (resolver/digital) converter (RDC3AL) of RH850/U2B6.

1.1 Feature Used

The RH850/U2B6 hardware feature used in this application note is shown below.

- R/D (resolver/digital) converter (RDC3AL)

2. R/D Converter Basics

2.1 Resolver and Resolver Digital Converter

2.1.1 The Usage of Resolver

A resolver is used where an angle sensor is required to be operated under the severe environment condition.

Major usage : Detecting angle for automobile use, aerospace, factory, and other severe environment.

A resolver is also used for control motors mounted on engine of HV and EV in the automobile field.

Figure 2-1 shows an example of the brushless DC motor control using a resolver and an R/D converter.

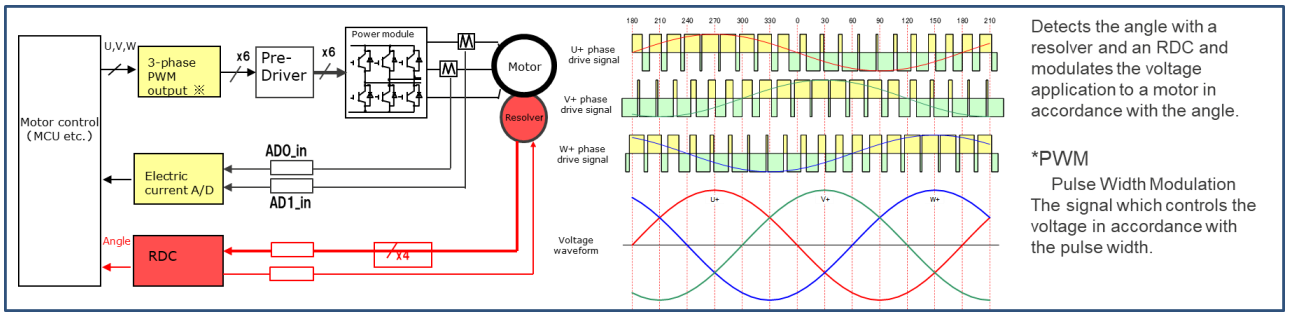


Figure 2-1 Brushless DC Motor Control

2.1.2 The Mechanism of Resolver

A resolver is a sensor used to detect the angle of the rotating shaft. The schematic diagram is shown in Figure 2-2. It is an analog device that has 2 excitation signal input pins (Ex+, Ex-) and 4 angle signal output pins (S1,S3,S2,S4). By inputting the AC signal into excitation signal input pins, signals including angle information can be obtained from angle signal output pins.

Signals output from angle signal output pins are converted to the digital angle (resolver angle : θ) with an R/D converter. The connection between S1-S3, S2-S4, and Ex+-Ex- are windings and thus short-circuited in terms of DC.

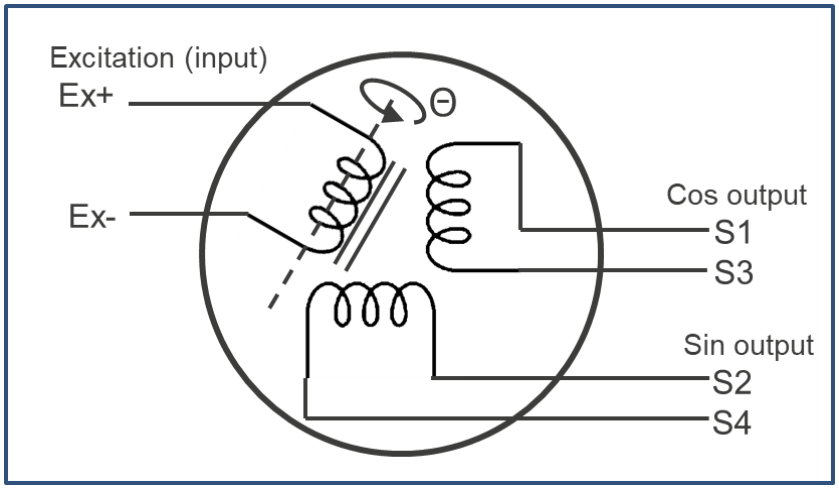


Figure 2-2 Mechanism of Resolver

A resolver operates as a variable coupling transformer which varies the amount of magnetic couplings between the primary winding(excitation) and the 2 secondary windings (Cos output, Sin output) according to the angle of the rotating shaft.

The excitation signal (input) : $f(\omega t)=(Ex+)-Ex(-)=E1 \cdot Sin(\omega t)$ Frequency (ω) ~10kHz

The Cos signal (output) : $S1-S3 = k \cdot Cos(\theta) \times f(\omega t)$

The Sin signal (output) : $S2-S4 = k \cdot Sin(\theta) \times f(\omega t)$ **Θ= The shaft angle**

2.1.3 Connecting Resolver and R/D Converter

The connection required for obtaining an angle from a resolver is shown in Figure 2-3.

A resolver receives the excitation signal which is output from either the reference signal generation circuit in an R/D converter or the sine wave generation circuit, and the R/D converter receives the output from the resolver. Generally, the differential amplifier receives outputs by considering noise immunity. Sometimes, the differential amplifier is incorporated in an R/D converter. When an R/D converter does not have any reference signal generating functions, the reference signal is input to the R/D converter and the excitation buffer amplifier from the outside.

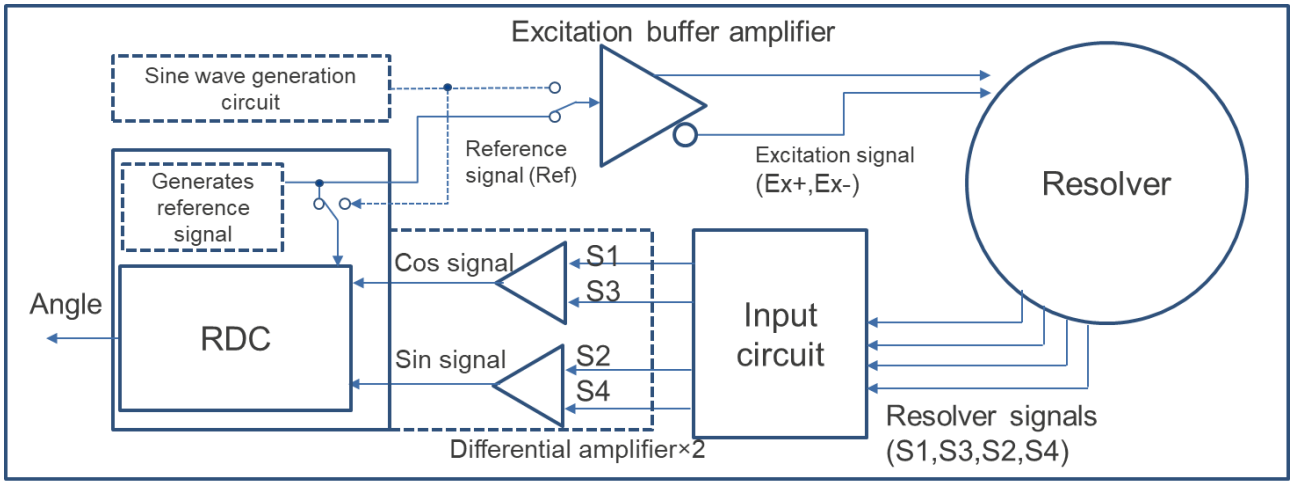


Figure 2-3 Connecting Resolver and R/D Converter

An example of the excitation signal input to a resolver and obtained resolver signals is shown in Figure 2-4.

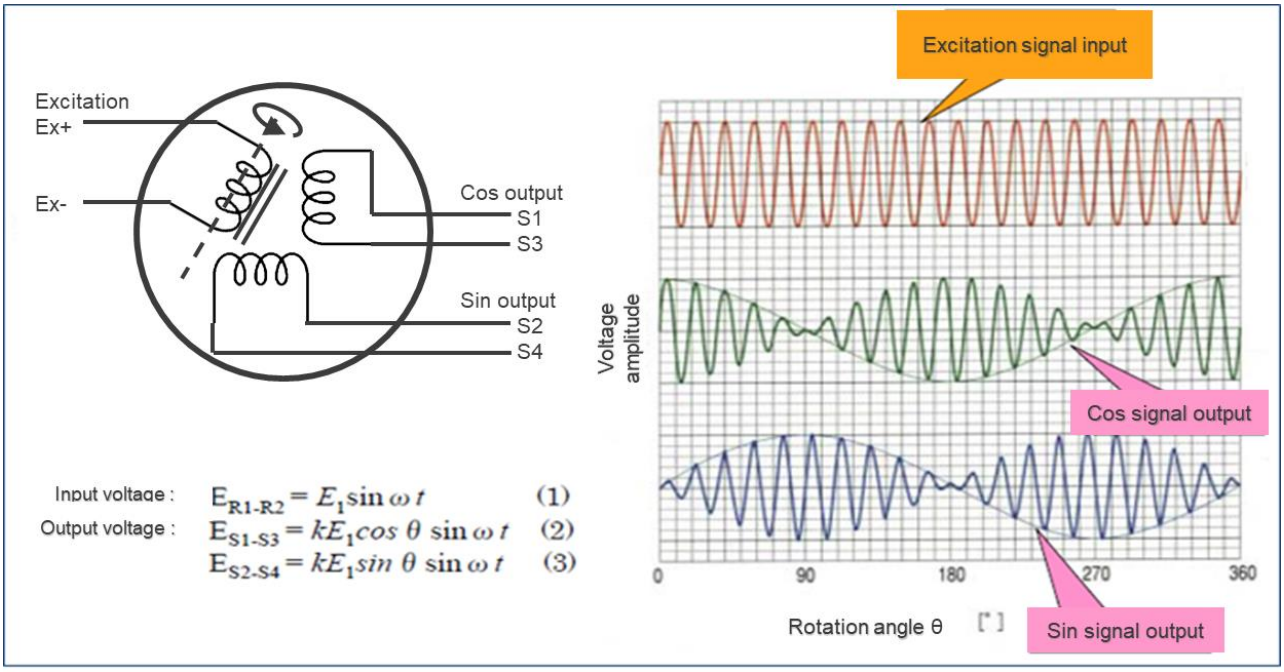


Figure 2-4 Output/Input Signal of Resolver

2.2 The Mechanism of R/D Converter

2.2.1 The Concept of R/D Converter

An R/D converter detects the resolver angle by using the resolver output signal (Cos signal and Sin signal), the reference signal, and the tracking loop which has an angle feedback. Figure 2-5 shows the schematic chart of R/D converter.

The difference between the resolver output signal and the preceding output angle is calculated as a deviation. The increase or decrease of the output angle is determined by the sign of the deviation.

When the output angle is correct (input angle θ = output angle Φ), the deviation ε becomes 0.

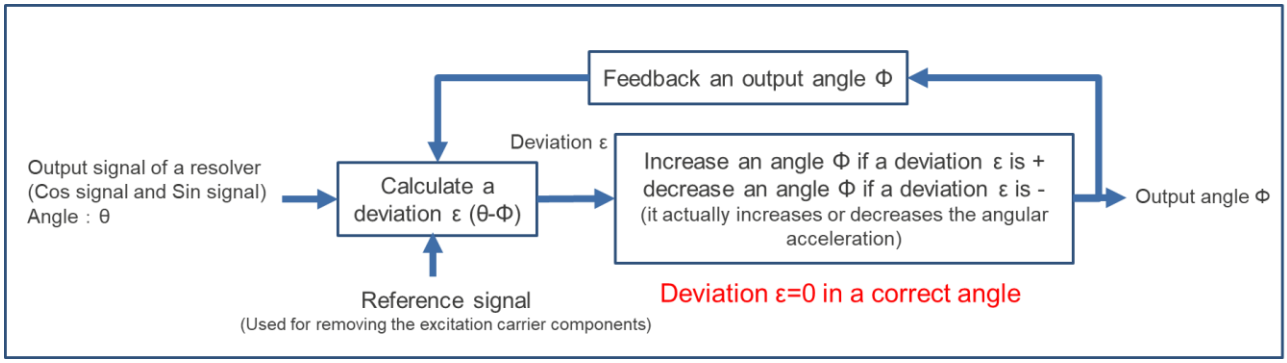


Figure 2-5 Concept of R/D Converter

2.2.2 The actual operation of an R/D converter

An R/D converter calculates digital angles from Cos signals and Sin signals and reference signals.

The feedback loop is designed as shown in Figure 2-6 Feedback Loop of an R/D Converter so as to eliminate the difference between the angle of input signal(θ) and the internal holding angle (Φ). (Type II feedback loop)

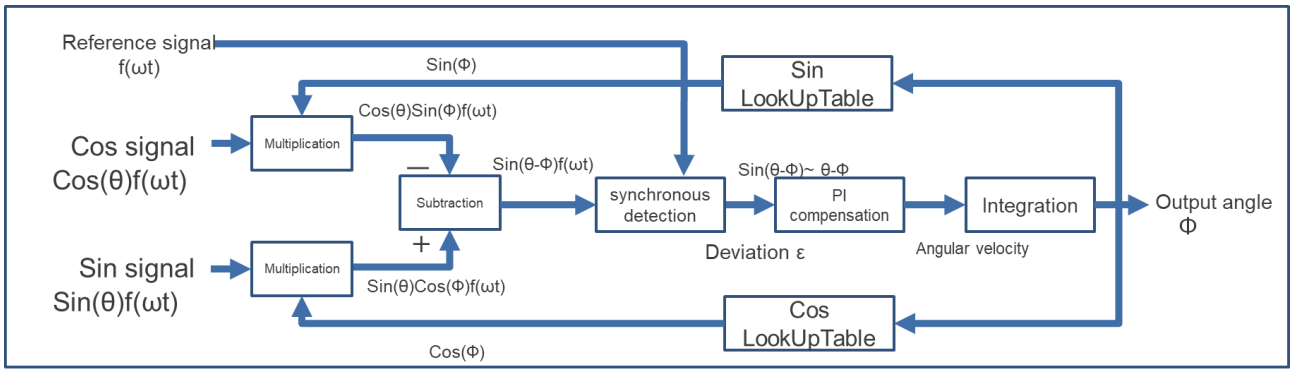


Figure 2-6 Feedback Loop of an R/D Converter

An R/D converter calculates an angle using the principle below.

Multiplies Cos signal and Sin table in a Look Up Table $Cos(\theta)\cdot f(\omega t)\cdot Sin(\Phi)$ -(1)

Multiplies Sin signal and Cos table in a Look Up Table $Sin(\theta)\cdot f(\omega t)\cdot Cos(\Phi)$ -(2)

Calculates (2)-(1) $(Sin(\theta)\cdot f(\omega t)\cdot Cos(\Phi))-(Cos(\theta)\cdot f(\omega t)\cdot Sin(\Phi))$

$= ((Sin(\theta)\cdot Cos(\Phi))-(Cos(\theta)\cdot Sin(\Phi)))\cdot f(\omega t)$

Since $(Sin(\theta)\cdot Cos(\Phi))-(Cos(\theta)\cdot Sin(\Phi)) = Sin(\theta-\Phi)$

$= Sin(\theta-\Phi)\cdot f(\omega t) \sim (\theta-\Phi)\cdot f(\omega t)$ -(3)

Eliminates f(ωt) with the synchronous detection by using the input f(ωt)

$(\theta-\Phi)\cdot f(\omega t) \rightarrow \theta-\Phi = \varepsilon$ -(4)

ε is the control deviation in this control loop. The negative feedback control provides feedback so that the control deviation becomes 0. When θ = Φ, the analog angle information from a resolver has been converted to the digital angle Φ.

Sets the response speed with the PI compensator in a loop.

2.2.3 Setting the R/D Converter Bandwidth

The bandwidth of the PI compensator needs to be set when an R/D converter is used. The bandwidth is expressed by the frequency. When a higher frequency is set, the response will be quicker but easily influenced by other factors such as noise. On the other hand, when a lower frequency is set, the response will be slower but has higher immunity toward noise and the R/D converter output becomes more stable. For the R/D converter mounted on the Renesas MCU, the default is 800Hz, but it can be changed.

Some R/D converters have a function to set the bandwidth automatically. When this function is used, the bandwidth is set low when the resolver is stable, and it is set high automatically when the quick response is required such as at acceleration. The R/D converters mounted on the Renesas MCU have an auto-adjusted function.

The bandwidth setting of an R/D converter has influence on response speed for acceleration and angle step but has no influence on the maximum speed of when a resolver is rotating stationary. For example, when the bandwidth is set low (around 200Hz), if a resolver is slowly accelerated, it can be tracked even the final speed is high (for example 1000Hz=60000rpm). Also, when a resolver is rotating stationary at high speed, the inside of the R/D converter remains stationary (ε is small) and the bandwidth is set low in auto-adjust.

Figure 2.7 shows the difference in output by the bandwidth of PI compensator setting.

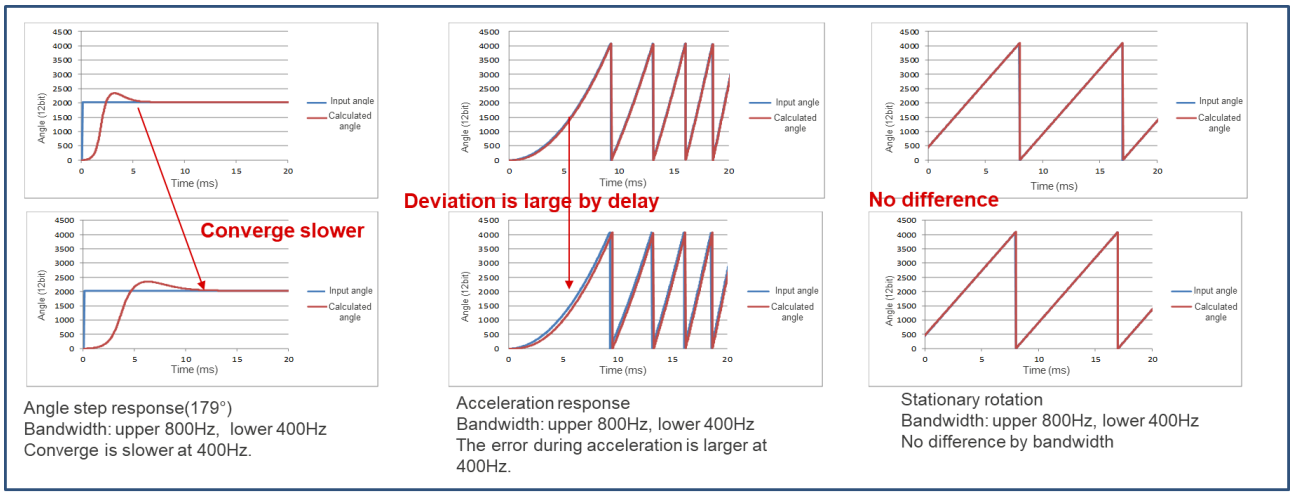


Figure 2-7 Output Change by the Bandwidth Change of PI Compensator

2.3 Additional Information

2.3.1 The Handling of Angles in the Motor Control

In the brushless DC motor control, the input voltage into a motor is varied according to the shaft angle of the motor.
It should be noted that the mechanical shaft angle of a motor (mechanical angle), the output angle of a resolver (resolver angle) and the angle which determines the voltage applied to a motor (electrical angle) are not always equal depending on number of poles. The definitions of terms in this document are as follows.

- Mechanical angle — The mechanical shaft angle of a motor
- Resolver angle — The angle output from an R/D converter
- Electrical angle — The angle which determines the voltage applied to a motor
- The number of resolver poles — The ratio of mechanical angle to resolver angle (mechanical angle : resolver angle=1 : the number of resolver poles)
- The number of motor pole pairs — The ratio of mechanical angle to electrical angle (mechanical angle : electrical angle=1 : the number of motor pole pairs)

Example : When the number of resolver poles is 2 and the number of motor pole pairs is 4.

> When the mechanical shaft rotates once, the resolver angle rotates twice and the voltage to the motor rotates 4 times. In this case, the controller device doubles the resolver angle (number of motor pole pairs/number of resolver poles) and calculates the applied voltage to the motor. The number of poles needs to be considered for the angular offset.

The reason for increasing the number of motor pole pairs in the brushless DC motor is because it enables the increase of the torque(rotation power of the motor). Since the number of poles of the VR resolver is more than 2, the mechanical angle, the electrical angle and the resolver angle are usually not equal. On the other hand, when the number of resolver poles and the number of motor pole pairs are same, the electrical angle and the resolver angle become equal.

Figure 2-8 shows an example of the angular relation when the number of resolver poles =2, the number of motor pole pairs=4.

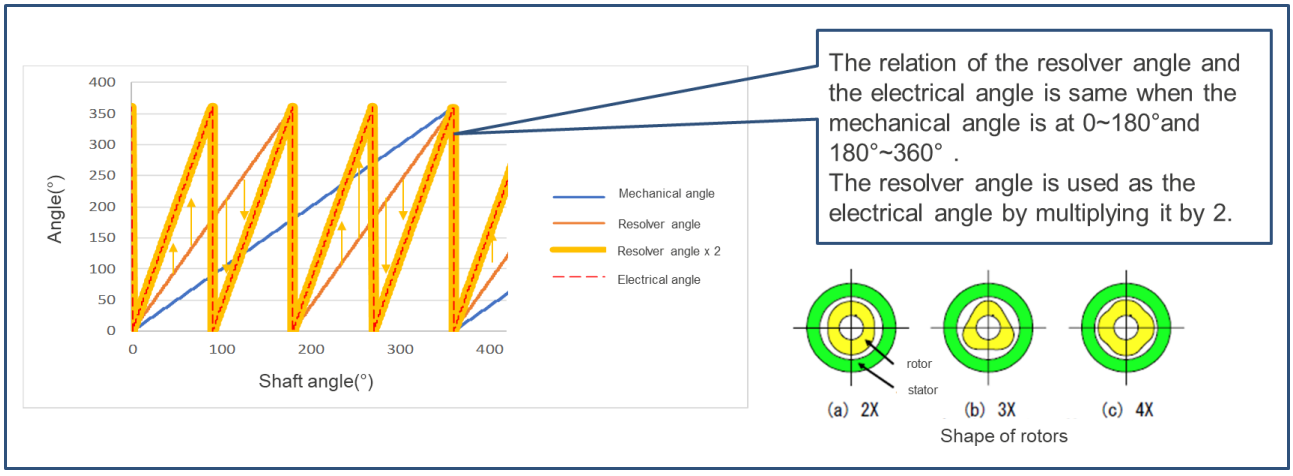


Figure 2-8 Relationship between Pole and Angle

When the number of resolver poles is large, the absolute value of the mechanical angle cannot be determined.(The mechanical angle X degree and X + 180degree cannot be distinguished.)

For the motor control, the relative angle can be used for the rotation control as long as the number of motor pole pairs ≥ the number of resolver poles. For the VR resolver, the number of poles is always more than 2 because of its mechanism.

2.3.2 Occurrence of Errors/Occurrence Factors

When the input signal of an RDC is not ideal, error will occur in angle calculation. The main factors of errors are as follows.

- The amplitude of Sin signal and Cos signal is not aligned
- The offset is added to Sin signal or Cos signal.
- There is a large phase difference between Sin signal, Cos signal, and Ref signal.
- Sin signal and/or Cos signal are distorted.
- The resolver is attached inclined.

When error is caused by above factors, there are many cases where error has a cycle per rotation. Figure 2-9 shows the calculated angle when the amplitude of Sin signal and Cos signal do not match. It can be seen that two error cycles are occurring in one rotation.

When an error is seen in the calculated angle, it is required to take measures such as investigating the cause and correcting it.

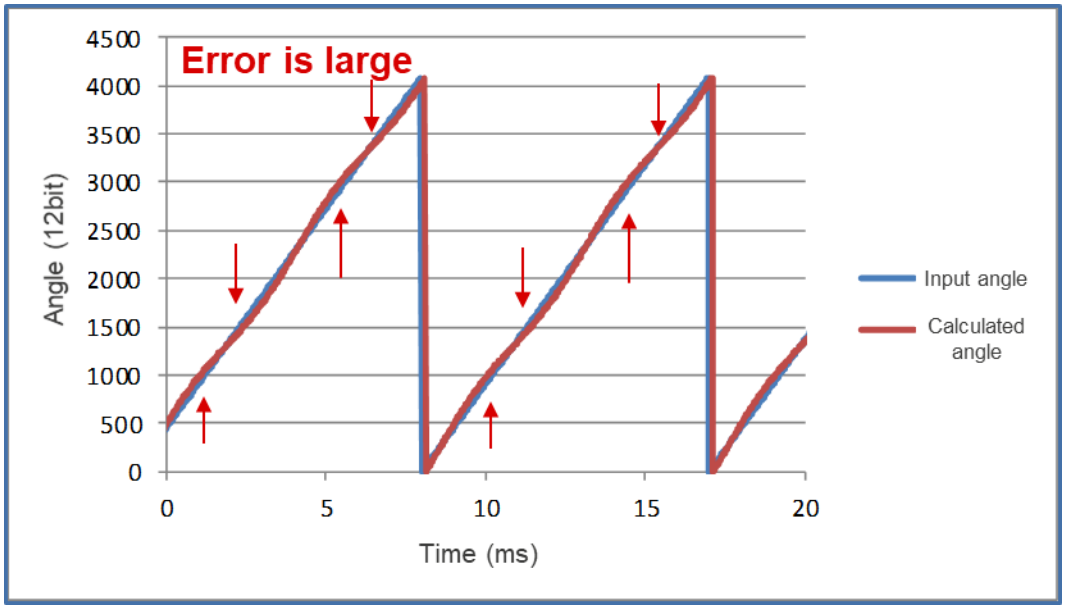


Figure 2-9 Calculated Angle When Amplitude Does Not Match

3. How to Use RDC3AL

3.1 Initialization Flow

Perform the initialization according to the flowchart below.

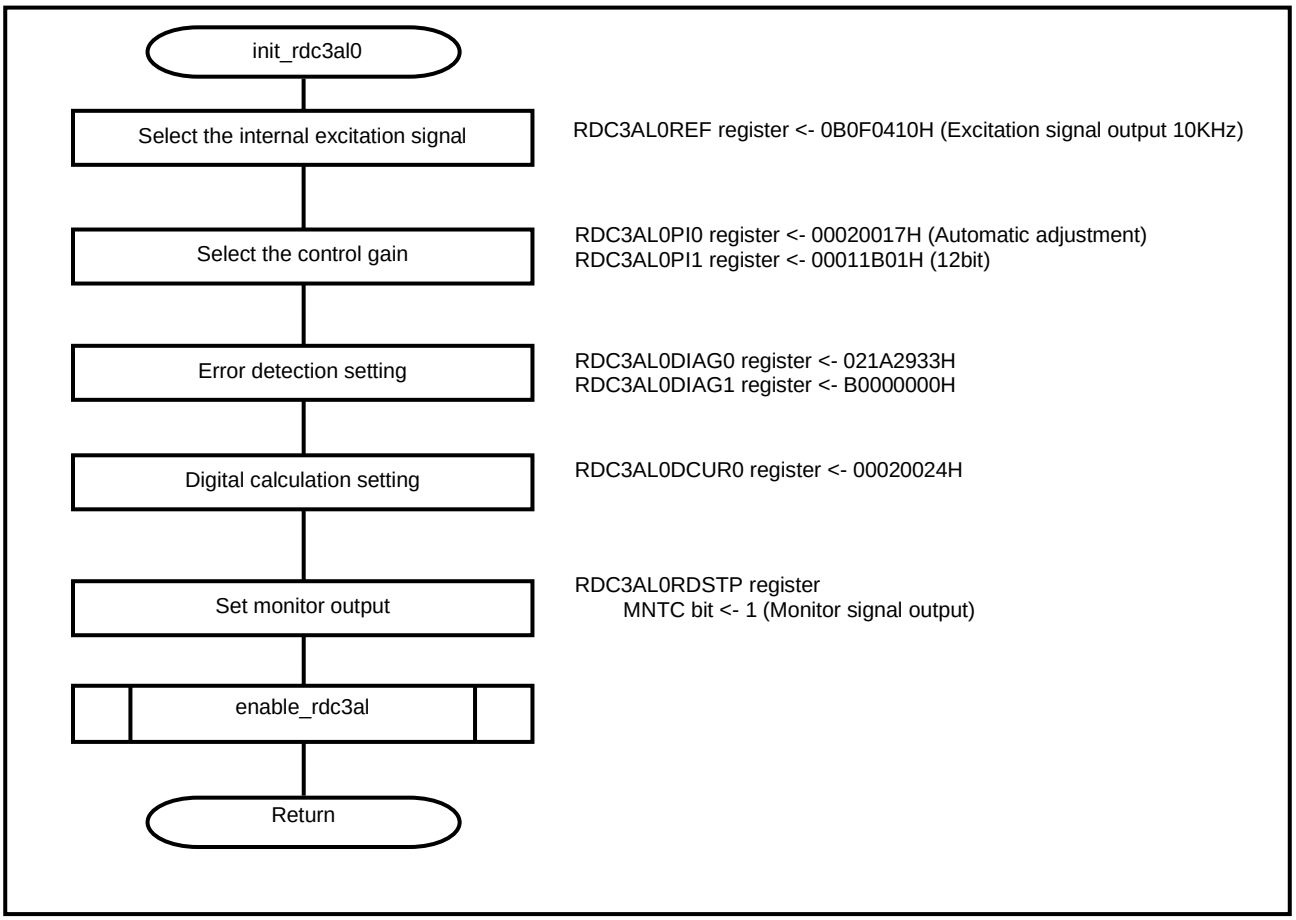


Figure 3-1 Operation Flow (1/2)

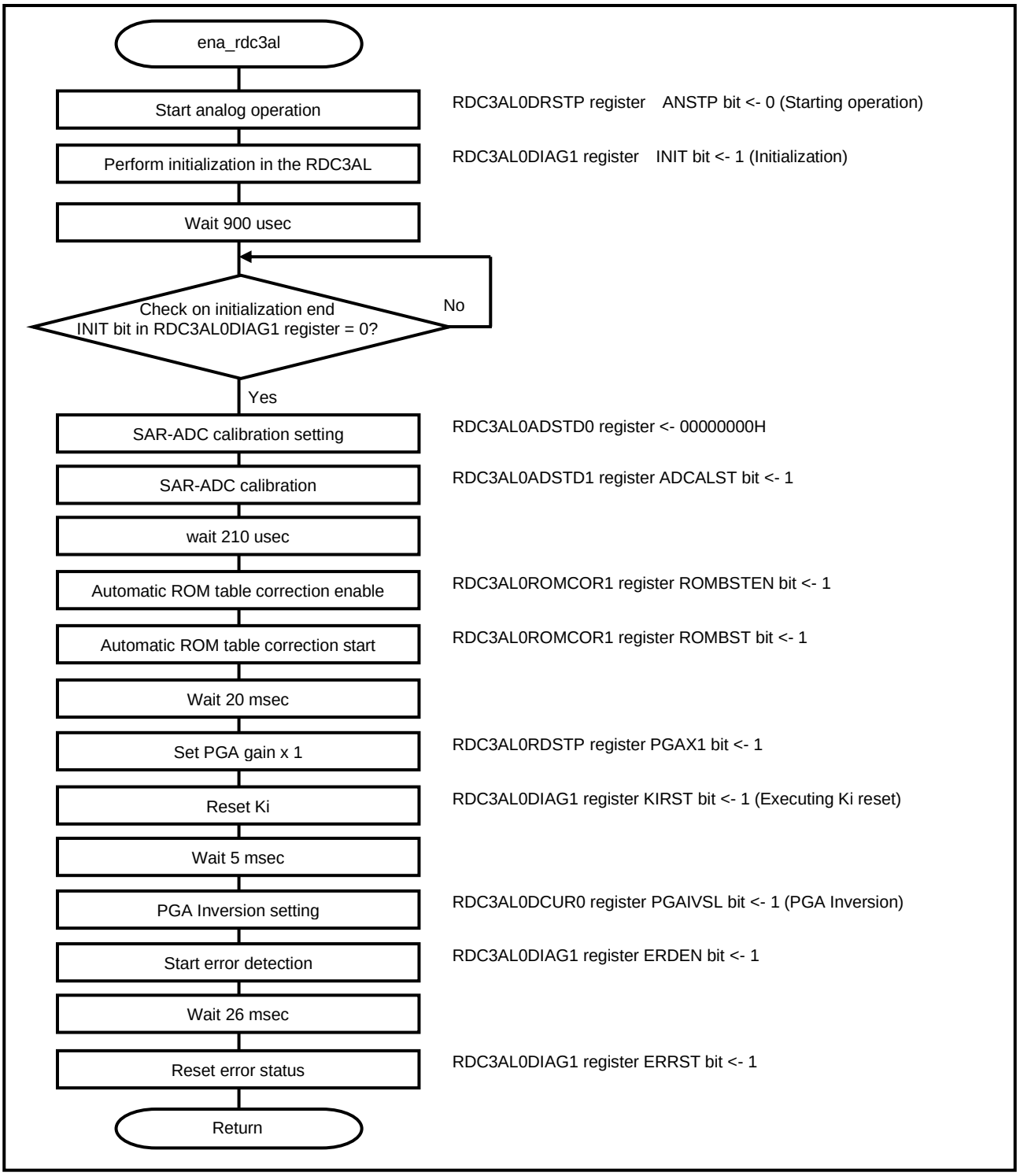


Figure 3-2 Operation Flow (2/2)

3.2 Supplementary Explanation of R/D Converter Usage

3.2.1 Control Variation Determination Clock

User's Manual states to set the control variation determination clock period to be longer than the excitation signal period currently used. Please set longer control variation determination clock period to stabilize the operation when problems such as unable to track occur.

3.2.2 Input Signal Amplitude of Ki Reset

If Ki reset is performed when the SINMNT/COSMNT signal amplitude is smaller than as specified in User's Manual, the R/D converter will attempt to track the abnormal signal. Even if the SINMNT/COSMNT signal amplitude returns to normal afterwards, tracking cannot be performed or takes longer time to track.

3.2.3 Various Gain Values of Forced Gain Control

The 12-Level AGC is selected for the gain in the forced gain control, and the first Kv gain becomes the maximum value (x128). During the forced gain control, the Kv gain is automatically determined according to the AGC. Ki and Kp gains are fixed to the values exclusive for the forced gain control.

3.2.4 ADC Calibration

Perform the ADC calibration even though the angular conversion mode 0 is selected because the ADC that is used in angular conversion mode 1 is operating for error detection.

3.2.5 When starting to use angle conversion mode 0

Depending on the excitation phase difference between the excitation signal and the SINMNT / COSMNT signal, R / D conversion error and 2-path comparison conversion error may occur.

In that case, try the following settings during the forced gain period (5ms) after Ki reset at startup. If the user setting value is different from the setting value below, return the setting after the forced gain period ends.

Step 1. Changed control variation determination clock (DEVCK) to 101 (800us)

Step 2. Changed maximum angular velocity (MAXV) to 000 (120000 rpm)

* If you cannot solve the problem by steps 1 and 2, please contact us.

3.3 RDC3AL Use Case

3.3.1 Overview of Specifications

In this usage example, a VR resolver is excited and the angle is calculated from the output resolver signal.

The RDC3AL0 is set to 10 kHz excitation output, VR resolver mode, maximum angular velocity of 240000 rpm (12 bits), automatic gain adjustment, and operation enabled. Because stable operation wait processing is performed in the RDC3AL0 operation enable processing, angle calculation is not made until the RDC3AL0 initialization function completes. The angle is calculated and then stored in the memory by the main function.

3.3.2 System Configuration

Figure 3-3 shows the system configuration.

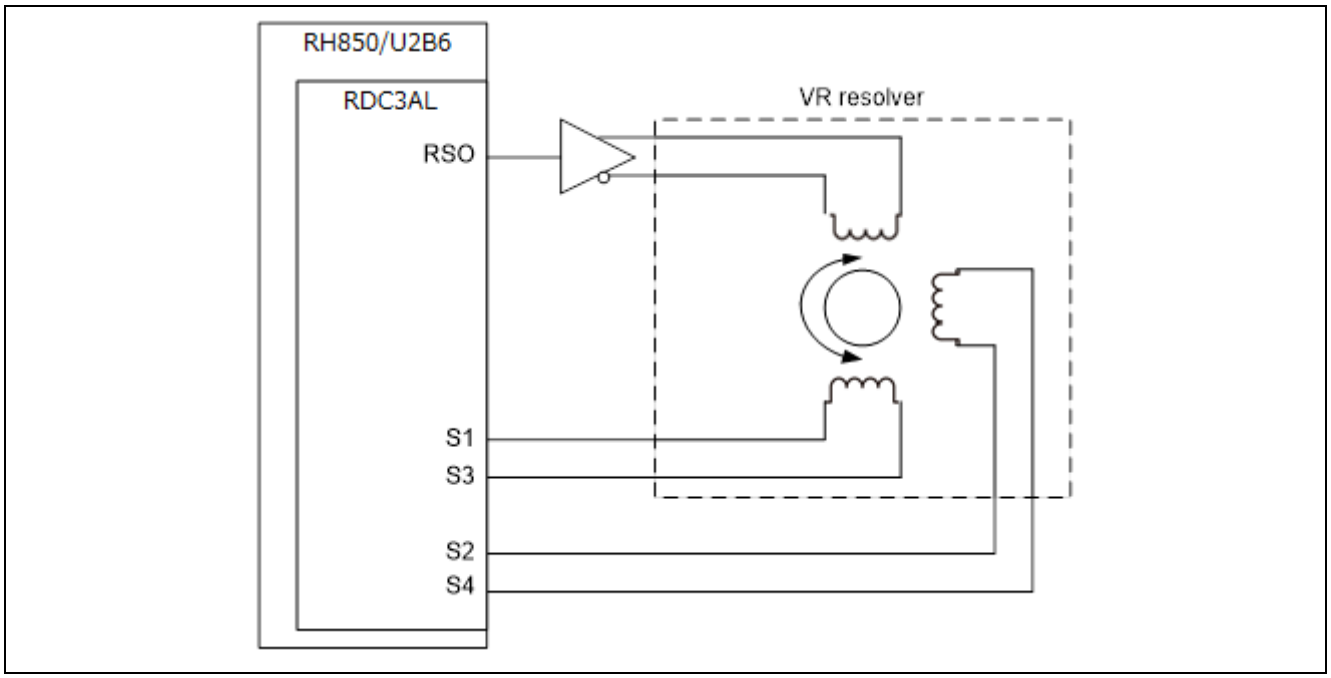


Figure 3-3 System Configuration

3.3.3 Initialization Explanation

- Modules

Modules used in this initialization explanation are listed below.

Table 3-1 List of Modules

Function Name	Description
main_pm1	Calls each function.
init_rdc3al0	Makes RDC3AL0 initial settings.
ena_rdc3al0	Makes RDC3AL0 startup processing.

- Register settings

Register settings for each feature used in this operation example are listed below.

Table 3-2 Example of RDC3AL Register Settings (1/2)

Register Name/Symbol	Set Value	Description
Excitation setting register / RDC3AL0REF	0x0B0F0410	EXFS2 [3: 0] b0000: Excitation frequency selection bit 2. EXFS [4: 0] b01111: Excitation signal frequency selection bit. * 10 kHz selection in combination with EXFS. RFEXS 1 (default): Excitation component extraction function valid excitation component extraction function valid bit. SENS 1 (default): VR resolver use sensor selection bit. EXIO 1: Voltage excitation output RSO, COM input / output switch bit. EXF 15 0: Excitation signal frequency is the frequency set by EXFS [4: 0]. COMSTS [2: 0] b000: Do not stop. AD comparator stop function select bit. PLSNFS 1: The noise filter is used excitation extraction noise filter
Control gain selection register 0 / RDC3AL0PI0	0x00020017	KVMS [1: 0] b 00 (default): AGC 12 step 1 step shift method Kv gain method selection bit. DVW [1: 0] b 00 (default): × 1 ERR deviation weighting bit. KPF 0 (default): Do not multiply Kp gain by 4. Kp gain 4 times bit. KPS [1: 0] b00 (default): × 1 Kp gain select bit. KIS [2: 0] b000 (default): × 1 Ki gain selection bit. DEVCK [2: 0] b010 (default): 200 µs Clock selection bit for periodic clock control deviation judgment. LKVS [3: 0] b0000 (default): × 1 Low Kv gain select bit. HKVS [3: 0] b 0000 (default): × 32 High Kv gain select bit. BWCS 1 (default): 1: The LPGS [2: 0] bits set the PI compensator. Select PI compensator setting method. LPGS [2: 0] b 111: Automatic adjustment selection loop gain setting bit.
Control gain selection register 1 / RDC3AL0PI1	0x00011B01	SAGD 0 (default): Use the forced gain control function. Short time BIST. recovery Forced gain control function Disable bit. AGCD 0 (default): Use the forced gain control function. Forced gain control function disable bit. AGDS 1 (default): Kv does not transition to high gain during excitation failure and Ki reset. AGST [3: 0] b0000 (default): × 4 Short time BIST return Initial AGC gain bit AGC Kv High gain transition limit bit. HKVLM[3:0] b0001(default) : X64 (7 levels can be set) LKVLM[3:0] b1011(default) : X0.0625 (7 levels can be set) MAXVS [2: 0] b001 (default): Kv transitions to high gain at excitation failure and Ki reset. AGC Kv High gain transition limit bit Maximum angular velocity selection Maximum angular velocity 240000 rpm Resolution 12 bits.
Error detection register 0 / RDC3AL0DIAG0	0x021A2933	P2ANT [1: 0] b10 : ± 32 LSB (@ 12 bit resolution) 2 Route conversion abnormality threshold setting bit. EXCETH [7: 0] 1Ah (default): 0.102 × RVCC (Vpp) Resolver signal abnormality comparison threshold setting bit. SGBTH [7: 0] 29 H (default): 0.58 × RVCC (V) disconnection abnormality comparison threshold setting bit (VR resolver). SGBDTH [7: 0] 33 H (default): 0.85 × RVCC (V) disconnection abnormality comparison threshold setting bit (DC resolver).

Table 3-2 Example of RDC3AL Register Settings (2/2)

Register Name/Symbol	Set Value	Description
Error detection register 1 / RDC3AL0DIAG1	0xB0000000	CVEDS 0 (default): Selects a circuit that supports high-speed rotation of the RD conversion error detection signal. Conversion abnormality detection circuit selection bit EDPS [1: 0] b11 (default): 7.37 msec R / D conversion error determination time selection bit VGASL [1: 0] b00: No detection VGST 0 (default): Vertical ground fault detection start bit
Digital Operation Register 0 / RDC3ALnDCUR0	0x00020024	AVE4[1:0] b01 : Use this setting if the excitation frequency is less than 30 kHz.
RDC stop register/ RDC3AL0RDSTP	0x00000100-	MNTC 1 : Open external output terminals of sinmnt and cosmnt. sinmnt, cosmnt External pin setting bit. ANSTP 0: Analog circuit operation RD converter active.
12-Bit SAR-ADC Digital Circuit Block Setting Register 0 / RDC3AL0ADSTD0	0x00000000	ADCALCK[1:0] b00(default)：ADC calibration setting 0
12-Bit SAR-ADC Digital Circuit Block Setting Register 1 / RDC3AL0ADSTD1	0x00010000	ADCALST 1：ADC Calibration Start
Automatic ROM Table Correction Register 1 / RDC3ALnROMCOR1	0x00001001	ROMBSTEN 1：Automatic ROM Table Correction Enable ROMBST 1：Automatic ROM Table Correction Start
RDC Stop Register / RDC3AL0RDSTP	-	PGAX1 1：PGA Gain X1 Setting
Error detection register 1 / RDC3AL0DIAG1	-	INIT 1: Initialize RDC3AL0 KIRST 1: Ki reset Ki integrator value and accumulator integrator value = 0 ERDEN 1: Error detection start SQERST 1: Square sum amplitude abnormal excitation counter reset ERRST 1: Error signal reset
Encoder register 1 / RDC3AL0ENC1	-	ANG[15:0] Angle data Angle is stored with a 16-bit width. Angle = 360 $2^{16} \times$ n (°) [n = read value]

4. Error Detection

4.1 Overview of Error Detection Function

4.1.1 Configuration of R/D Converter

Figure 4-1 shows configuration of a resolver and the R/D converter. The R/D converter consists of the input signal part from a resolver and the tracking loop which converts input signals to digital angles.

RDC3AL has a function to detect errors of each of them.

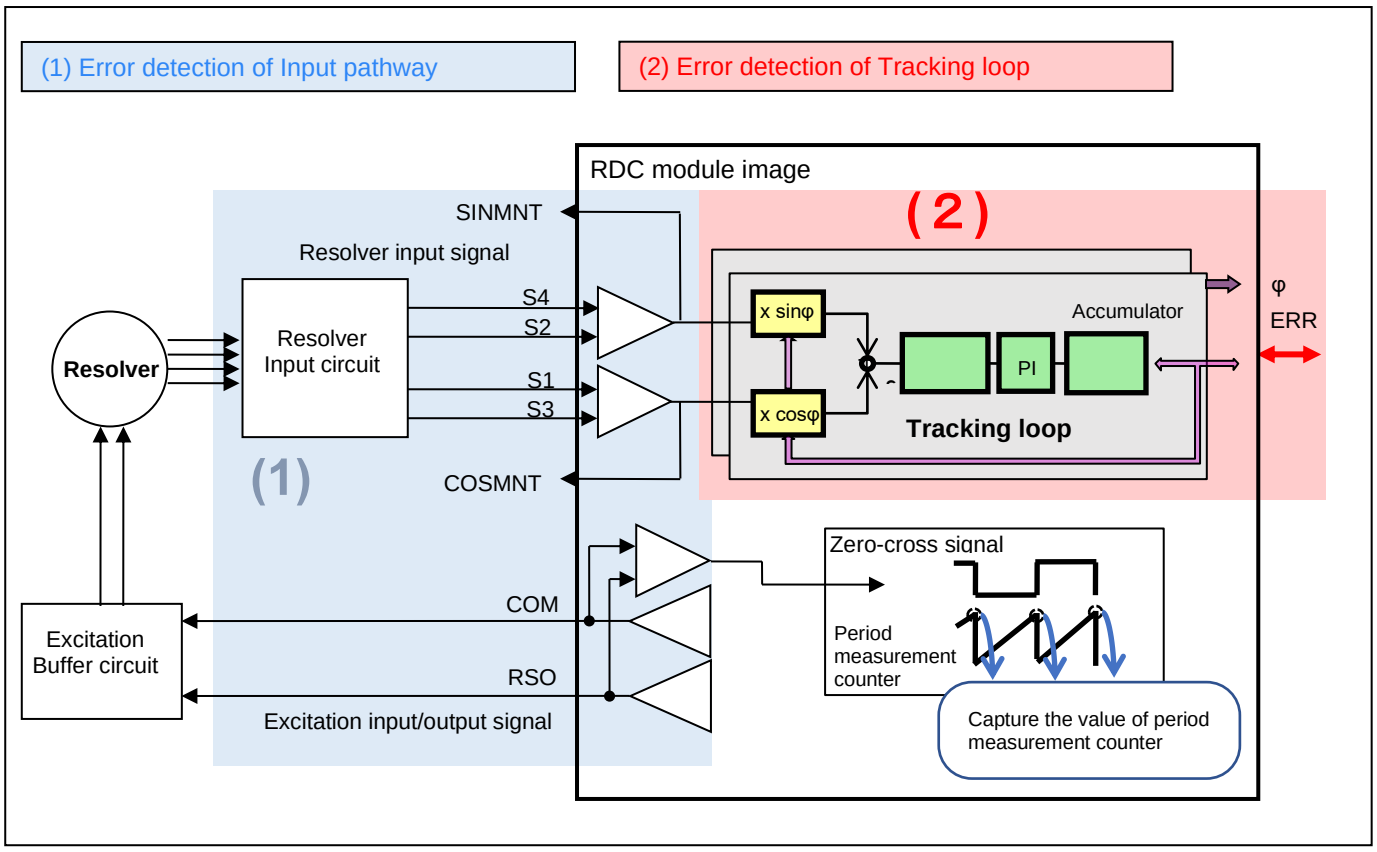


Figure 4-1 Simplified Diagram of R/D Converter

4.1.2 Error Detection in Input Paths

There are five kinds of error detections in input paths as shown in Figure 4-2.

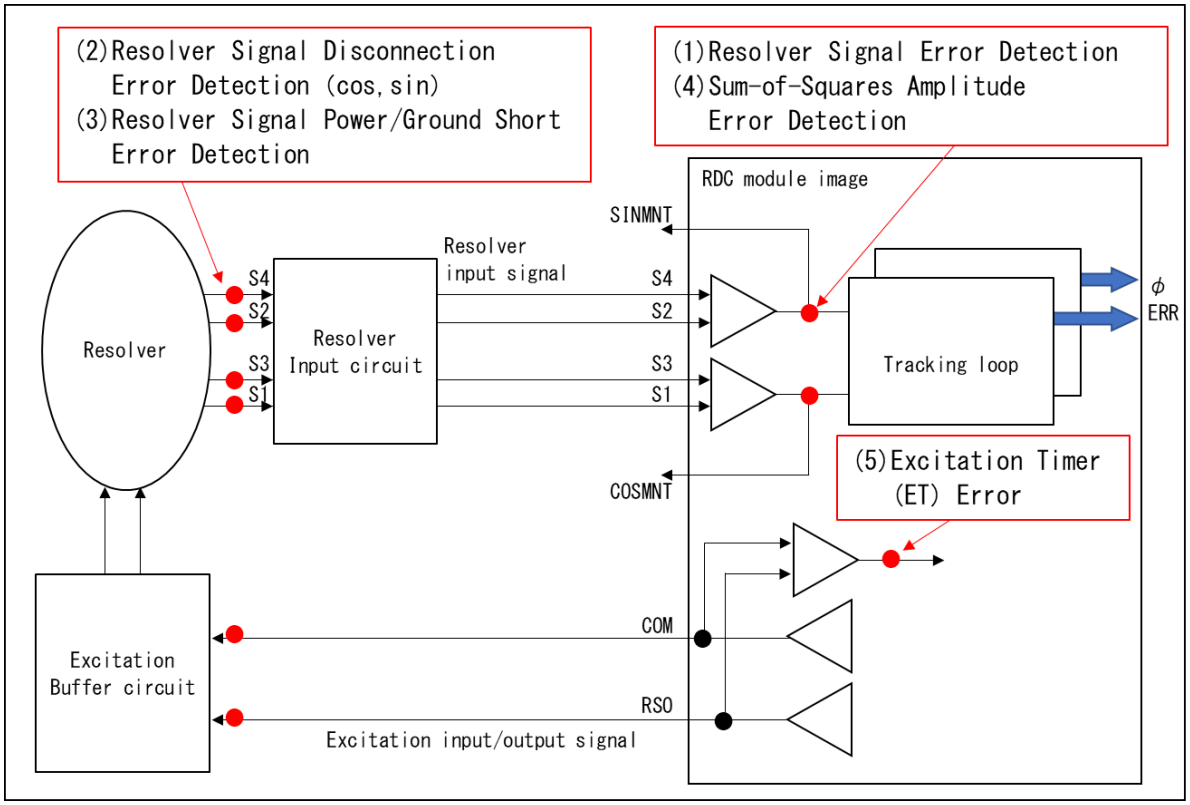


Figure 4-2 Error Detection in Input Paths

The overview of each error detection is as follows.

1. Resolver Signal Error Detection
   This function detects the amplitude reduction of the resolver signal caused by an error in the excitation signal. An error occurs when the resolver signal continues being within the threshold for a certain time.

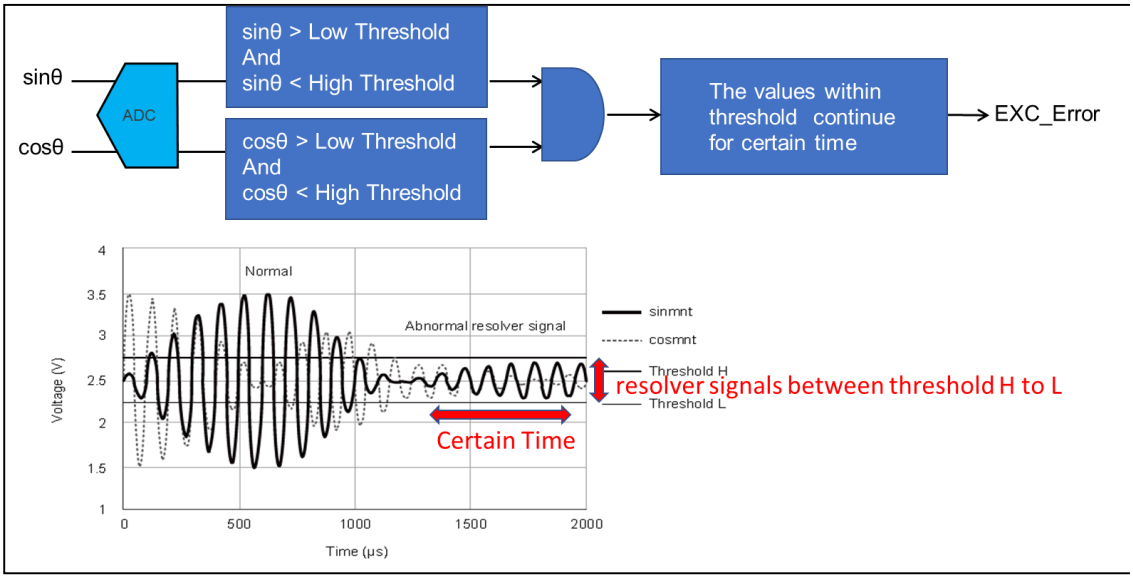


Figure 4-3 Overview of Resolver Signal Error Detection

2. Resolver Signal Disconnection Error Detection (cos, sin)
   This function detects disconnection of the resolver signal.
   For the VR resolver, error is detected when the common potential (the central potential of amplitude) of SINMNT and COSMNT continues to exceed the threshold value. For the DC resolver, an error is detected when the potential of SINMNT and COSMNT exceeds the threshold.

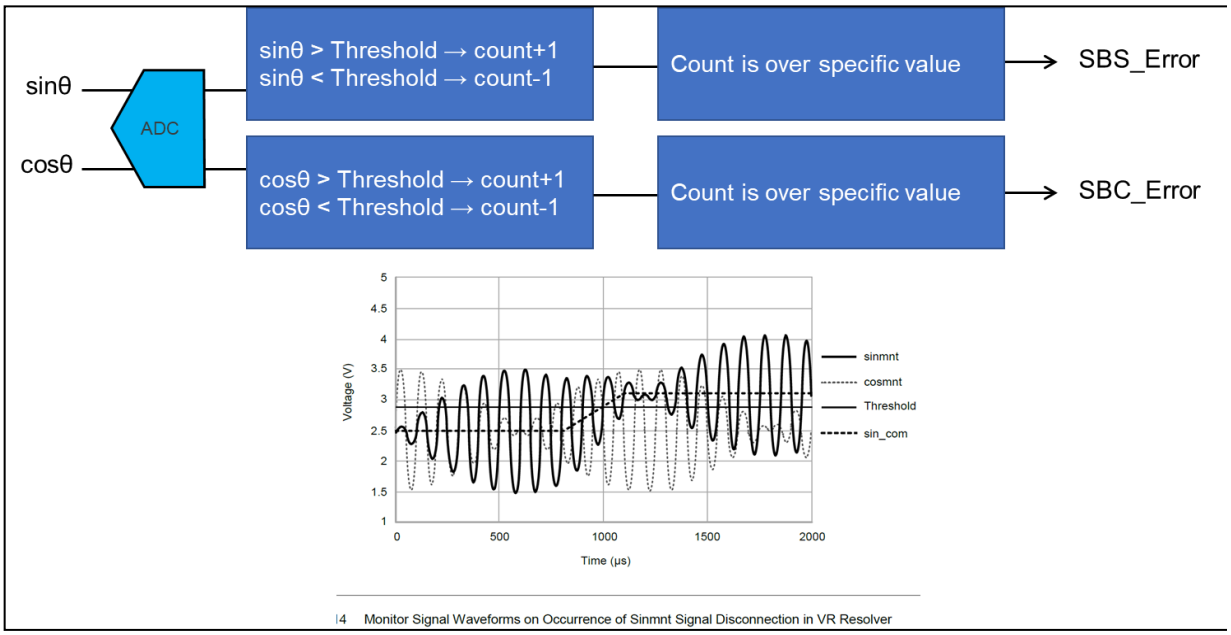


Figure 4-4 Overview of Resolver Signal Disconnection Error Detection (cos, sin)

3. Resolver Signal Power/Ground Short Error Detection
   This function detects short circuits of resolver pins (S1, S2, S3, S4, RSO, COM) to the power supply or to the ground with analog pins of the R/D converter. Six analog pins are cyclically monitored.

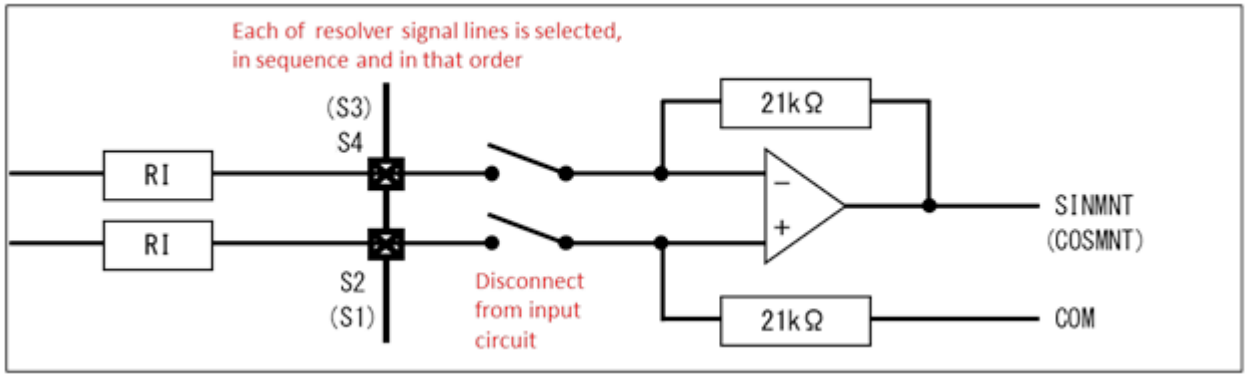


Figure 4-5 Overview of Resolver Signal Power/Ground Short Error Detection

4. Sum-of-Squares Amplitude Error Detection
   This function detects modulation, distortion, and noise in the amplitudes of the resolver signal.

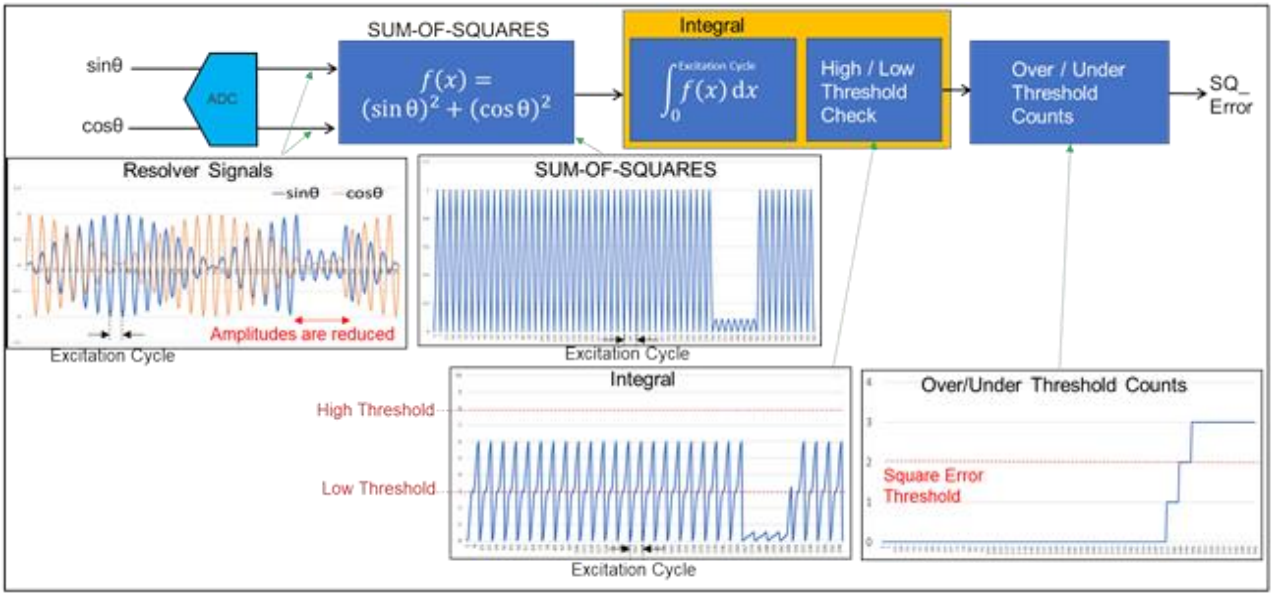


Figure 4-6 Overview of Sum-of Squares Amplitude Error Detection

5. Excitation Period Error Detection
   This function measures the period of the excitation signal. An error occurs when the period of the excitation signal is exceeding the expected value.

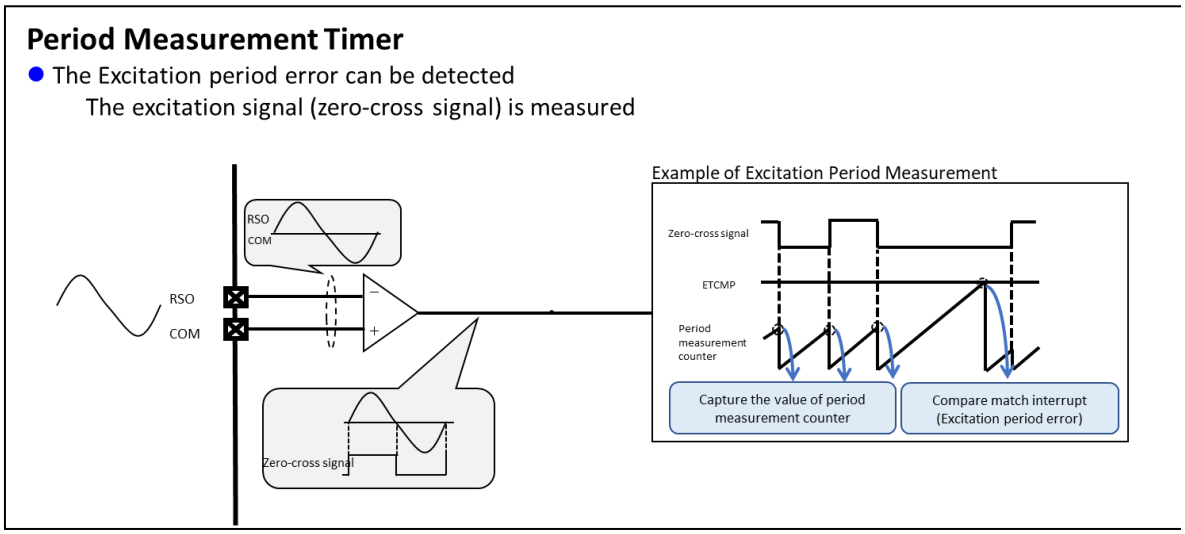


Figure 4-7 Overview of Excitation Period Error Detection

4.1.3 Error Detection in the Tracking Loop

There are two kinds of error detections in the tracking loop as shown in Figure 4-8.

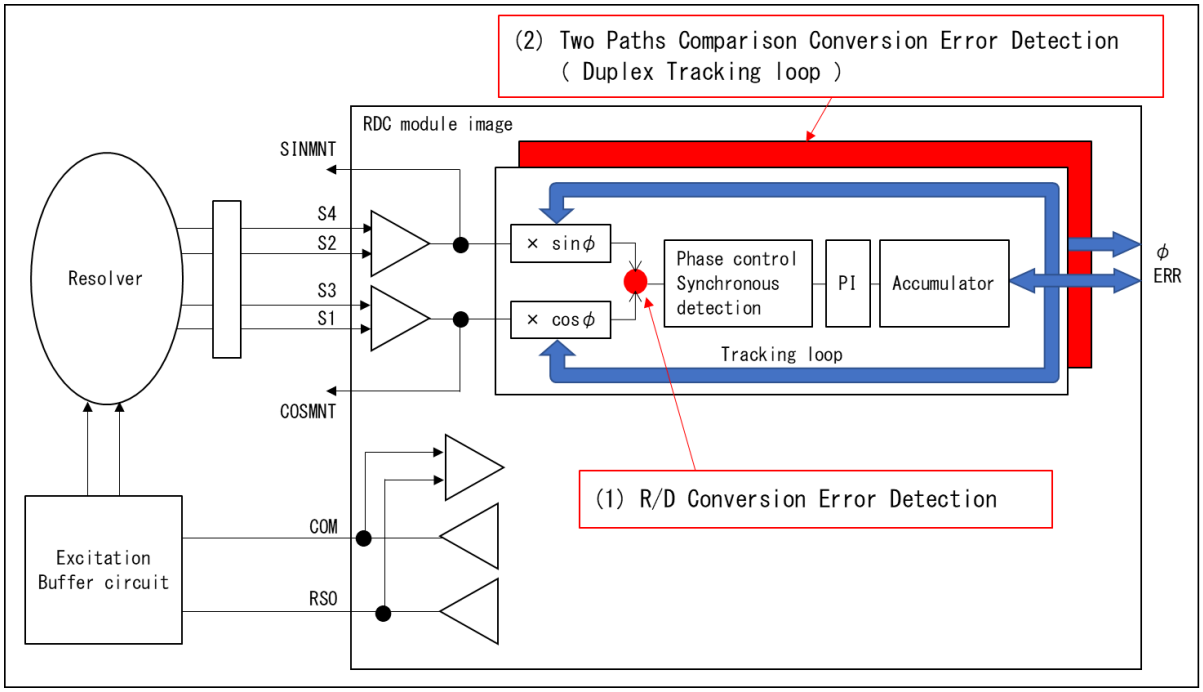


Figure 4-8 Error Detection in the Tracking Loop

The overview of each error detection is as follows.

1. R/D Conversion Error Detection
   This function monitors the control variation in the R/D conversion loop, and detects calculation errors in the R/D conversion function.

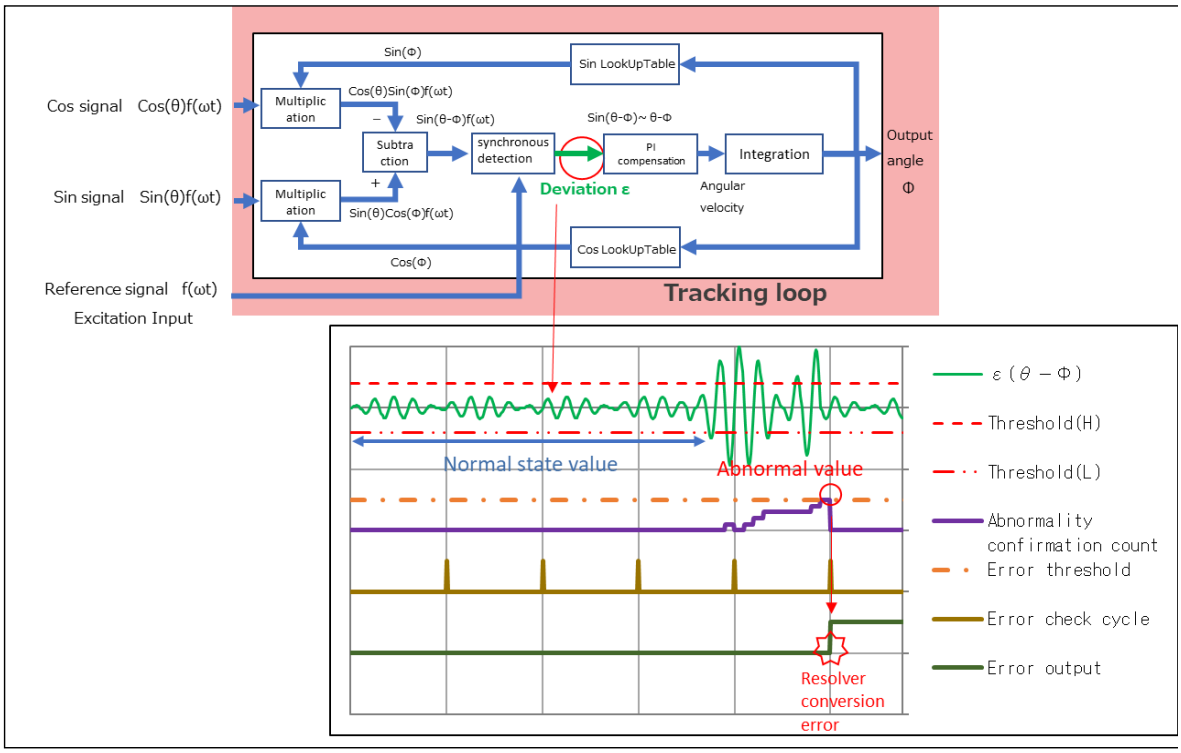


Figure 4-9 Overview of R/D Conversion Error

2. Two Paths Comparison Conversion Error Detection
   This function monitors the redundancy by comparing results of angle conversion in two paths. phi0 and phi1 in Figure 4-10 are always compared and monitored. An error occurs when results of phi0 and phi1 are different.

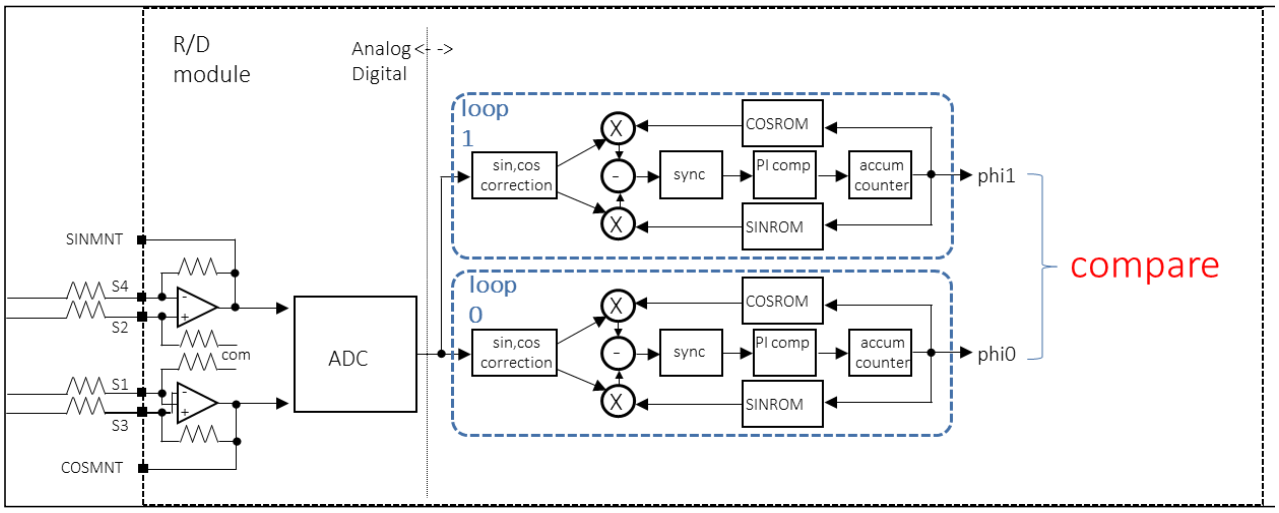


Figure 4-10 Overview of Two Paths Comparison Conversion Error Detection

4.2 Details of Error Detection Function

This section explains details of the error detection method of the RDC3AL.

4.2.1 Resolver Signal Error Detection

This function detects the amplitude reduction of the resolver signal caused by an error in excitation signals input to the resolver. When a resolver signal error is detected, the RDC error interrupt request signal becomes high.

A resolver signal error is detected if the monitor outputs (SINMNT, COSMNT) fall below the threshold for approximately 220µs or longer. As for the DC resolver which does not have the excitation signal, a resolver signal error is detected if the monitor outputs fall below the threshold for approximately 220µs or longer.

The threshold can be set by "EXCETH[7:0]×RVCC / 256 (Vpp)".

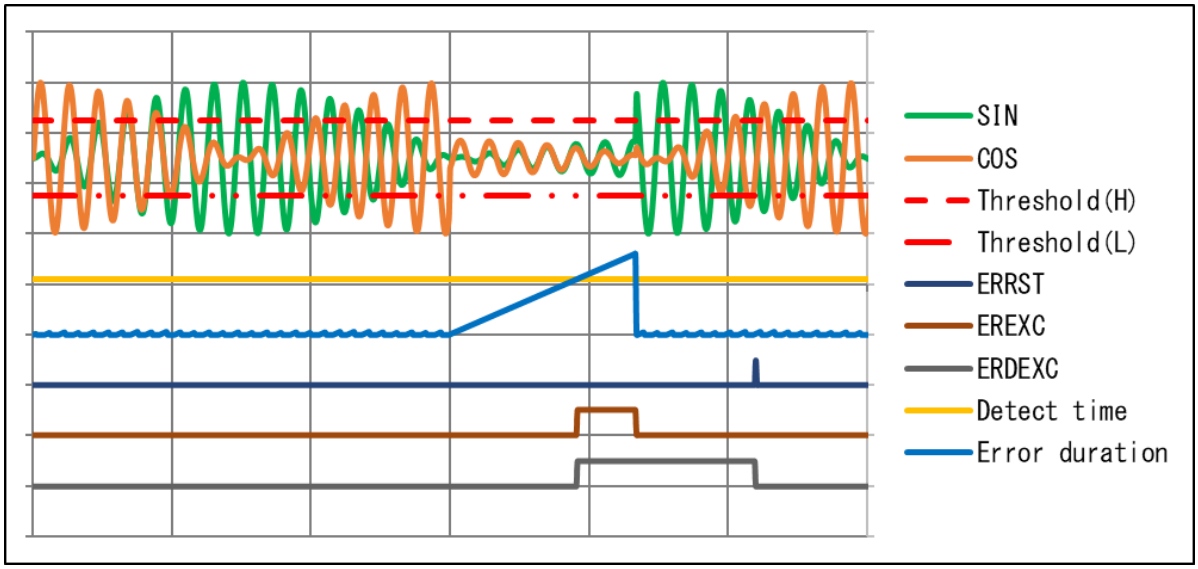


Figure 4-11 Resolver Signal Error Detection When VR Resolver is Used

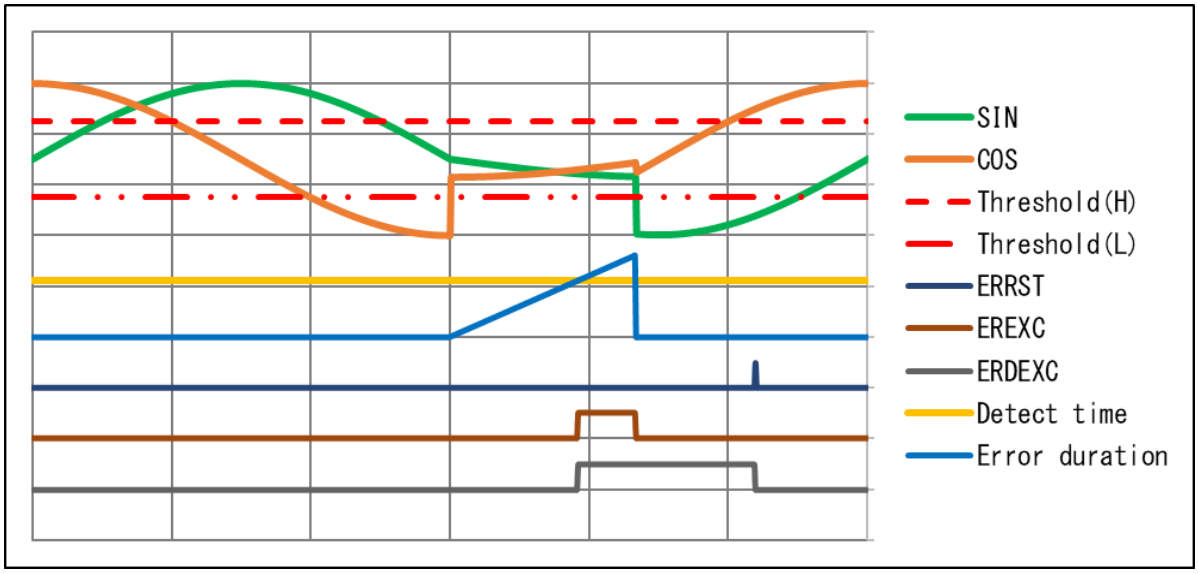


Figure 4-12 Resolver Signal Error Detection When DC Resolver is Used

4.2.1.1 Example of Register Settings

Table 4-1 shows the example of register settings of when the resolver signal error detection function is used.

Table 4-1 Example of Register Settings of When Resolver Signal Error Detection Function is Used

Register name/ Abbreviation	Bit name/ Abbreviation	Set Value	Function
Error detection register 0/ RDC3ALnDIAG0	Resolver Signal Error Comparison Threshold/ EXCETH[7:0]	0x1A	Sets the threshold for use in detecting errors in the resolver signal. Set value in the left column is 0.102 × RVCC(Vpp).
Error detection register 1/ RDC3ALnDIAG1	Error Detection Start / ERDEN	1	Error detection is enabled when the error detection output mask is released after 26 milliseconds have elapsed following this bit being set to 1.
	Error Signal Reset Bit / ERRST	1	Writing 1 to this bit resets “error detection output register 1” to 0. Note that each of these bits remains at 1 if an error is continuous.
Error detection register 2/ RDC3ALnDIAG2	Resolver Signal Error Select / EREXCS	0	Set the bits ERR, ERHD, EREXC, and ERDEXC to 1 on occurrence of a resolver signal error.

4.2.2 Resolver Signal Disconnection Error Detection

This function detects disconnection (including contact failure) of the resolver signals (S1 to S4). When a resolver signal disconnect error is detected, the RDC error interrupt request signal becomes high.

When operation with a VR resolver is selected (by setting value as SENS =1), this function monitors the common levels fluctuation of the monitored signal output (SINMNT, COSMNT) and determines any case of them exceeding the configured threshold to be a disconnection error. The threshold can be set by "0.5×RVCC＋SGBTH[7:0]×RVCC / 512 (V)".

When operation with a DC resolver is selected (by setting the combination of values as EXIO = 1 and SENS = 0), this function monitors whether the DC level of the monitored signals is exceeding the threshold or not. The threshold can be set by "0.5×RVCC＋(SGBDTH[7:0]×8＋1024)×RVCC / 4096 (V)".

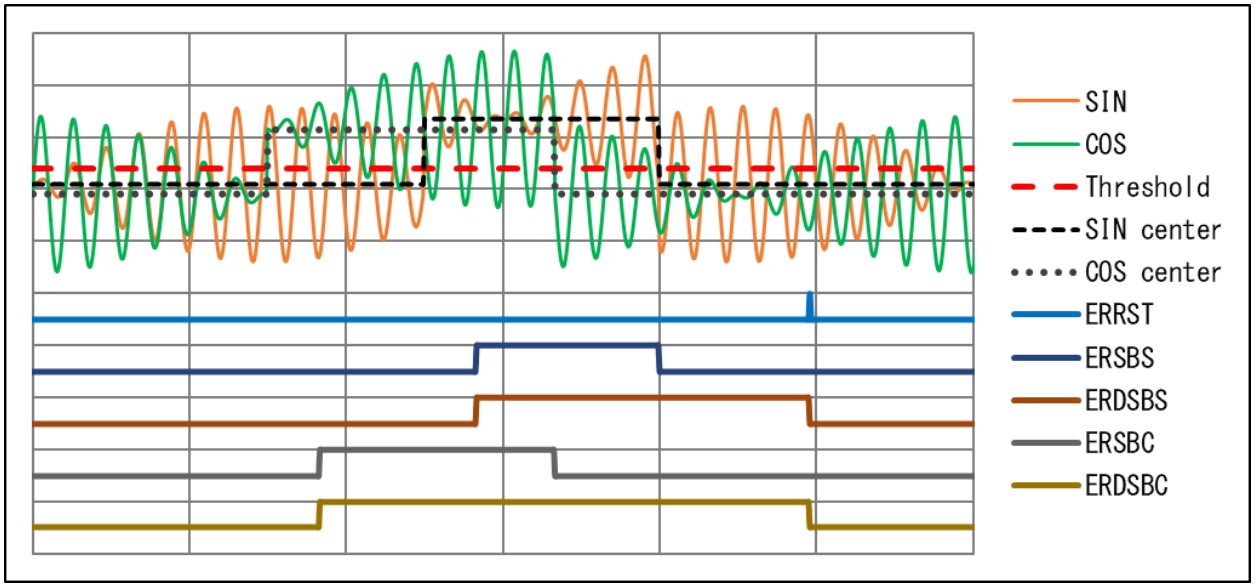


Figure 4-13 Resolver Signal Disconnection Error Detection When VR Resolver is Used

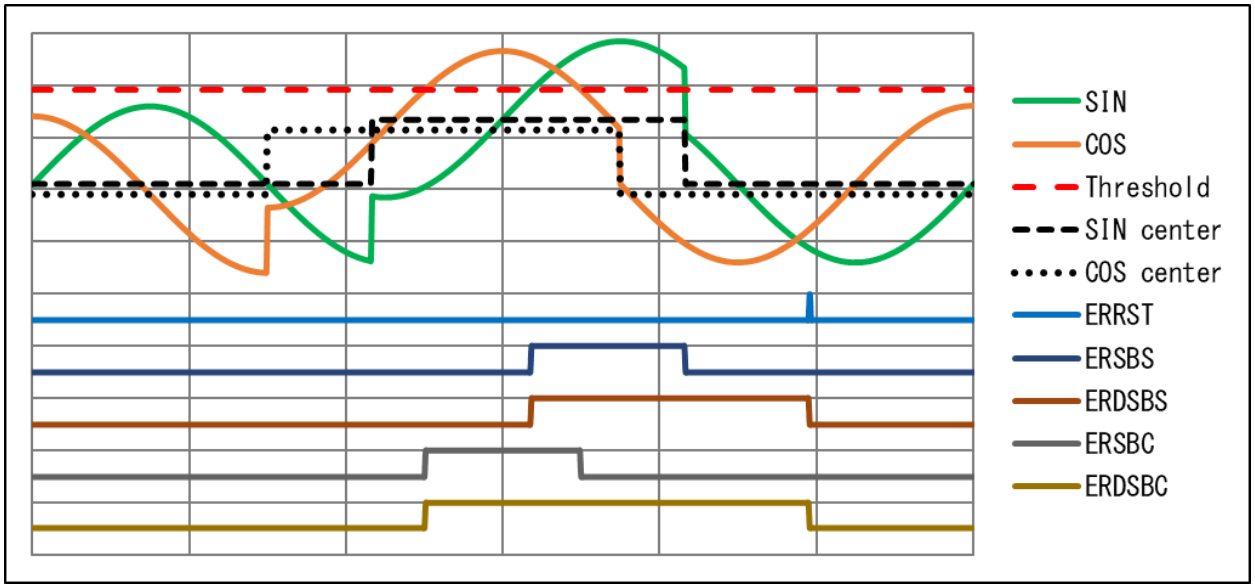


Figure 4-14 Resolver Signal Disconnection Error Detection When DC Resolver is Used

4.2.2.1 Example of Register Settings

Table 4-2 shows the example of register settings of when the resolver signal disconnection error detection function is used.

Table 4-2 Example of Register Settings of When Resolver Signal Disconnection Error Detection Function is Used

Register name/ Abbreviation	Bit name/ Abbreviation	Set Value	Function
Error detection register 0/ RDC3ALnDIAG0	Disconnect Error Comparison Threshold (for VR Resolver) / SGBTH[7:0]	0x29	Sets the threshold for use in detecting disconnect errors when the VR resolver is used. Set value in the left column is 0.58 × RVCC(V).
	Disconnect Error Comparison Threshold Setting (for DC Resolver) / SGBDTH[7:0]	0x33	Sets the threshold for use in detecting disconnect errors when the DC resolver is used. Set value in the left column is 0.85 × RVCC(V).
Error detection register 1/ RDC3ALnDIAG1	Error Detection Start / ERDEN	1	Error detection is enabled when the error detection output mask is released after 26 milliseconds have elapsed following this bit being set to 1.
	Error Signal Reset Bit / ERRST	1	Writing 1 to this bit resets “error detection output register 1” to 0. Note that each of these bits remains at 1 if an error is continuous.
Error detection register 2/ RDC3ALnDIAG2	Disconnect Error (Cosine) Select / ERSBCS	0	Set the bits ERR, ERHD, ERSBC, and ERDSBC to 1 on occurrence of a disconnect error (cosine side)
	Disconnect Error (Sine) Select / ERSBSS	0	Set the bits ERR, ERHD, ERSBS, and ERDSBS to 1 on occurrence of a disconnect error (sine side)

4.2.3 R/D Conversion Error Detection

This function monitors the control variation in R/D conversion loop, and detects operation errors in the R/D conversion function. When an R/D conversion error is detected, the RDC error interrupt request signal becomes high.

A control variation (ε) is recognized as excessive if the control variation rises above or falls below a configured threshold level. The threshold is a fixed value (see Section 39.5.3, Error Detect Characteristics in the user's manual for details). An R/D conversion error is detected if the control variation stay excessive for more than 50% of the error determination time set in the EDPS[1:0] bits in the RDC3ALnDIAG1 register.

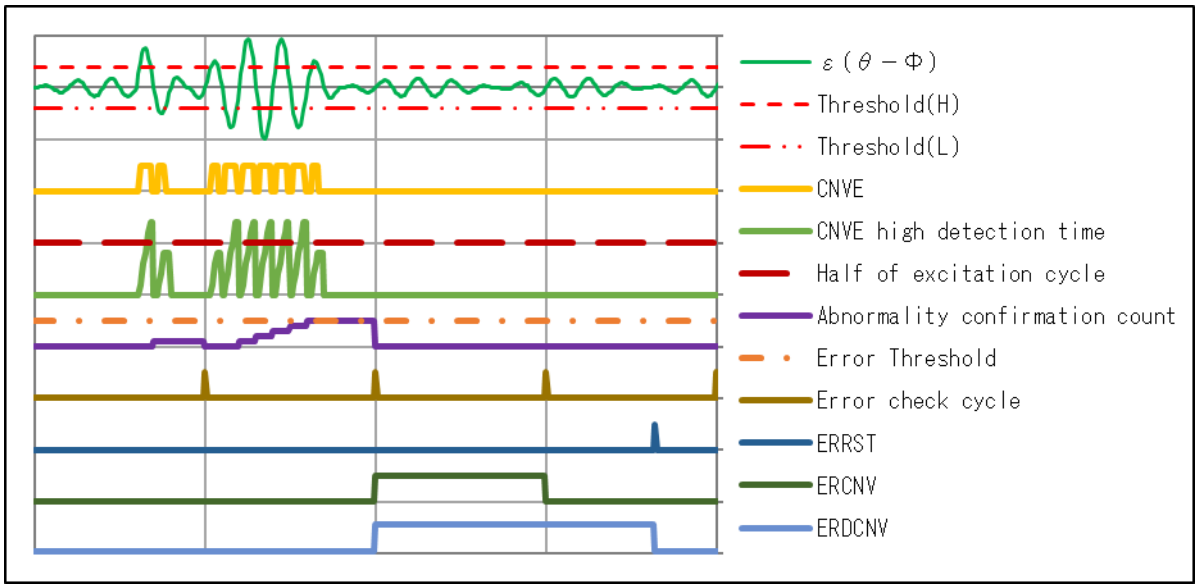


Figure 4-15 R/D Conversion Error Detection

"The internal control variation ε" is a formula in a red frame which is explaining operating principle in Section 26.2.3 in the user's manual. When there is a difference between θ and Φ, the control variation becomes sine wave shape of the excitation period. ε in a blue frame is the control variation which is used to determine the gain of the PI compensator.

26.2.3 Operating Principle

The following describes the operating principles of the RDC3A module.

This R/D converter module uses the tracking method to convert analog resolver signals to digital signals (R/D conversion).

The tracking loop runs at 20 MHz.

When the excitation signal f(t) is input to the excitation coil, f(t) • sinθ and f(t) • cosθ are output from the resolver according to the angle (θ) of the resolver rotor. These signals are input to the RDC3AnS2-RDC3AnS4 and RDC3AnS1-RDC3AnS3 pins, respectively.

These signals are amplified and then input to the multiplying D/A converter. At the same time, cos ϕ (or sin ϕ) is generated by passing the accumulator output through COS ROM (or SIN ROM) and is fed back to the corresponding D/A converter. Then, the subtraction is performed on the outputs from both D/A converters.

$$f(t) \cdot (\sin\theta \cdot \cos\phi - \cos\theta \cdot \sin\phi)$$

$$= f(t) \cdot \sin(\theta - \phi)$$

$$\approx f(t) \cdot (\theta - \phi)$$

The result is converted to 1-bit digital value by the comparator (CMP) and then passed to the digital block.

The excitation component f(t) is removed in the synchronous detection circuit to obtain the control variation $\varepsilon = \theta - \phi$.

Figure 4-16 Excerpt of "26.2.3 Operating Principle" in User's Manual

When a resolver input angle (θ) and an R/D output angle (φ) are different, ε becomes a signal with an amplitude in the excitation period as sin(θ-φ) has a value (Figure 4-17). When a resolver input angle (θ) and an R/D output angle (φ) are matching, the value of ε will be nearing COM(2.5V) (Figure 4.16).

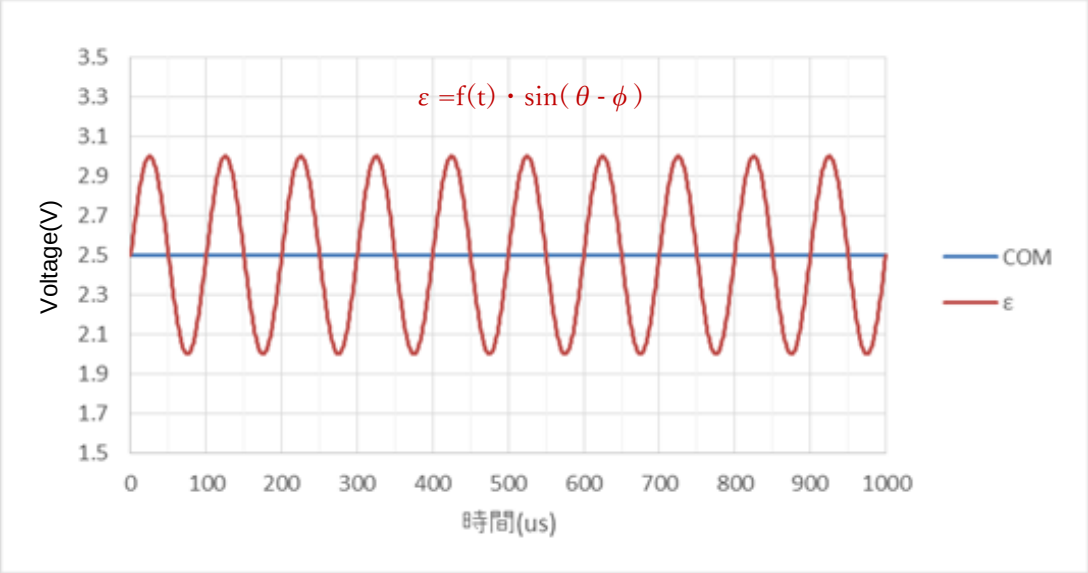


Figure 4-17 The Internal Control Variation of When Angles are Different

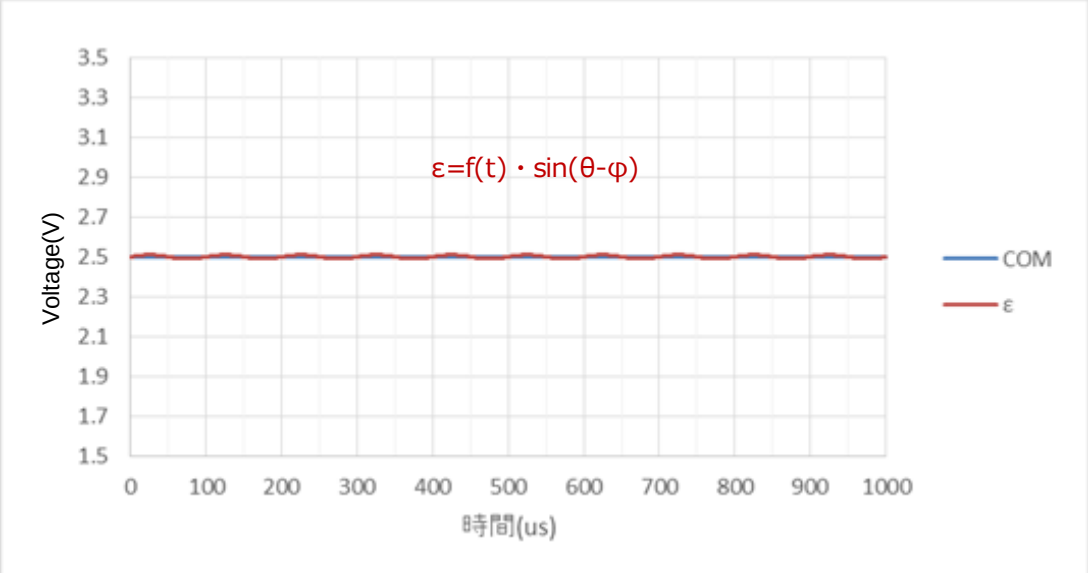


Figure 4-18 The Internal Control Variation of When Angles are Matching

Since ε has an amplitude in the conversion error state in which a resolver input angle (θ) and a R/D output angle (φ) are different, set thresholds on the high side and the low side, and CNVE signal will be generated whenever the ε value is out of the ranges. When the CNVE is 1, the amplitude of ε is large.

The proportion of 1 and 0 of the CNVE signal can be determined at the counter circuit at every half period of excitation signal. When the proportion of 1 is exceeding 50% of the entire excitation half period, that excitation half period is determined as abnormal, and determined as normal when it is not exceeding. Determinations of normal and abnormal of each excitation half period for the conversion error determination time (e.g., 7.3ms) which is selected by EDPS bit are aggregated. When abnormal half period is exceeding 50% of the entire half period, ERCNV bit and ERDCNV bit are set as an R/D conversion error.

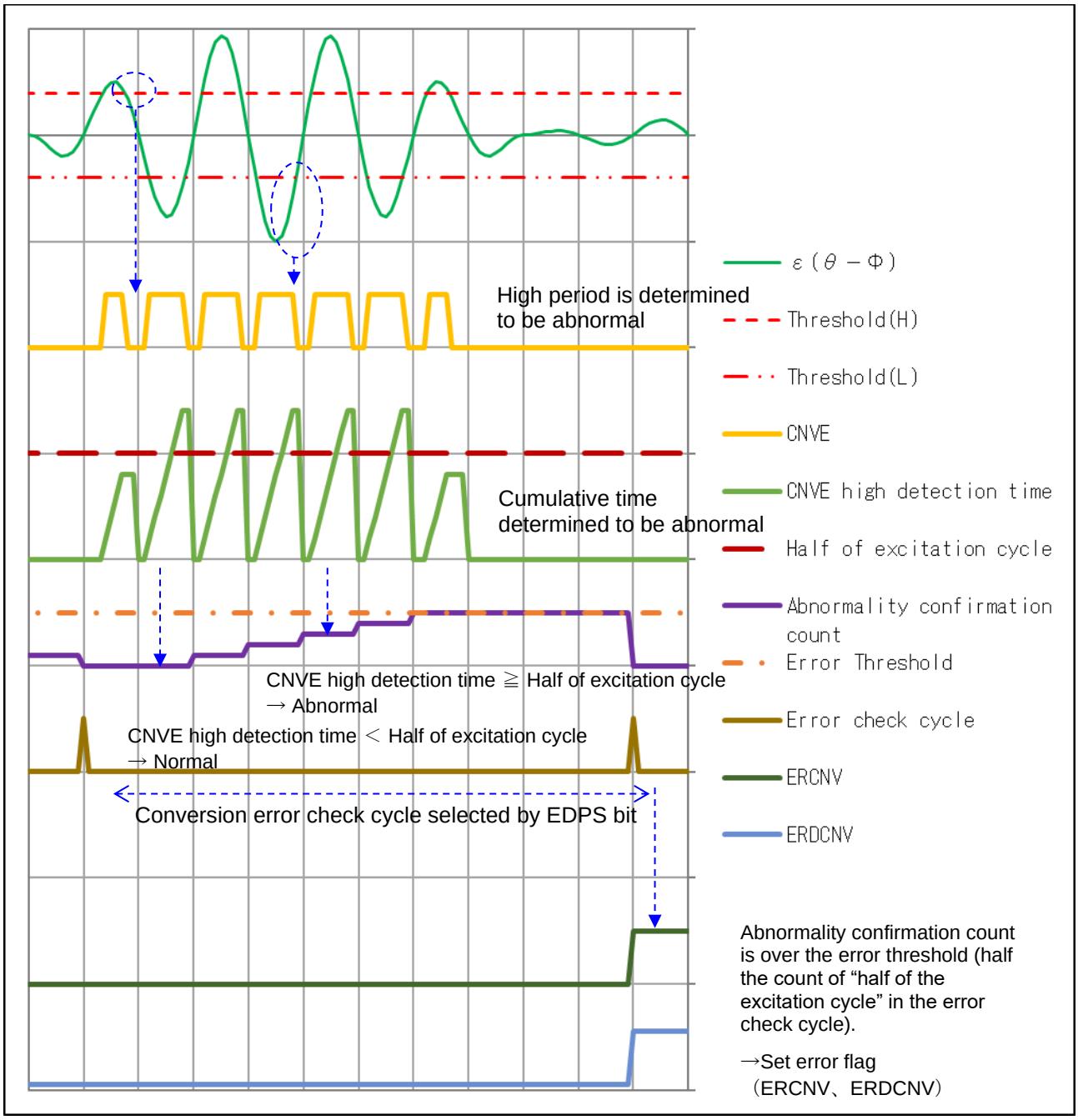


Figure 4-19 Principle of R/D Conversion Error Detection

4.2.3.1 Example of Register Settings

Table 4-3 shows the example of register settings of when the R/D conversion error detection function is used.

Table 4-3 Example of Register Settings of When R/D Conversion Error Detection Function is Used

Register name/ Abbreviation	Bit name/ Abbreviation	Set Value	Function
Error detection register 1/ RDC3ALnDIAG1	Conversion Error Detection Circuit Select / CVEDS	0	The conversion error detection circuit which supports high-speed rotation of the RD conversion error detection signal.
	RD Conversion Error Determination Time Select / EDPS[1:0]	3	Selects the error determination time (for preventing sudden acceleration) for RD conversion Errors. 11b：7.37 msec
	Error Detection Start / ERDEN	1	Error detection is enabled when the error detection output mask is released after 26 milliseconds have elapsed following this bit being set to 1.
	Error Signal Reset Bit / ERRST	1	Writing 1 to this bit resets “error detection output register 1” to 0. Note that each of these bits remains at 1 if an error is continuous.
Error detection register 2/ RDC3ALnDIAG2	Conversion Error Select / ERCNVS	0	Set the bits ERR, ERHD, ERCNV, and ERDCNV to 1 on occurrence of a conversion Error.

4.2.4 Two Paths Comparison Conversion Error Detection

This function compares the results of angle conversion from two loops, and detects conversion errors and failures in the circuit. In the angular conversion mode 0 (ADRD = 0), this function compares the phi angles output from the angular conversion mode 0 path and that from the angular conversion mode 1 path, and if the difference between two angles is larger than the threshold, this is judged to be a two paths comparison conversion error. The threshold value is set by the P2ANT[1:0] bits.

In the angular conversion mode 1 (ADRD = 1), this function detects angles output of two conversion circuits operated in the angular conversion mode 1 by ±1LSB error.

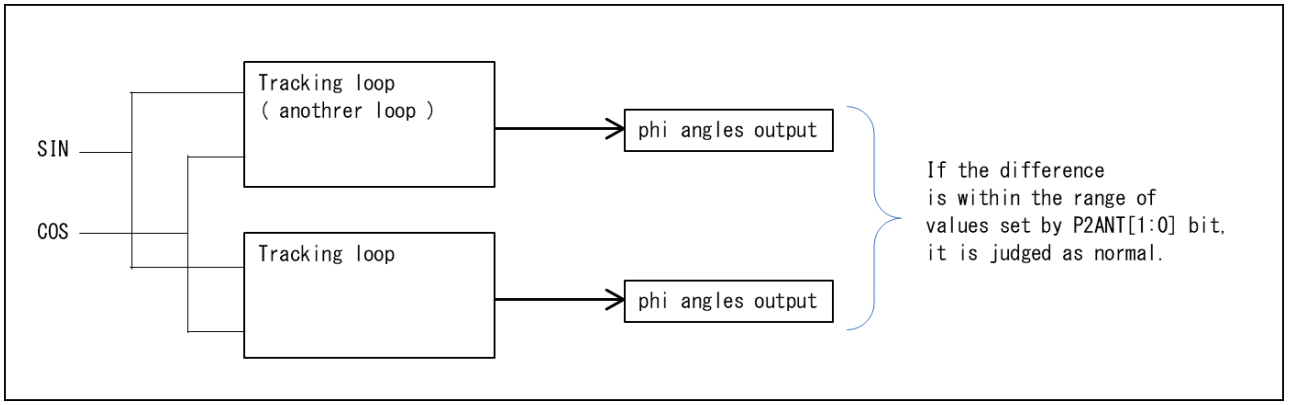


Figure 4-20 Two Paths Comparison Conversion Error Detection

4.2.4.1 Example of Register Settings

Table 4-4 shows the example of register settings of when the two paths comparison conversion error detection function is used.

Table 4-4 Example of Register Settings of When Two Paths Comparison Conversion Error Detection Function is Used

Register name/ Abbreviation	Bit name/ Abbreviation	Set Value	Function
Error detection register 0/ RDC3ALnDIAG0	Two Paths Conversions Error Threshold / P2ANT [1:0]	2	Sets the threshold for use in detecting errors by comparing the results of conversion from the path for the angular conversion mode 0 and that for the angular conversion mode 1 to ±32LSB. (Available only in the angular conversion mode 0)
Error detection register 1/ RDC3ALnDIAG1	Error Detection Start / ERDEN	1	Error detection is enabled when the error detection output mask is released after 26 milliseconds have elapsed following this bit being set to 1.
	Error Signal Reset Bit / ERRST	1	Writing 1 to this bit resets “error detection output register 1” to 0. Note that each of these bits remains at 1 if an error is continuous.
Error detection register 2/ RDC3ALnDIAG2	Two Paths Conversion Error Select / ERP2S	0	Set the bits ERR, ERHD, ERP2, and ERDP2 to 1 on occurrence of a two paths conversion error

4.2.5 Resolver Signal Power/Ground Short Error Detection

This function detects power short errors (short circuits to the power supply) and ground short errors (short circuits to the ground) of the resolver signal lines RSO, COM, S1, S2, S3, and S4. Note that if these errors are on the RSO and COM pins, they are not correctly detected when the internal excitation signal is in use (EXIO = 1) due to a conflict between the current from the short to the power supply or ground and the excitation current from the buffer. When an external excitation signal is used (EXIO = 0), errors on those pins are detected.

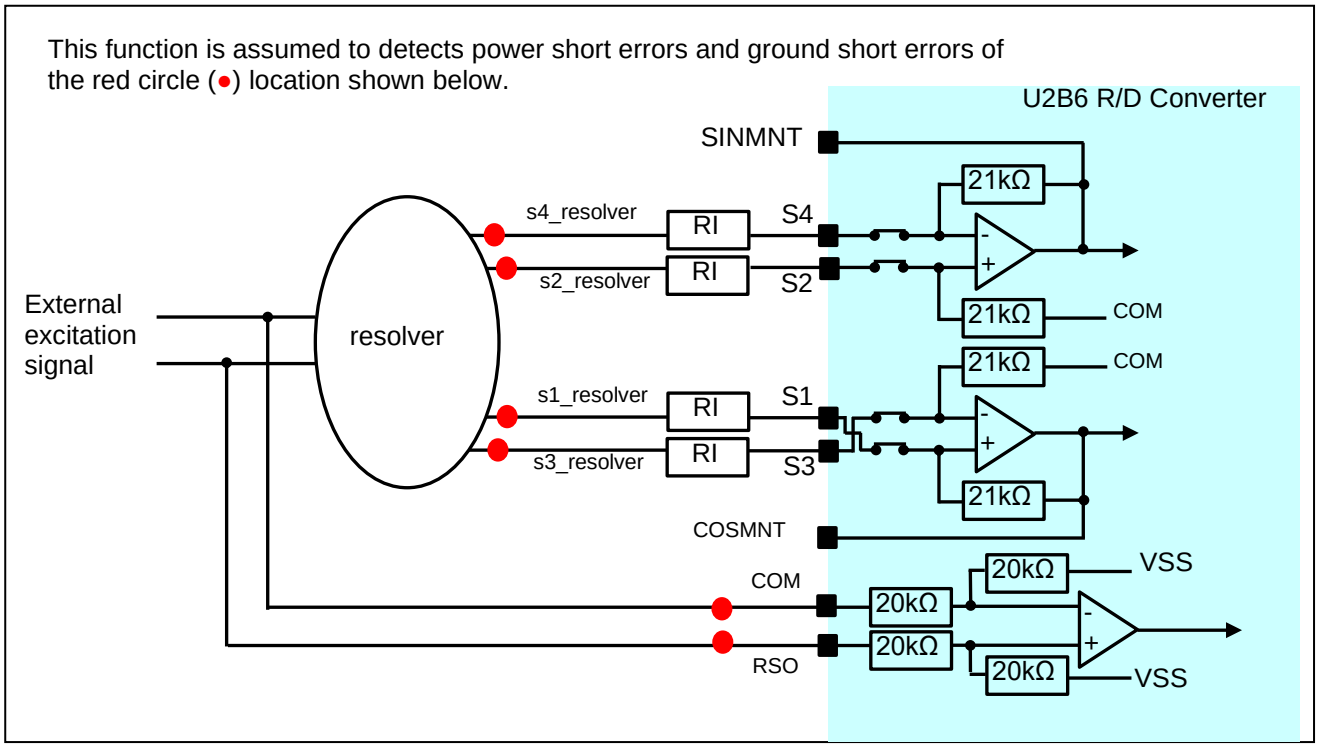


Figure 4-21 Assumed Circuit of Resolver Signal Power/Ground Short Error Detection

Since S1 to S4 input pins are incorporating the amplifier, even if S1 to S4 pins of the resolver are short circuited to the power supply or ground, the potential of S1 to S4 input pins of the R/D converter does not necessarily become the power supply or the ground voltage level. Therefore, power/ground short error can be detected by disconnecting the amplifier input temporarily with a switch. Short circuits of 6 pins RSO, COM, S1 to S4 are detected while disconnecting. The disconnecting time by a switch is about 78µs (13µs x 6pins). The output level of SINMNT and COSMNT becomes same level as COM because the input is disconnected during this time. The output angle of the R/D converter continues tracking angles in accordance with the rotational speed at the beginning of the resolver signal power/ground short error detection function.

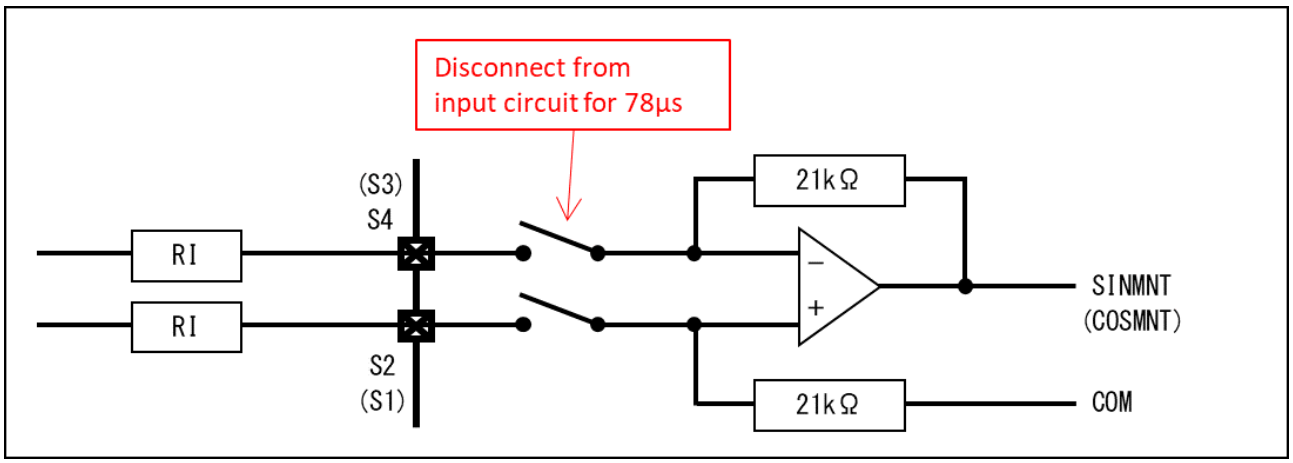


Figure 4-22 Disconnecting Position at the Time of Power/Ground Short Error Detection

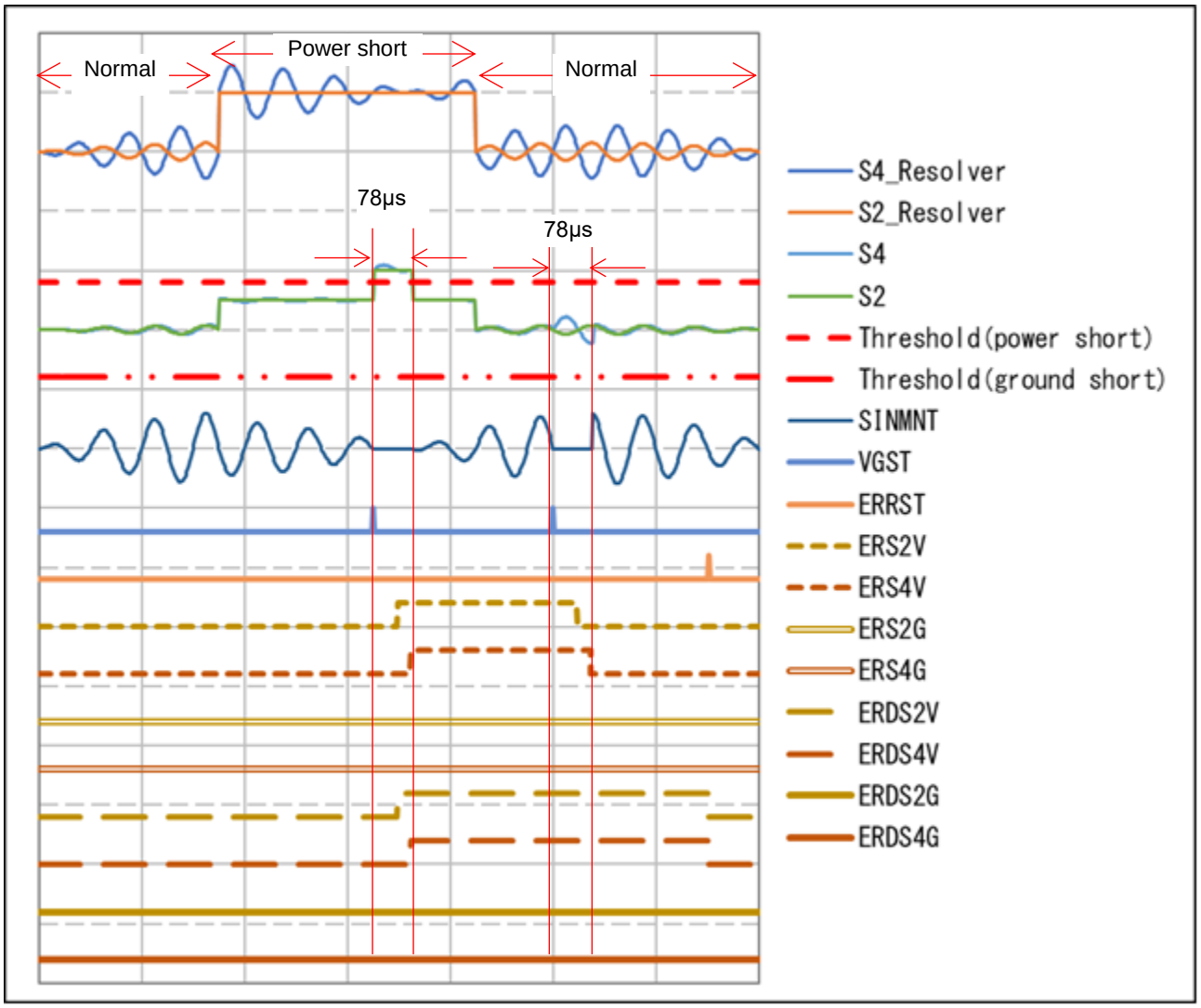


Figure 4-23 Detecting Power Short Caused by the Short Circuit of the S2 Signal

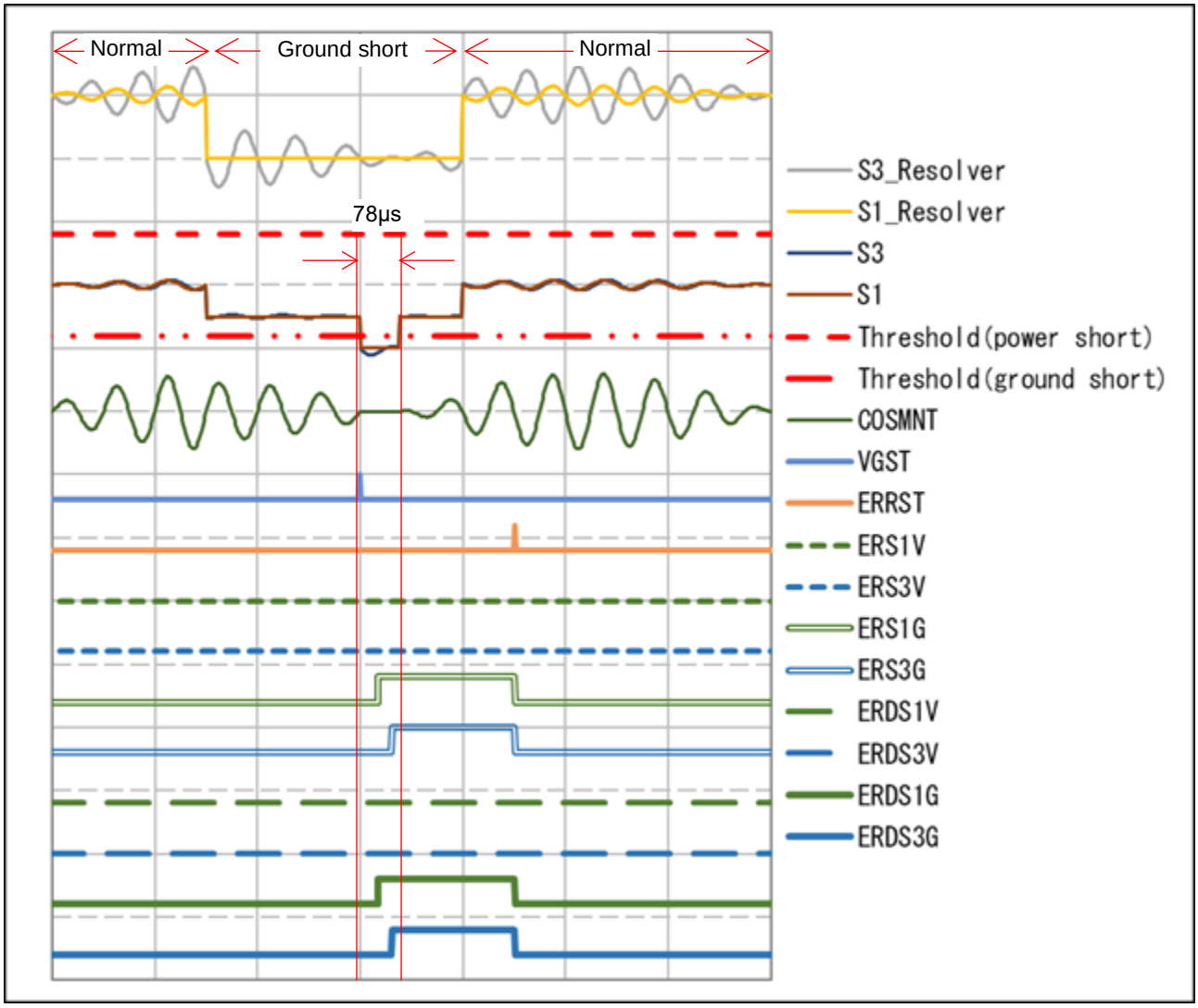


Figure 4-24 Detecting Ground Short Caused by Short Circuit of the S1 Signal to the Ground

4.2.5.1 Example of Register Settings

Table 4-5 shows the example of register settings of when the resolver signal power/ground short error detection function is used.

Table 4-5 Example of Register Settings of When Resolver Signal Power/Ground Short Error Detection Function is Used

Register name/ Abbreviation	Bit name/ Abbreviation	Set Value	Function
Error detection register 1/ RDC3ALnDIAG1	Power/Ground Short Error Detection Start Method Select / VGASL[1:0]	1	When 1 is written to the VGST bit, a power/ground short error detection is started.
	Power/Ground Short Error Detection Start / VGST	1	Writing 1 to this bit executes power/ground short error detection a single time.
	Error Detection Start / ERDEN	1	Error detection is enabled when the error detection output mask is released after 26 milliseconds* have elapsed following this bit being set to 1.
	Error Signal Reset Bit / ERRST	1	Writing 1 to this bit resets “error detection output register 1” to 0. Note that each of these bits remains at 1 if an error is continuous.
Error detection register 2/ RDC3ALnDIAG2	RSO Power Short Error Select / ERR1VS	0	Set the bits ERR, ERHD, ERR1V, and ERDR1V to 1 on occurrence of an RSO pin power short error.
	COM Power Short Error Select / ERR1VS	0	Set the bits ERR, ERHD, ERR2V, and ERDR2V to 1 on occurrence of a COM pin power short error.
	S1 Power Short Error Select / ERS1VS	0	Set the bits ERR, ERHD, ERCNV, ERS1V, and ERDS1V to 1 on occurrence of an S1 pin power short error.
	S2 Power Short Error Select / ERS2VS	0	Set the bits ERR, ERHD, ERCNV, ERS2V, and ERDS2V to 1 on occurrence of an S2 pin power short error.
	S3 Power Short Error Select / ERS3VS	0	Set the bits ERR, ERHD, ERCNV, ERS3V, and ERDS3V to 1 on occurrence of an S3 pin power short error.
	S4 Power Short Error Select / ERS4VS	0	Set the bits ERR, ERHD, ERCNV, ERS4V, and ERDS4V to 1 on occurrence of an S4 pin power short error.
	RSO Ground Short Error Select / ERR1GS	0	Set the bits ERR, ERHD, ERR1G, and ERDR1G to 1 on occurrence of an RSO pin ground short error.
	COM Ground Short Error Select / ERR2GS	0	Set the bits ERR, ERHD, ERR2G, and ERDR2G to 1 on occurrence of a COM pin ground short error.
	S1 Ground Short Error Select / ERS1GS	0	Set the bits ERR, ERHD, ERCNV, ERS1G, and ERDS1G to 1 on occurrence of an S1 pin ground short error.
	S2 Ground Short Error Select / ERS2GS	0	Set the bits ERR, ERHD, ERCNV, ERS2G, and ERDS2G to 1 on occurrence of an S2 pin ground short error.
	S3 Ground Short Error Select / ERS3GS	0	Set the bits ERR, ERHD, ERCNV, ERS3G, and ERDS3G to 1 on occurrence of an S3 pin ground short error.
	S4 Ground Short Error Select / ERS4GS	0	Set the bits ERR, ERHD, ERCNV, ERS4G, and ERDS4G to 1 on occurrence of an S4 pin ground short error.

4.2.6 Sum-of-Squares Amplitude Error Detection

This function detects modulation, distortion and noise in the amplitudes of the sine and cosine signals input from the resolver.

The sum-of-squares of the monitored signals (SINMNT, COSMNT) acquired in the ADC within the RDC are taken and integrated within the excitation period. Upper and lower threshold values are set for the value thus calculated and the number of times the calculated value rise above or fall below the thresholds is counted. If the number exceeds the threshold for the counted value, it is output as a sum-of-squares amplitude error. The procedure runs automatically, but the user is required to set the upper and lower threshold for the integrated sum-of-squares values in the SQHTH and SQLTH bits and the threshold for the number of times the calculated value falls outside the range in the SQCTH bits. The counter values are cleared at the desired time by the writing to the SQERST bit.

Figure 4-25 shows an example of waveforms where the amplitudes of the signals input to the resolver are reduced, the calculated value fell outside the threshold range five times, and a sum-of-squares amplitude error is generated.

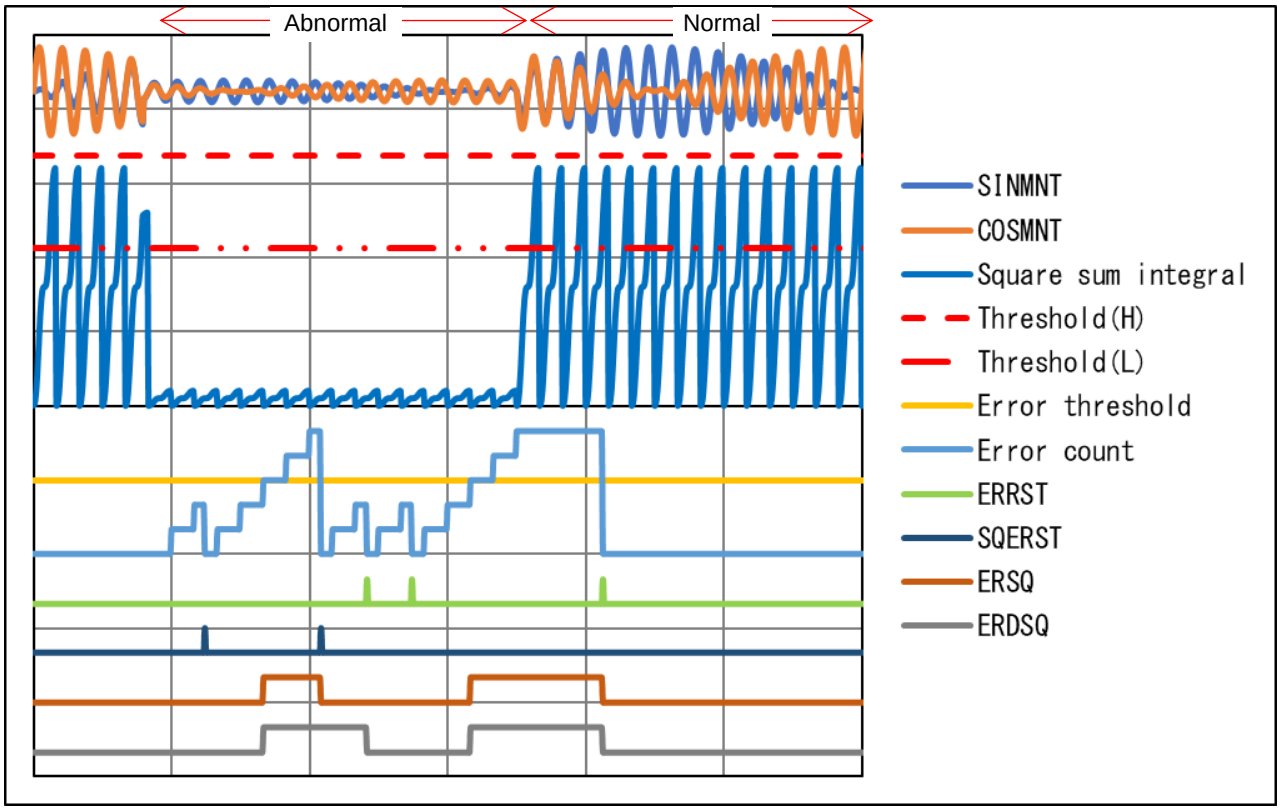


Figure 4-25 Sum-of-Squares Amplitude Error Detection

4.2.6.1 Example of Threshold Determination Method

The table below show the values of the integrated sum-of-squares amplitude for the ideal waveform. They are different from actual values due to other influences such as noises. Set thresholds by considering these influences.
Calculate values which are not in the following tables by linear interpolation.

Table 49.49 Relationship between the Resolver Signal (MNT Signal) Amplitude, Excitation Frequency, and Values of the Integrated Sum-of-Squares Amplitude

excitation frequency (kHz)→	5kHz	7.5kHz	10kHz	12.5kHz	15kHz	17.5kHz	20kHz
MNT signal amplitude ↓							
0.1 × RVCC (Vpp)	254	169	128	104	83	72	63
0.2 × RVCC (Vpp)	1032	692	520	417	341	296	255
0.3 × RVCC (Vpp)	2304	1533	1156	921	771	649	582
0.4 × RVCC (Vpp)	4104	2719	2052	1638	1364	1169	1031
0.5 × RVCC (Vpp)	6435	4296	3222	2583	2152	1847	1601
0.6 × RVCC (Vpp)	9230	6127	4595	3685	3067	2633	2294
0.7 × RVCC (Vpp)	12567	8379	6282	5041	4177	3577	3144
0.8 × RVCC (Vpp)	16420	10942	8167	6574	5471	4684	4096
0.9 × RVCC (Vpp)	20761	13855	10355	8281	6909	5918	5212

∗ Table is a transcription of "Table 49.49" in the user's manual.

The example below is a case where the sum-of-squares amplitude error detection is executed under the following conditions.

- Resolver signal amplitude : 2.1Vpp
- Excitation frequency : 10kHz
- The number of conversions in the excitation frequency : SINMNT/COSMNT, 50 times each
- Acceptable error ranges from the ideal waveform : ±0.3Vp-p (1.8 to 2.4Vp-p)

From above conditions, the lower-limit value(1.8Vp-p) and the upper-limit value(2.4Vp-p) used for the sum-of-squares amplitude error detection are not described in above tables. Therefore, find values by linear interpolation between two points close to respective values. In the above example, when ADRD=0, the lower- and the upper-limit values become as follows.

- Lower-limit value :1694 Upper-limit value :2988

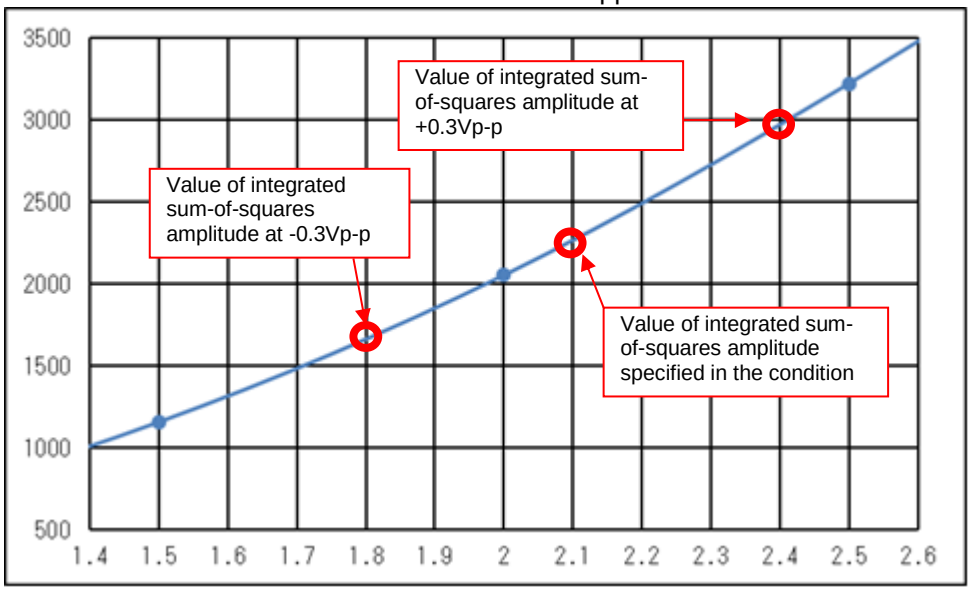


Figure 4-26 Image of Upper- and Lower-Limit Values Used In the Sum-of-Squares Amplitude Error Detection

4.2.6.2 Example of Register Settings

Table 4-6 shows the example of register settings of when the sum-of-squares amplitude error detection function is used.

Table 4-6 Example of Register Settings of When Sum-of-Squares Amplitude Error Detection Function is Used

Register name/ Abbreviation	Bit name/ Abbreviation	Set Value	Function
Error detection register 1/ RDC3ALnDIAG1	Error Detection Start / ERDEN	1	Error detection is enabled when the error detection output mask is released after 26 milliseconds have elapsed following this bit being set to 1.
	Sum-of-Squares Amplitude Error Excitation Counter Reset / SQERST	1	Writing 1 to this bit resets the sum-of-squares amplitude error excitation counter to 0.
	Error Signal Reset Bit / ERRST	1	Writing 1 to this bit resets "the error detection register 1" to 0. Note that each of these bits remains at 1 if an error is continuous.
Error detection register 2/ RDC3ALnDIAG2	Sum-of-Squares Amplitude Error Select / ERSQS	0	Set the bits ERR, ERHD, ERSQ, and ERDSQ to 1 on occurrence of a sum-of-squares amplitude error
Error detection register 3/ RDC3ALnDIAG3	Sum-of-Squares Amplitude Upper Threshold / SQHTH[15:0]	8192	Sets the upper threshold for values of the integrated sum-of-squares amplitude.
	Sum-of-Squares Amplitude Lower Threshold / SQLTH[15:0]	512	Sets the lower threshold for the values of the integrated sum-of-squares amplitude.
Error detection register 4/ RDC3ALnDIAG4	Sum-of-Squares Amplitude Error Excitation Counts Threshold / SQCTH[2:0]	4	Selects the number of excitation periods in which abnormal amplitudes may be generated in the judgment of integrated sum-of-squares amplitude errors. The number of times set in these bits being exceeded is judged to represent an integrated sum-of-squares amplitude error.
Error detection register / RDC3ALnREF	Excitation Extraction Noise Filter /PLSNFS	1	Selects the noise filter for the excitation component extraction circuit. 1: The noise filter is used.

4.2.7 Excitation Period Error Detection

The period measurement timer measures the cycle of excitation signal (zero-crossing signal). When an edge (selectable between rise edge or fall edge) of the zero-crossing signal is detected, the value of the period measurement counter is captured and stored in the RDC3ALnETCAP register. By reading the RDC3ALnETCAP register, the cycle of excitation signal can be obtained.

When the IREN bit in the RDC3ALnETEN register is set to 1 (enables the interrupt), an excitation timer interrupt request is generated if the value set in the RDC3ALnETCAP register matches the period measurement counter value. The excitation signal cycle error can be detected by setting a value of longer duration than the excitation signal cycle to the RDC3ALnETCAP register. An excitation signal cycle error is detected upon the occurrence of an excitation timer interrupt request.

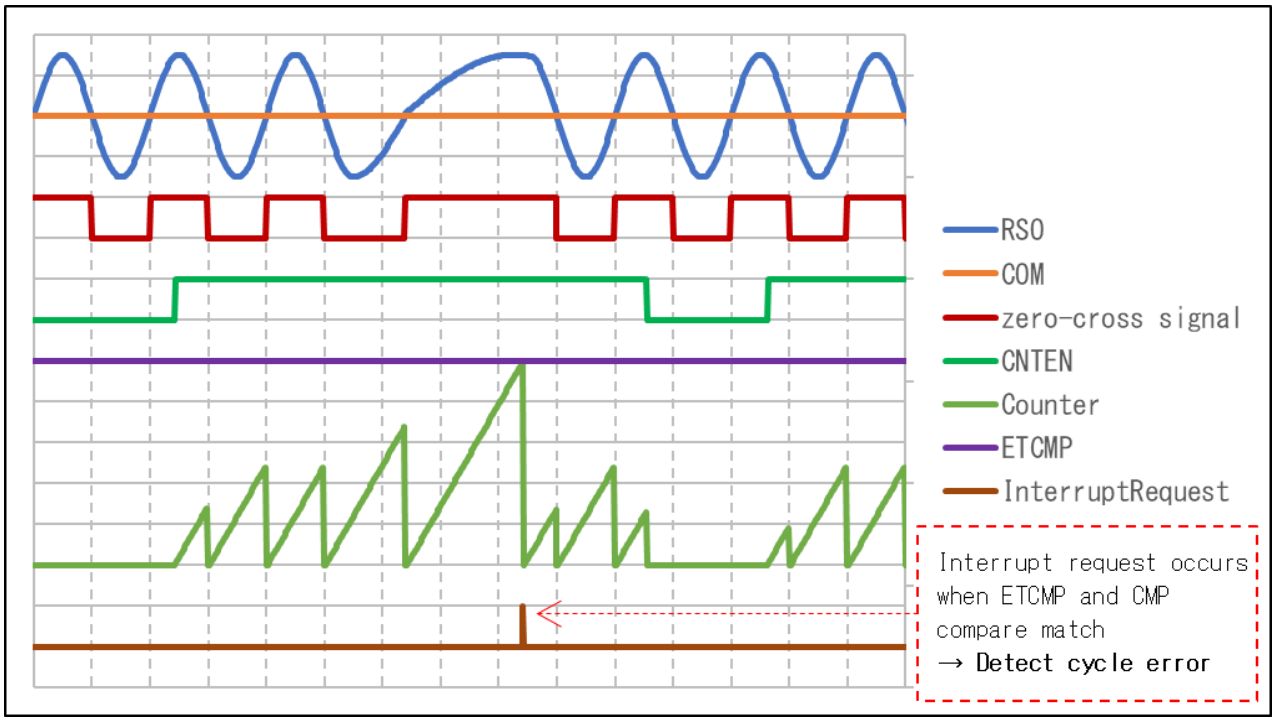


Figure 4-27 Excitation Period Error Detection

4.2.7.1 Example of Register Settings

Table 4-7 shows the example of register settings of when the period measurement timer of excitation signal is used as the excitation period error detection function.

Table 4-7 Example of Register Settings of When Excitation Period Error Detection Function is Used

Register name/ Abbreviation	Bit name/ Abbreviation	Set Value	Function
ET Control Register / RDC3ALnETEN	Compare Match Function Enable / CMPEN	1	Enables and disables the compare match function. 1: Enables the compare match function.
	Interrupt Request Enable / IREN	1	Enables and disables interrupt requests. 1: Enables the output of interrupt.
	Counter Operation Enable / CNTEN	1	This is the count enable signal for the period measurement timer and the event timer. 1: The period measurement timer and the event timer are operated.
ET Capture Register / RDC3ALnETCAP	ET Compare / CMP[15:0]	0x1F40	Sets count value to generate a compare match. This example setting is the doubled value of the 10kHz excitation signal period (200µsec).

4.3 Notes on Error Detections

4.3.1 Notes on Resolver Signal Disconnection Error Detection

- For the resolver signal disconnection error detection, the level used to compare to the threshold in a VR resolver and a DC resolver are different. The common level of SINMNT/COSMNT is compared with the threshold when operating with a VR resolver, the level of SINMNT/COSMNT itself is compared with threshold when operating with a DC resolver. Thresholds for each resolver is set individually.

4.3.2 Notes on Sum-of-Squares Amplitude Error Detection

- The sum-of-squares amplitude error detection function is only available for resolvers that require the input of signals with excitation components, but not for DC resolvers, which do not require this.

- Setting the ERSQS bit to 0 enables the detection of sum-of-squares amplitude errors. After setting this bit to 0, clear the counted value by setting the SQERST bit to 1.

- In checking for a power/ground short error, the excitation amplitude disappears for 78μs, so the resulting error is counted once in sum-of-squares amplitude error detection. When checking for a power/ground short error by writing to the VGST bit when VGASL[1:0] = 01, set the ERSQS bit to 1 to switch sum-of-squares amplitude error detection off during the check.

- When checking for power/ground short errors is to proceed at 10ms intervals because the setting of VGASL[1:0] = 10, clear the effect of this on the counting of sum-of-squares amplitude errors at least once per 10ms by using the SQERST bit.

- If you want to check for power/ground short errors but do not require checking of sum-of-squares amplitude errors, leave the value of ERSQS as 1.

- In the sum-of-squares amplitude error detection, be sure to set the excitation extraction noise filter bit (PLSNFS) of the excitation setting register (RDC3ALnREF) to 1(The noise filter is used). This setting will prevent from extracting noise as the excitation period when the excitation signal has noise.

4.4 Flowchart of Entire Error Detection Register Settings

The flowchart below shows register settings of this operation example.

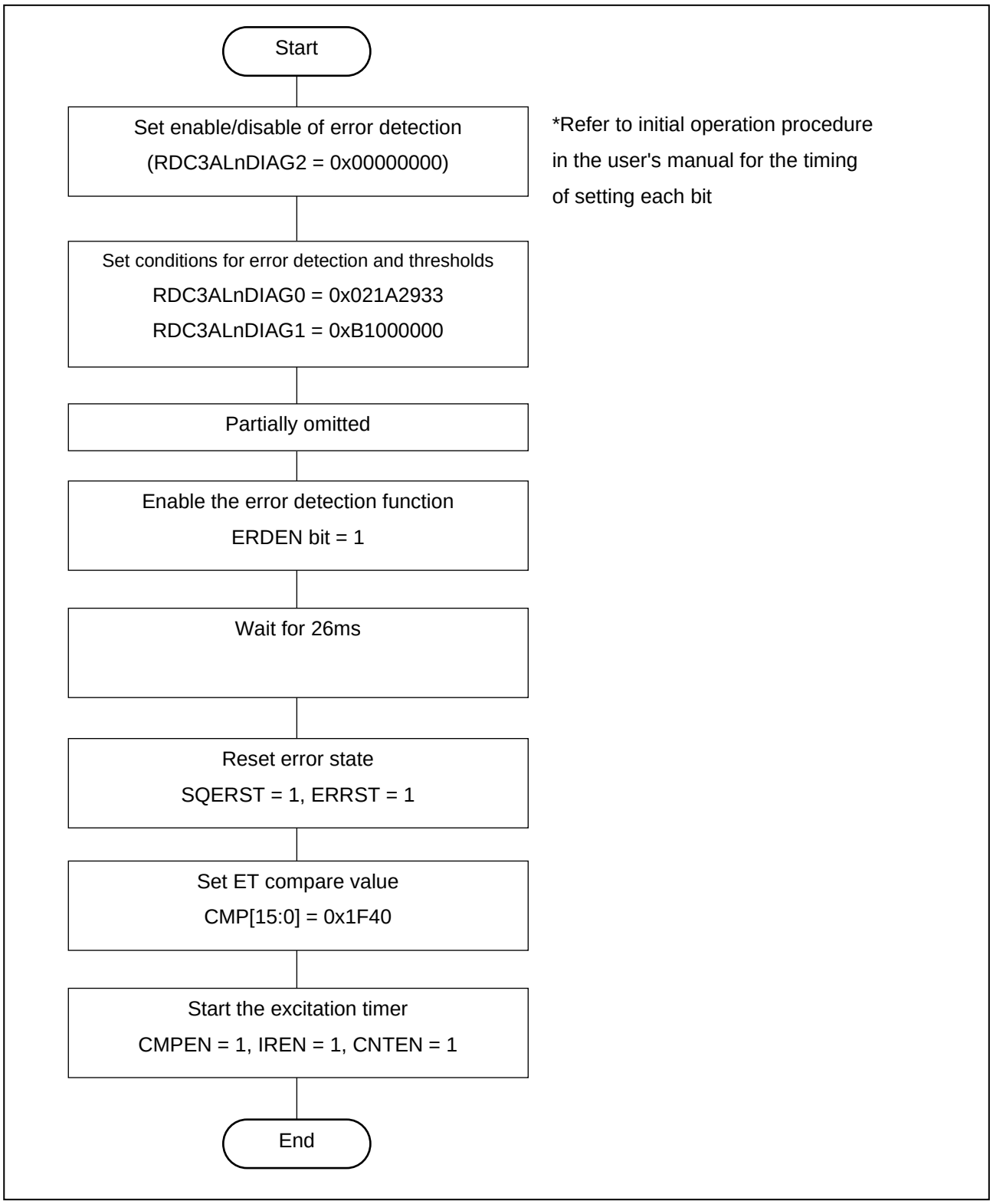


Figure 4-28 Flowchart of Register Settings

5. Self-Diagnosis

5.1 Built-in Self-Test Function (BIST)

RDC3AL has a built-in self-test (BIST) function to check the validity of specified operations.

By setting the BIST command in the RDC3ALnBIST1 register, this function generates the desired signal input that is simulated internally, and monitors the signal output in response.

The test items are shown below.

Table 5-1 BIST function

Items	Diagnosis
Angle Conversion BIST	Self-test of the R/D conversion function The following electrical angles can be set as a resolve signal input: ● Target angle 0° ● Target angle 45° ● Target angle 270°
Error Detection BIST	Self-test for the error detection function ● Resolver signal error detection BIST ● Resolver signal disconnect error detection BIST (sin / cos) ● R/D conversion error detection BIST ● Power/ground short error detection BIST ● Sum-of-Squares amplitude error detection BIST (high side / low side)
AD BIST	Self-test for the validity of the result of 12-bit SAR-ADC conversion ● Apply voltages of 1, 2.5, and 4 V in order and judge the result of ADC conversion. ● The threshold value for determination is set by the ADB3TH[1:0] bits.

5.2 Details of BIST

5.2.1 Types of BIST

BIST is classified into two types depending on the length of execution time: short-period and long-period.

Long-period BIST can only be executed at power-on. Long-period BIST operates with an internally generated simulated signal for up to 10 ms BIST, so the angle output does not match the resolver input.

Short-period BIST can be performed during angle conversion and maintains angle conversion tracking during BIST execution. Short-period BIST can be performed even when the power is turned on, but long-period BIST should be performed first.

- Short-period BIST : ADBIST, resolver signal error detection BIST, resolver signal disconnect error detection BIST(sin/cos), power short error BIST, ground short error BIST, sum-of-squares amplitude error detection BIST (high side/low side)
- Long-period BIST : angle conversion BIST, conversion error BIST

5.2.2 Execution of BIST

Perform the following settings to execute BIST.

(1) Enable the forced gain control function when executing a BIST. (Set the AGCD bit in the RDC3ALnPI1 register to 0.)

(2) To execute a short-period BIST, set the EINTEN bit to 0 to disable error interrupts.

(3) Set the VGASL[1:0] bits to 00B when executing a BIST.

(4) Read the VGFLG bit (Power/ground short error detection running bit) as 0. If the value is 1, read the bit again after waiting for about 80 μs.

(5) Set the phase correction bits in the sine and cosine angle correction register to 0° when executing the angle conversion BIST.

Sine phase correction bits SINPO[11:0] = 000_H

Cosine phase correction bits COSPO[11:0] = 000_H

(6) To execute conversion error BIST, set the EDPS bit to 10_B.

(7) Set the input gain resistance value at default (21 kΩ) and the excitation buffer amplitude value at default (2Vpp) when executing a BIST.

PGX1=0, IRSS0 = 1, EXOC[1:0] = 10B, IRSC[3:0] = 0100B, IRSS1 = 0, EXOS = 0, EAATSP = 1

(8) Clear the count value in the SQERST bit by setting 1 before running sum-of-squares amplitude detection BIST (high side/low side).

(9) When the BIST is completed,

set the BISTCL bit in the RDC3ALnBIST1 register to 1 to clear the BIST results.

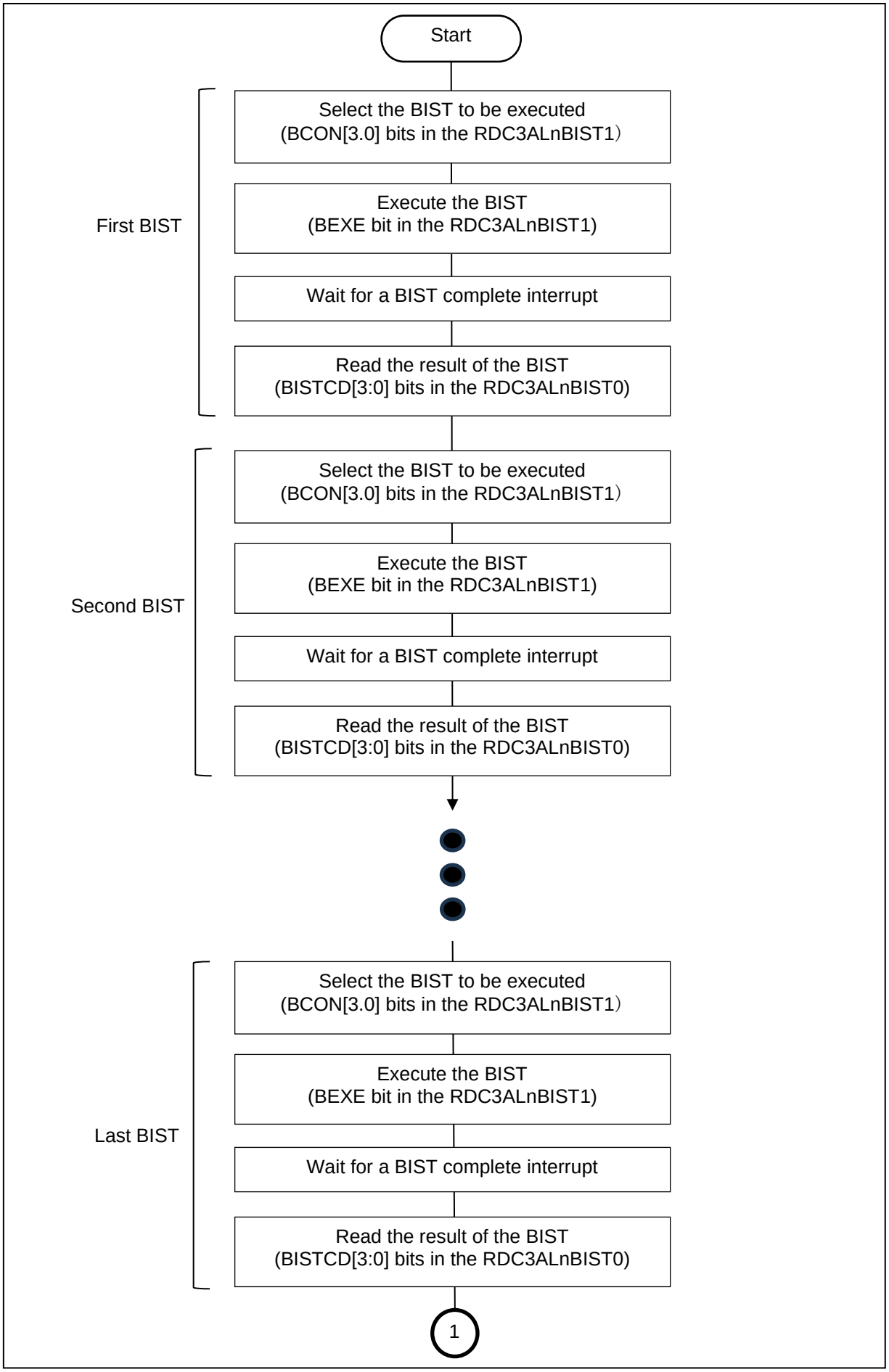
set the ERRST bit in the RDC3ALnDIAG1 register to 1 to reset the error signal.

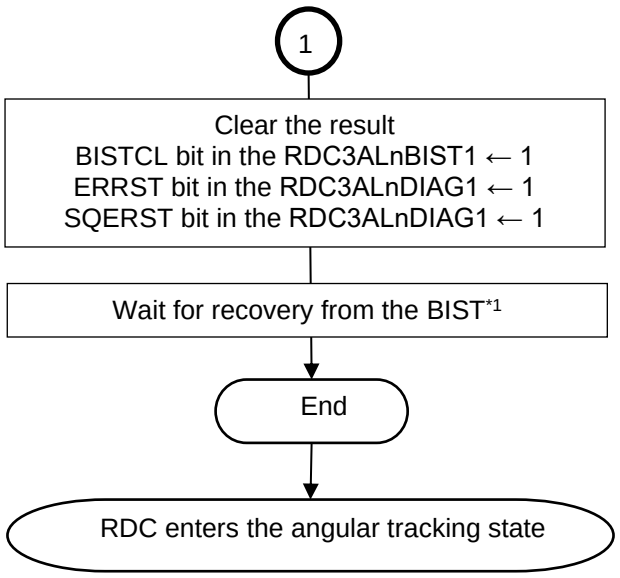
set the SQERST bit in the RDC3ALnDIAG1 register to 1 to reset the counter value of sum-of squares amplitude error.

Return the settings of the registers which were changed in steps (1), (2), (3), (5), (6), and (7) to their original values.

Table 5-2 BISTs for Each Setting of Values

BCON[3:0]	BIST to be Executed
0000	BEXE bit is disabled
0001	This setting is not allowed.
0010	Sum-of-squares amplitude error detection BIST (low side)
0011	Sum-of-squares amplitude error detection BIST (high side)
0100	ADBIST
0101	Angle conversion BIST (0°)
0110	Angle conversion BIST (45°)
0111	Angle conversion BIST (270°)
1000	This setting is not allowed.
1001	Error detection BIST: resolver signal error detection BIST
1010	Error detection BIST: resolver signal disconnection detection BIST (cosine side)
1011	Error detection BIST: Resolver signal disconnection detection BIST (sine side)
1100	Error detection BIST: conversion error BIST
1101	Error detection BIST: power short error BIST
1110	Error detection BIST: ground short error BIST
1111	This setting is not allowed.

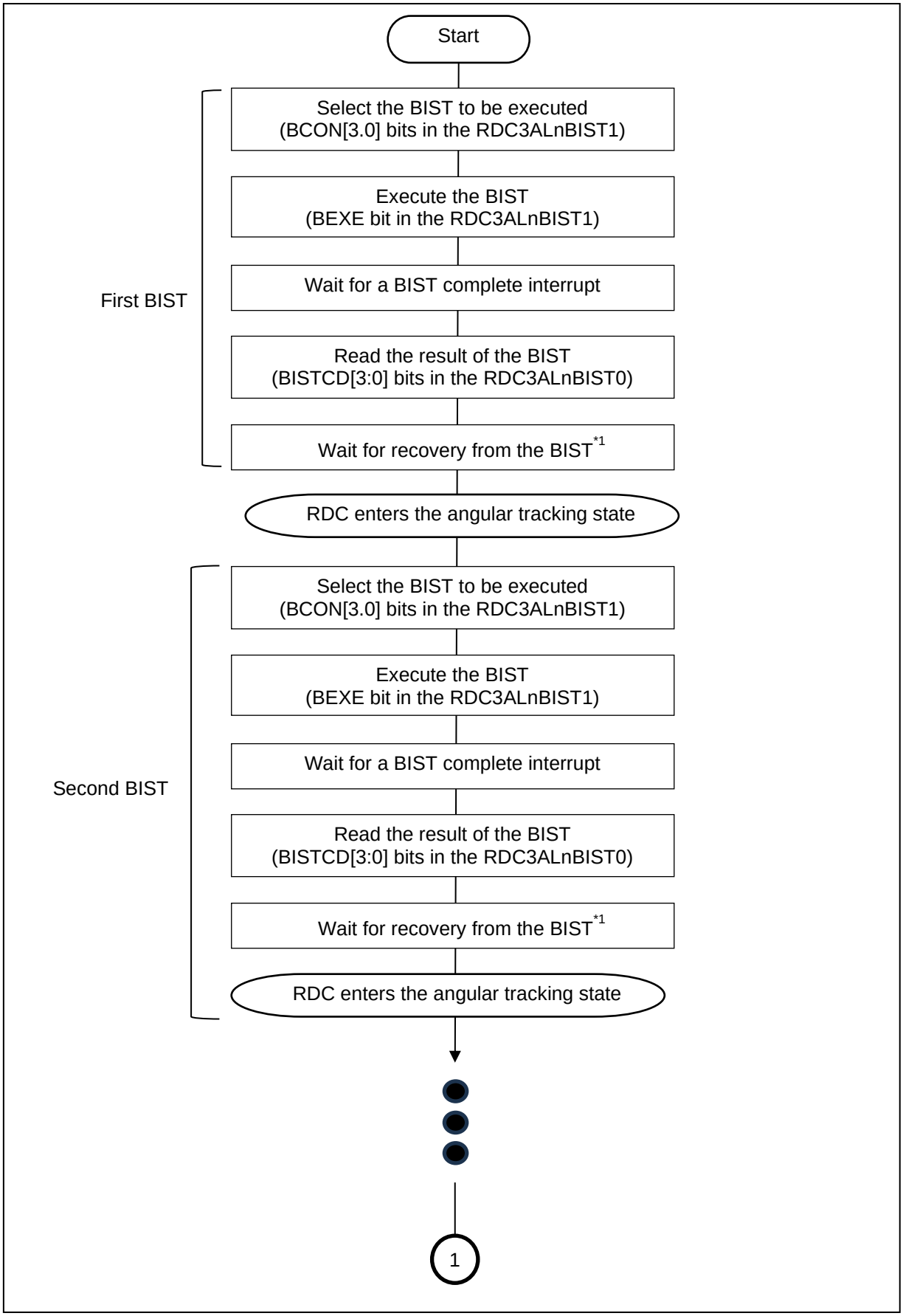

Start
First BIST
Select the BIST to be executed
(BCON[3.0] bits in the RDC3ALnBIST1)
Execute the BIST
(BEXE bit in the RDC3ALnBIST1)
Wait for a BIST complete interrupt
Read the result of the BIST
(BISTCD[3:0] bits in the RDC3ALnBIST0)
Second BIST
Select the BIST to be executed
(BCON[3.0] bits in the RDC3ALnBIST1)
Execute the BIST
(BEXE bit in the RDC3ALnBIST1)
Wait for a BIST complete interrupt
Read the result of the BIST
(BISTCD[3:0] bits in the RDC3ALnBIST0)
Last BIST
Select the BIST to be executed
(BCON[3.0] bits in the RDC3ALnBIST1)
Execute the BIST
(BEXE bit in the RDC3ALnBIST1)
Wait for a BIST complete interrupt
Read the result of the BIST
(BISTCD[3:0] bits in the RDC3ALnBIST0)
1

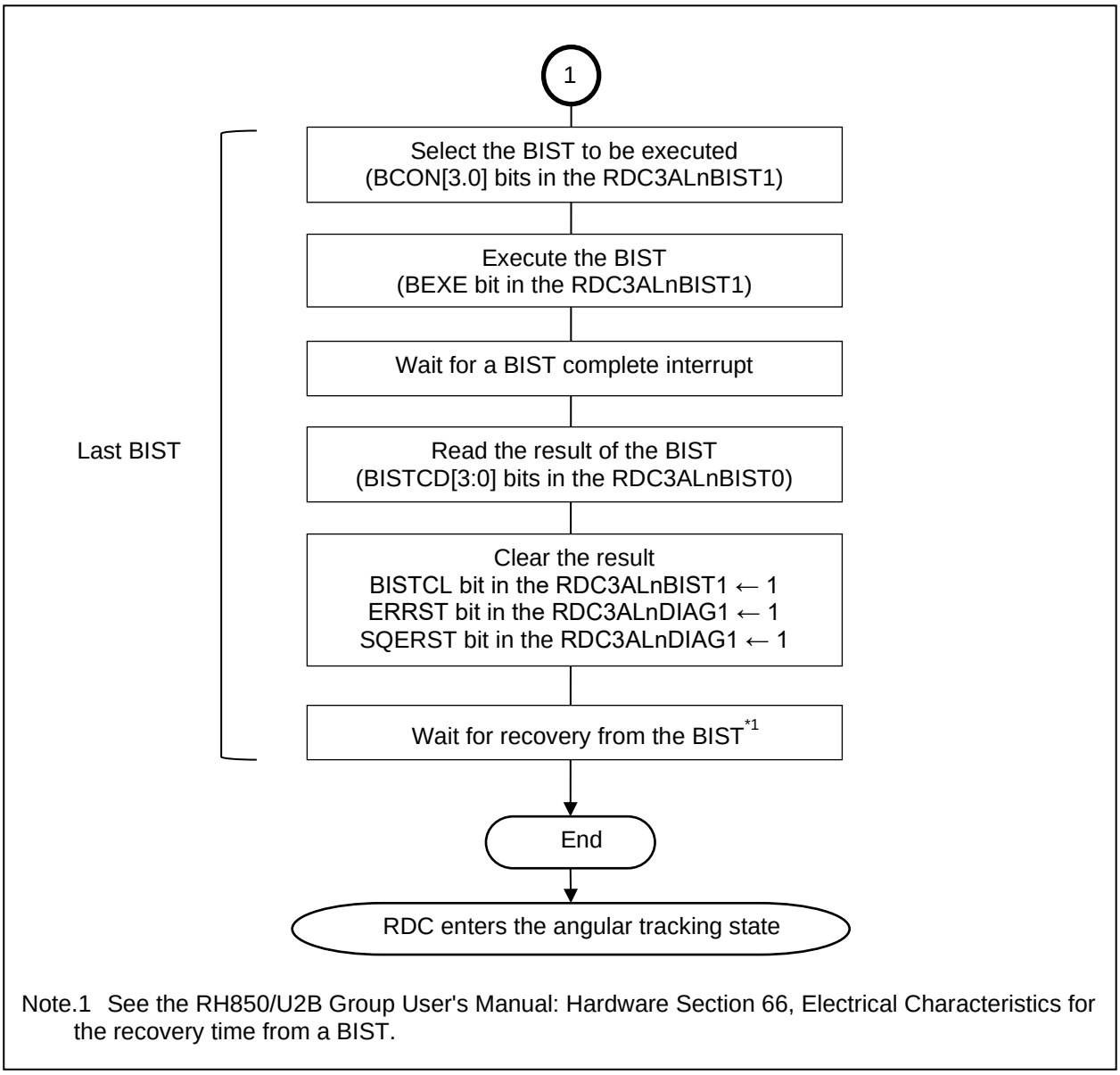


Note.1 See the RH850/U2B Group User's Manual: Hardware Section 66, Electrical Characteristics for the recovery time from a BIST.

Perform all long-period BISTs you want to perform first, and then perform short-period BISTs.

Figure 5-1 Sequence of Executing BISTs after Starting Up the Power


Start
First BIST
Select the BIST to be executed
(BCON[3.0] bits in the RDC3ALnBIST1)
Execute the BIST
(BEXE bit in the RDC3ALnBIST1)
Wait for a BIST complete interrupt
Read the result of the BIST
(BISTCD[3:0] bits in the RDC3ALnBIST0)
Wait for recovery from the BIST*1
RDC enters the angular tracking state
Second BIST
Select the BIST to be executed
(BCON[3.0] bits in the RDC3ALnBIST1)
Execute the BIST
(BEXE bit in the RDC3ALnBIST1)
Wait for a BIST complete interrupt
Read the result of the BIST
(BISTCD[3:0] bits in the RDC3ALnBIST0)
Wait for recovery from the BIST*1
RDC enters the angular tracking state
1



Note.1 See the RH850/U2B Group User's Manual: Hardware Section 66, Electrical Characteristics for the recovery time from a BIST.

Figure 5-2 Sequence of Executing BISTs during Angle Conversion (Short-period BIST)

5.2.3 ADC software BIST

Failures in the ADC are diagnosed by the CPU through the following procedure: the DAC code in the 12-bit SAR-ADC written to the relevant register is converted in the ADC and the result is read from the relevant register. The user can set the DAC codes freely, that is, to any of the 4096 codes for the 12-bit ADC.

In the ideal state, the software will return the same value of the DAC code which was set for the software BIST as the result of A/D conversion.

In actual operations, however, values with errors are output due to non-ideal factors.

Therefore, users are required to set a suitable value for the CPU to judge these errors (around ± 32 LSB). With this software BIST, it is possible to diagnose the normality of the combination functions of all the switches of the DAC in the ADC.

On the other hand, the ADBIST described in section (1)., Built-in Self-Test Function, diagnoses the results of conversion by applying three voltages to the input nodes of the ADC.

By using ADBIST and this software BIST together, it is possible to diagnose failures in almost all nodes in the 12-bit ADC.

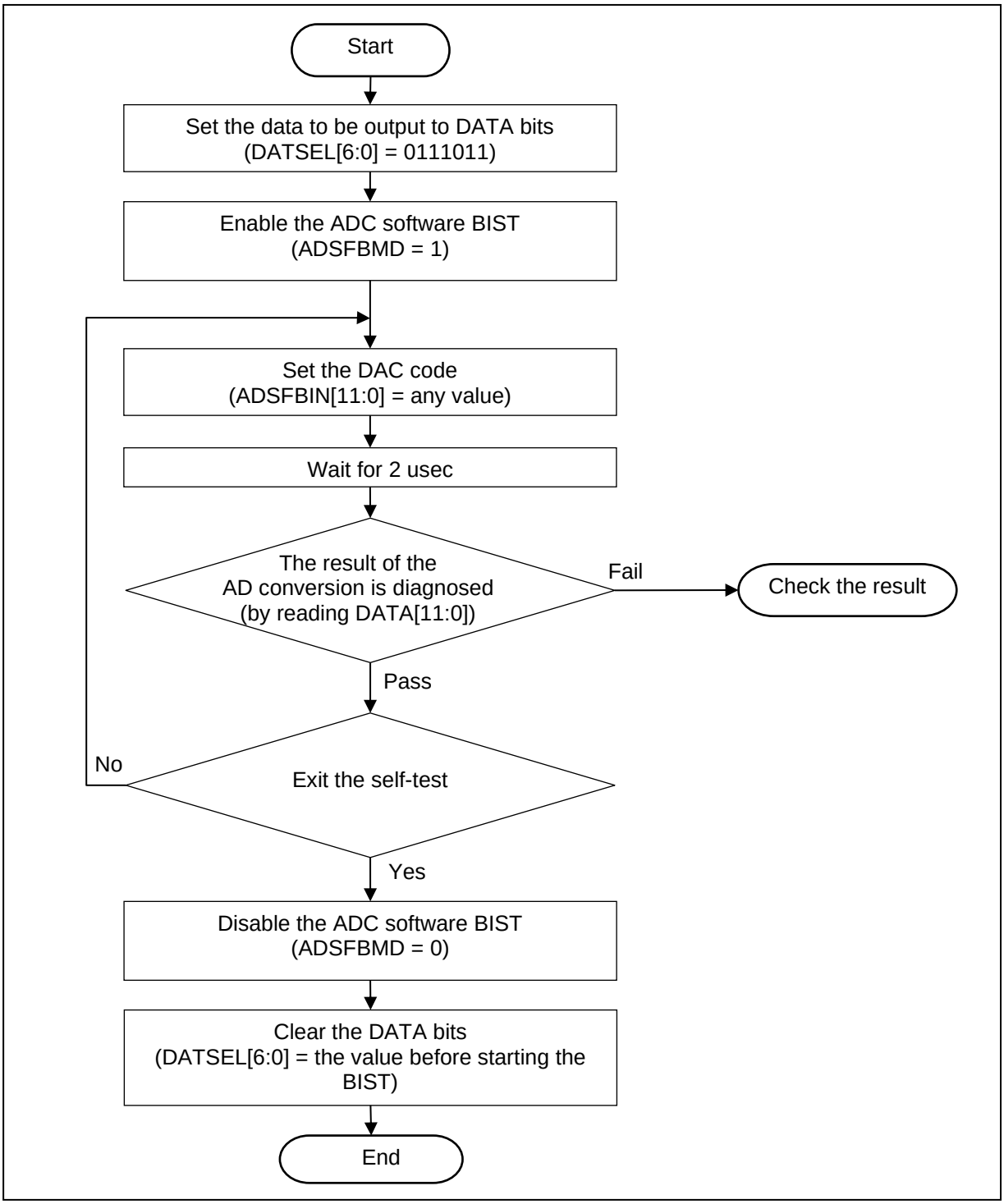


Figure 5-3 Operating Sequence of the ADC Software BIST

5.3 Notes of BIST

- Depending on the BIST, a RDC error interrupt is generated due to the erroneous internal state.
  If the occurrence of this error disturbs the operation, disable RDC error interrupt by the EINTEN bit.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2022.03.31	-	First edition
2.00	2023.09.29	44-	Add “5. Self-Diagnosis”

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   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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