RL78/F22, F25

Interrupt Source Determination Procedure

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Introduction

Some interrupt vector tables of the target devices (RL78/F22, F25) share multiple interrupt sources with one interrupt vector table as shown in the following **Table**. When using multiple interrupt sources assigned to the same interrupt vector table at the same time, it is necessary to determine which interrupt has occurred in the interrupt handler, or whether both interrupts have occurred.

This application note describes how to determine the interrupt source when using both interrupt sources simultaneously.

Table. List of Multiple Interrupt Sources that are Shared in One Interrupt Vector Table (1/2)

Vector Table Address	Interrupt Source Note 1		Reference Section
	Name	Trigger	
0010H	INTP4	Pin input edge detection 4	**1.1**
	INTSPM	Stack pointer overflow/underflow detection	
0012H	INTP5	Pin input edge detection 5	**1.2**
	INTCMP0 Note 3	Comparator detection 0	
0014H	INTP13 Note 3	Pin input edge detection 13	**1.3**
	INTCLM	PLL clock stop detection	
002AH	INTP8	Pin input edge detection 8	**1.4**
	INTRTC	RTC pretimed signal or alarm match detection	
002EH	INTTM01	Timer interrupt of TAU0 channel 1	**1.5**
	INTLIN2TRM Note 3	LIN2 transmission	
0030H	INTTM02	Timer interrupt of TAU0 channel 2	
	INTLIN2RVC Note 3	LIN2 reception completed	
0032H	INTTM03	Timer interrupt of TAU0 channel 3	
	INTLIN2STA/INTLIN2 Note 3	LIN2 reception status/ LIN2 interrupt	
0036H	INTP6	Pin input edge detection 6	Cannot identify both interrupt sources.
	INTLIN2WUP Note 3	LIN2 reception pin input detection	
	INTTM11H	Upper 8-bit interval timer interrupt of TAU1 channel 1	
0038H	INTP7	Pin input edge detection 7	
	INTTM13H	Upper 8-bit interval timer interrupt of TAU1 channel 3	
003AH	INTP9	Pin input edge detection 9	
	INTTM01H	Upper 8-bit interval timer interrupt of TAU0 channel 1	
003CH	INTP10 Note 3	Pin input edge detection 10	
	INTTM03H	Upper 8-bit interval timer interrupt of TAU0 channel 3	
0044H	INTTM05	Timer interrupt of TAU0 channel 5	**1.6**
	INTLIN0TRM	LIN0 transmission	
0046H	INTTM06	Timer interrupt of TAU0 channel 6	
	INTLIN0RVC	LIN0 reception completed	
0048H	INTTM07	Timer interrupt of TAU0 channel 7	
	INTLIN0STA/INTLIN0	LIN0 reception status/ LIN0 interrupt	
004AH	INTP11 Note 3	Pin input edge detection 11	Cannot use both simultainiously.Note2
	INTLIN0WUP	LIN0 reception pin input detection	
004EH	INTTM11	Timer interrupt of TAU1 channel 1	**1.7**
	INTLIN1TRM Note 3	LIN1 transmission	

Notes 1: It depends on the product. For details, show the user's manual.
2: Select the interrupt to be used with the target bit in the ISC register. For details on the ISC register, see "Figure. Input Switch Register (ISC) Format".
3: Only RL78/F25 product. RL78/F22 product does not have this interrupt.

Table. List of Multiple Interrupt Sources that are Shared in One Interrupt Vector Table (2/2)

Vector Table Address	Interrupt Source Note 1		Reference Section
	Name	Trigger	
0050H	INTTM12	Timer interrupt of TAU1 channel 2	**1.7**
	INTLIN1RVC Note 3	LIN1 reception completed	
0052H	INTTM13	Timer interrupt of TAU1 channel 3	
	INTLIN1STA/INTLIN1 Note 3	LIN1 reception status/ LIN1 interrupt	
005CH	INTKR	Key interrupt detection	Cannot identify both interrupt sources.
	INTRCAN0GRVC Note 3	CAN0 global receive message buffer reception	
006CH	INTP12	Pin input edge detection 12	Cannot use both simultainiously.Note2
	INTLIN1WUP Note 3	LIN1 reception pin input detection	
0074H	INTTM14 Note 3	Timer interrupt of TAU1 channel 4	**1.8**
	INTRCAN1GRVC Note 3	CAN1 global receive message buffer reception	
0076H	INTTM15 Note 3	Timer interrupt of TAU1 channel 5	
	INTRCAN1ERR Note 3	CAN1 channel error detection	
0078H	INTTM16 Note 3	Timer interrupt of TAU1 channel 6	
	INTRCAN1CFR Note 3	CAN1 transmit/receive FIFO message reception	
007AH	INTTM17 Note 3	Timer interrupt of TAU1 channel 7	
	INTRCAN1TRM Note 3	CAN1 channel transmit	

Notes 1: It depends on the product. For details, show the user's manual.
2: Select the interrupt to be used with the target bit in the ISC register. For details on the ISC register, see "**Figure. Format of Input Switch Control Register (ISC)**".
3: Only RL78/F25 product. RL78/F22 product does not have this interrupt.

Address: F0073H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ISC	0	0	0	ISC4	ISC3	ISC2	0	ISC0

ISC4	Input selection for external interrupt INTP6
0	INTP6 pin input signal is selected as external interrupt input.
1	LRXD2 pin input signal is selected as external interrupt input.

ISC3	Input selection for external interrupt INTP12
0	INTP12 pin input signal is selected as external interrupt input.
1	LRXD1 pin input signal is selected as external interrupt input.

ISC2	Input selection for external interrupt INTP11
0	INTP11 pin input signal is selected as external interrupt input.
1	LRXD0 pin input signal is selected as external interrupt input.

ISC0	Input selection for external interrupt INTP0
0	INTP0 pin input signal is selected as external interrupt input.
1	RXD0 pin input signal is selected as external interrupt input.

Cautions 1. Be sure to set the ISC3, ISC4 bits to 0 in RL78/F22 products.
2. For RL78/F22 product, when using the external interrupt of LRXD0, set the ISC2 bit to 1.

Figure. Format of Input Switch Control Register (ISC)

Contents

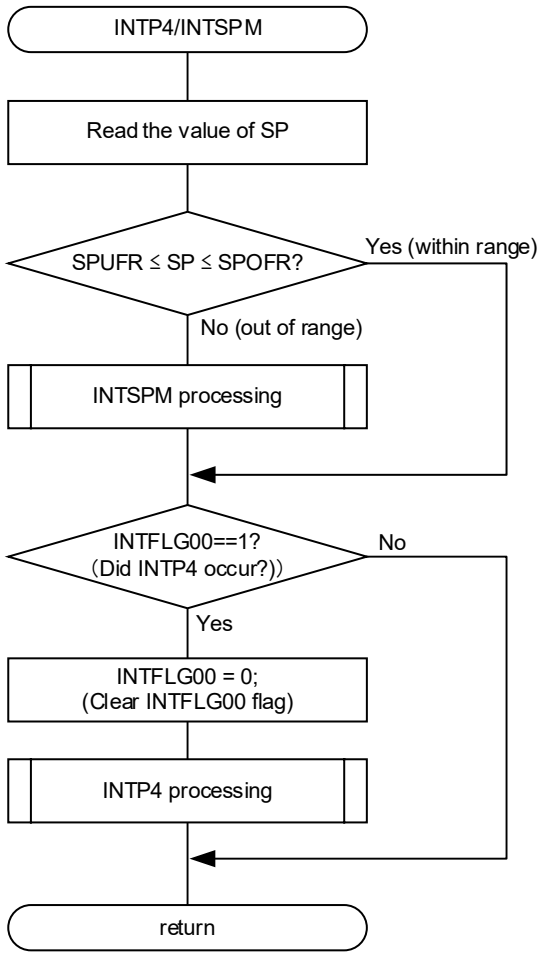
1. Interrupt Source Determination Procedure

In some interrupt vector tables of the target devices (RL78/F22, F25), multiple interrupt sources share one interrupt vector table. This chapter explains how to determine interrupt sources when using interrupts assigned to the same vector table at the same time.

1.1 Determination between INTP4 and INTSPM

Figure 1-1 shows an interrupt processing example in case of both INTP4 (Pin input edge detection 4) and INTSPM (Stack pointer overflow/underflow) are enabled.

Interrupt by INTP4 can be determined from INTFLG00 bit of INTFLG0. And interrupt by INTSPM can be determined by reading stack pointer from user software.



Caution: When both INTP4 and INTSPM are enabled, enable multiple interrupt servicing (before each interrupt request is acknowledged, the EI instruction must be issued.).

Remarks: SPOFR: SP overflow address setting register
SPUFR: SP underflow address setting register

Figure 1-1 INTP4/INTSPM Interrupt Judgement Example

1.2 Determination between INTP5 and INTCMP0

Figure 1-2 shows an interrupt processing example in case of both INTP5 (Pin input edge detection 5) and INTCMP0 (Comparator detection 0) are enabled.

Interrupt by INTP5 can be determined from INTFLG01 bit of INTFLG0. And interrupt by INTCMP0 can be determined from INTFLG06 bit of INTFLG0.

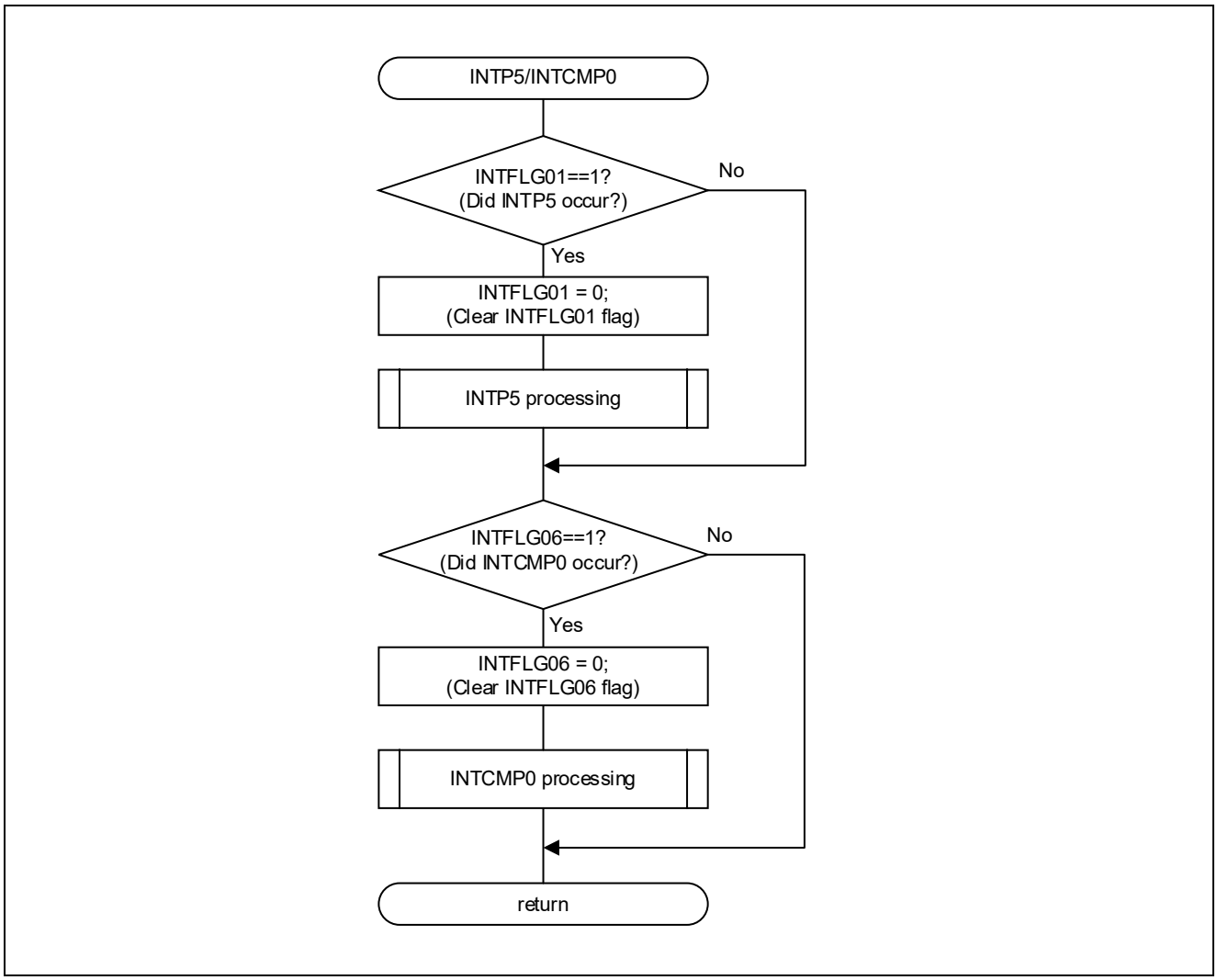
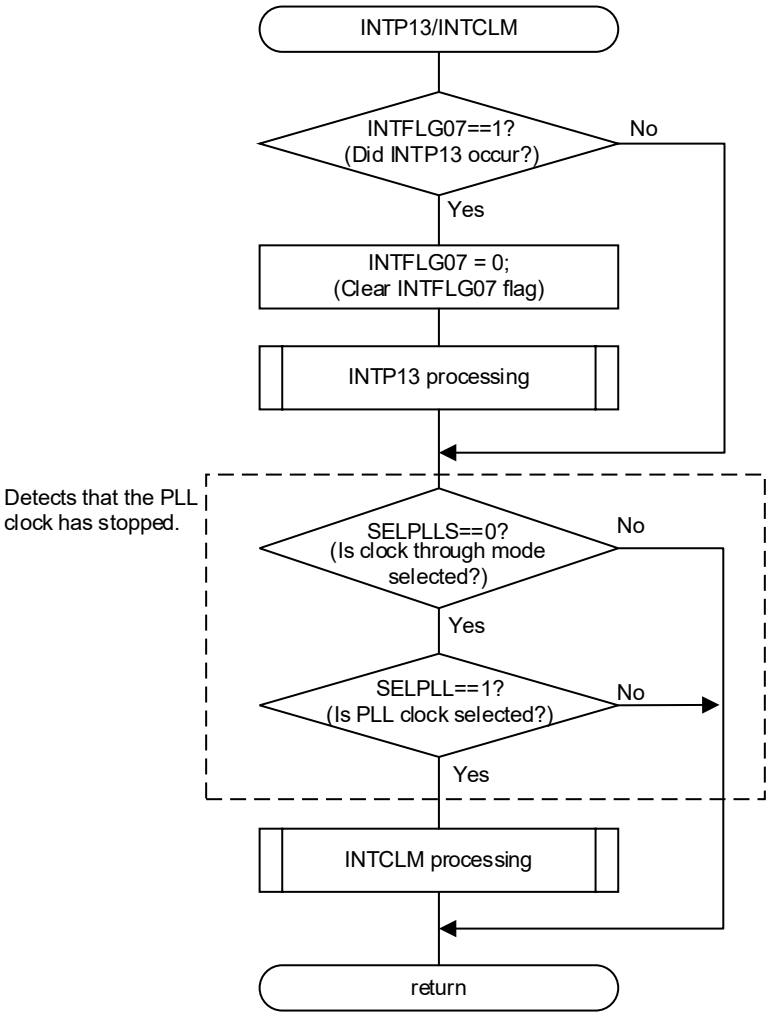


Figure 1-2 INTP5/INTCMP0 Interrupt Judgement Example

1.3 Determination between INTP13 and INTCLM

Figure 1-3 shows an interrupt processing example in case of both INTP13 (Pin input edge detection 13) and INTCLM (PLL clock stop detection) are enabled.

Interrupt by INTP13 can be determined from INTFLG07 bit of INTFLG0. And interrupt by INTCLM can be determined from SELPLLS bit of PLLSTS and SELPLL bit of PLLCTL.



Caution: Be sure to switch the main / PLL selection clock (f_{MP}) to PLL clock frequency (f_{PLL}) before enabling both INTP13 and INTCLM interrupts.

Figure 1-3 INTP13/INTCLM Interrupt Judgement Example

1.4 Determination between INTP8 and INTRTC

Figure 1-4 shows an interrupt processing example in case of both INTP8 (Pin input edge detection 8) and INTRTC (RTC pretimed signal or alarm match detection) are enabled.

Interrupt by INTP8 can be determined from INTFLG02 bit of INTFLG0. And interrupt by INTRTC can be determined from WAFG bit and RIFG bit of RTCC1.

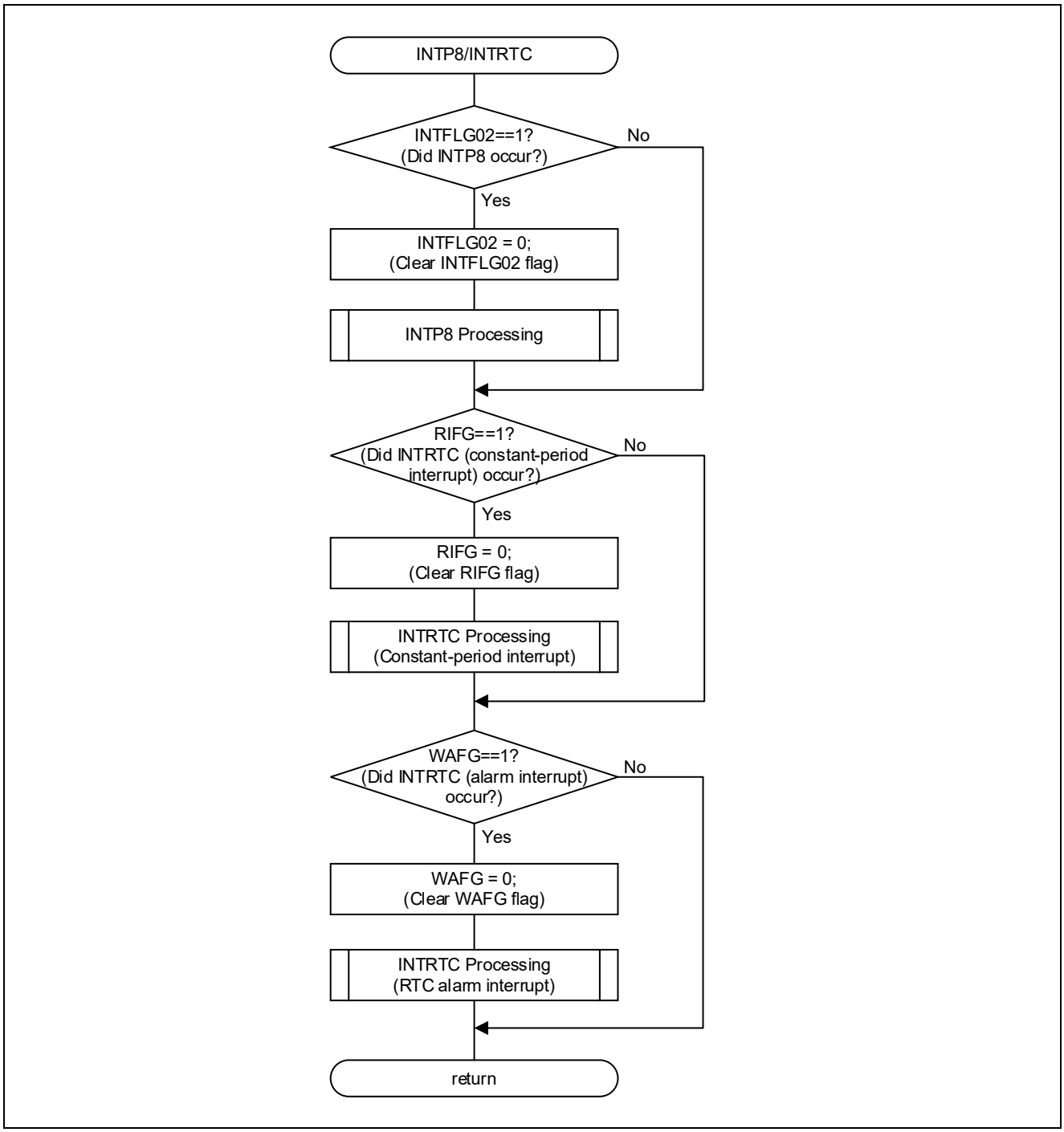


Figure 1-4 INTP8/INTRTC Interrupt Judgement Example

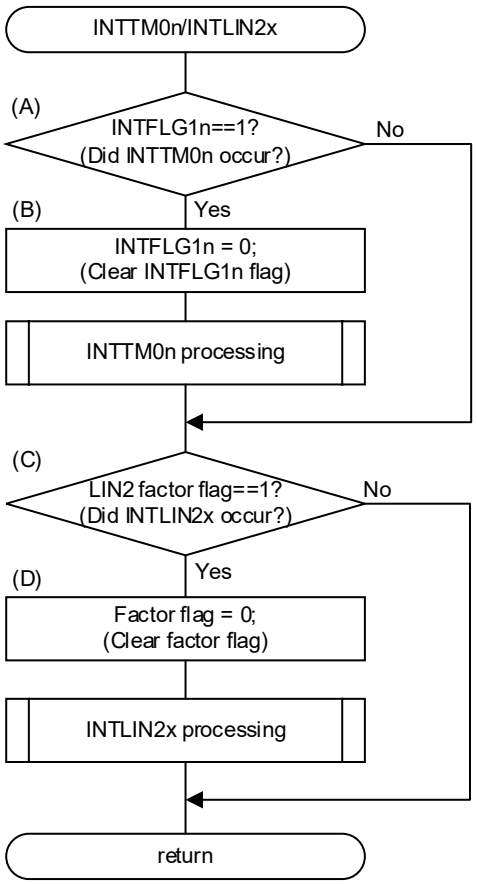
1.5 Determination between INTTM0n and INTLIN2x

Figure 1-5 shows an interrupt processing example in case of both INTTM0n (timer interrupt of TAU0 channel n) and INTLIN2x (LIN2 transmission/reception/status interrupt) are enabled.

Interrupt by INTTM0n can be determined from INTFLG1n bit of INTFLG1 (Interrupt source determination flag register 1). And interrupt by INTLIN2x can be determined from the interrupt request flag inside of the LIN2 module. On the other hand, if INTLIN2RVC is used as UART mode, it is impossible to identify both interrupt source. In that case, disable INTTM02 interrupts before using INTLIN2RVC.

Remarks: n = 1 to 3

x = TRM, RVC, STA



	INTTM01/INTLIN2TRM	INTTM02/INTLIN2RVC	INTTM03/INTLIN2STA/INTLIN2
(A), (B)	INTFLG11 flag	INTFLG12 flag	INTFLG13 flag
(C), (D) [LIN Master]	LST2.HTRC and LST2.FTC flags	LST2.FRC flag	LST2.ERR flag (or each flag in LEST2 register)
(C), (D) [LIN Slave]	LST2.FTC flag	LST2.HTRC and LST2.FRC flags	LST2.ERR flag (or each flag in LEST2 register)
(C), (D) [INTLIN2]	–	–	Flags of each factor (INTLIN2TRM, INTLIN2RVC, or INTLIN2STA)
(C), (D) [UART]	LST2.FTC flag	Cannot be used simultaneously	LST2.ERR flag (or each flag in LEST2 register)

Figure 1-5 INTTM0n/INTLIN2x Interrupt Judgement Example

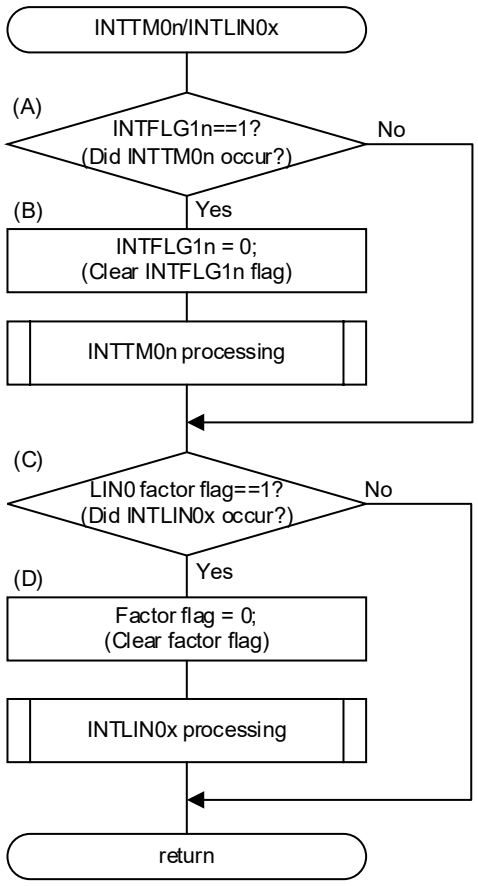
1.6 Determination between INTTM0n and INTLIN0x

Figure 1-6 shows an interrupt processing example in case of both INTTM0n (timer interrupt of TAU0 channel n) and INTLIN0x (LIN0 transmission/reception/status interrupt) are enabled.

Interrupt by INTTM0n can be determined from INTFLG1n bit of INTFLG1 (Interrupt source determination flag register 1). And interrupt by INTLIN0x can be determined from the interrupt request flag inside of the LIN0 module. On the other hand, if INTLIN0RVC is used as UART mode, it is impossible to identify both interrupt source. In that case, disable INTTM06 interrupts before using INTLIN0RVC.

Remarks: n = 5 to 7

x = TRM, RVC, STA



	INTTM05/INTLIN0TRM	INTTM06/INTLIN0RVC	INTTM07/INTLIN0STA/INTLIN0
(A), (B)	INTFLG15 flag	INTFLG16 flag	INTFLG17 flag
(C), (D) [LIN Master]	LST0.HTRC and LST0.FTC flags	LST0.FRC flag	LST0.ERR flag (or each flag in LEST0 register)
(C), (D) [LIN Slave]	LST0.FTC flag	LST0.HTRC and LST0.FRC flags	LST0.ERR flag (or each flag in LEST0 register)
(C), (D) [INTLIN2]	–	–	Flags for each factor (INTLIN0TRM, INTLIN0RVC, INTLIN0STA)
(C), (D) [UART]	LST0.FTC flag	When using INTLIN0RVC, disable INTTM06.	LST0.ERR flag (or each flag in LEST0 register)

Figure 1-6 INTTM0n/INTLIN0x Interrupt Judgement Example

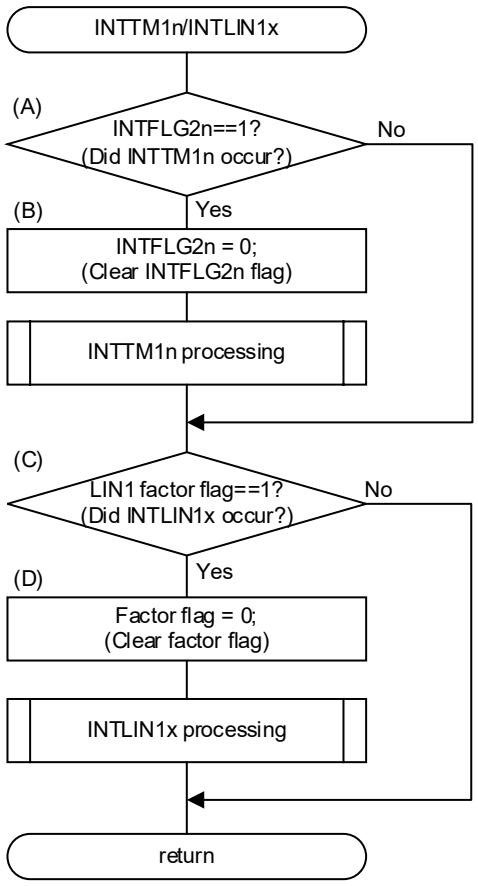
1.7 Determination between INTTM1n and INTLIN1x

Figure 1-7 shows an interrupt processing example in case of both INTTM1n (timer interrupt of TAU1 channel n) and INTLIN1x (LIN1 transmission/reception/status interrupt) are enabled.

Interrupt by INTTM1n can be determined from INTFLG2n bit of INTFLG2 (Interrupt source determination flag register 2). And interrupt by INTLIN1x can be determined from the interrupt request flag inside of the LIN1 module. On the other hand, if INTLIN1RVC is used as UART mode, it is impossible to identify both interrupt source. In that case, disable INTTM12 interrupts before using INTLIN1RVC.

Remarks: n = 1 to 3

x = TRM, RVC, STA



	INTTM11/INTLIN1TRM	INTTM12/INTLIN1RVC	INTTM13/INTLIN1STA/INTLIN1
(A), (B)	INTFLG21 flag	INTFLG22 flag	INTFLG23 flag
(C), (D) [LIN Master]	LST1.HTRC and LST1.FTC flags	LST1.FRC flag	LST1.ERR flag (or each flag in LEST1 register)
(C), (D) [LIN Slave]	LST1.FTC flag	LST1.HTRC and LST1.FRC flags	LST1.ERR flag (or each flag in LEST1 register)
(C), (D) [INTLIN2]	–	–	Flags for each factor (INTLIN1TRM, INTLIN1RVC, INTLIN1STA)
(C), (D) [UART]	LST1.FTC flag	When using INTLIN1RVC, disable INTTM12.	LST1.ERR flag (or each flag in LEST1 register)

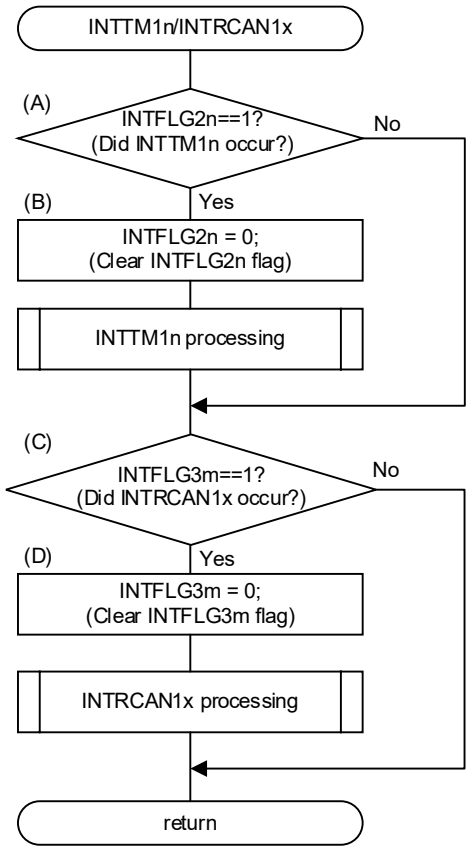
Figure 1-7 INTTM1n/INTLIN1x Interrupt Judgement Example

1.8 Determination between INTTM1n and INTRCAN1x

Figure 1-8 shows an interrupt processing example in case of both INTTM1n (timer interrupt of TAU1 channel n) and INTRCAN1x (CAN1 reception/error detection/FIFO reception/transmission interrupt) are enabled.

Interrupt by INTTM1n can be determined from INTFLG2n bit of INTFLG2 (Interrupt source determination flag register 2). And interrupt by INTRCAN1x can be determined from INTFLG3m bit of INTFLG3 (Interrupt source determination flag register 3). For CAN1 interrupt request flags, clear (0) all corresponding flags within the INTRCAN1x interrupt handler.

Remarks: n = 4 to 7, m = 2 to 5
x = TRM, RVC, STA



	INTTM14/ INTRCAN1GRVC	INTTM15/ INTRCAN1GERR	INTTM16/ INTRCAN1CFR	INTTM17 /INTRCAN1TRM
(A), (B)	INTFLG24 flag	INTFLG25 flag	INTFLG26 flag	INTFLG27 flag
(C), (D)	INTFLG32 flag	INTFLG33 flag	INTFLG34 flag	INTFLG35 flag
(C), (D) Interrupt request flag	RMNS[15:0] bit of RMND1 registre	DEF, MES, THLES, and CMPOF bits of GERFL1 register	CFRXIF bit of CFSTS1 register	TMTRF[1:0] bit of TMSTSy1 register CFTXIF bit of CFSTS1 register THLIF bit of THLSTS1 register

Figure 1-8 INTTM1n/INTRCAN1x Interrupt Judgement Example

2. Notes on Interrupt Source Determination

2.1 Notes when Clearing bit of INTFLGn Register

If a new interrupt of the same source occurs during interrupt processing, the interrupt request (IF bit) may become "1" even if the INTFLGnm bit of INTFLGn register is cleared. In this case, the interrupt is generated, but its interrupt factor INTFLGnm bit is “0” (no interrupt request), so its interrupt is terminated without processing.

The above case will be explained using the INTP4 / INTSPM interrupt as an example. After the INTFLG00 bit is determined to be “1” (INTP4 request is occurred) in the interrupt processing shown in **Figure 2-1** and if a new effective edge is input to the INTP4 pin before the INTFLG00 bit is cleared, the PIF4 bit of the IF0L register is set to “1”. After that, the INTFLG00 bit is cleared and the INTP4 interrupt processing ends. And the INTP4 / INTSPM interrupt occurs again as the PIF4 bit is “1”. However, at this time, since the INTFLG00 bit has already been cleared to “0”, the next processing is executed without executing INTP4 Processing.

When using multiple interrupts with them enabled, consider the above notes when designing.

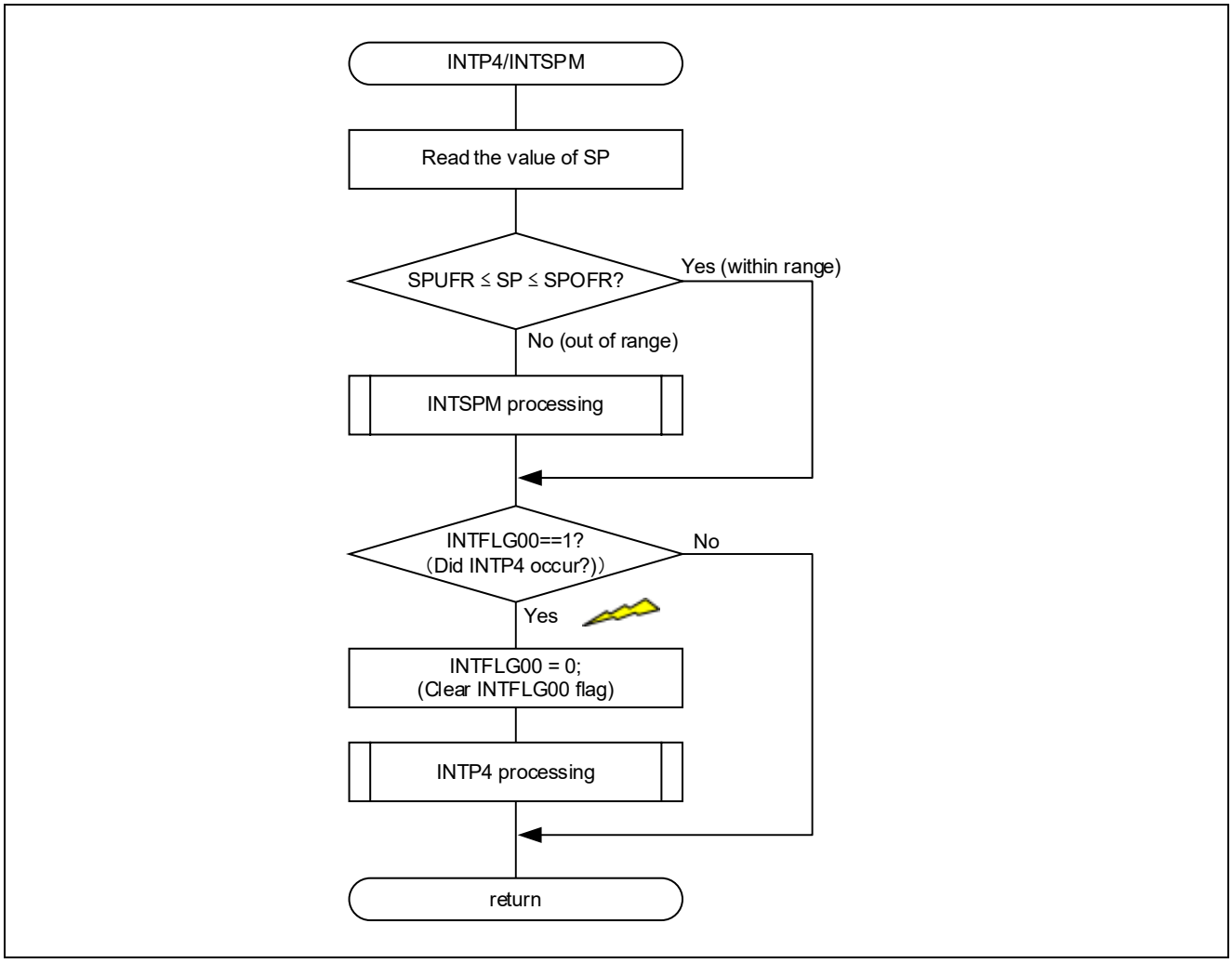


Figure 2-1 INTP4/INTSPM Interrupt Judgement Example (INTP4 occurs continuously)

2.2 Notes when Using INTSPM and INTCLM

The CPU stack pointer monitor function or Clock monitor function are a safety function, it is recommended to set those interrupt priority level high.

2.3 Notes when Using RS-CANFD lite Interrupts

All interrupt request flags for RS-CANFD lite must be cleared within the interrupt handler. As shown in **Figure 2-2**, clear the interrupt request flags in software and confirm that all interrupt request flags for enabled interrupt sources have been cleared before terminating interrupt processing.

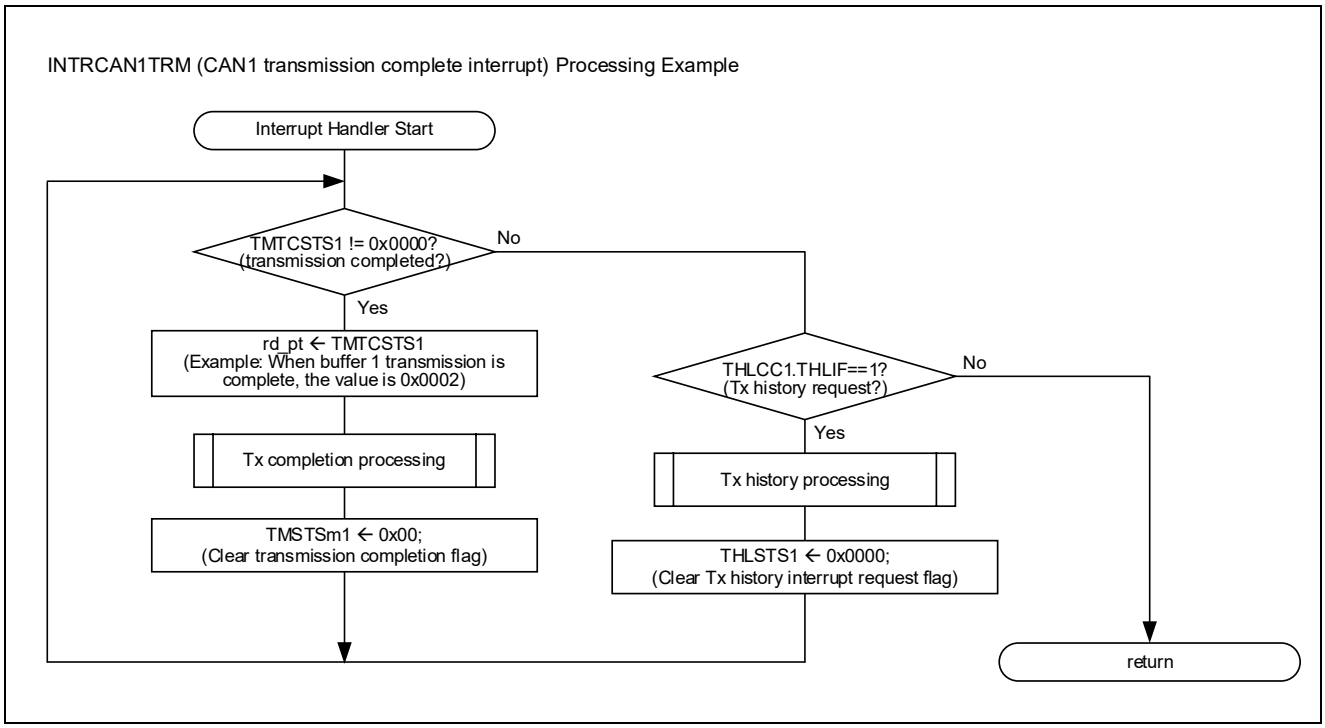


Figure 2-2 CAN Interrupt Handler Example (INTRCAN1TRM)

3. References

Documents referenced in this application note are shown below. When referring to these documents, make sure to obtain the latest version of each document from Renesas Electronics website.

- RL78/ F22, F25 User's Manual: Hardware [R01UH1061EJ]

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2025. 9. 30	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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