

RL78/G1G

Timer RD in Complementary PWM mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Introduction

This application note explains how to output complementary PWM waveforms and output inverted waveforms every half period using RL78/G1G timer RD in complementary PWM mode. This application note also describes how to forcibly cut off PWM output using the PWM option unit.

Target Device

RL78/G1G

When using this application note for other microcomputers, please change it according to the corresponding specification and evaluate thoroughly before use.

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RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

1. Specifications

This application note explains how to output complementary PWM waveforms and output inverted waveforms every half period using RL78/G1G timer RD in complementary PWM mode. This application note also describes how to forcibly cut off PWM output with the PWM option unit.

Timer RD outputs a total of seven 350μs PWM waveforms per period: three normal-phase (three-phase, sawtooth wave modulation, and no dead time), three counter-phase, and one inverted-phase every half period. Buffer operations are used to switch PWM waveforms each fixed period. The three normal-phase and counter-phase waveforms output the same signal, respectively. The PWM option unit uses a programmable gain amp (PGA) and comparator to forcibly cut off PWM output. The comparator's internal reference voltage described in this application note is set to approximately 40% ($(PVDD/256) \times 102$) of the voltage of the VDD pin (PVDD) in the MCU, and PGA gain is set to x8. The comparator compares the PGA output voltage and its internal reference voltage. When PGA output exceeds the internal reference voltage, the PWM waveform is forcibly cut off and the PWM output pin goes to Hi-Z state. When PGA output is lower than the internal reference voltage, the PWM output pin outputs a PWM waveform.

Table 1.1 Peripheral Functions and Corresponding Usage as implemented in this application. Figure 1.1, Figure 1.2, Figure 1.3, and Figure 1.4 show the Operation Outline, Internal Comparator Output → Timer RD Forced Cutoff Function Explanation, Complementary PWM Output Waveforms, and PWM Option Unit Forced Cutoff Timing

Table 1.1 Peripheral Functions and Corresponding Usage

Peripheral Function	Usage
Timer RD (timer RD0, Timer RD1)	● PWM waveform output
PGA	Comparator positive-side input pins Amplify overcurrent detection signal x 8 and input to comparator
Comparator 0	Overcurrent detection function Because overcurrent detection is not used, internal reference voltage is set to 0 so that waveform is not forcibly cut off.
Comparator 1	Overcurrent detection function When PGA output voltage exceeds Comparator 1's internal reference voltage ($(PVDD/266) \times 102$), PWM output is forcibly cut off and the PWM output pin goes to Hi-Z mode. When PGA output voltage is lower than internal reference voltage ($(PVDD/266) \times 102$), the pin starts to PWM output.

RL78/G1G Timer RD in Complementary PWM Mode and
Using PWM Option Unit to Forcibly Cut Off PWM Output

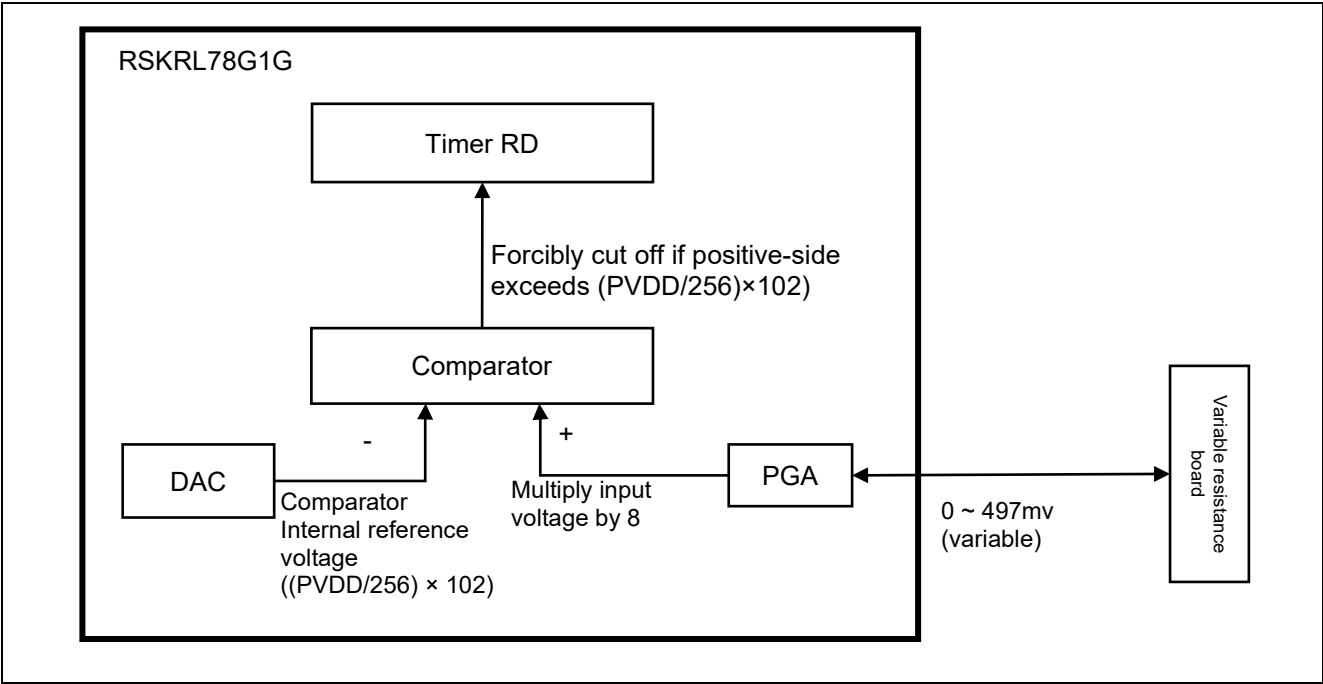


Figure 1.1 Operation Outline

RL78/G1G offers two key types of forced shut off functions as described below; this application note uses Method 1.

Internal comparator usage example		Forced cutoff path	Response speed	Pin mode at cutoff
Method 1 (used in this app note)	Does not use ELC	CMPnHZO CMPnHZO → MPnHZO control	Immediate	Hi-z only
Method 2	Uses ELC	CMPnELC event → Output cutoff control	Time is generated through ELC	Can be set to Hi-z or H/L output

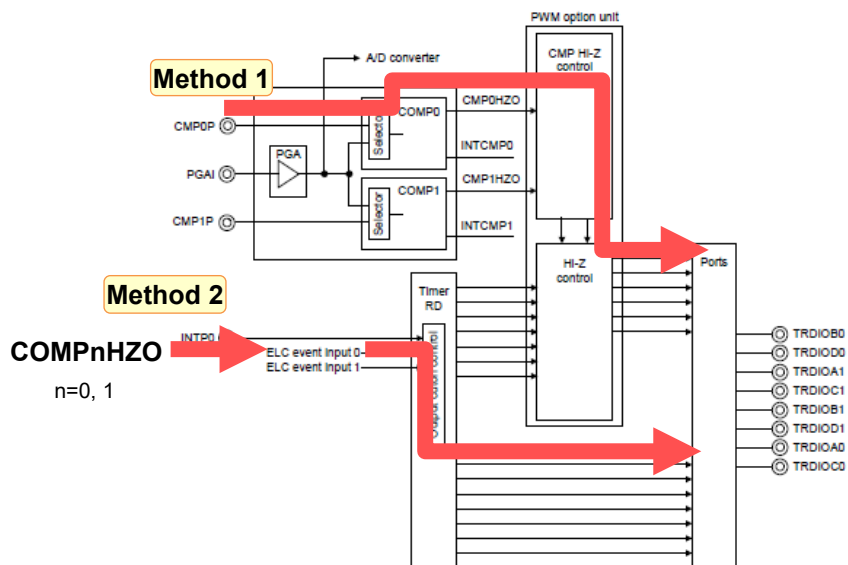


Figure 1.2 Internal Comparator Output → Timer RD Forced Cutoff Function Explanation

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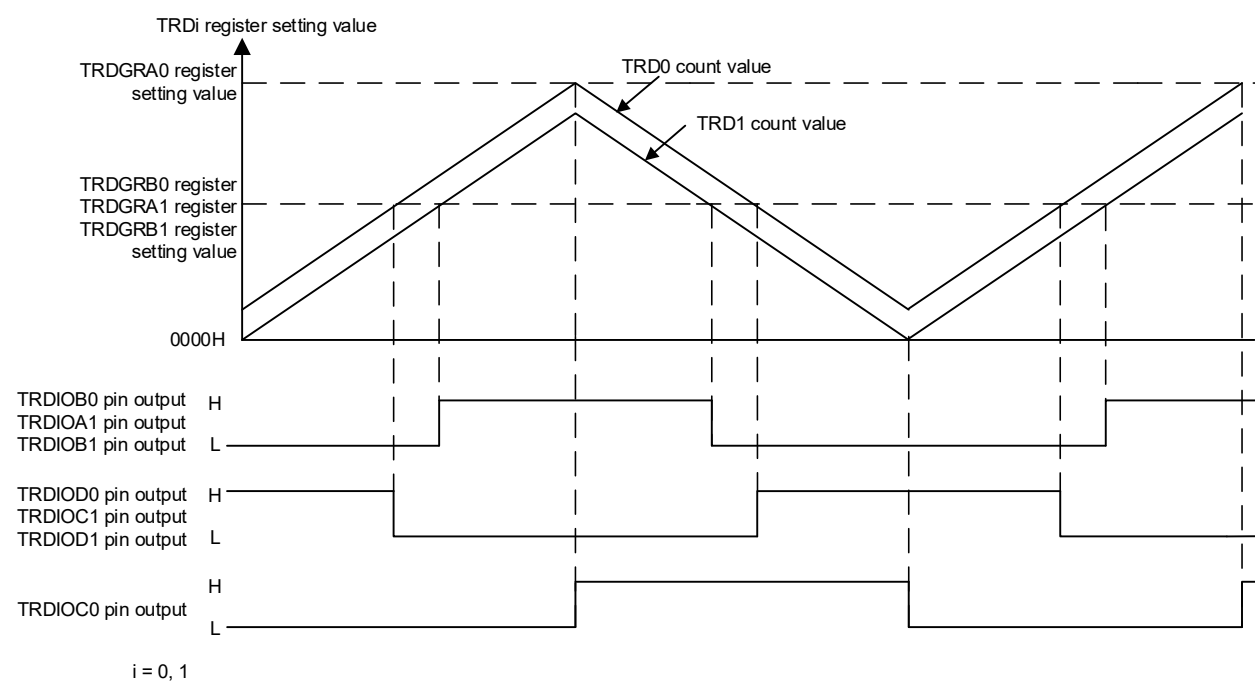


Figure 1.3 Complementary PWM Output Waveforms

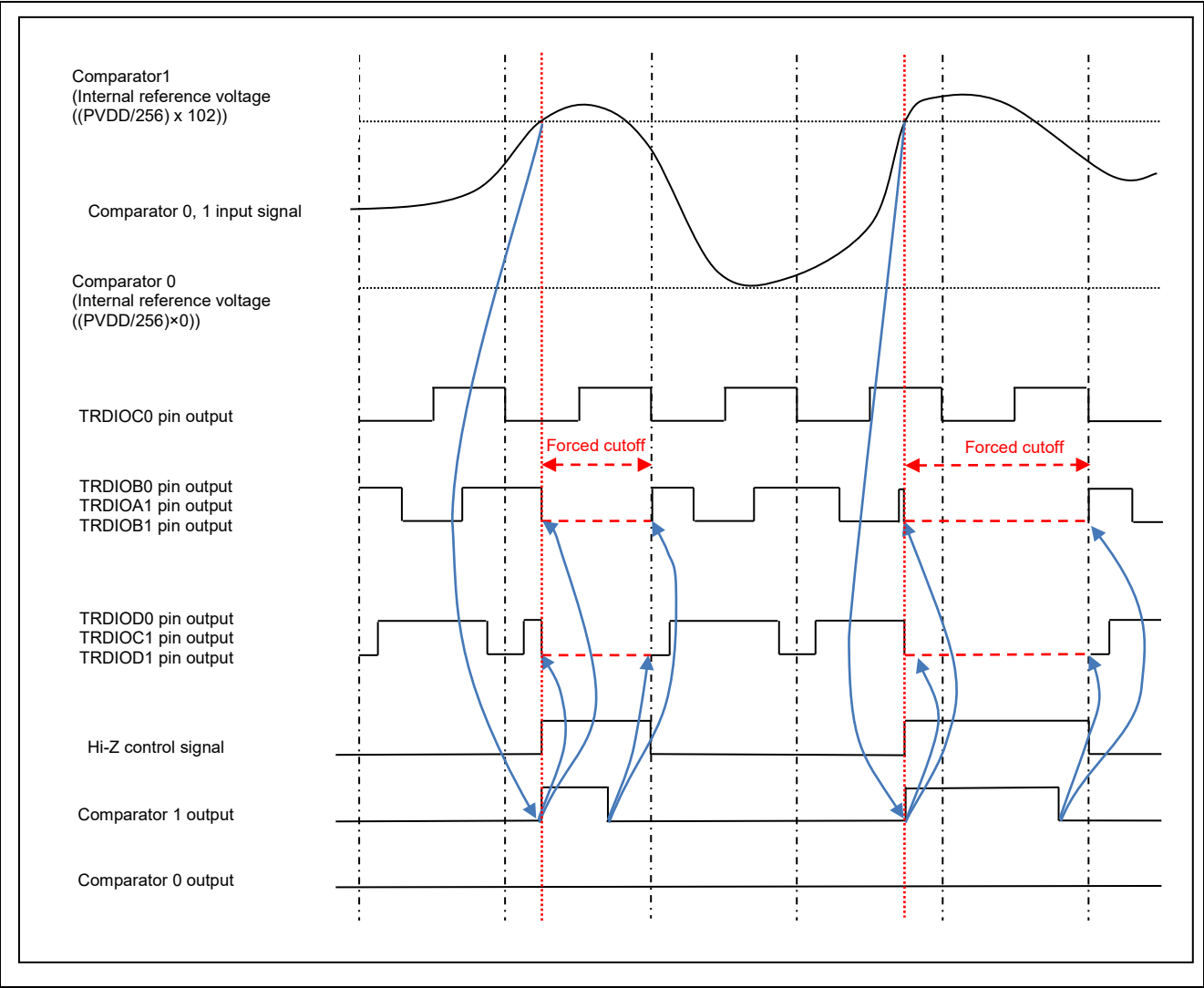


Figure 1.4 PWM Option Unit Forced Cutoff Timing

1.1 Conditions for Confirming Operations

The sample codes used in this application note were confirmed under the following conditions.

Table 2.1 Conditions for Confirming Operations

Item	Description
MCU	RL78/G1G (R5F11EFAA)
Operating frequency	● High-speed on-chip oscillator clock (f_{HOCO}): 16MHz (reference) ● CPU/peripheral hardware clock (f_{CLK}): 16MHz
Operating voltage	5.0V (operating range 2.9V to 5.5V) LVD operations (V_{LVI}): reset mode (rising edge TYP. 2.81V / falling edge TYP. 2.75V)
Integrated development environment (CS+)	Made by Renesas Electronics Corp. CS+ V3.00.00
C compiler (CS+)	Made by Renesas Electronics Corp. CA78K0R V1.71
Integrated development environment (e2studio)	Made by Renesas Electronics Corp. e2studio V3.1.2.10
C compiler (e2studio)	Made by Renesas Electronics Corp. KPIT GNURL78-ELF Toolchain V14.0.3
Board	RL78/G1G CPU board (RSKRL78G1G) ● Due to shipping conditions, operations were confirmed after removing R121.

2. Related Application Notes

Application notes related to this document are shown below. Please refer to these as needed.

RL78/G13 Initialization (R01AN0451J) Application Note

3. Hardware Explanation

3.1 Hardware Structure Example

Figure 3.1 shows the hardware used in this application note.

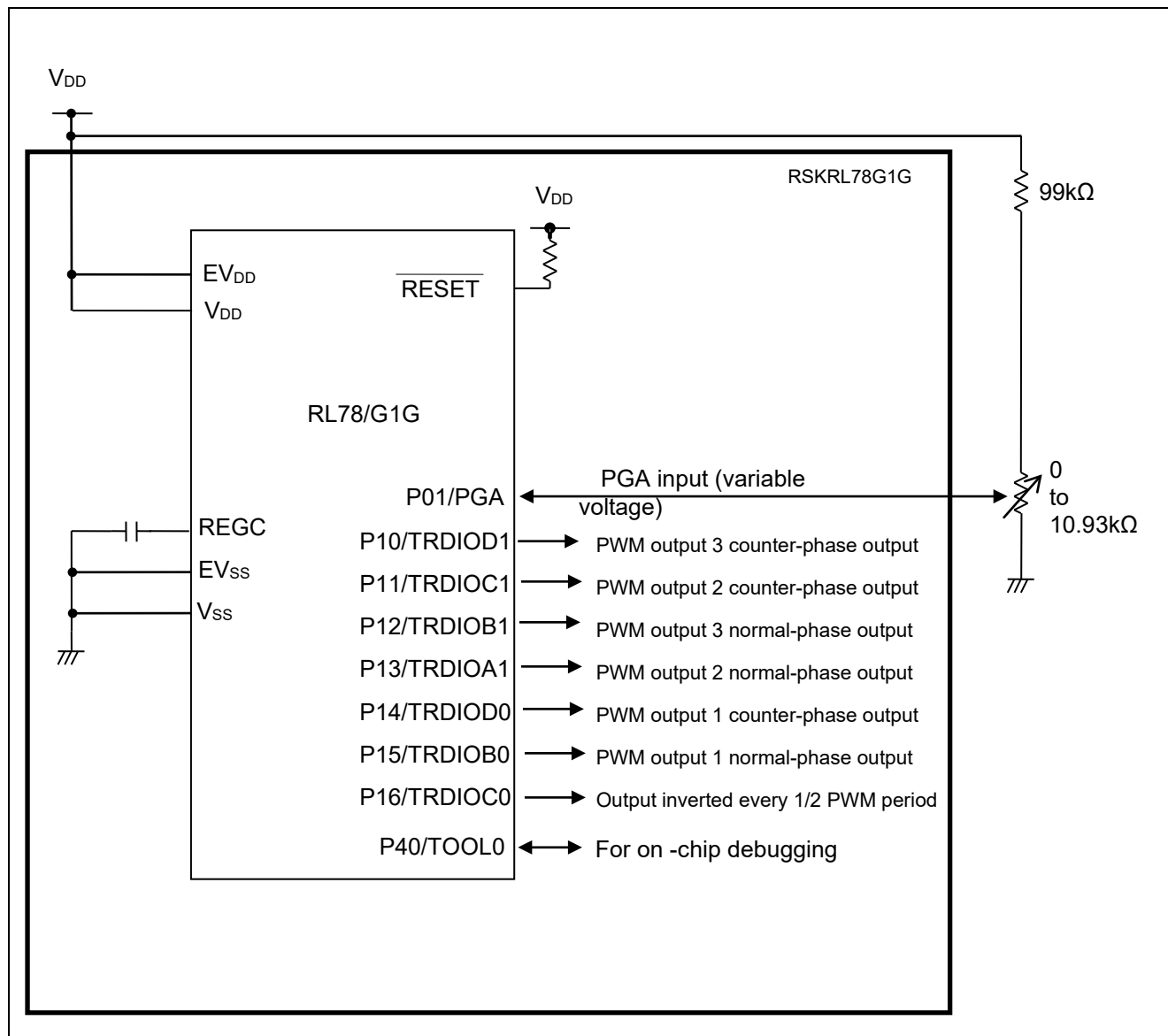


Figure 3.1 Hardware Configuration Example

Note: 1. This simplified circuit diagram was created to show an overview of connections only.

When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

(Connect each input-only port to V_{DD} or V_{SS} through a resistor.)

2. If a pin name starts with EV_{SS} , connect the pin to V_{SS} , if it starts with EV_{DD} , connect it to V_{DD} .
3. Make V_{DD} higher than the RESET release voltage (V_{LVI}) set in LVD.

3.2 Pin List

Table 3.1 provides a list of the pins used in this application note and their functions.

Table 3.1 List of Pins and Functions

Pin Name	Input/Output	Function
P01/PGAI	Input	PGA input (variable voltage)
P15/TRDIOB0	Output	PWM output 1 normal-phase output
P14/TRDIOD0	Output	PWM output 1 counter-phase output
P13/TRDIOA1	Output	PWM output 2 normal-phase output
P11/TRDIOC1	Output	PWM output 2 counter-phase output
P12/TRDIOB1	Output	PWM output 3 normal-phase output
P10/TRDIOD1	Output	PWM output 3 counter-phase output
P16/TRDIOC0	Output	Output inverted every half PWM period

4. Software Explanation

4.1 Operation Outline

This application note explains how to output complementary PWM waveforms and output inverted waveforms every half period using RL78/G1G timer RD in complementary PWM mode. This application note also describes how to forcibly cut off PWM output using the PWM option unit.

Timer RD outputs a total of seven 350µs PWM waveforms per period: three normal-phase (three-phase, sawtooth wave modulation, and no dead time), three counter-phase, and one inverted-phase every half period. Buffer operations are used to switch PWM waveforms each fixed period. The three normal-phase and counter-phase waveforms output the same signal, respectively. The PWM option unit uses a programmable gain amp (PGA) and comparator to forcibly cut off PWM output. The comparator's internal reference voltage described in this application note is set to approximately 40% ($(PVDD/256) \times 102$) of the voltage of the VDD pin (PVDD) in the MCU, and PGA gain is set to x8. The comparator compares the PGA output voltage and its internal reference voltage. When PGA output exceeds the internal reference voltage, the PWM waveform is forcibly cut off and the PWM output pin goes to Hi-Z state. When PGA output is lower than the internal reference voltage, the PWM output pin outputs a PWM waveform.

Details pertaining to the above specifications are listed below, (1) to (10).

(1) Timer RD initialization

<Setting conditions>

- Select f_{CLK} (16MHz) as count source.
- TRD0 register: continue count even after a compare match TRDGRA0 register.
- TRD1 register: continue count even after a compare match TRDGRA1 register.
- TRDGRD0 register: use as buffer register of TRDGRB0 register.
- TRDGRC1 register: use as buffer register of TRDGRA1 register.
- TRDGRD1 register: use as buffer register of TRDGRB1 register.
- When TRD1 register underflows, transfer data from buffer register to general register
- Enable output of the following pins: TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, and TRDIOD1
- Set output level of the following pins to active level low and initial output level to inactive level high: TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, and TRDIOD1
- Pulse output forced cutoff input function is not used. (Forced cutoff is performed by PWM option unit function.)
- Enable TRD0 register and TRDGRA0 register compare match interrupt

(2) Comparator and PGA initialization

<Setting conditions>

- Select comparator 0, comparator 1 and PGA.
- Set PWM option unit to overcurrent/induced current detection mode.
- Set comparator 0 as follows:
 - Positive-side input setting: PGA output
 - To inhibit detection of induced current, set comparator internal reference voltage to 0%.
- Set comparator 1 as follows:
 - Positive-side input setting: PGA output
 - To detect overcurrent, set comparator internal reference voltage to 80%
- Set PGA 1 as follows:
 - Select x8 as the gain.

(3) Main processing initialization

<Setting conditions>

- Set PER1 register PWMOPEN bit to “1” (PWM open unit input clock supply).
- Set OPMR register HDM bit to “1” (overcurrent/induced current detection mode).

(4) Comparator 0 operation start

- Set COMPMDR register C0ENB bit to “1” (comparator 0 operation enabled).
- Select comparator 0 operation stabilization wait time (3 μ s).
- Set COMPOCR register C0OE bit to “1” (comparator 0 operation enabled).
- Set INCMP0 register CMPIF0 bit to “0” (interrupt request signal not generated).
- Set IF2L register CMPMK0 bit to “0” (interrupt request servicing enabled).

(5) Comparator 1 operation start

- Set COMPMDR register C1ENB bit to “1” (comparator 1 operation enabled).
- Select comparator 1 operation stabilization wait time (3 μ s).
- Set COMPOCR register C0OE bit to “1” (comparator 1 operation enabled).
- Set INCMP1 register CMPIF1 bit to “0” (interrupt request signal not generated).
- Set IF2H register CMPMK1 bit to “0” (interrupt request servicing enabled).

(6) PGA operation start

- Set PGACTL register PGAEN bit to “1” (PGA operation enabled).

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(7) Timer RD0, RD1 operations start

- Set TRDSR0 register to "00H" (clear overflow flag, input capture/compare match flag D to A)
- Set INTTRD0 register to TRDIF0 bit to "0" (interrupt request signal not generated).
- Set IF2H register TRDMK0 bit to "0" (interrupt servicing enabled).
- Set TRDSTR register TSTART1 bit to "1" (TRD1 count start) and TSTART0 bit to "1" (TRD0 count start).

(8) When PWM output continues ($\text{PWM output} \leq (\text{PVDD}/256) \times 102$)

- Set TRDSR0 register to "1" (when TRD0 and TRDGRA0 values match).
- Increment variable g_int_cnt (interrupt counter).
- Set the following when variable g_int_cnt (interrupt counter) is higher than 10:
 - Set variable g_int_cnt (interrupt counter) to "0".
 - Increment variable g_output_chg_mode (waveform switch mode).
 - When variable g_output_chg_mode (waveform switch mode) is higher than "5", set variable g_output_chg_mode to "0".
 - Waveform switch mode settings
 - ◆ When variable g_output_chg_mode (waveform switch mode) is "0" (PWM waveform 1→ PWM waveform 2), set the buffer registers of TRDGRD0, TRDGRC1, and TRDGRD1 to the value for active level 100μs.
 - ◆ When variable g_output_chg_mode (waveform switch mode) is "1" (PWM waveform 2→ PWM waveform 3), set the buffer registers of TRDGRD0, TRDGRC1, and TRDGRD1 to the value for active level 350μs.
 - ◆ When variable g_output_chg_mode (waveform switch mode) is "2" (PWM waveform 3→ PWM waveform 2), set the buffer registers of TRDGRD0, TRDGRC1, and TRDGRD1 to the value for active level 100μs.
 - ◆ When variable g_output_chg_mode (waveform switch mode) is "3" (PWM waveform 2→ PWM waveform 4), set the buffer registers of TRDGRD0, TRDGRC1, and TRDGRD1 to the value for active level 0μs.
 - ◆ When variable g_output_chg_mode (waveform switch mode) is "4" (PWM waveform 4→ PWM waveform 1), set the buffer registers of TRDGRD0, TRDGRC1, and TRDGRD1 to the value for active level 250μs.
 - ◆ In all other cases, set variable g_output_chg_mode (waveform switch mode) to "4" and set the buffer registers of TRDGRD0, TRDGRC1, and TRDGRD1 to the value for active level 250μs.

(9) When PWM is forcibly cut off ($\text{PGA output} > (\text{PVDD}/256) \times 102$)

- The rising edge of comparator 1 is detected, and pins TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, and TRDIOD1 go to Hi-Z output state. If PGA output is lower than the internal reference voltage of comparator 1 ($\text{PVDD}/256) \times 102$, the falling edge of comparator 1 is detected, Hi-Z output state is released, and PWM output starts.

(10) After that, steps (8) and (9) are repeated.

4.1.1 Description of Output Waveform

PWM waveform type output from each pin, as well as active/inactive level and dead time, are calculated by the following expression.

$$\begin{aligned}\text{PWM period: } 350\mu\text{s} &= 1/16\text{MHz} \times (\text{TRDGRA0} + 2 - \text{TRD0}) \times 2 \\ &= 62.5\text{ns} \times (3200 - 400) \times 2\end{aligned}$$

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(1) PWM waveform 1

Normal-phase output: High inactive level period (50 μ s) $\rightarrow$ Low active level period (250 μ s) $\rightarrow$ High inactive level

level period (50 μ s)

Counter-phase output: Low active level period (25 μ s) $\rightarrow$ Dead time (25 μ s) $\rightarrow$ High inactive level period (250 μ s)

$\rightarrow$ Dead time (25 μ s) $\rightarrow$ Low active level period (25 μ s)

The formula below shows how to calculate the low active level period/high inactive level period and dead time when PWM waveform 1 is output.

PWM waveform 1 normal-phase output: Pins TRDIOB0, TRDIOA1, TRDIOB1

$$\begin{aligned}\text{Low active level period: } 250 \mu\text{s} &= 1/16 \text{ MHz} \times (\text{TRDGRA0} - n - \text{TRD0} + 1) \times 2 \\ &= 62.5 \text{ ns} \times (3198 - 799 - 400 + 1) \times 2\end{aligned}$$

$$\begin{aligned}\text{High inactive level period: } 50 \mu\text{s} &= 1/16 \text{ MHz} \times (n + 1) \\ &= 62.5 \text{ ns} \times (799 + 1)\end{aligned}$$

PWM waveform 1 counter-phase output: Pins TRDIOD0, TRDIOC1, TRDIOD1

$$\begin{aligned}\text{Low active level period: } 25 \mu\text{s} &= 1/16 \text{ MHz} \times (n + 1 - \text{TRD0}) \\ &= 62.5 \text{ ns} \times (799 + 1 - 400)\end{aligned}$$

$$\begin{aligned}\text{High inactive level period: } 250 \mu\text{s} &= 1/16 \text{ MHz} \times (\text{TRDGRA0} - n - \text{TRD0} + 1) \times 2 \\ &= 62.5 \text{ ns} \times (3198 - 799 - 400 + 1) \times 2\end{aligned}$$

$$\begin{aligned}\text{Dead time (High): } 25 \mu\text{s} &= 1/16 \text{ MHz} \times \text{TRD0} \\ &= 62.5 \text{ ns} \times 400\end{aligned}$$

“n” is TRDGRB0 register setting value (PWM output 1), TRDGRA1 register setting value (PWM output 2), and TRDGRB1 register setting value (PWM output 3). In this sample code, the same signal is output.

Figure 4.1 shows PWM Waveform 1.

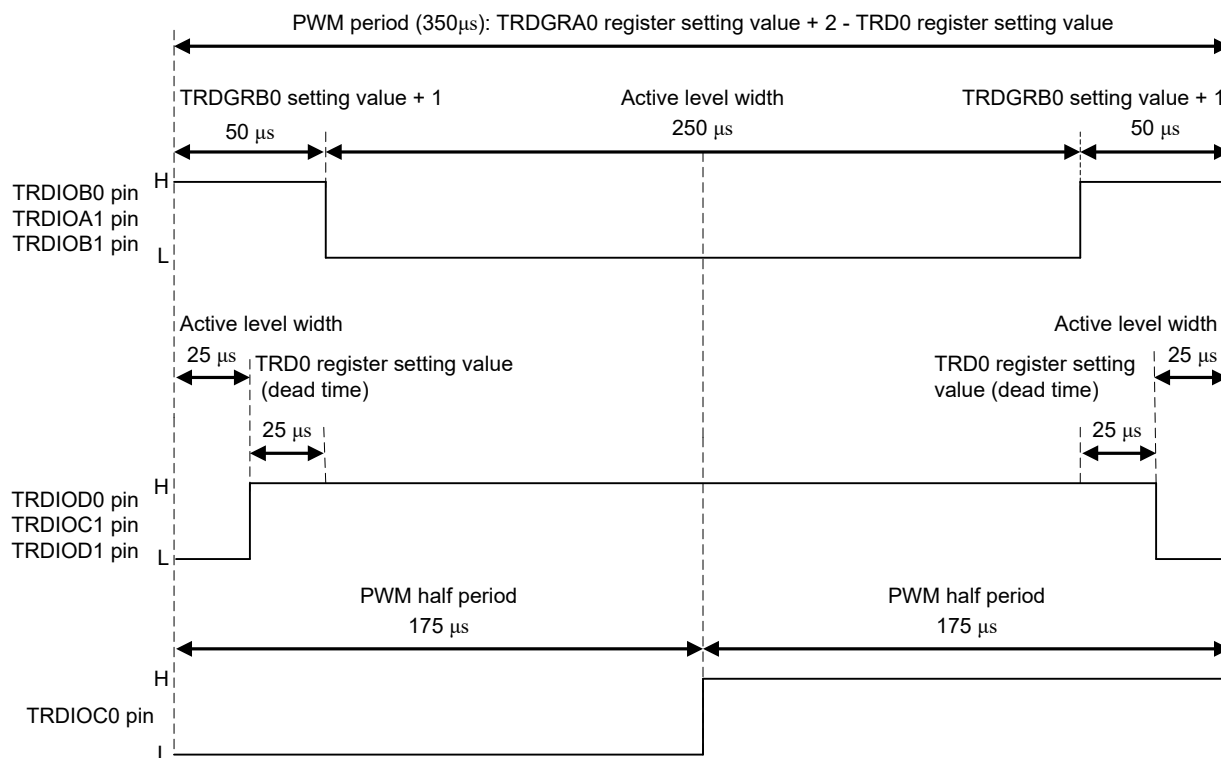


Figure 4.1 PWM Waveform 1

PWM waveform 2

Normal-phase output: High inactive level period (125 μ s) $\rightarrow$ Low active level period (100 μ s) $\rightarrow$ High inactive level period (125 μ s)

level period (125 μ s)

Counter-phase output: Low active level period (100 μ s) $\rightarrow$ Dead time (25 μ s) $\rightarrow$ High inactive level period (100 μ s) $\rightarrow$ Dead time (25 μ s) $\rightarrow$ Low active level period (100 μ s)

The formula below shows how to calculate the low active level period/high inactive level period and dead time when

PWM waveform 2 is output.

PWM waveform 2 normal-phase output: Pins TRDIOB0, TRDIOA1, TRDIOB1

$$\begin{aligned} \text{Low active level period: } 100 \mu\text{s} &= 1/16 \text{ MHz} \times (\text{TRDGRA0} - n - \text{TRD0} + 1) \times 2 \\ &= 62.5 \text{ ns} \times (3198 - 1999 - 400 + 1) \times 2 \end{aligned}$$

$$\begin{aligned} \text{High inactive level period: } 125 \mu\text{s} &= 1/16 \text{ MHz} \times (n + 1) \\ &= 62.5 \text{ ns} \times (1999 + 1) \end{aligned}$$

PWM waveform 2 counter-phase output: Pins TRDIOD0, TRDIOC1, TRDIOD1

$$\begin{aligned} \text{Low active level period: } 100 \mu\text{s} &= 1/16 \text{ MHz} \times (n + 1 - \text{TRD0}) \\ &= 62.5 \text{ ns} \times (1999 + 1 - 400) \end{aligned}$$

$$\begin{aligned} \text{High inactive level period: } 100 \mu\text{s} &= 1/16 \text{ MHz} \times (\text{TRDGRA0} - n - \text{TRD0} + 1) \times 2 \\ &= 62.5 \text{ ns} \times (3198 - 1999 - 400 + 1) \times 2 \end{aligned}$$

$$\begin{aligned} \text{Dead time (H): } 25 \mu\text{s} &= 1/16 \text{ MHz} \times \text{TRD0} \\ &= 62.5 \text{ ns} \times 400 \end{aligned}$$

“n” is TRDGRB0 register setting value (PWM output 1), TRDGRA1 register setting value (PWM output 2), and TRDGRB1 register setting value (PWM output 3). In this sample code, the same signal is output.

Figure 4.2 shows PWM Waveform 2.

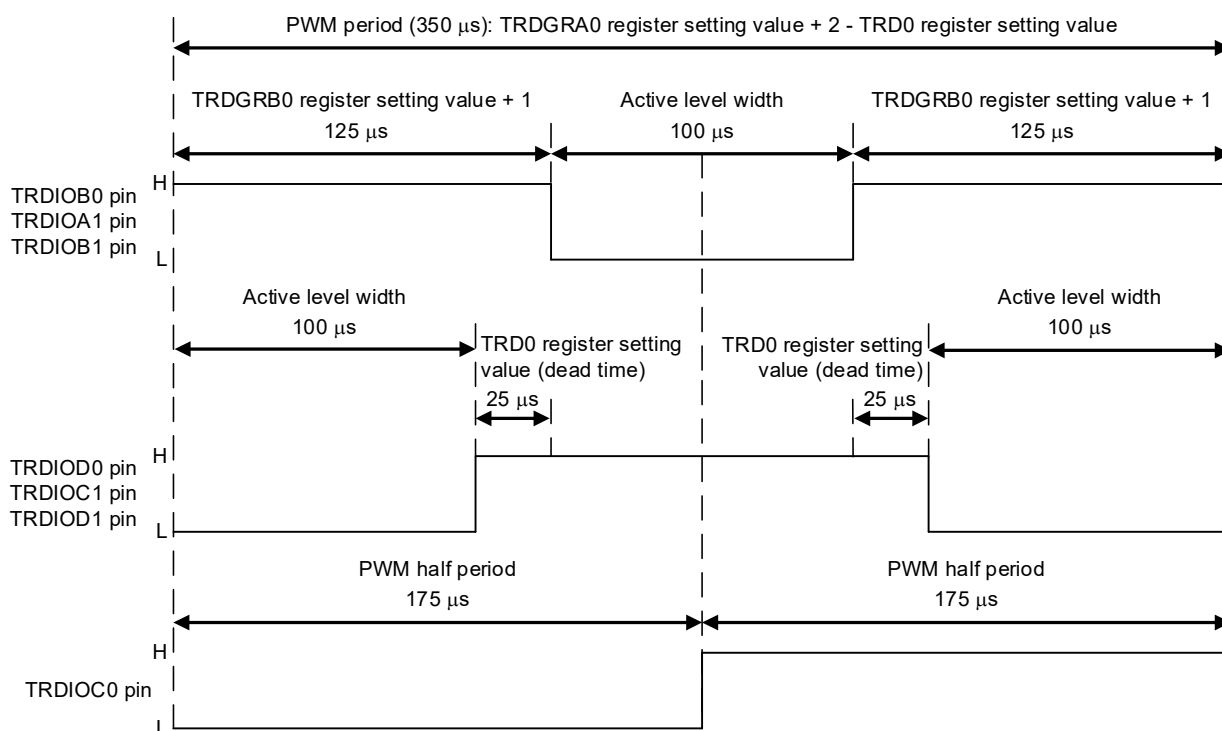


Figure 4.2 PWM Waveform 2

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(2) PWM waveform 3

Normal-phase output: Low active level period (350 μ s)

Counter-phase output: High inactive level period (350 μ s)

After setting the buffer registers (registers TRDGRD0, TRDGRC1, and TRDGRD1) to 0000H, if the TRD0 and TRDGRA0 registers are compare matched, the levels below are output.

PWM waveform 3 normal-phase output: Pins TRDIOB0, TRDIOA1, TRDIOB1

Low active level period: 350 μ s

PWM waveform 3 counter-phase output: Pins TRDIOD0, TRDIOC1, TRDIOD1

High inactive level period: 350 μ s

In this sample code, the same signal is output.

Figure 4.3 shows PWM waveform 3.

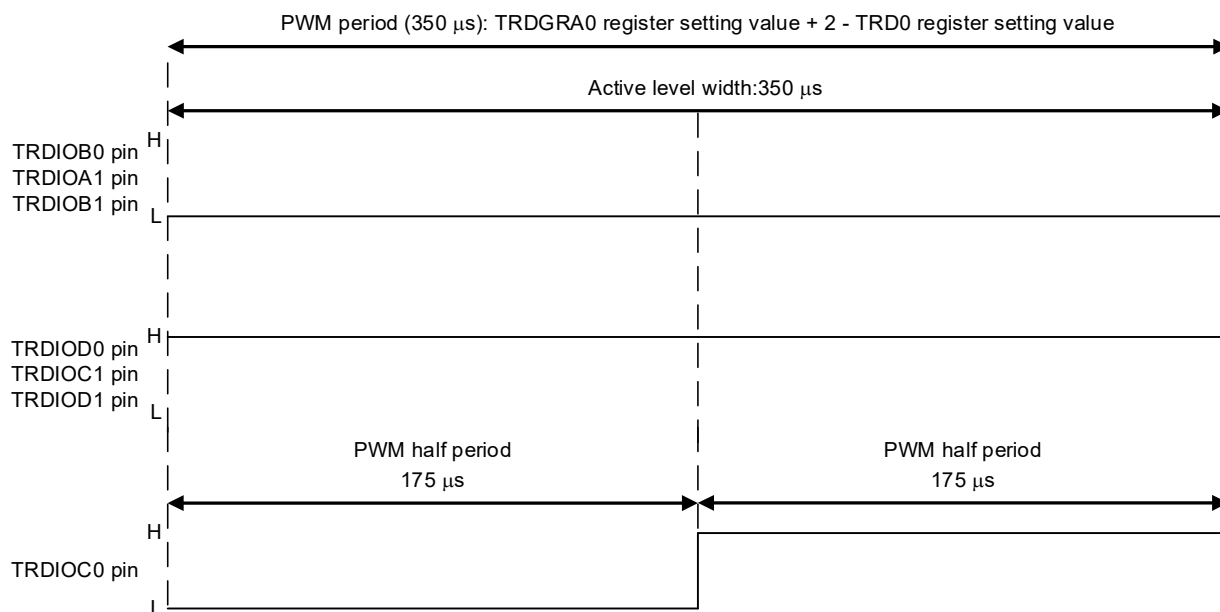


Figure 4.3 PWM Waveform 3

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

(3) PWM waveform 4

Normal-phase output: High inactive level period (350 μ s)

Counter-phase output: Low active level period (350 μ s)

When the TRD1 register underflows after setting the value more than the TRDGRA0 register setting value to the buffer registers (registers TRDGRD0, TRDGRC1, and TRDGRD1), levels below are output.

PWM waveform 4 normal-phase output: Pins TRDIOB0, TRDIOA1, TRDIOB1

High inactive level period: 350 μ s

PWM waveform 4 counter-phase output: Pins TRDIOD0, TRDIOC1, TRDIOD1

Low active level period: 350 μ s

In this sample code, the same signal is output.

Figure 4.4 shows PWM waveform 4.

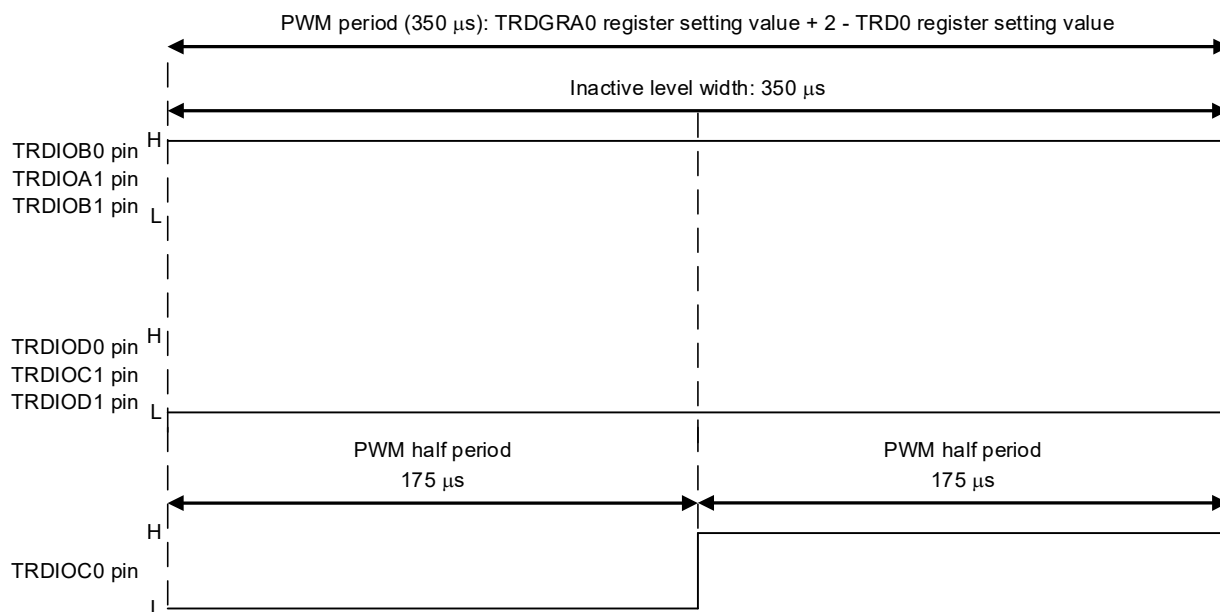


Figure 4.4 PWM Waveform 4

4.1.2 Timing Diagram

When the compare match interrupt is generated for registers TRD0 and TRDGRA0 for the 10th time, a buffer operation is used to switch the PWM waveform.

The figures below show timing diagrams for PWM waveform switching.

PWM waveform 1 → PWM waveform 2

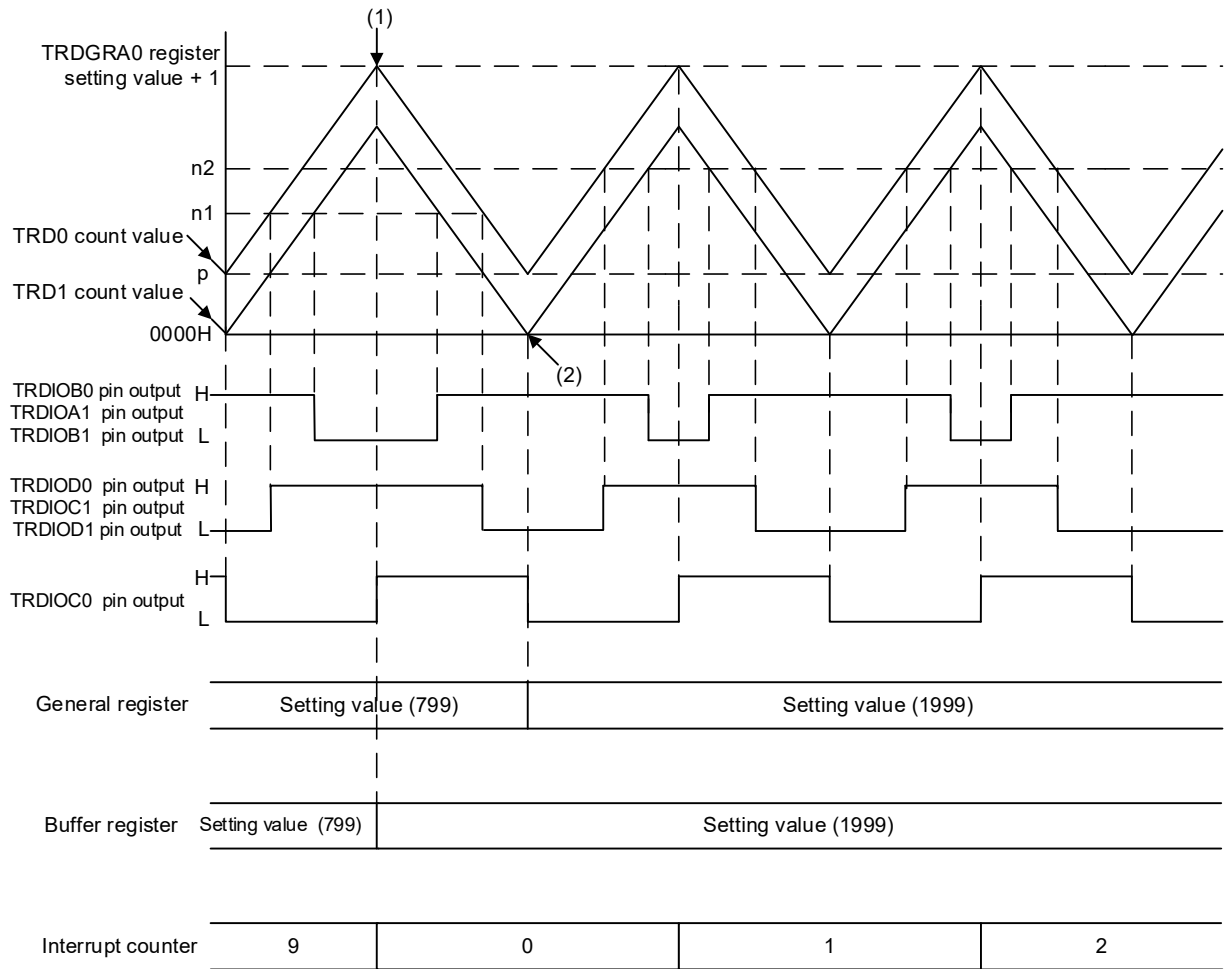
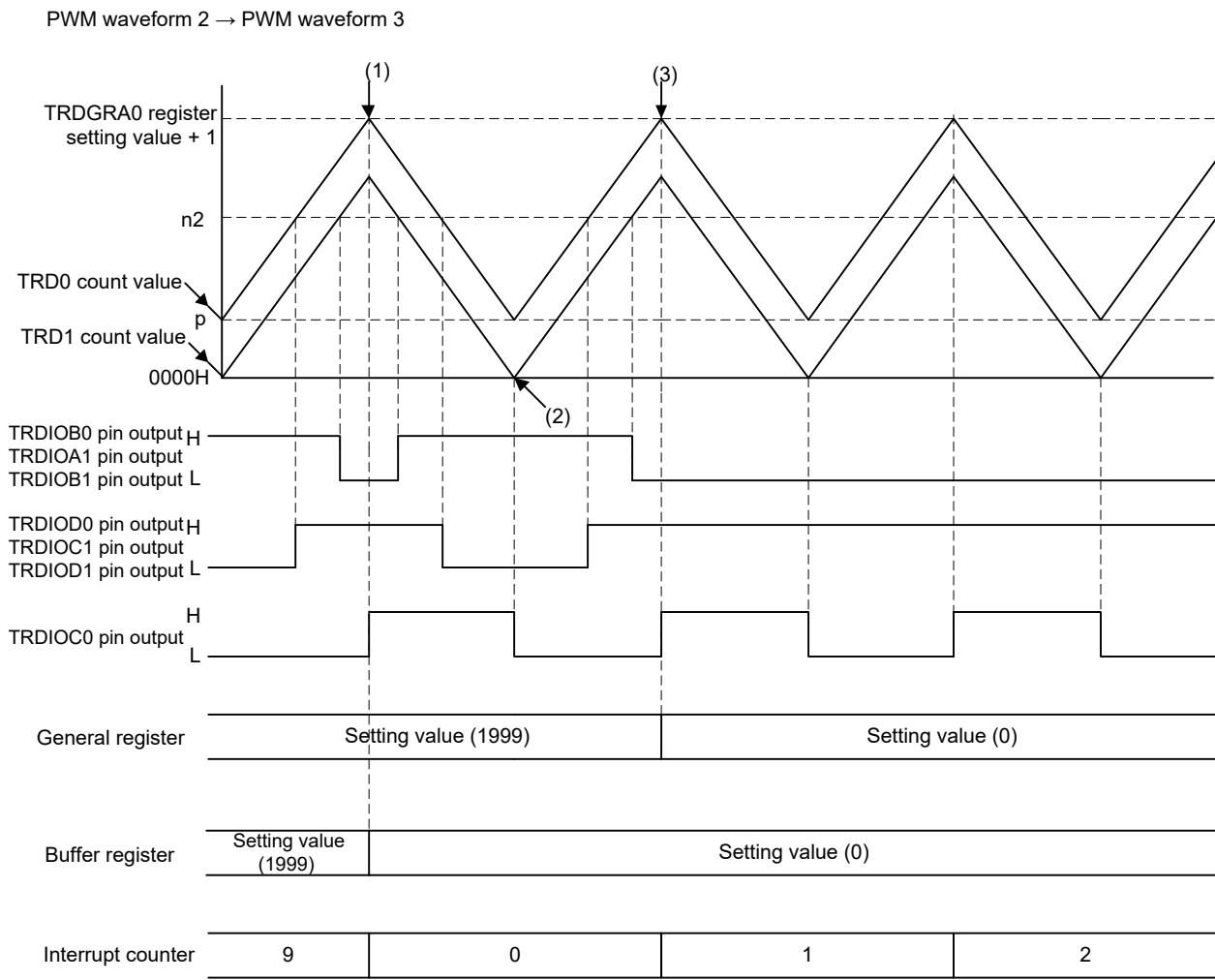


Figure 4.5 Switch Timing from PWM Waveform 1 to PWM Waveform 2

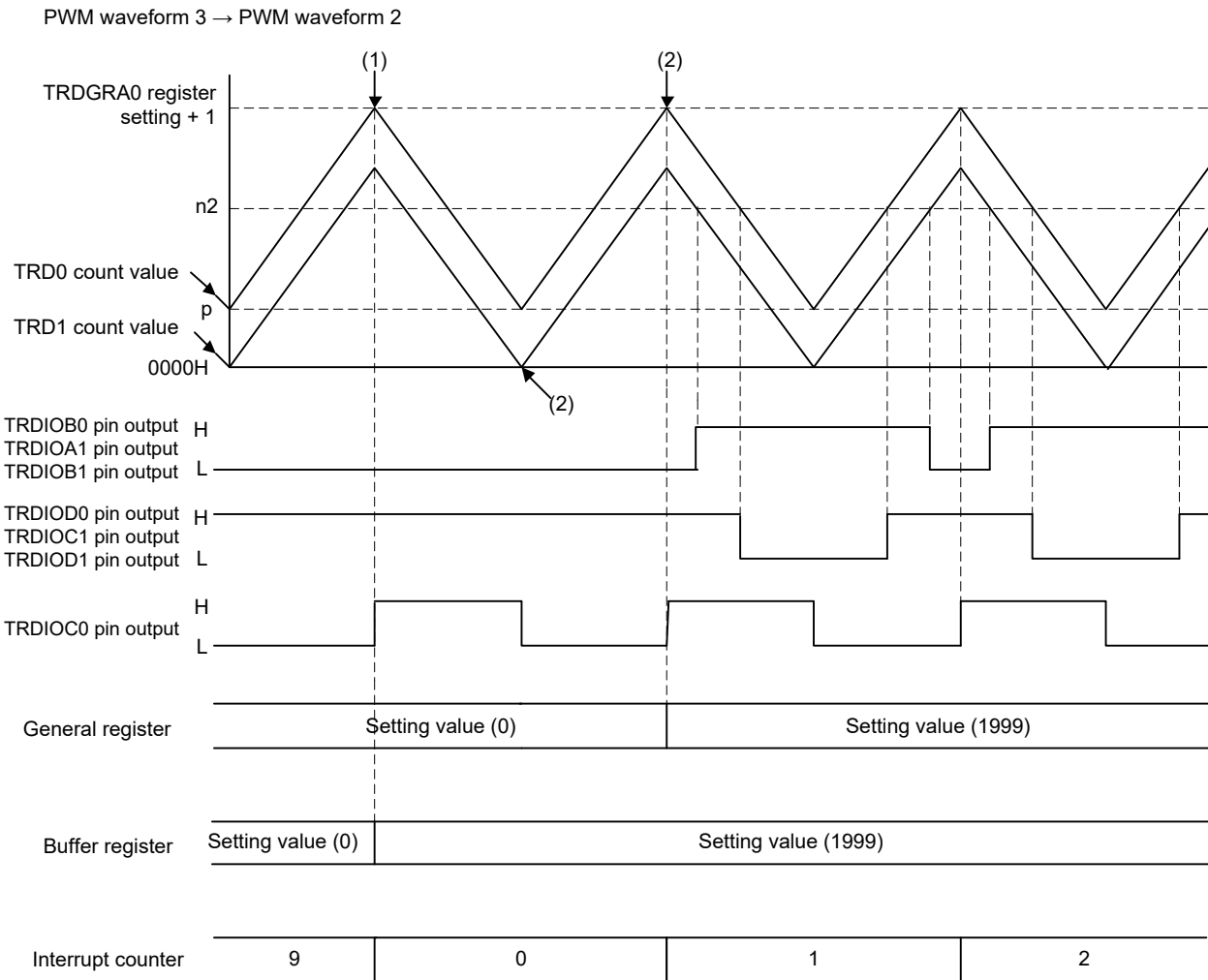
RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output



- p: TRD0 register setting value (400)
n2: General register setting value (1999) when PWM waveform 2 is output
- (1) Set 0000H to the buffer register at the 10th match of registers TRD0 and TRDGRA0.
(2) Since the buffer register setting value is 0000H, data is not transferred from the buffer register to the general register when the TRD1 register underflows.
(3) Since the buffer register setting value is 0000H, data is transferred from the buffer register to the general register when the TRD0 register matches with the TRDGRA0 register.

Figure 4.6 Switch Timing from PWM Waveform 2 to PWM Waveform 3

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output



- p: TRD0 register setting value (400)
n2: General register setting value (1999) when PWM waveform 2 is output
- (1) Set n2 to the buffer register at the 10th match of registers TRD0 and TRDGRA0.
 - (2) Data is not transferred from the buffer register to the general register because the first TRD1 register underflows after setting the buffer register setting value from 0000H to n2.
 - (3) Data is transferred from the buffer register to the general register because of the first match of registers TRD0 and TRDGRA0 after setting the buffer register setting value from 0000H to n2.

Figure 4.7 Switch Timing from PWM Waveform 3 to PWM Waveform 2

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

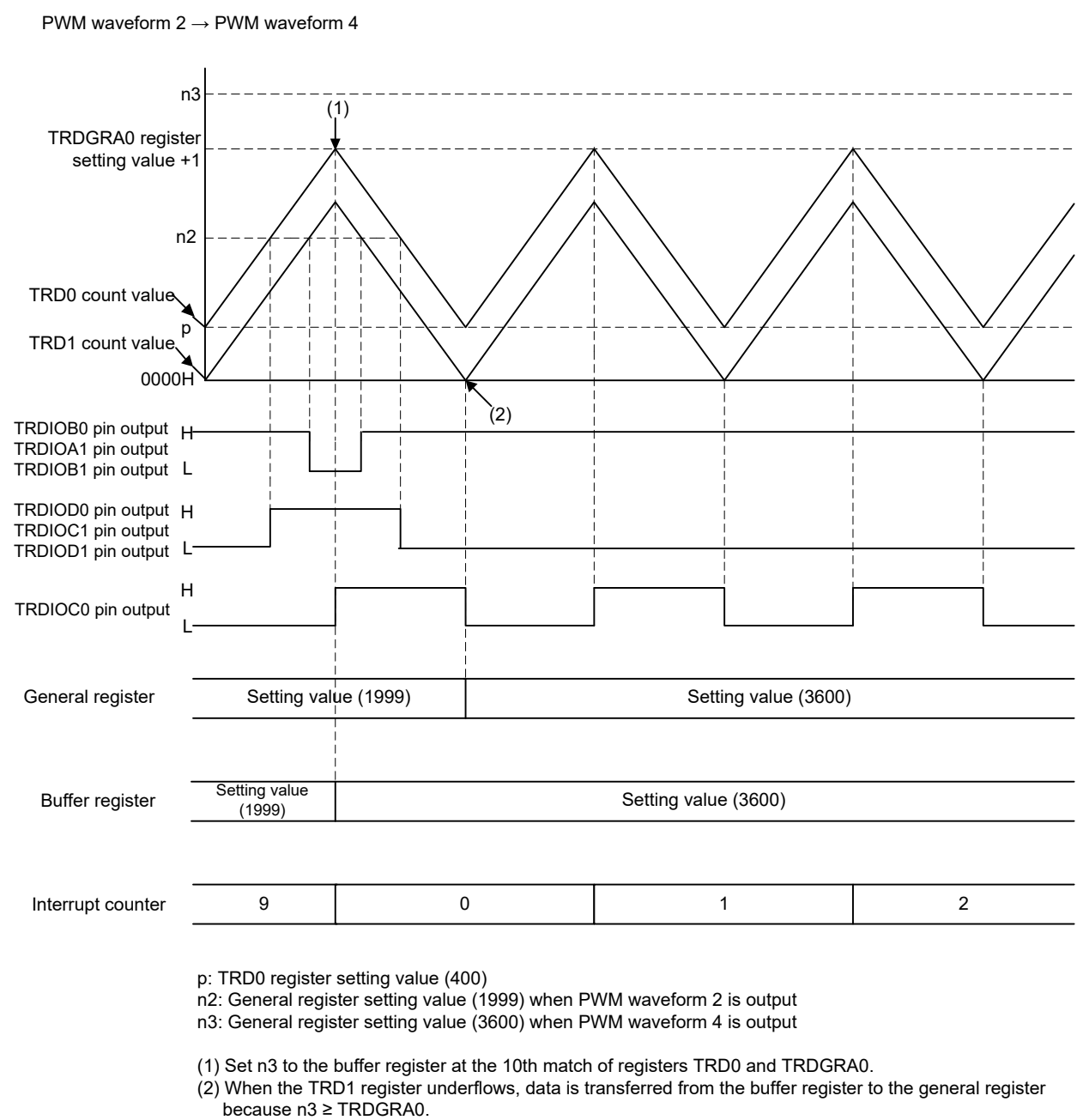
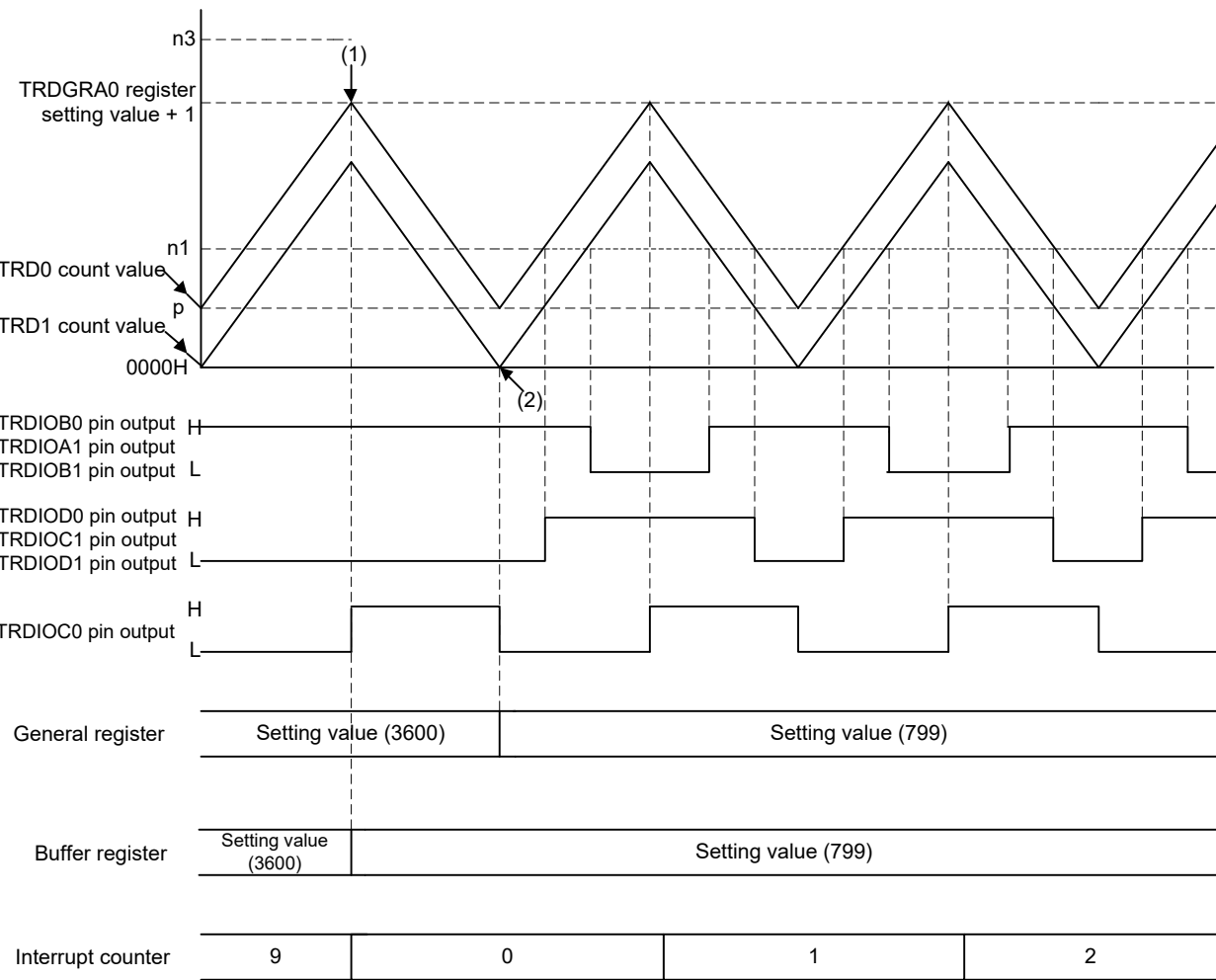


Figure 4.8 Switch Timing from PWM Waveform 2 to PWM Waveform 4

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

PWM waveform 4 → PWM waveform 1



p: TRD0 register setting value (400)
n1: General register setting value (799) when PWM waveform 1 is output
n3: General register setting value (3600) when PWM waveform 4 is output

(1) Set n1 to the buffer register at the 10th match of registers TRD0 and TRDGRA0.
(2) The data is transferred from the buffer register to the general register because the first TRD1 register underflows after setting the TRDGRD0 register setting value from n3 ($n3 \geq \text{TRDGRA0}$) to n1.

Figure 4.9 Switch Timing from PWM Waveform 4 to PWM Waveform 1

4.1.3 PWM Option Unit

The PWM option unit features two key functions: overcurrent/induced current detection and two-stage overcurrent detection.

This application note uses the overcurrent/induced current detection function. When PGA output voltage exceeds the reference voltage, the PWM output pins are set to Hi-Z state, when lower than the reference voltage, the Hi-Z state is released.

Please refer to the timing charts for overcurrent/induced current detection and two-stage overcurrent detection for more details.

The overcurrent/induced current detection timing diagram is shown in Figure 4.10.

Overcurrent/induced current detection function

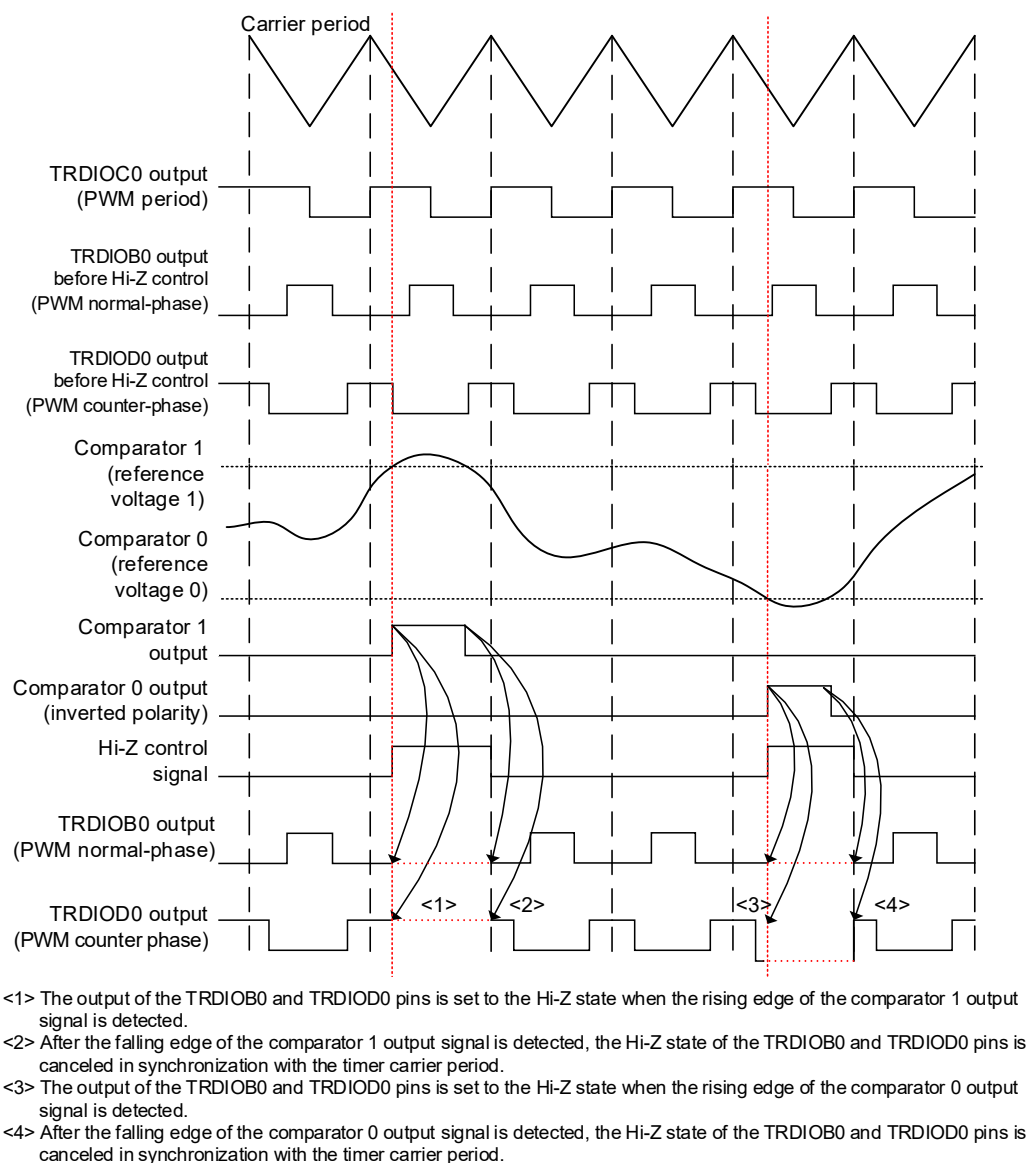


Figure 4.10 Overcurrent/induced Current Detection Function Timing Chart

The two-stage overcurrent detection timing diagram is shown in Figure 4.11.

Two-stage overcurrent detection function

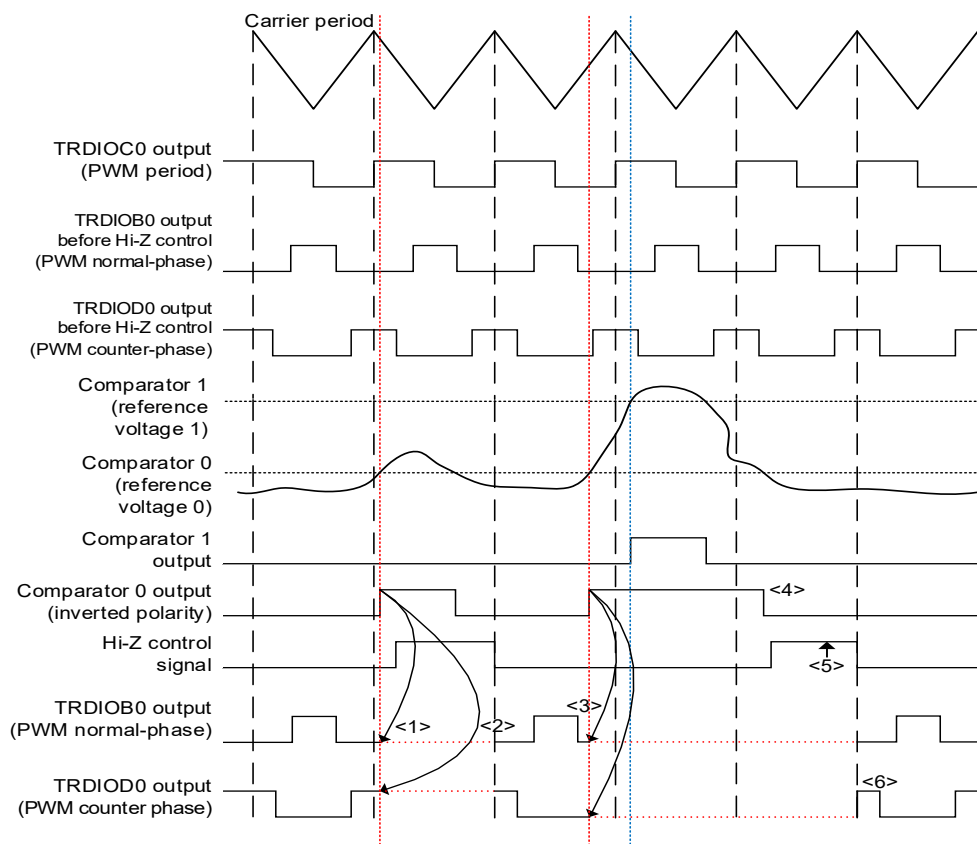


Figure 4.11 Two-stage Overcurrent Detection Function Timing Chart

4.2 Option Byte Settings

Table 4.1 lists the Option Byte Settings.

Table 4.1 Option Byte Settings

Address	Setting Value	Contents
000C0H/010C0H	11101111B	Watchdog timer operation is stopped (count is stopped after reset)
000C1H/010C1H	01111111B	LVD operation (V_{LVI}): reset mode Detection voltage: Rising edge 2.81 V/falling edge 2.75 V
000C2H/010C2H	11101001B	Internal high-speed oscillation HS mode: 16 MHz
000C3H/010C3H	10000100B	On-chip debugging enabled

4.3 Constants

Table 4.2 lists the Constants Used in the Sample Code.

Table 4.2 Constants Used in the Sample Code

Constant Name	Setting Value	Contents
ACT_250us_100us	0	Waveform switch mode: PWM waveform 1 → PWM waveform 2
ACT_100us_LOUT	1	Waveform switch mode: PWM waveform 2 → PWM waveform 3
ACT_LOUT_100us	2	Waveform switch mode: PWM waveform 3 → PWM waveform 2
ACT_100us_HOUT	3	Waveform switch mode: PWM waveform 2 → PWM waveform 4
ACT_HOUT_250us	4	Waveform switch mode: PWM waveform 4 → PWM waveform 1
ACT_250us	0	Register setting value index of PWM waveform 1
ACT_100us	1	Register setting value index of PWM waveform 2
ACT_HOUT	2	Register setting value index of PWM waveform 4
ACT_LOUT	3	Register setting value index of PWM waveform 3

4.4 Variables

Table 4.3 lists the Global Variables.

Table 4.3 Global Variables

Type	Variable Name	Contents	Function Used
unsigned char	g_int_cnt	Interrupt counter	r_tmrd0_interrupt
unsigned char	g_output_chg_mode	Waveform switch mode	r_tmrd0_interrupt

Table 4.4 list the const Variable.

Table 4.4 const Variable

Type	Variable Name	Contents	Function Used
unsigned short const	TRDGRB0_VALU E_TBL[]	Active level setting value table	r_tmrd0_interrupt

4.5 Functions

Table 4.5 lists the Functions.

Table 4.5 Functions

Function Name	Outline
hdwinit	Initial setting
R_Systeminit	Initial setting of peripheral functions
R_PORT_Create	Initial setting of ports
R_CGC_Create	Initial setting of CPU clock
R_TMRD0_Create	Initial setting of timer RD
R_COMPPGA_Create	Initial setting of comparator/PGA
Main	Main processing
R_MAIN_UserInit	Initial setting of main
R_COMP0_Start	Comparator 0 start setting
R_COMP1_Start	Comparator 1 start setting
R_PGA_Start	PGA start setting
timer_rd0_start	Timer RD0 and timer RD1 count start setting
r_tmrd0_interrupt	Timer RD0 interrupt

4.6 Functions

The following are the sample code functions used in this application note.

hdwinit

Outline	Initial setting
Header	None
Declaration	void hdwinit(void)
Description	Perform the initial setting of peripheral functions.
Argument	None
Return Value	None
Notes	None

R_Systeminit

Outline	Initial setting of peripheral functions
Header	None
Declaration	void R_Systeminit(void)
Description	Perform the initial setting of peripheral functions used in this document.
Argument	None
Return Value	None
Notes	None

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

R_PORT_Create

Outline	Initial setting of ports
Header	r_cg_port.h
Declaration	void R_PORT_Create(void)
Description	Perform the initial setting of ports
Argument	None
Return Value	None
Notes	None

R_CGC_Create

Outline	Initial setting of CPU clock
Header	r_cg_cgc.h
Declaration	void R_CGC_Create(void)
Description	Perform the initial setting of the CPU clock.
Argument	None
Return Value	None
Notes	None

R_TMRD0_Create

Outline	Initial setting of of timer RD
Header	r_cg_tmrd.h
Declaration	void R_TMRD0_Create (void)
Description	Perform the initial setting of timer RD
Argument	None
Return Value	None
Notes	None

R_COMPPGA_Create

Outline	Initial setting of comparator/PGA
Header	r_cg_comppga.h
Declaration	void R_COMPPGA_Create(void)
Description	Perform the initial setting of the comparators and PGA.
Argument	None
Return Value	None
Notes	None

main

Outline	Main processing
Header	None
Declaration	void main(void)
Description	Perform main processing.
Argument	None
Return Value	None
Notes	None

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R_MAIN_UserInit

Outline	Initial setting of main
Header	None
Declaration	void R_MAIN_UserInit(void)
Description	Perform initial setting of main.
Argument	None
Return Value	None
Notes	None

R_COMP0_Start

Outline	Comparator 0 start setting
Header	r_cg_comppga.h
Declaration	void R_COMP0_Start(void)
Description	Set comparator 0 to start enabled.
Argument	None
Return Value	None
Notes	None

R_COMP1_Start

Outline	Comparator 1 start setting
Header	r_cg_comppga.h
Declaration	void R_COMP1_Start(void)
Description	Set comparator 1 to start enabled.
Argument	None
Return Value	None
Notes	None

R_PGA_Start

Outline	PGA start setting
Header	r_cg_comppga.h
Declaration	void R_PGA_Start(void)
Description	Set PGA to start enabled.
Argument	None
Return Value	None
Notes	None

timer_rd0_start

Outline	Timer RD0 and timer RD1 count start setting
Header	r_cg_tmrd.h
Declaration	void timer_rd0_start(void)
Description	Set timer RD0 and RD1 to count start.
Argument	None
Return Value	None
Notes	None

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

r_tmr0_interrupt

Outline	Timer RD0 interrupt
Header	r_cg_tmr.h
Declaration	__interrupt static void r_tmr0_interrupt(void)
Description	When the 10th interrupt is generated, set the buffer register value.
Argument	None
Return Value	None
Notes	None

4.7 Flowcharts

Figure 4.12 shows the entire flow of the sample code.

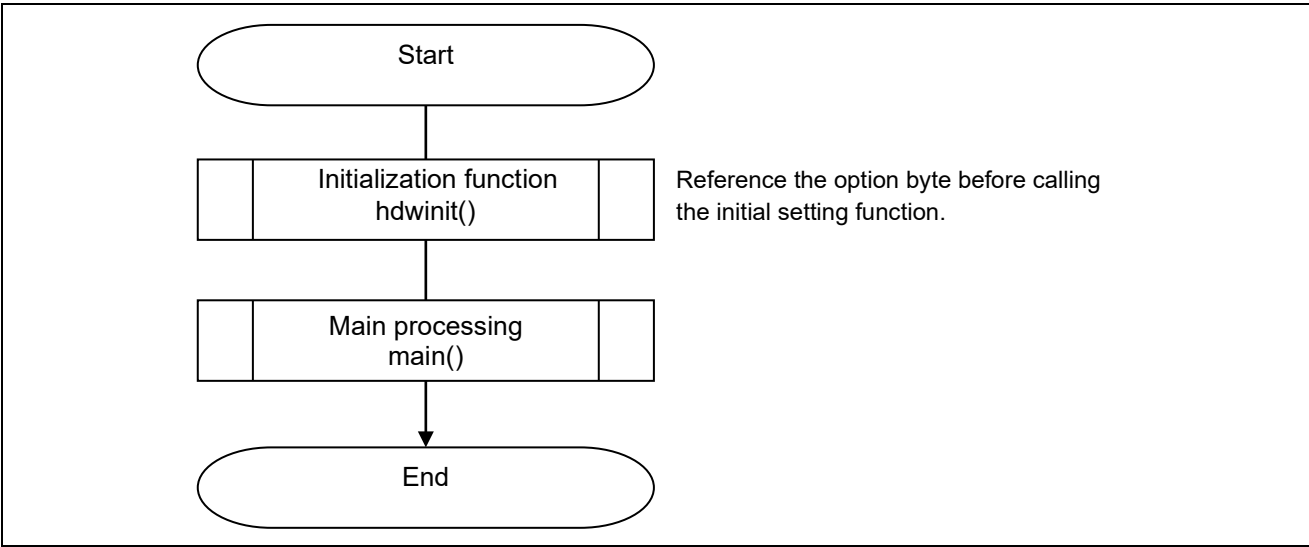


Figure 4.12 Entire Flow

4.7.1 Initialization

Figure 4.13 shows the flowchart for initialization.

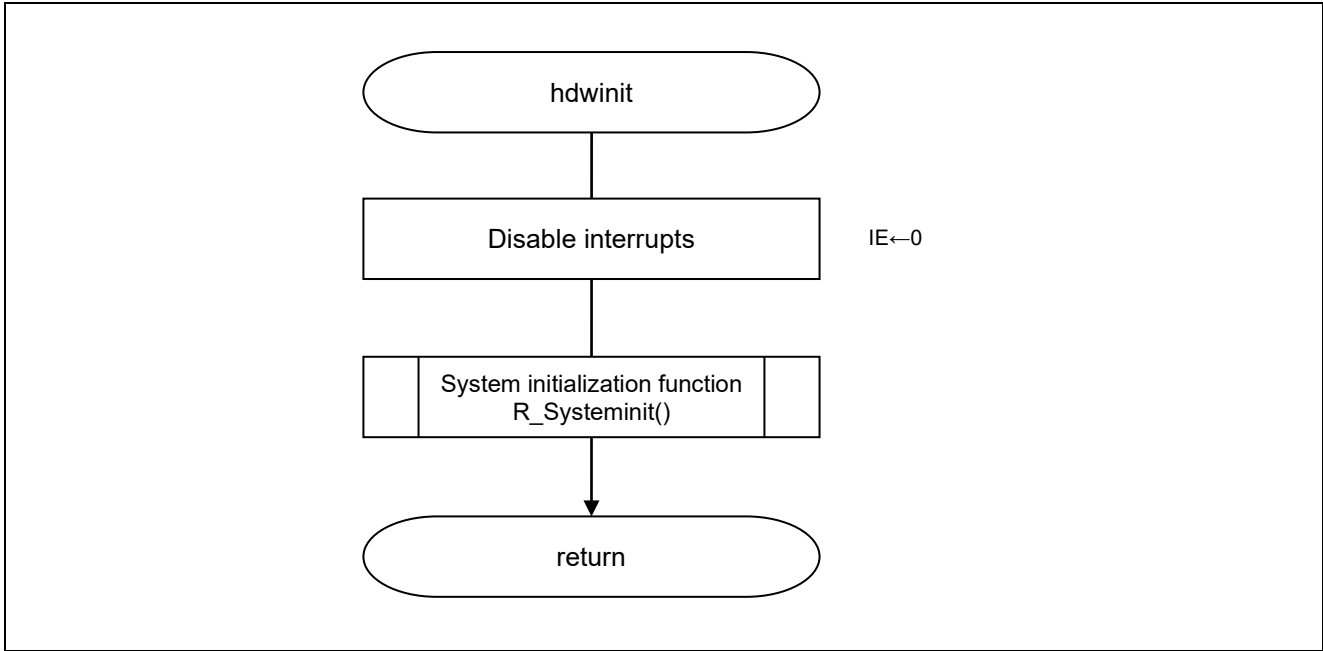


Figure 4.13 Initialization

4.7.2 Initialization of Peripheral Functions

Figure 4.14 shows the flowchart for the initialization of peripheral functions.

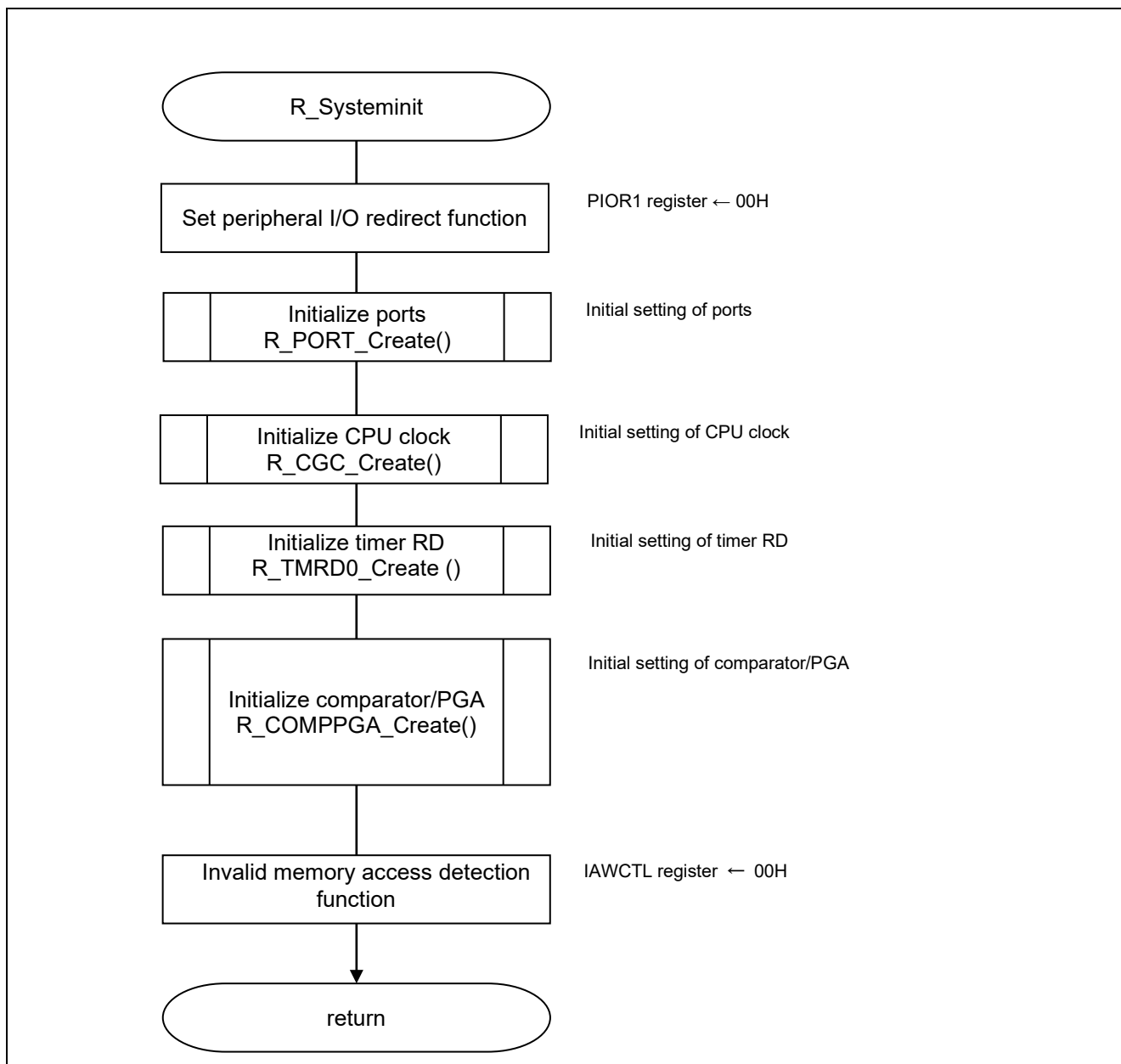


Figure 4.14 Initialization of Peripheral Functions

4.7.3 Initialization of Ports

Figure 4.15 shows the flowchart for the initialization of ports.

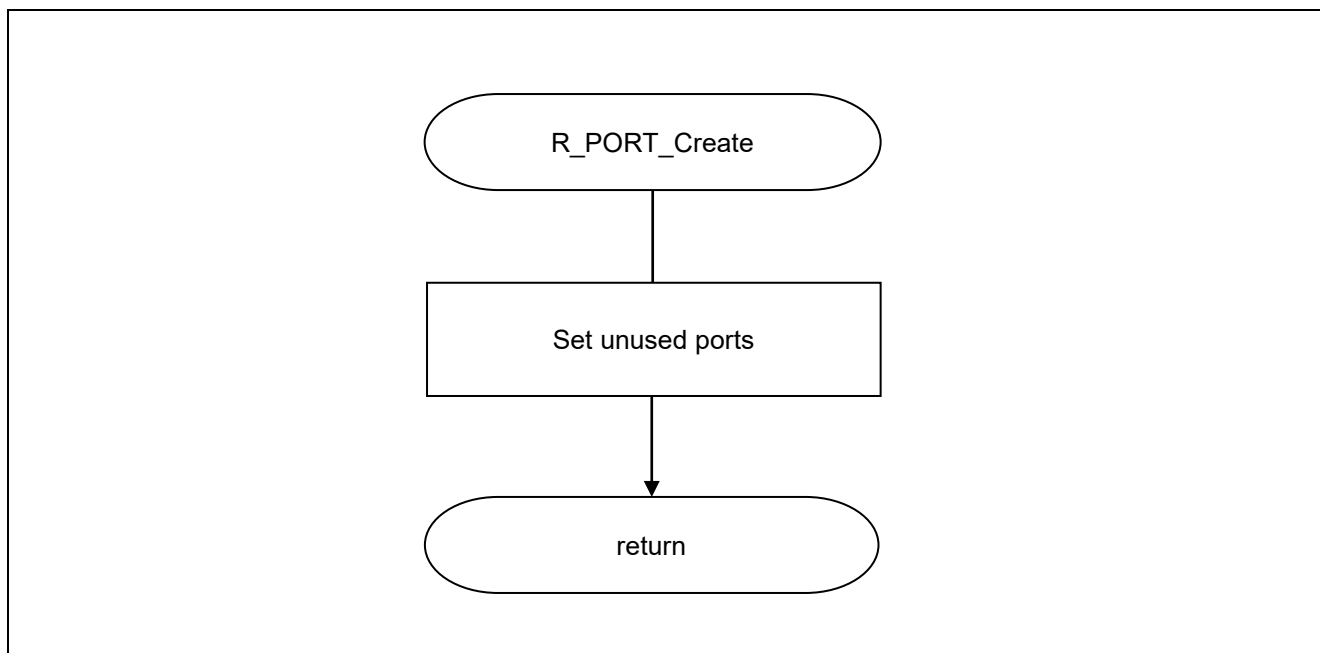


Figure 4.15 Initialization of Ports

- Note: 1. Refer to the initialization flowchart in the RL78/G13 Initialization (R01AN0451J) Application Note for details on how to set unused ports.
2. When designing circuits, always make sure unused ports are properly processed and all electrical characteristics are met. Also make sure each unused input-only port is connected to V_{DD} or V_{SS} through a resistor.

4.7.4 Initial Setting of CPU Clock

Figure 4.16 shows the flowchart for the initialization of the CPU clock.

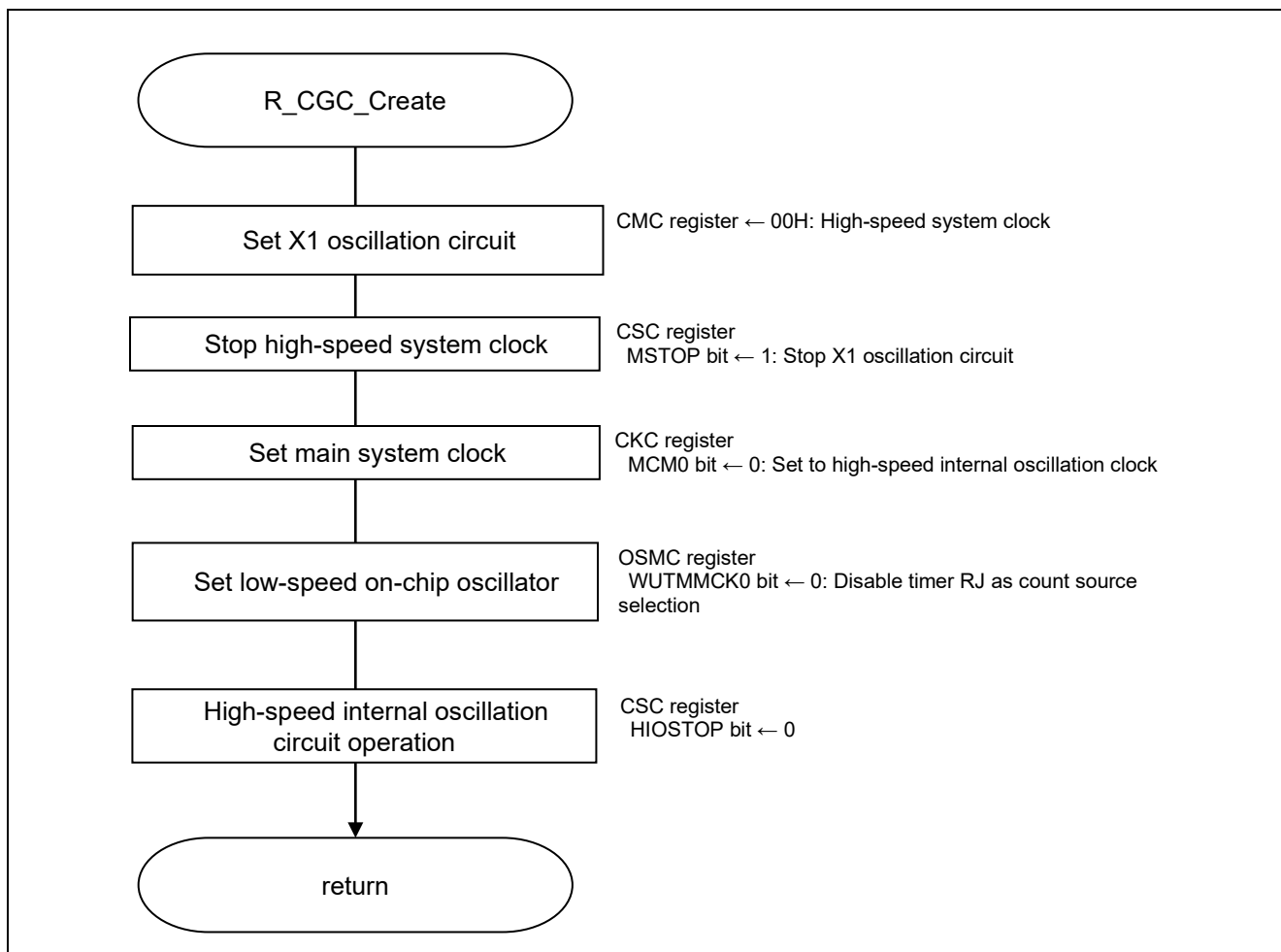


Figure 4.16 Initial Setting of CPU Clock

4.7.5 Initial Setting of Timer RD

Figure 4.17 to 4.19 show the flowchart for the initial setting of timer RD.

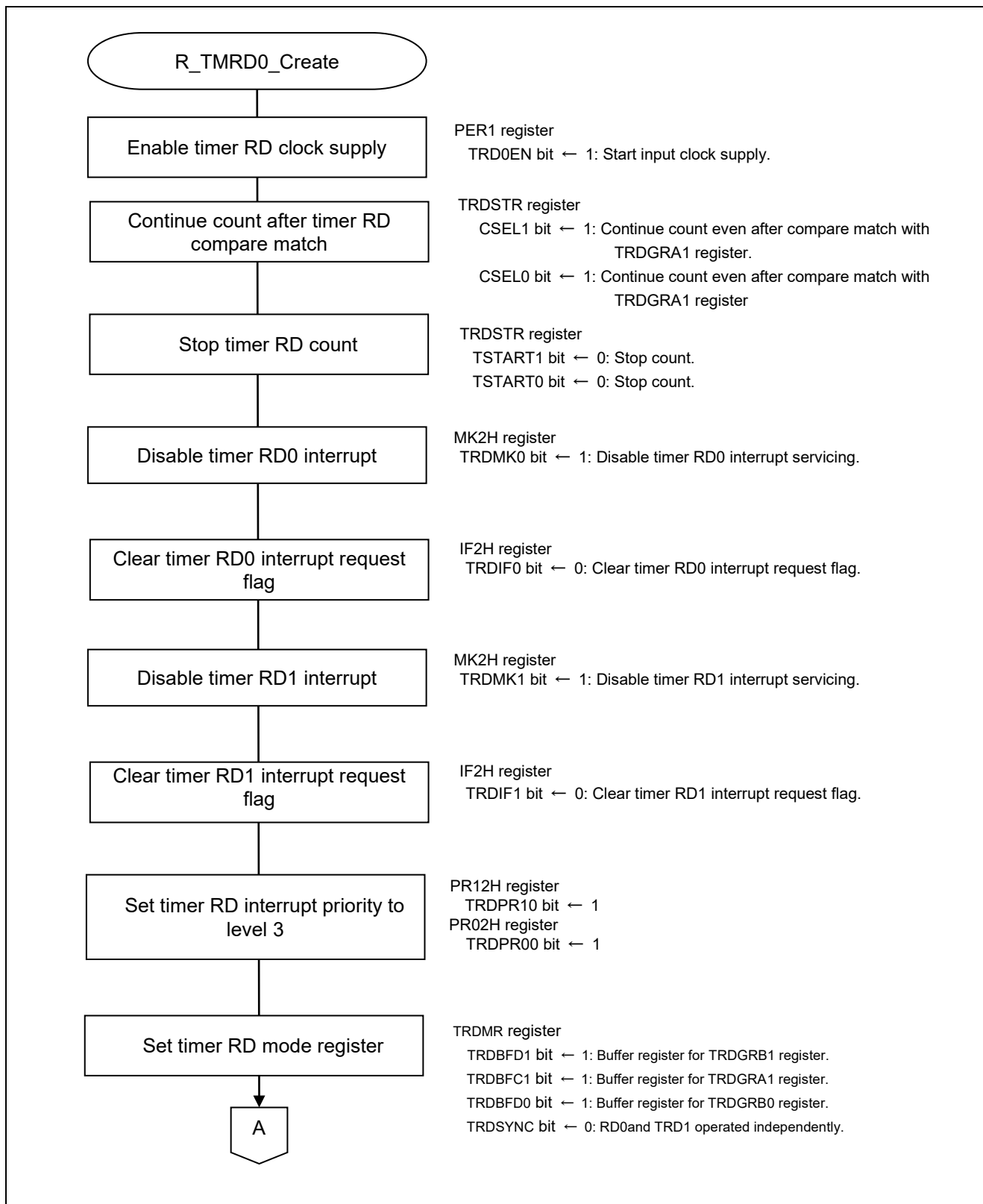


Figure 4.17 Initialization of Timer RD (1/3)

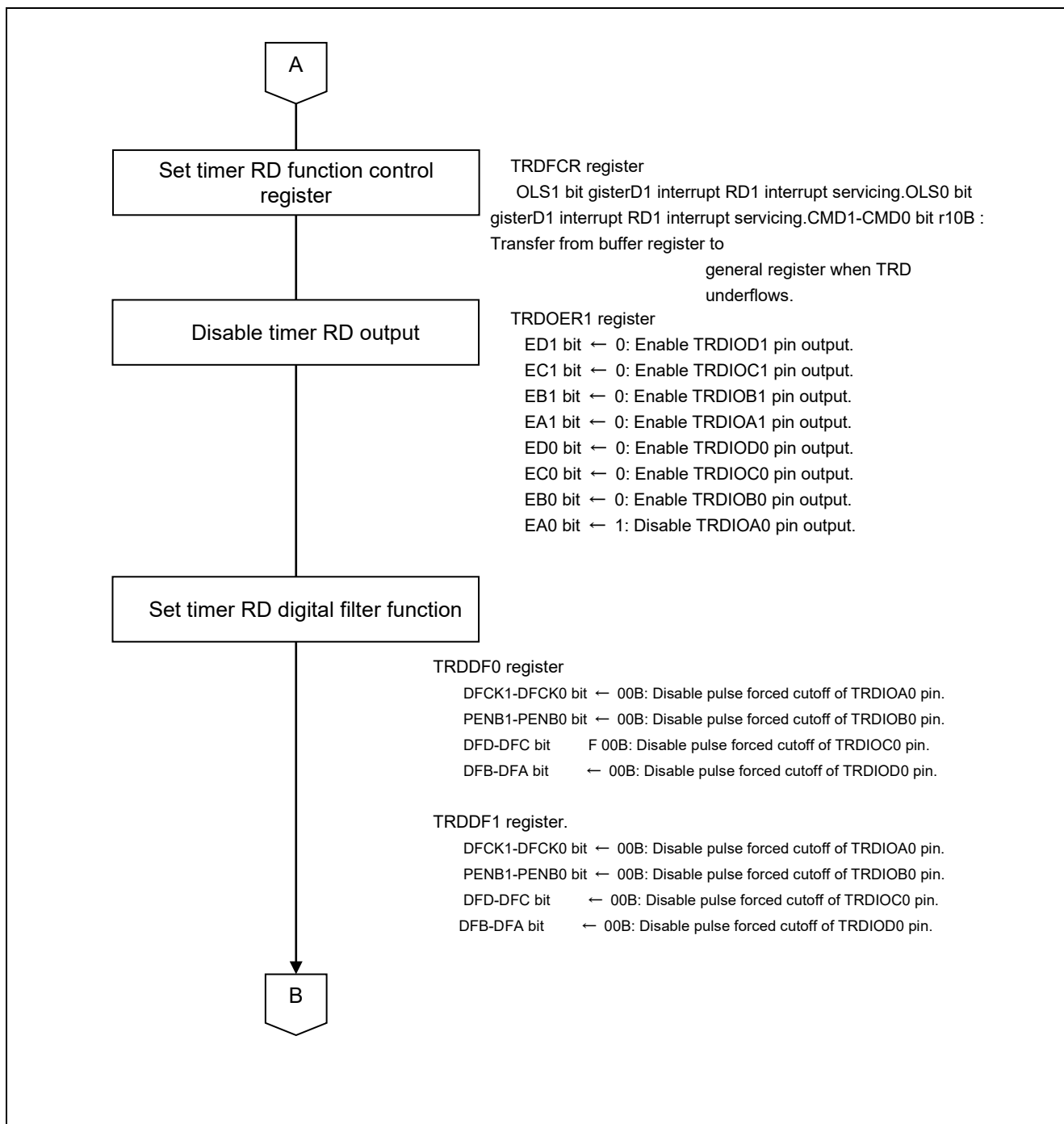


Figure 4.18 Initialization of Timer RD (2/3)

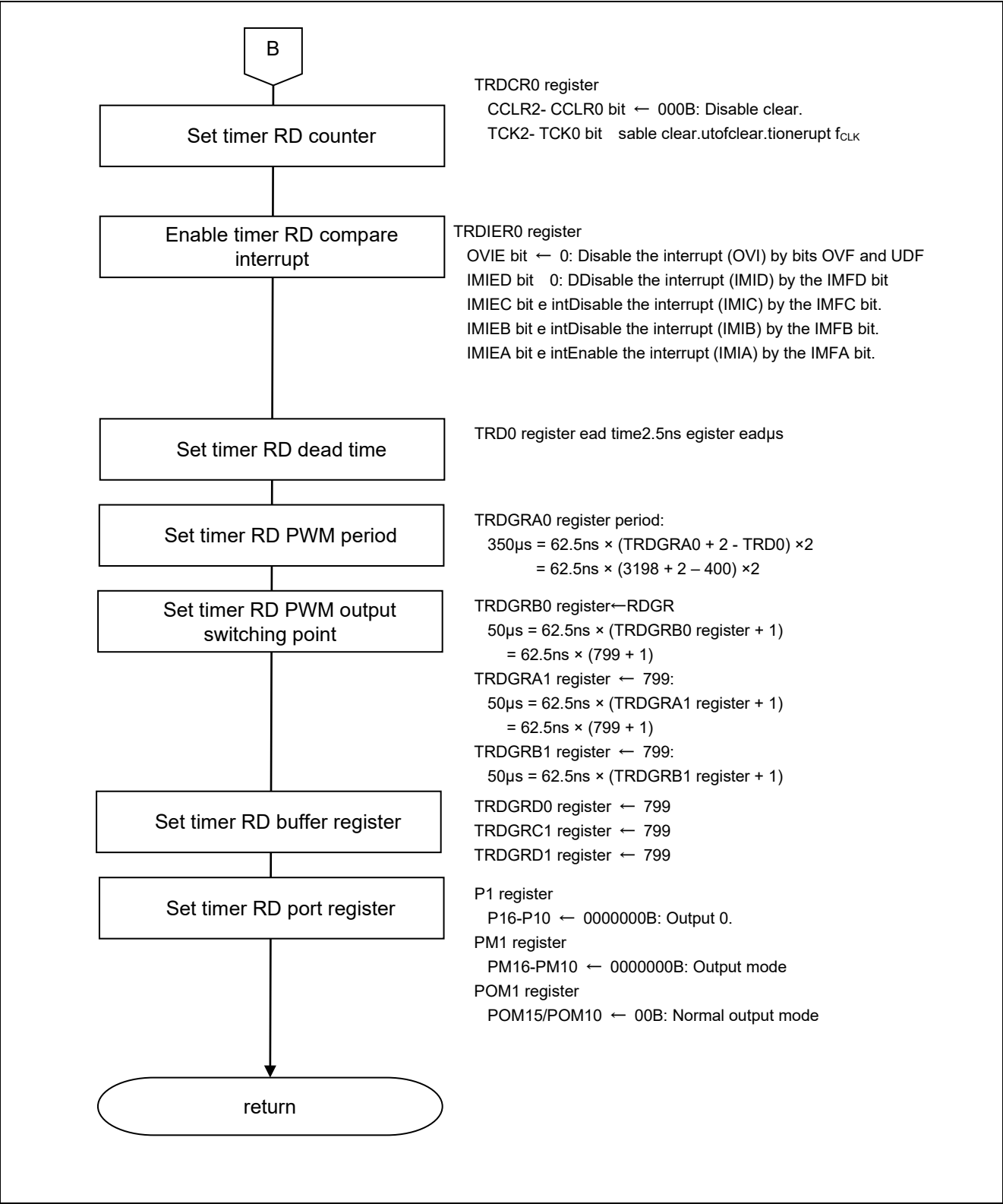


Figure 4.19 Initialization of Timer RD (3/3)

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Enable timer RD clock supply.

- Peripheral Enable Register 1 (PER1)
Enable clock supply to timer RD.

Symbol: PER1

7	6	5	4	3	2	1	0
TMKAEN	PWMOPEN	OACMPEN	TRD0EN	0	0	0	TRJ0EN
x	x	x	1	0	0	0	x

Bit 4

TRD0EN	Control of timer RD input clock supply
0	Stops input clock supply.
1	Enables input clock supply.

Continue/stop count after timer RD compare match

- Timer RD Mode Register (TRDSTR)
Set count to continue after timer RD compare match.
Stop timer RD count.

Symbol: TRDSTR

7	6	5	4	3	2	1	0
0	0	0	0	CSEL1	CSEL0	TSTART1	TSTART0
0	0	0	0	1	1	0	0

Bit 3

CSEL1	TRD1 count operation select
0	Count stops at compare match with TRDGRA1 register
1	Count continues after compare match with TRDGRA1 register

Bit 2

CSEL0	TRD0 count operation select
0	Count stops at compare match with TRDGRA0 register
1	Count continues after compare match with TRDGRA0 register

Bit 1

TSTART1	TRD1 count start flag
0	Count stops
1	Count starts

Bit 0

TSTART0	TRD0 count start flag
0	Count stops
1	Count starts

Set timer RD interrupts.

- Interrupt Mask Flag Register (MK2H)
Disable INTTRD0 and INTTRD1 interrupts.
- Interrupt Request Flag Register (IF2H)
Clear timer RD0 and RD1 interrupt request flags.

Symbol: MK2H

7	6	5	4	3	2	1	0
FLMK	1	1	1	1	TRDMK1	TRDMK0	CMPMK1
1	1	1	1	1	1	1	x

Bit 2

TRDMK1	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Bit 1

TRDMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Symbol: IF2H

7	6	5	4	3	2	1	0
FLIF	0	0	0	0	TRDIF1	TRDIF0	CMPIF1
1	0	0	0	0	0	0	x

Bit 2

TRDIF1	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Bit 1

TRDIF0	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Set timer RD interrupt priority level.

- Priority Specification Flag Registers (PR02H and PR12H)
Set to level 3 (low priority).

Symbol: PR12H

7	6	5	4	3	2	1	0
FLPR1	1	1	1	1	TRDPR11	TRDPR10	CMPPR11
x	1	1	1	1	x	1	x

Symbol: PR02H

7	6	5	4	3	2	1	0
FLPR0	1	1	1	1	TRDPR01	TRDPR00	CMPPR01
x	1	1	1	1	x	1	x

Bit 1

TRDPR10	TRDPR00	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	1	Specify level 3 (low priority level)

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Set timer RD operation mode register.

- Timer RD Mode Register (TRDMR)

Use registers TRDGRB1, TRDGRA1, and TRDGRB0 as buffer registers.

Symbol: TRDMR

7	6	5	4	3	2	1	0
TRDBFD1	TRDBFC1	TRDBFD0	TRDBFC0	0	0	0	TRDSYNC
1	1	1	0	0	0	0	0

Bit 7

TRDBFD1	TRDGRD1 register function select
0	General register
1	Buffer register for TRDGRB1 register

Bit 6

TRDBFC1	TRDGRC1 register function select
0	General register
1	Buffer register for TRDGRA1 register

Bit 5

TRDBFD0	TRDGRD0 register function select
0	General register
1	Buffer register for TRDGRB0 register

Bit 4

TRDBFC0	TRDGRC0 register function select
0	General register
1	Buffer register for TRDGRA0 register

Bit 0

TRDSYNC	Timer RD synchronous
0	TRD0 and TRD1 operate independently
1	TRD0 and TRD1 operate synchronously

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Set the timer RD function control register.

- Timer RD Function Control Register (TRDFCR)
Use high initial output and low active level.
Set to transfer from buffer register to general register when timer RD1 underflows.

Symbol: TRDFCR

7	6	5	4	3	2	1	0
PWM3	STCLK	0	0	OLS1	OLS0	CMD1	CMD0
x	0	0	0	0	0	1	0

Bit 6

STCLK	External clock input select
0	External clock input disabled
1	External clock input enabled

Bit 3

OLS1	Counter-phase output level select
0	High initial output and low active level
1	Low initial output and high active level

Bit 2

OLS0	Normal-phase output level select
0	High initial output and low active level
1	Low initial output and high active level

Bit 0

CMD0	CMD0	Combination mode select
1	0	Transfer from buffer register to general register when TRD1 underflows
1	1	Transfer from buffer register to general register at compare match between registers TRD0 and TRDGRA0
Other than the above		Do not set

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Timer RD output enable setting

- Timer RD Output Master Enable Register 1 (TRDOER1)
Enable all timer RD output other than TRDIOA0.

Symbol: TRDOER1

7	6	5	4	3	2	1	0
ED1	EC1	EB1	EA1	ED0	EC0	EB0	EA0
0	0	0	0	0	0	0	1

Bit 7

ED1	TRDIOD1 output disable
0	Output enabled
1	Output disabled (TRDIOD1 pin functions as an I/O port.)

Bit 6

EC1	TRDIOC1 output disable
0	Output enabled
1	Output disabled (TRDIOD1 pin functions as an I/O port.)

Bit 5

EB1	TRDIOB1 output disable
0	Output enabled
1	Output disabled (TRDIOD1 pin functions as an I/O port.)

Bit 4

EA1	TRDIOA1 output disable
0	Output enabled
1	Output disabled (TRDIOD1 pin functions as an I/O port.)

Bit 3

ED0	TRDIOD0 output disable
0	Output enabled
1	Output disabled (TRDIOD1 pin functions as an I/O port.)

Bit 2

EC0	TRDIOC0 output disable
0	Output enabled
1	Output disabled (TRDIOD1 pin functions as an I/O port.)

Bit 1

EB0	TRDIOB0 output disable
0	Output enabled
1	Output disabled (TRDIOD1 pin functions as an I/O port.)

Bit 0

EA0	TRDIOA0 output disable
0	Output enabled
1	Output disabled (TRDIOD1 pin functions as I/O port)

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Set timer RD0 digital filter

- Timer RD Digital Filter Function Select Register 0 (TRDDF0)
Disable pulse forced cutoff.

Symbol: TRDDF0

7	6	5	4	3	2	1	0
DFCK1	DFCK0	PENB1	PENB0	DFD	DFC	DFB	DFA
0	0	0	0	0	0	0	0

Bits 7 and 6

DFCK1	DFCK0	TRDIOA0 pin pulse forced cutoff control
0	0	Forced cutoff disabled
0	1	High-impedance output
1	0	Low output
1	1	High output

Bits 5 and 4

PENB1	PENB0	TRDIOB0 pin pulse forced cutoff control
0	0	Forced cutoff disabled
0	1	High-impedance output
1	0	Low output
1	1	High output

Bits 3 and 2

DFD	DFC	TRDIOC0 pin pulse forced cutoff control
0	0	Forced cutoff disabled
0	1	High-impedance output
1	0	Low output
1	1	High output

Bits 1 and 0

DFB	DFA	TRDIOD0 pin pulse forced cutoff control
0	0	Forced cutoff disabled
0	1	High-impedance output
1	0	Low output
1	1	High output

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Set timer RD1 digital filter

- Timer RD Digital Filter Function Select Register 1 (TRDDF1)
Disable pulse forced cut-off.

Symbol: TRDDF1

7	6	5	4	3	2	1	0
DFCK1	DFCK0	PENB1	PENB0	DFD	DFC	DFB	DFA
0	0	0	0	0	0	0	0

Bits 7 and 6

DFCK1	DFCK0	TRDIOA1 pin pulse forced cutoff control
0	0	Forced cutoff disabled
0	1	High-impedance output
1	0	Low output
1	1	High output

Bits 5 and 4

PENB1	PENB0	TRDIOB1 pin pulse forced cutoff control
0	0	Forced cutoff disabled
0	1	High-impedance output
1	0	Low output
1	1	High output

Bits 3 and 2

DFD	DFC	TRDIOC1 pin pulse forced cutoff control
0	0	Forced cutoff disabled
0	1	High-impedance output
1	0	Low output
1	1	High output

Bits 1 and 0

DFB	DFA	TRDIOD1 pin pulse forced cutoff control
0	0	Forced cutoff disabled
0	1	High-impedance output
1	0	Low output
1	1	High output

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Set timer RD counter.

- Timer RD Control Register 0 (TRDCR0)
Set fCLK to the count source of timer RD0.

Symbol: TRDCR0

7	6	5	4	3	2	1	0
CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
0	0	0	0	0	0	0	0

Bits 7 and 5

CCLR2	CCLR1	CCLR0	TRD0 counter clear select
0	0	0	Set to 000B (clear disabled: free-running operation)

Bits 4 and 3

CKEG1	CKEG0	External clock edge select
0	0	Count at rising edge
0	1	Count at falling edge
1	0	Count at both edge
Other than above		Do not set.

Bits 2 and 0

TCK2	TCK1	TCK0	Count source select
0	0	0	fCLK, fHOCO
0	0	1	fCLK/2
0	1	0	fCLK/4
0	1	1	fCLK/8
1	0	0	fCLK/32
1	0	1	TRDCLK input
Other than above			Do not set.

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Enable timer RD compare match interrupt.

- Timer RD Interrupt Enable Register 0 (TRDIER0)
Enable the interrupt by the IMFA bit.

Symbol: TRDIER0

7	6	5	4	3	2	1	0
0	0	0	OVIE	IMIED	IMIEC	IMIEB	IMIEA
0	0	0	0	0	0	0	1

Bit 4

OVIE	Overflow/underflow interrupt enable
0	Interrupt (OVI) by bits OVF and UDF disabled
1	Interrupt (OVI) by bits OVF and UDF enabled

Bit 3

IMIED	Input capture/compare match interrupt enable D
0	Interrupt (IMID) by the IMFD bit is disabled
1	Interrupt (IMID) by the IMFD bit is enabled

Bit 2

IMIEC	Input capture/compare match interrupt enable C
0	Interrupt (IMIC) by the IMFC bit is disabled
1	Interrupt (IMIC) by the IMFC bit is enabled

Bit 1

IMIEB	Input capture/compare match interrupt enable B
0	Interrupt (IMIB) by the IMFB bit is disabled
1	Interrupt (IMIB) by the IMFB bit is enabled

Bit 0

IMIEA	Input capture/compare match interrupt enable A
0	Interrupt (IMIA) by the IMFA bit is disabled
1	Interrupt (IMIA) by the IMFA bit is enabled

RL78/G1G Timer RD in Complementary PWM Mode and
Using PWM Option Unit to Forcibly Cut Off PWM Output

Set timer RD dead time.

- Timer RD Counter 0 (TRD0)
Set dead time to 25 μ s.

Symbol: TRD0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0

Bits 15 to 0

Function
Count the count source. Count operation is incremented When an overflow occurs, the OVF bit in the TRDSR0 register is set to 1.

Set the timer RD PWM period.

- Timer RD General Register A0 (TRDGRA0)
Set the PWM period to 350 μ s.

Symbol: TRDGRA0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0	0	1	1	1	1	1	1	0

Bits 15 to 0

Function	PWM output pin
General register. Set the PWM period at initialization.	TRDIOC0, output inverted every half period)

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Set timer RD PWD output changing point.

- Timer RD General Register A0 (TRDGRB0, TRDGRA1, TRDGRB1)
Set PWD output changing point to 50 μ s.

Symbol: TRDGRB0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1

Bits 15 to 0

Function	PWM output pin
General register. Set the changing point of PWM1 output at initialization.	TRDIOB0 TRDIOD0

Symbol: TRDGRA1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1

Bits 15 to 0

Function	PWM output pin
General register. Set the changing point of PWM2 output at initialization.	TRDIOA1 TRDIOC1

Symbol: TRDGRB1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1

Bits 15 to 0

Function	PWM output pin
General register. Set the changing point of PWM3 output at initialization.	TRDIOB1 TRDIOD1

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Set timer RD buffer register

- Timer RD General Register A0 (TRDGRD0, TRDGRC1, TRDGRD1)
Set the buffer registers.

Symbol: TRDGRD0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1

Bits 15 to 0

Register	Function	PWM output pin
TRDBFD0=1	Buffer register. Set the changing point of next PWM output.	TRDIOB0

Symbol: TRDGRC1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1

Bits 15 to 0

Register	Function	PWM output pin
TRDBFC1 = 1	Buffer register. Set the changing point of next PWM output.	TRDIOA1

Symbol: TRDGRD1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1

Bits 15 to 0

Register	Function	PWM output pin
TRDBFD1 = 1	Buffer register. Set the changing point of next PWM output	TRDIOB1

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Set timer RD port register.

- Port Register (P1)
Set output data to 0.
- Port Mode Register (PM1)
Set to output mode.
- Port Output Mode Register (POM1)
Set output mode of pins POM15 and POM10 to normal output mode.

Symbol: P1

7	6	5	4	3	2	1	0
P17	P16	P15	P14	P13	P12	P11	P10
x	0	0	0	0	0	0	0

Bits 6 to 0

P1n	Output data control (n = 0-6)
0	Output 0
1	Output 1

Symbol: PM1

7	6	5	4	3	2	1	0
PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10
x	0	0	0	0	0	0	0

Bits 6 to 0

PM1n	P1n pin I/O mode selection (n = 0-6)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Symbol: POM1

7	6	5	4	3	2	1	0
POM17	0	POM15	0	0	0	0	POM10
x	0	0	0	0	0	0	0

Bit 5

POM 15	P15 pin I/O mode selection
0	Normal output mode
1	N-ch open-drain output (VDD tolerance) mode

Bit 0

POM 10	P15 pin I/O mode selection
0	Normal output mode
1	N-ch open-drain output (VDD tolerance) mode

4.7.6 Initial Setting of Comparator and PGA

Figure 4.20 and 21 shows the flowchart for the initial setting of the comparator and PGA.

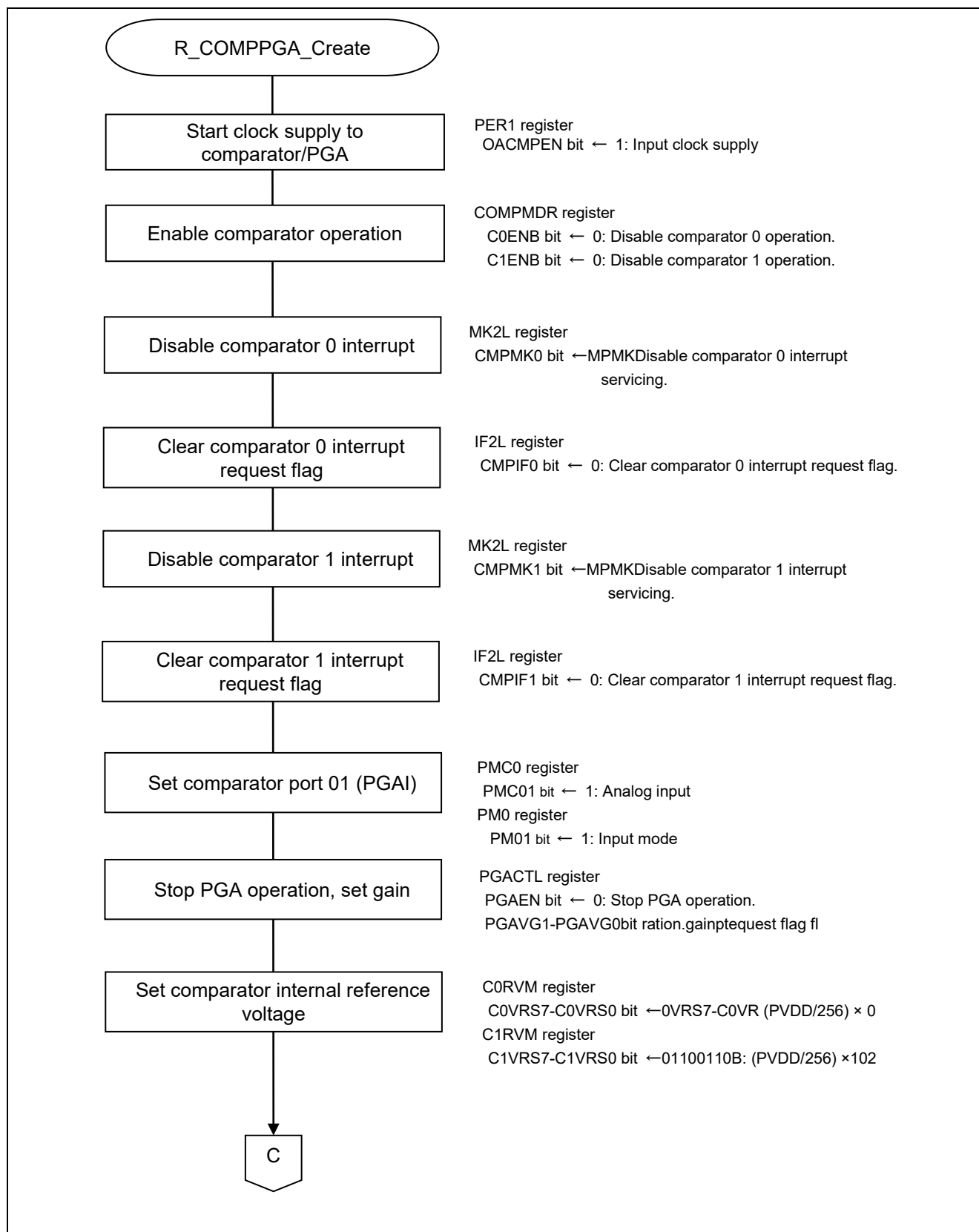


Figure 4.20 Initial Setting of Comparator/PGA (1/2)

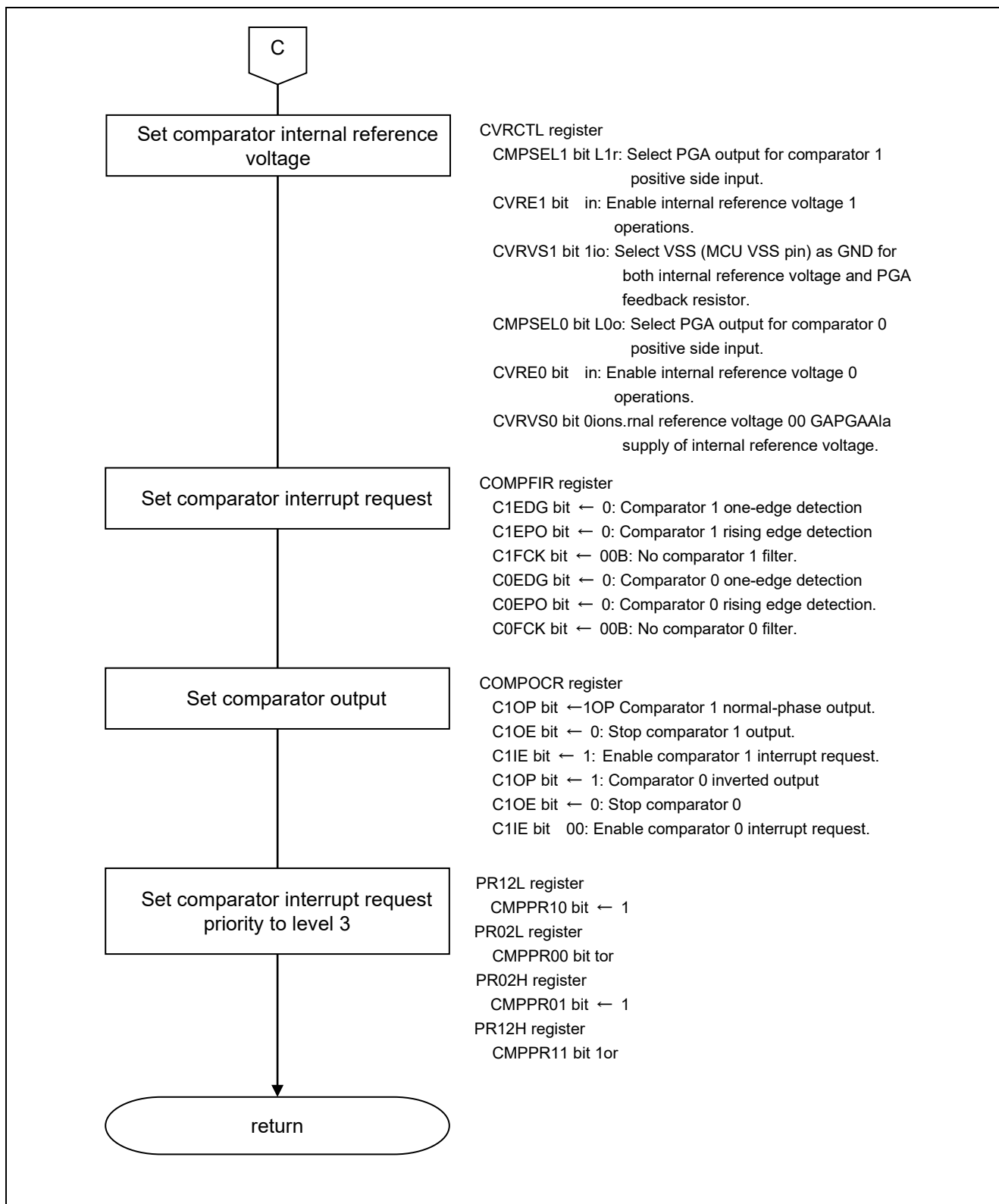


Figure 4.21 Initialization of Comparator/PGA (2/2)

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Start clock supply to Comparator/PGA.

- Peripheral Enable Register 1 (PER1)

Start clock supply to comparator and PGA

Symbol: PER1

7	6	5	4	3	2	1	0
TMKAEN	PWMOPEN	OACMPEN	TRD0EN	0	0	0	TRJ0EN
x	x	1	x	x	x	x	x

Bit 5

OACMPEN	Control of input clock supply for comparators 0 and 1 and programmable gain amp
0	Stops input clock supply.
1	Enables input clock supply

Enable comparator operations.

- Comparator Mode Setting Register (COMPMDR)

Enable operations of comparators 0 and 1.

Symbol: COMPMDR

7	6	5	4	3	2	1	0
C1MON	0	0	C1ENB	C0MON	0	0	C0ENB
x	0	0	0	x	0	0	0

Bit 4

C1ENB	Comparator 1 operation enable
0	Comparator 1 operation disabled
1	Comparator 1 operation enabled

Bit 0

C0ENB	Comparator 0 operation enable
0	Comparator 0 operation disabled
1	Comparator 0 operation enabled

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Set comparator interrupts.

- Interrupt Mask Flag Register (MK2L, MK2H)
Disable comparator 0 and 1 interrupts.
- Interrupt Request Flag Register (IF2L, IF2H)
Clear comparator 0 and 1 interrupt request flags.

Symbol: MK2L

7	6	5	4	3	2	1	0
CMPMK0	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1

Bit 7

CMPMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Symbol: MK2H

7	6	5	4	3	2	1	0
FLMK	1	1	1	1	TRDMK1	TRDMK0	CMPMK1
x	1	1	1	1	x	x	1

Bit 0

CMPMK1	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Symbol: IF2L

7	6	5	4	3	2	1	0
CMPIF0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

Bit 7

CMPIF0	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Symbol: IF2H

7	6	5	4	3	2	1	0
FLIF	0	0	0	0	TRDIF1	TRDIF0	CMPIF1
x	0	0	0	0	x	x	0

Bit 0

CMPIF1	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Set comparator port and register

- Port Register ((PMC0)
Set ports to analog input.
- Port Mode Register (PM0)
Set ports to input mode.

Symbol: PMC0

7	6	5	4	3	2	1	0
1	1	1	1	1	1	PMC01	PMC00
1	1	1	1	1	1	1	x

Bit 1

PMC01	P01 pin digital I/O/analog input selection
0	Digital I/O (alternate function other than analog input)
1	Analog input

Symbol: PM0

7	6	5	4	3	2	1	0
1	1	1	1	1	1	PM01	PM00
1	1	1	1	1	1	1	x

Bit 1

PM01	P01 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Set PGA controls (enable, stop, amplification factor)

- PGA Control Register (PGACTL)
Stop PGA operation.
Set gain to x8.

Symbol: PGACTL

7	6	5	4	3	2	1	0
PGAEN	0	0	0	0	0	PGAVG1	PGAVG0
0	0	0	0	0	0	0	1

Bit 7

PGAEN	Function
0	PGA operation stopped
1	PGA operation enabled

Bits1 and 0

PGAVG1	PGAVG0	Function
0	0	x 4 selected as gain
0	1	x 8 selected as gain
1	0	x 16 selected as gain
1	1	x 32 selected as gain

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Set comparator internal reference voltage

- Comparator Internal Reference Voltage Select Register 0 (C0RVM)
Set comparator 0 to 0.
- Comparator Internal Reference Voltage Select Register 1 (C1RVM)
Set comparator 0 to 102.

Symbol: C0RVM

7	6	5	4	3	2	1	0
C0VRS7	C0VRS6	C0VRS5	C0VRS4	C0VRS3	C0VRS2	C0VRS1	C0VRS0
0	0	0	0	0	0	0	0

Bits 7 to 0

C0VRS7 – C0VRS0	Comparator 0 internal reference voltage selection
00000000	{{(AVREFP or PVDD)/256} x 0
00000001	{{(AVREFP or PVDD)/256} x 1
.	.
11111110	{{(AVREFP or PVDD)/256} x 254
11111111	{{(AVREFP or PVDD)/256} x 255

Symbol: C1RVM

7	6	5	4	3	2	1	0
C1VRS7	C1VRS6	C1VRS5	C1VRS4	C1VRS3	C1VRS2	C1VRS1	C1VRS0
0	1	1	0	0	1	1	0

Bits 7 to 0

C1VRS7 – C1VRS0	Comparator 1 internal reference voltage selection
00000000	{{(AVREFP or PVDD)/256} x 0
00000001	{{(AVREFP or PVDD)/256} x 1
.	.
01100110	{{(AVREFP or PVDD)/256} x 102
.	.
11111110	{{(AVREFP or PVDD)/256} x 254
11111111	{{(AVREFP or PVDD)/256} x 255

Set comparator internal reference voltage controls

- Comparator Internal Reference Voltage Control Register (CVRCTL)

Set positive side of comparators 10 and 1 to PGA.

Enable operations for internal reference voltage 0 and 1.

Set GND to VSS.

Set internal reference voltage to PVDD.

Symbol: CVRCTL

7	6	5	4	3	2	1	0
0	CMPSEL1	CVRE1	CVRVS1	0	CMPSEL0	CVRE0	CVRVS0
0	1	1	0	0	1	1	0

Bit 6

CMPSEL1	Function
0	CPM1P pin is selected as positive-side input for comparator 1
1	Select PGA output as positive-side input for comparator 1

Bit 5

CVRE1	Function
0	Operation of internal reference voltage 1 stopped
1	Operation of internal reference voltage 1 enabled

Bit 4

CVRVS1	Function
0	VSS is selected as the GND of both internal reference voltage and PGA feedback resistor
1	AVREFM is selected as the GND of both internal reference voltage and PGA feedback resistor

Bit 2

CMPSEL0	Function
0	CMP0PI pin is selected as the positive-side input of comparator 0
1	PGA output is selected as the positive-side input of comparator 0

Bit 1

CVRE0	Function
0	Operation of internal reference voltage 0 stopped
1	Operation of internal reference voltage 0 enabled

Bit 0

CVRVS0	Function
0	PVDD (VDD pin in MCU) is selected as the power supply of the internal reference voltage
1	AVREFP is selected as the power supply of the internal reference voltage

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Set comparator interrupt request

- Comparator Filter Control Register (COMPFIR)
Set to one-edge (rising) detection.
Set to no filter.

Symbol: COMPFIR

7	6	5	4	3	2	1	0
C1EDG	C1EPO	C1FCK		C0EDG	C0EPO	C0FCK	
0	0	0	0	0	0	0	0

Bit 7

C1EDG	Comparator 1 edge detection selection
0	Interrupt request by comparator 1 one-edge detection
1	Interrupt request by comparator 1 both-edge detection

Bit 6

C1EPO	Comparator 1 edge polarity switching
0	Interrupt request at comparator 1 rising edge
1	Interrupt request at comparator 1 falling edge

Bits 5 to 4

C1FCK		Comparator 1 filter selection
0	0	No comparator 1 filter
0	1	Comparator 1 filter enabled, sampling at fCLK
1	0	Comparator 1 filter enabled, sampling at fCLK/8
1	1	Comparator 1 filter enabled, sampling at fCLK/32

Bit 3

C0EDG	Comparator 0 edge detection selection
0	Interrupt request by comparator 0 one-edge detection
1	Interrupt request by comparator 0 both-edge detection

Bit 2

C0EPO	Comparator 0 edge polarity switching
0	Interrupt request at comparator 0 rising edge
1	Interrupt request at comparator 0 falling edge

Bits 1 to 0

C0FCK		Comparator 0 filter selection
0	0	No comparator 0 filter
0	1	Comparator 0 filter enabled, sampling at fCLK
1	0	Comparator 0 filter enabled, sampling at fCLK/8
1	1	Comparator 0 filter enabled, sampling at fCLK/32

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Set comparator interrupt request.

- Comparator Output Control Register (COMPOCR)
Set comparator 0 output to inverted output, comparator 1 output to normal output.
Stop output of comparators 0 and 1.
Enable interrupts for comparator 0 and 1.

Symbol: COMPOCR

7	6	5	4	3	2	1	0
0	C1OP	C1OE	C1IE	0	C0OP	C0OE	C0IE
0	0	0	1	0	1	0	1

Bit 6

C1OP	Comparator 1 output polarity selection
0	Comparator 1 output is non-inverted output
1	Comparator 1 output is inverted output

Bit 5

C1OE	Comparator 1 output enable
0	Comparator 1 output stopped (CMP1HZO output fixed at low level)
1	Comparator 1 output enabled (CMP1HZO output enabled)

Bit 4

C1IE	Comparator 1 interrupt request enable
0	Comparator 1 interrupt request disabled
1	Comparator 1 interrupt request enabled

Bit 2

C0OP	Comparator 0 output polarity selection
0	Comparator 0 output is non-inverted output
1	Comparator 0 output is inverted output

Bit 1

C0OE	Comparator 0 output enable
0	Comparator 0 output stopped (CMP0HZO output fixed at low level)
1	Comparator 0 output enabled (CMP0HZO output enabled)

Bit 0

C0IE	Comparator 0 interrupt request enable
0	Comparator 0 interrupt request disabled
1	Comparator 0 interrupt request enabled

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Set comparator interrupt priority levels

- Priority Specification Flag Register (PR12L, PR02L, PR12H, PR02H)
Set to level 3 (low priority level).

Symbol: PR12L

	7	6	5	4	3	2	1	0
CMPPR10	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1

Symbol: PR02L

	7	6	5	4	3	2	1	0
CMPPR00	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1

Bit 7

CMPPR10	CMPPR00	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	1	Specify level 3 (low priority level)

Symbol: PR12H

7	6	5	4	3	2	1	0
FLPR1	1	1	1	1	TRDPR11	TRDPR10	CMPPR1
x	1	1	1	1	x	x	1

Symbol: PR02H

7	6	5	4	3	2	1	0
FLPR0	1	1	1	1	TRDPR01	TRDPR00	CMPPR01
x	1	1	1	1	x	x	1

Bit 0

CMPPR11	CMPPR01	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	1	Specify level 3 (low priority level)

4.7.7 Main Processing

Figure 4.22 shows the flowchart for main processing.

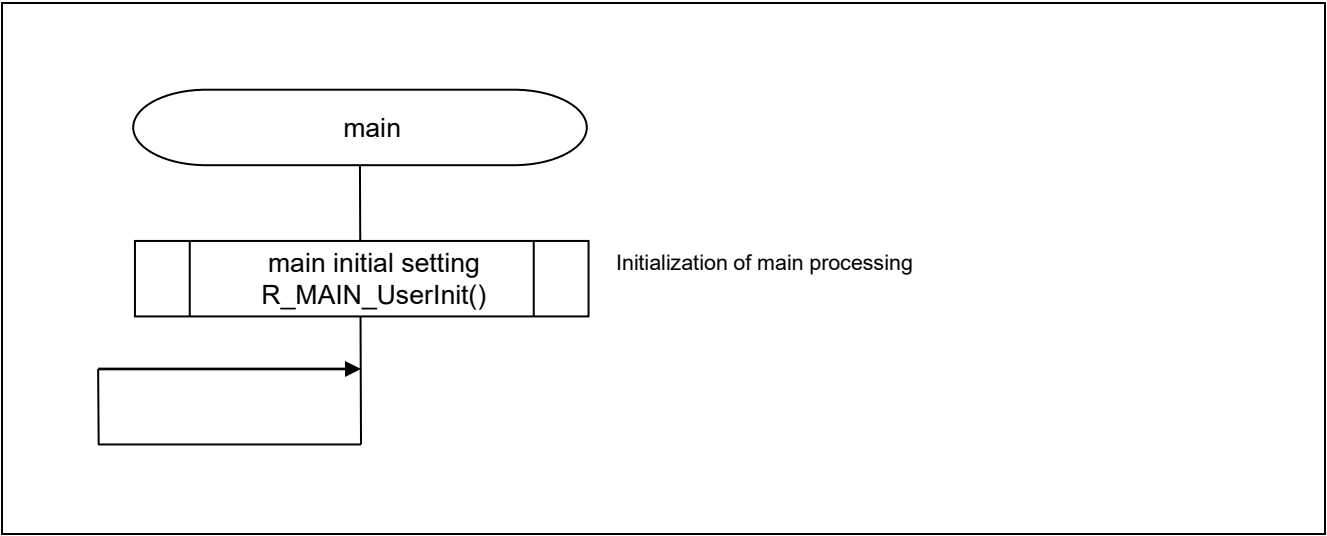


Figure 4.22 Main Processing

4.7.8 Initialization of Main Function

Figure 4.23 shows the flowchart for the initialization of main function.

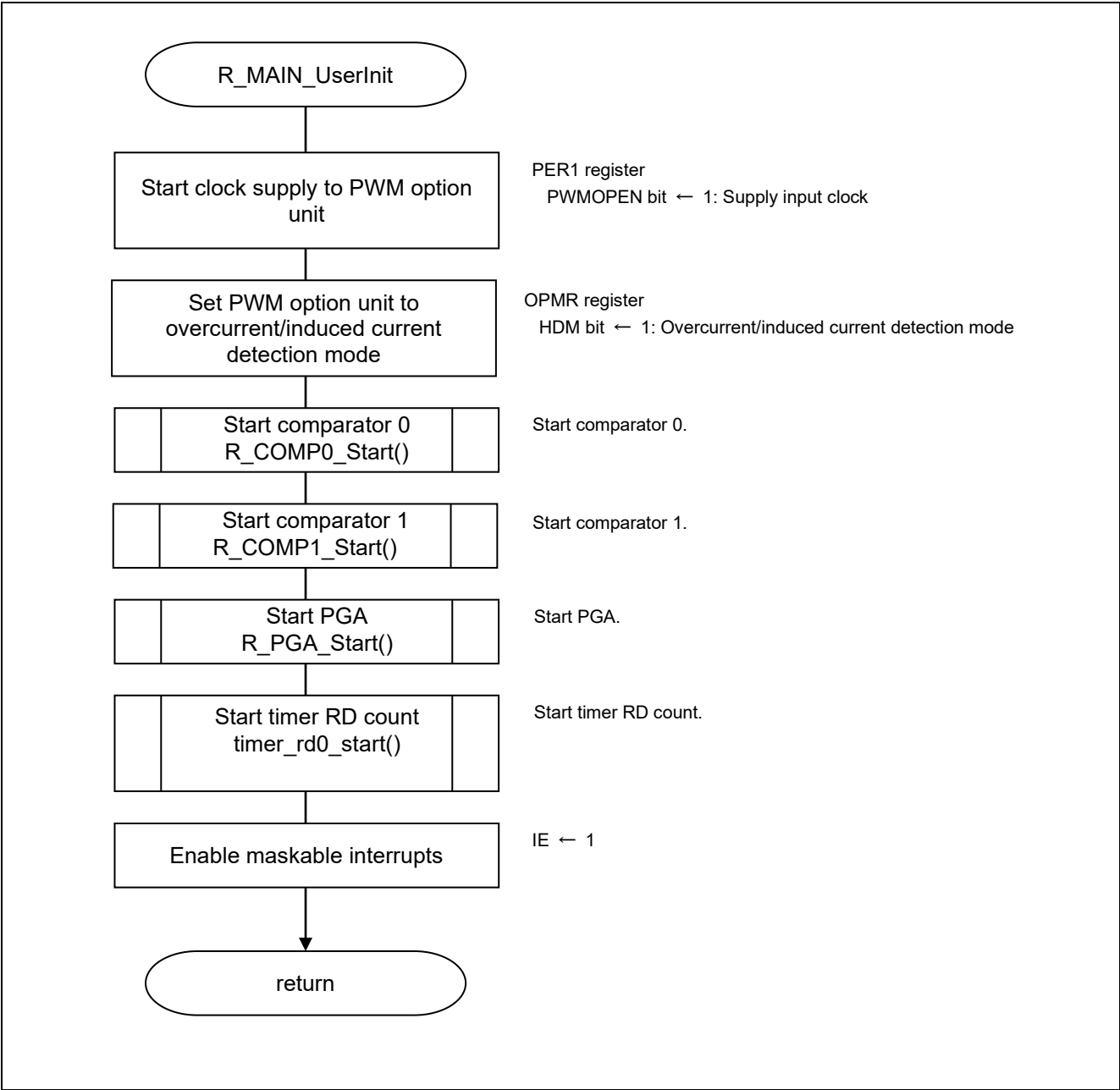


Figure 4.23 Initialization of Main Function

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Start PWM option unit clock supply

- Peripheral Enable Register 1 (PER1)

Start clock supply to PWM option unit.

Symbol: PER1

7	6	5	4	3	2	1	0
TMKAEN	PWMOPEN	OACMPEN	TRD0EN	0	0	0	TRJ0EN
x	1	x	x	0	0	0	x

Bit 6

PWMOPEN	Control of PWM option unit input clock supply
0	Stops input clock supply.
1	Enables input clock supply

Set PWM option unit overcurrent/induced current detection mode

- 6-phase PWM Option Mode Register (OPMR)

Set PWM unit to overcurrent/induced current detection mode.

Symbol: OPMR

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HDM	0
0	0	0	0	0	0	1	0

Bit 1

HDM	PWM option operating mode
0	Two-stage overcurrent detection mode
1	Overcurrent/induced current detection mode

4.7.9 Comparator 0 Startup

Figure 4.24 shows the flowchart for comparator 0 operations.

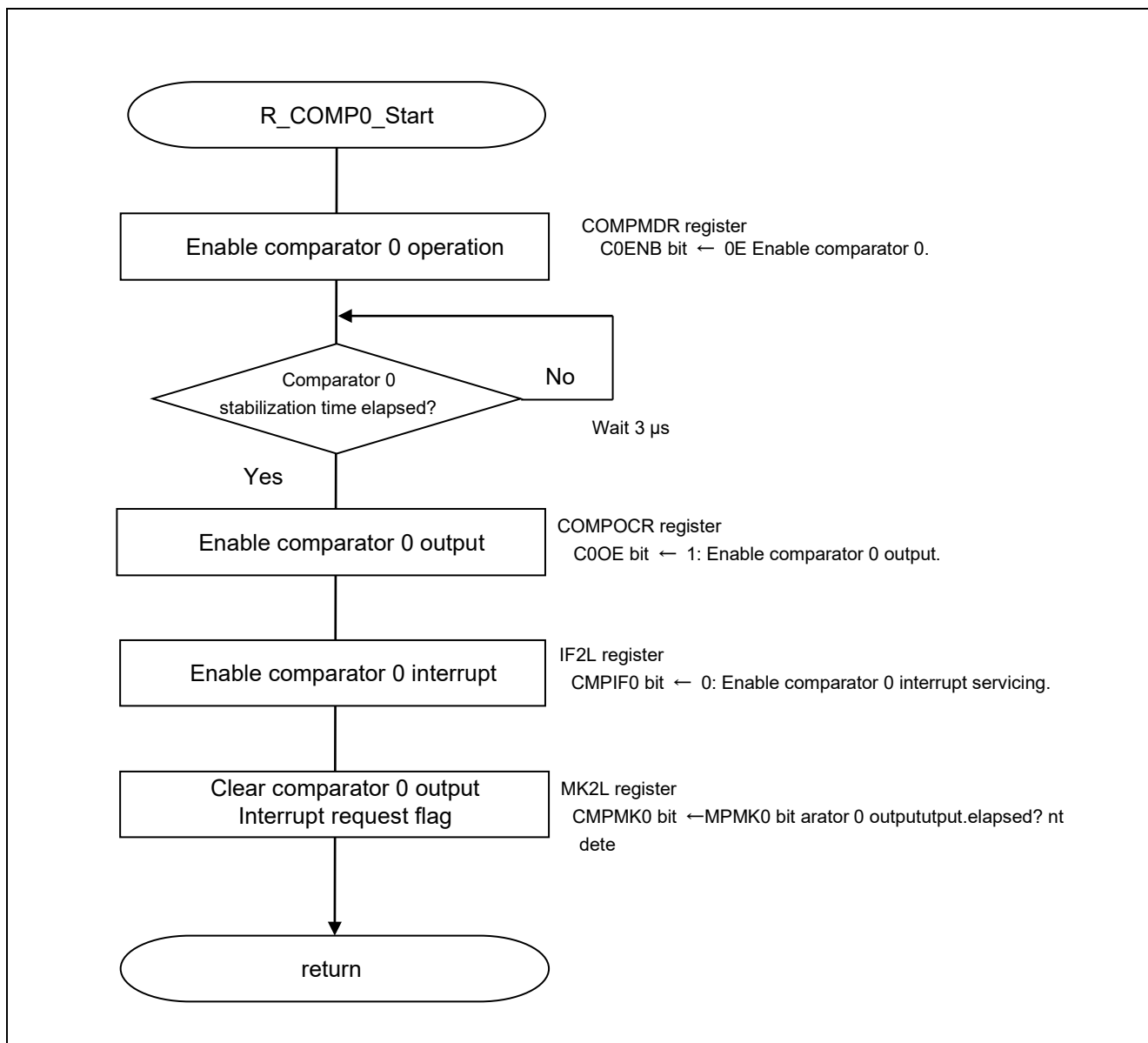


Figure 4.24 Comparator 0 Startup

Enable comparator operations.

- Comparator Mode Setting Register (COMPMDR)
Enable comparator 0 operations.

Symbol: COMPMDR

7	6	5	4	3	2	1	0
C1MON	0	0	C1ENB	C0MON	0	0	C0ENB
x	0	0	x	x	0	0	1

Bit 0

C0ENB	Comparator 0 operation enable
0	Comparator 0 operation disabled
1	Comparator 0 operation enabled

Enable comparator operations.

- Comparator Output Control Register (COMPOCR)
Enable comparator 0 operations.

Symbol: COMPOCR

7	6	5	4	3	2	1	0
0	C1OP	C1OE	C1IE	0	C0OP	C0OE	C0IE
0	x	x	x	0	x	1	x

Bit 1

C0OE	Comparator 0 output enable
0	Comparator 0 output stopped (CMP0HZO output fixed at low level)
1	Comparator 0 output enabled (CMP0HZO output enabled)

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Set comparator interrupts.

- Interrupt Request Flag Register (MK2L)
Enable comparator 0 interrupt.
- Interrupt Request Flag Register (IF2L)
Clear comparator 0 interrupt request flag.

Symbol: MK2L

	7	6	5	4	3	2	1	0
CMPMK0		1	1	1	1	1	1	1
0		1	1	1	1	1	1	1

Bit 7

CMPMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Symbol: IF2L

	7	6	5	4	3	2	1	0
CMPIF0		0	0	0	0	0	0	0
0		0	0	0	0	0	0	0

Bit 7

CMPIF0	Interrupt request flag
0	Interrupt request signal is not generated
1	Interrupt request is generated, interrupt request status

4.7.10 Comparator 1 startup

Figure 4.25 shows the flowchart for comparator 1 startup.

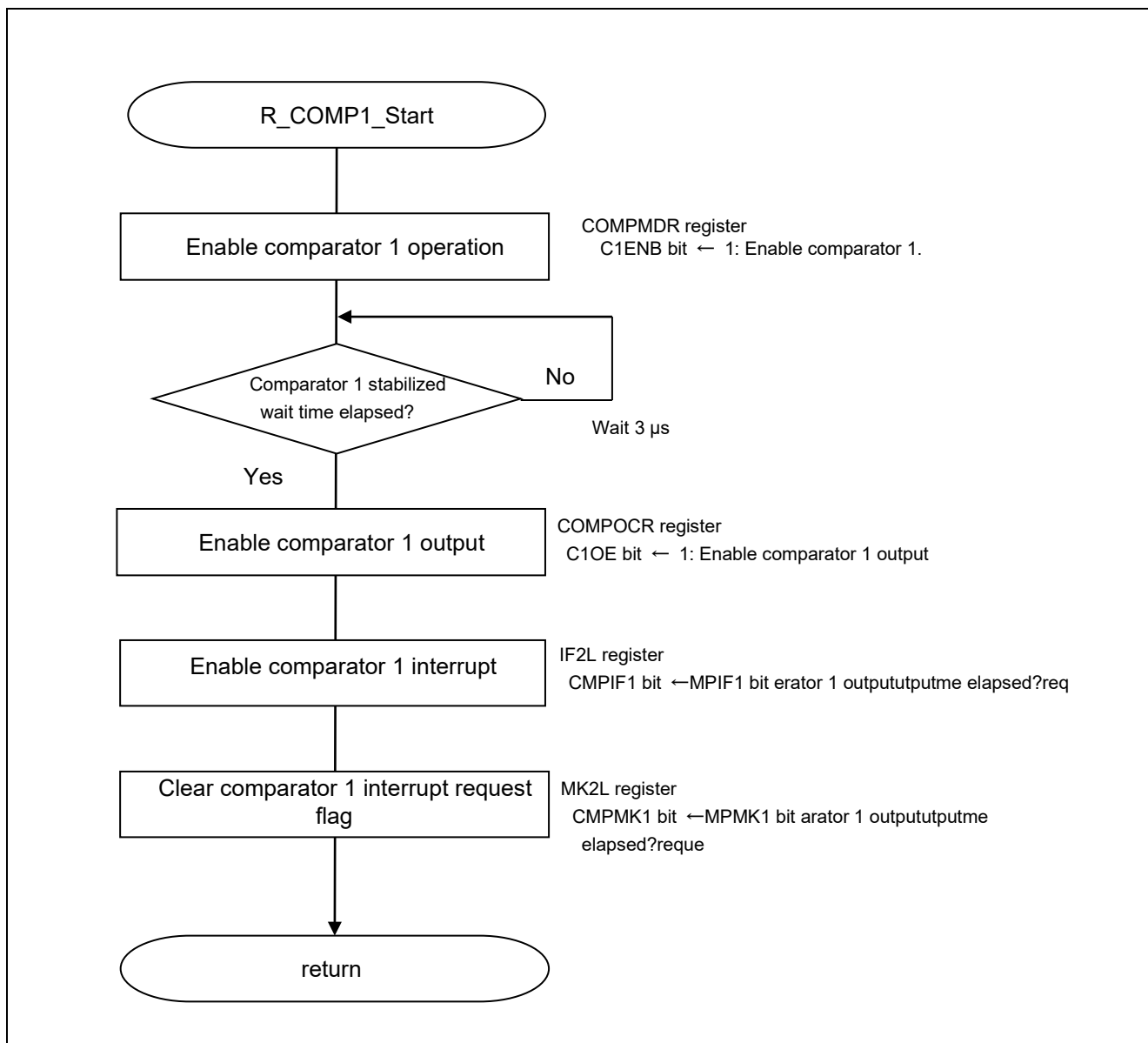


Figure 4.25 Comparator 1 Startup

Enable comparator operation.

- Comparator Mode Setting Register (COMPMDR)

Enable comparator 1 operation.

Symbol: COMPMDR

7	6	5	4	3	2	1	0
C1MON	0	0	C1ENB	C0MON	0	0	C0ENB
x	0	0	1	x	0	0	x

Bit 4

C1ENB	Comparator 1 operation enable
0	Comparator 1 operation disabled
1	Comparator 1 operation enabled

Enable comparator operation.

- Comparator Output Control Register (COMPOCR)

Enable comparator 1 operation.

Symbol: COMPOCR

7	6	5	4	3	2	1	0
0	C1OP	C1OE	C1IE	0	C0OP	C0OE	C0IE
0	x	1	x	0	x	x	x

Bit 4

C1OE	Comparator 1 output enable
0	Comparator 1 output stopped (CMP1HZO output fixed at low level)
1	Comparator 1 output enabled (CMP1HZO output enabled)

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Set comparator interrupts.

- Interrupt Mask Flag Register (MK2H)
Enable comparator 1 interrupt.
- Interrupt Request Flag Register (IF2H)
Clear comparator 1 interrupt request flag.

Symbol: MK2H

7	6	5	4	3	2	1	0
FLMK	1	1	1	1	TRDMK1	TRDMK0	CMPMK1
x	1	1	1	1	x	x	0

Bit 0

CMPMK1	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Symbol: IF2H

7	6	5	4	3	2	1	0
FLIF	0	0	0	0	TRDIF1	TRDIF0	CMPIF1
x	0	0	0	0	x	x	0

Bit 0

CMPIF1	Interrupt servicing flag
0	Interrupt request signal not generated
1	Interrupt request is generated, interrupt request status

4.7.11 PGA Startup

Figure 4.26 shows the flowchart for PGA startup.

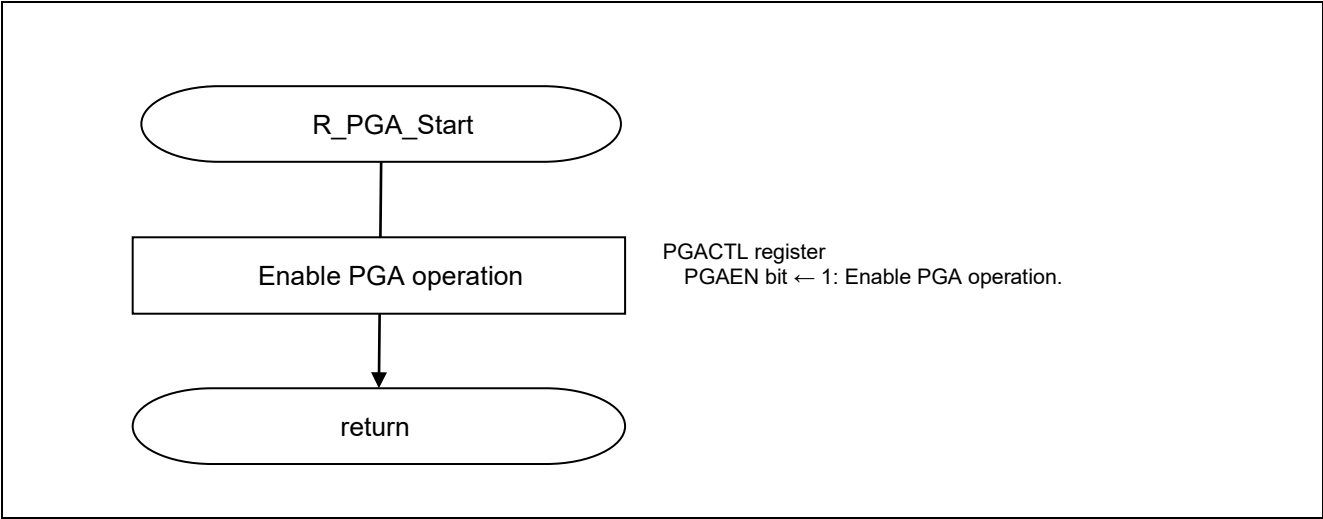


Figure 4.26 PGA Startup

Enable PGA operation.

- PGA Control Register (PGACTL)
Enable PGA operation.

Symbol: PGACTL

7	6	5	4	3	2	1	0
PGAEN	0	0	0	0	0	PGAVG1	PGAVG0
1	0	0	0	0	0	x	x

Bit 7

PGAEN	Function
0	PGA operation stopped
1	PGA operation enabled

4.7.12 Timer RD Count Start Setting

Figure 4.27 shows the flowchart for the Timer RD Count Start Setting.

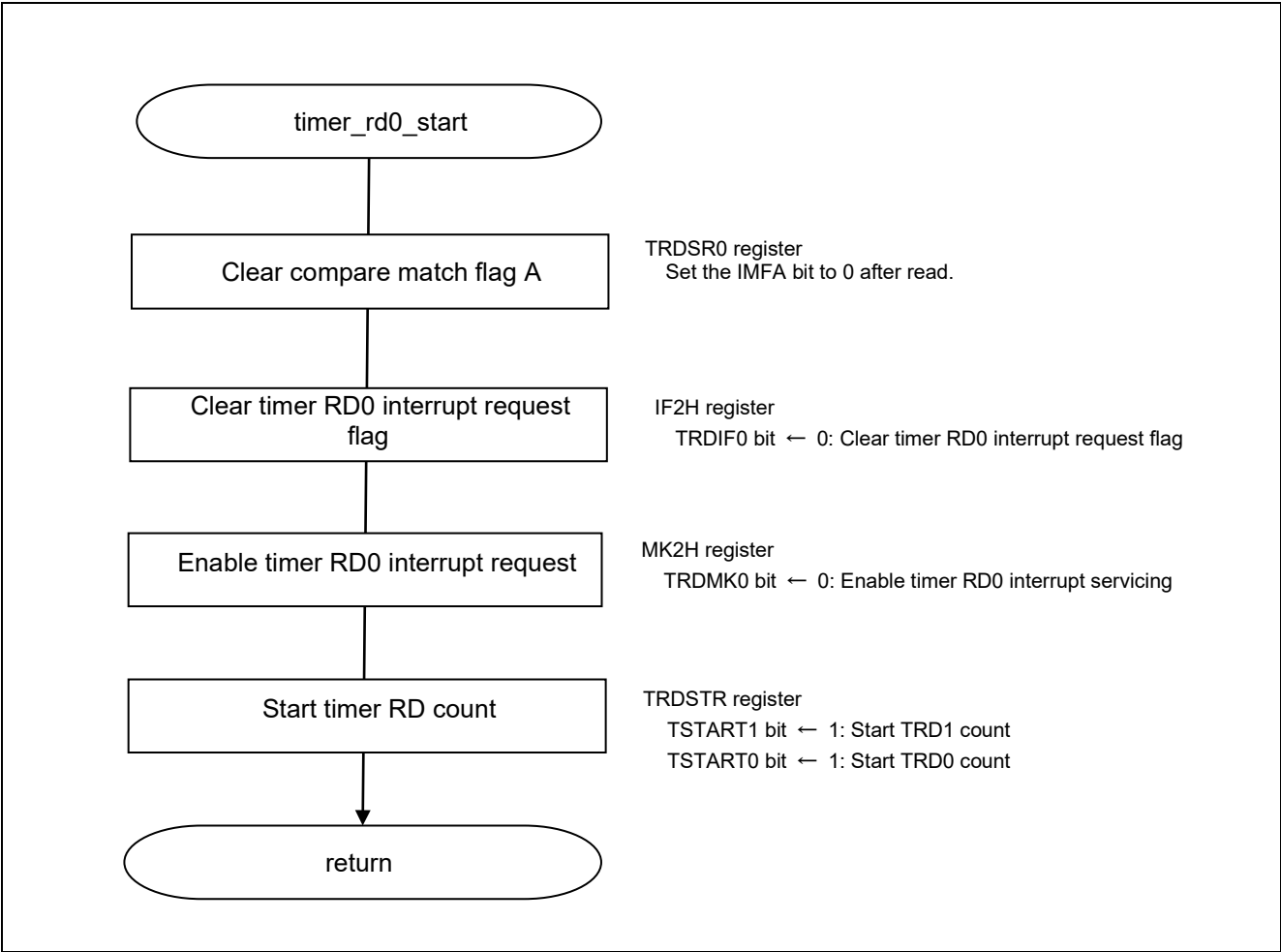


Figure 4.27 Timer RD Count Start Setting

RL78/G1G Timer RD in Complementary PWM Mode and Using PWM Option Unit to Forcibly Cut Off PWM Output

Clear compare match flag A.

- Timer RD Status Register 0 (TRDSR0)
Enable PGA operation.

Symbol: TRDSR0

7	6	5	4	3	2	1	0
0	0	0	OVF	IMFD	IMFC	IMFB	IMFA
0	0	0	x	x	x	x	0

Bit 0

IMFA	Input capture/compare match flag A
[Source for setting to 0] Write 0 after reading. [Source for setting to 1] TRDIOA0 pin input edge	

Set timer RD interrupt.

- Interrupt Mask Flag Register (MK2H)
Enable timer RD0 interrupt.
- Interrupt Request Flag Register (IF2H)
Clear timer RD0 interrupt request flag.

Symbol: MK2H

7	6	5	4	3	2	1	0
FLMK	1	1	1	1	TRDMK1	TRDMK0	CMPMK1
x	1	1	1	1	x	0	x

Bit 1

TRDMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Symbol: IF2H

7	6	5	4	3	2	1	0
FLIF	0	0	0	0	TRDIF1	TRDIF0	CMPIF1
x	0	0	0	0	x	0	x

Bit 1

TRDIF0	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Start timer RD count.

- Interrupt Request Flag Register (TRDSTR)
Start timer RD0 and RD1 counts.

Symbol: TRDSTR

7	6	5	4	3	2	1	0
0	0	0	0	CSEL1	CSEL0	TSTART1	TSTART0
0	0	0	0	x	x	1	1

Bit 1

TSTART1	TRD1 count start flag
0	Count stopped
1	Count started

Bit 0

TSTART0	TRD0 count start flag
0	Count stopped
1	Count started

4.7.13 Timer RD Interrupt

Figure 4.28 and 4.29 show the flowchart for timer RD interrupt.

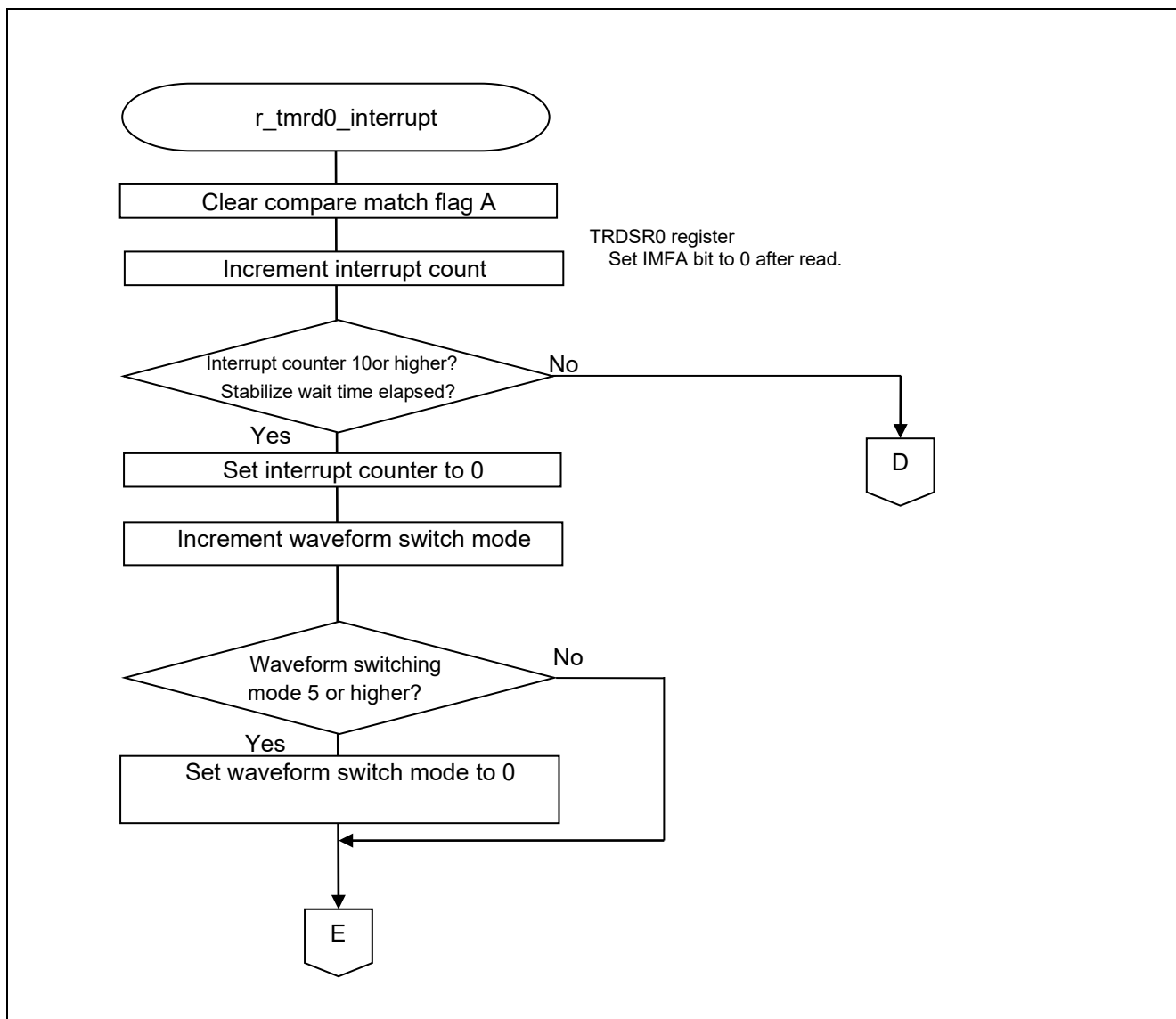


Figure 4.28 Timer RD Interrupt (1/2)

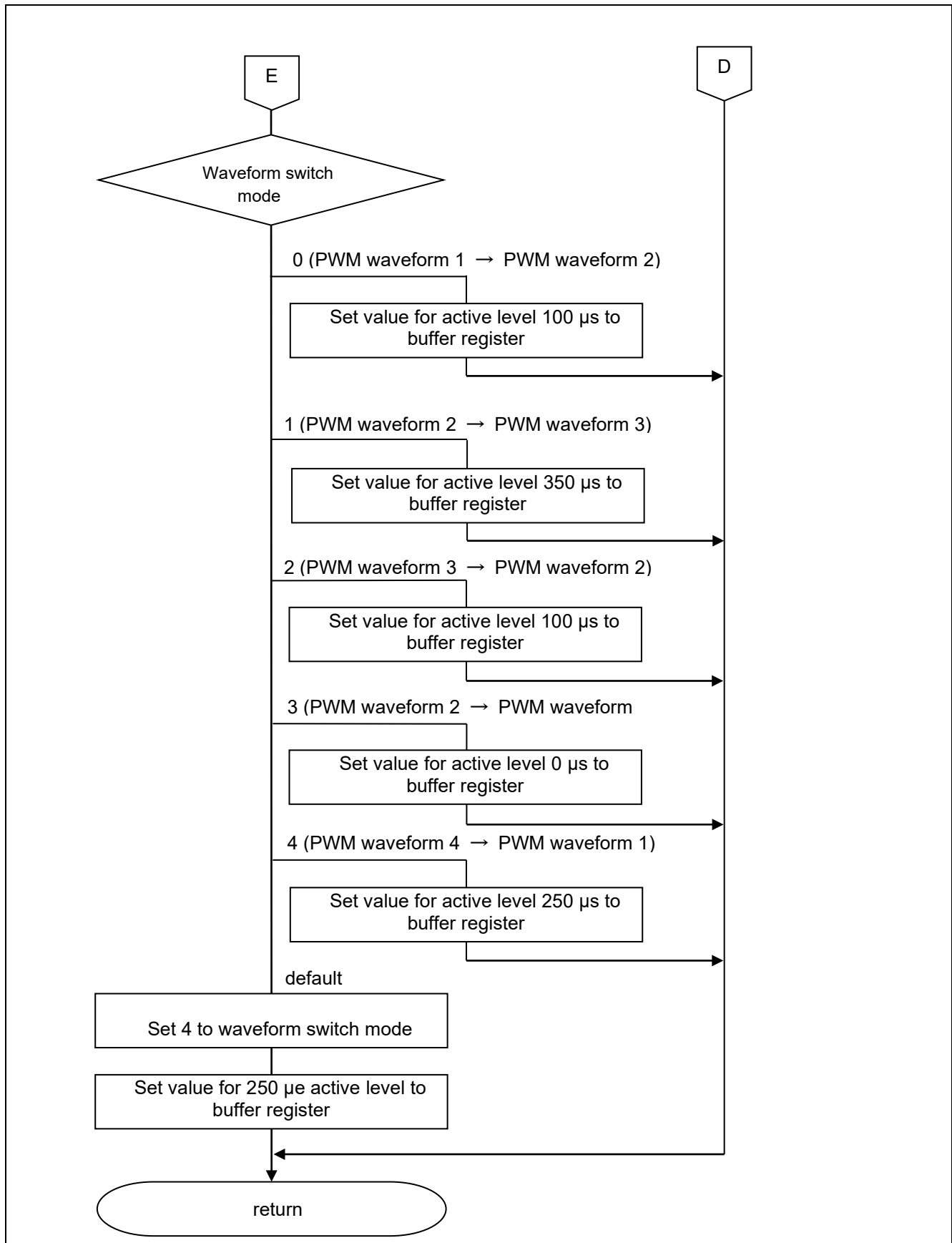


Figure 4.29 Timer RD Interrupt (2/2)

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

User's Manual Hardware

RL78/G1G User's Manual: Hardware Rev.1.10 (R01UH0499J)

RL78 Family User's Manual: Software Rev.1.00 (R01US0015J)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jan. 26, 2015	—	First edition issued
1.10	Sep. 12. 2022	7	Updated operation check conditions

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

- **1. Precaution against Electrostatic Discharge (ESD)**

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
- **2. Processing at power-on**

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
- **3. Input of signal during power-off state**

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
- **4. Handling of unused pins**

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
- **5. Clock signals**

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
- **6. Voltage application waveform at input pin**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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