

RL78/G22

A/D Converter (Software Trigger and Sequential Conversion Modes)

Introduction

This application note describes how to convert an analog voltage to a digital voltage with the RL78/G22 A/D converter (supporting software trigger and sequential conversion modes).

It also describes how A/D conversion results are converted to data and the converted values are stored in the on-chip RAM.

Target Device

RL78/G22

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

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1. Specifications

1.1 Overview of Specifications

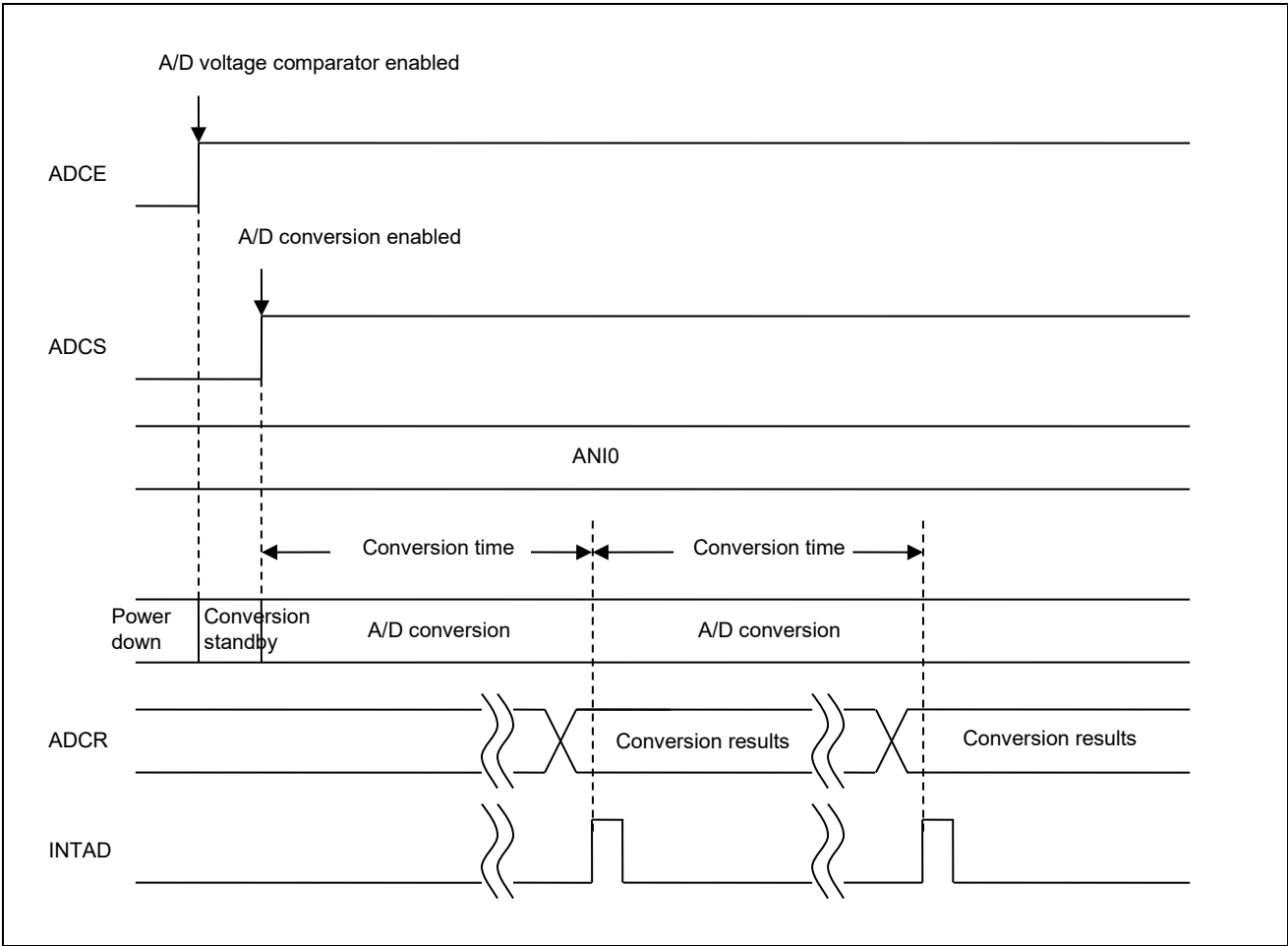
This application note shows an example of the use of the A/D converter in select mode and sequential conversion mode. The A/D converter is set to select mode and analog input signal level of the P20 / ANI0 pin are converted to digital values. Then the A/D conversion results are converted to data and the converted values are stored in the on-chip RAM.

Table 1-1 shows the peripheral function and use. Figure 1-1 shows conversion operation of the A/D converter.

Table 1-1 Peripheral Function and Use

Peripheral Function	Use
A/D converter	Converts analog input signal levels of the P20 / ANI0 pin.

Figure 1-1 Outline of the A/D Converter Conversion Processing



1.2 Outline of Operation

This sample code performs A/D conversion on the analog voltage that is input to pin ANI0 using the software trigger and sequential conversion modes of the A/D converter. In HALT mode, completion of A/D conversion is waited for. Upon completion of A/D conversion, the A/D conversion results are converted to data and the converted values are stored in the on-chip RAM.

The following describes the main settings.

(1) Initial settings for the A/D converter

Make initial settings as shown in Table 1-2.

Table 1-2 A/D Converter Initial Setting Conditions

Register Name	Setting Value	Content
ADM0	20H	Conversion time setting Conversion time mode: Normal 1 Conversion time: $114/f_{CLK}$ (3.5625 μ s) A/D conversion channel selection mode: Select mode
ADM1	00H	A/D conversion mode: Sequential conversion mode A/D conversion trigger mode: Software trigger mode
ADM2	00H	A/D conversion resolution: 10-bit resolution Reference voltage source setting $V_{REF}(+)$: V_{DD} $V_{REF}(-)$: V_{SS}
ADUL	FFH	Conversion result comparison upper limit: FFH
ADLL	00H	Conversion result comparison lower limit: 00H
PMCA2	01H	Set ANI0 to analog input function
PM2	01H	Set ANI0 to input
ADS	00H	Analog input channel: ANI0
-	-	Use the A/D conversion end interrupt request signal (INTAD).

(2) Main processing

- The sample program sets the ADCS bit of the ADM0 register to 1 (A/D conversion start) to start A/D conversion and executes the HALT instruction to place the chip in the HALT mode and wait for an A/D conversion end interrupt.
- After completing the A/D conversion of the voltage input from pin ANI0, the A/D converter transfers the result of A/D conversion to the ADCR register and generates an A/D conversion end interrupt.
- On release from the HALT mode in response to the A/D conversion end interrupt, the sample program reads the result of A/D conversion from the ADCR register, shifts the result 6 bits to the right, and stores the shifted data in the internal RAM of the RL78/G13.
- The chip returns to the HALT mode and waits for an A/D conversion end interrupt.

2. Operation Confirmation Conditions

The operation of the sample code provided with this application note has been tested under the following conditions.

Table 2-1 Operation Confirmation Conditions

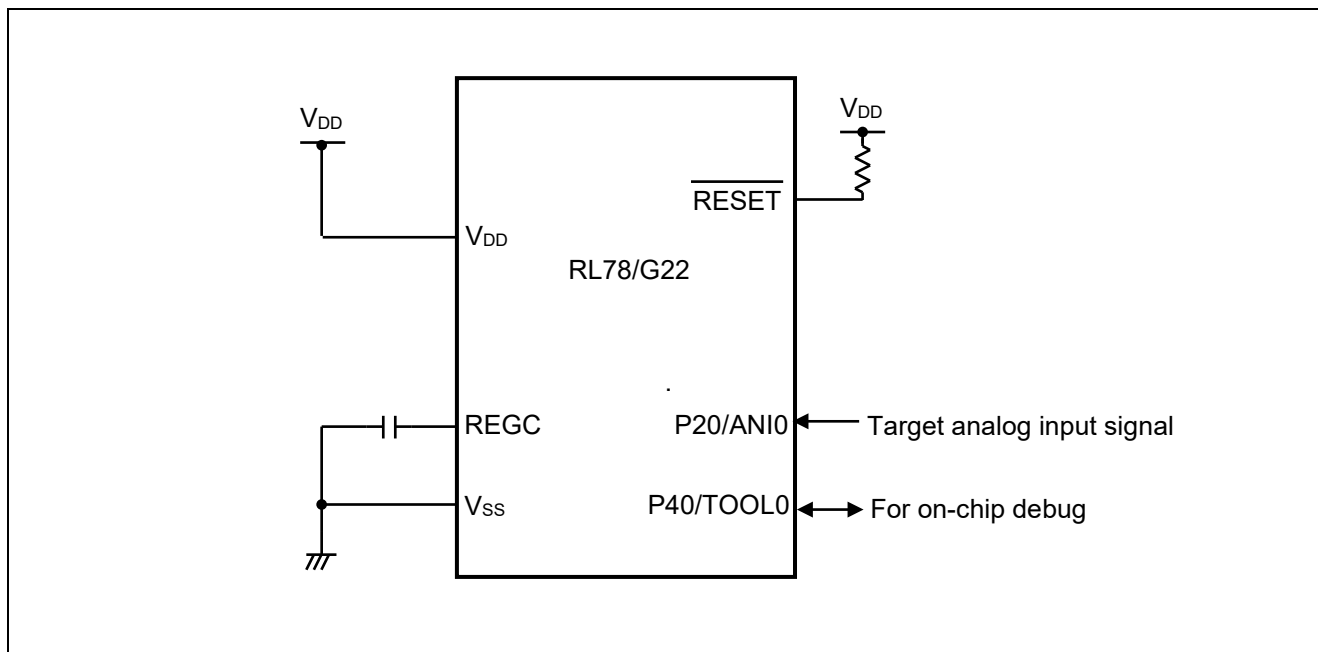
Item	Description
MCU used	RL78/G22 (R7F100GLG)
Board used	RL78/G22-48p Fast Prototyping Board (RTK7RLG220CLG000BJ)
Operating frequency	- High-speed on-chip oscillator clock (f_{IH}): 32 MHz - CPU/peripheral hardware clock: 32 MHz
Operating voltage	3.3 V (can be operated at 2.7 V to 5.5 V) LVD0 operations (V_{LVD0}): Reset mode At rising edge TYP. 2.970 V (2.88 V to 3.06 V) At falling edge TYP. 2.910 V (2.82 V to 3.00 V)
Integrated development environment (CS+)	CS+ for CC E8.10.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.12.01 from Renesas Electronics Corp.
Integrated development environment (e2studio)	e2studio V2023-01 (23.1.0) from Renesas Electronics Corp.
C compiler (e2studio)	CC-RL V1.12.01 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V5. 10. 1 from IAR Systems Corp.
C compiler (IAR)	IAR C/C++ Compiler for Renesas RL78 V5.10.1.2673 from IAR Systems Corp.
Smart configurator (SC)	V1.5.0 from Renesas Electronics Corp.
Board support package (BSP)	V1.40 from Renesas Electronics Corp.

3. Hardware Descriptions

3.1 Example of Hardware Configuration

Figure 3-1 shows an example of the hardware configuration used in the application note.

Figure 3-1 Hardware Configuration



Note 1. This simplified circuit diagram was created to show an overview of connections only. When actually designing your circuit, make sure the design includes appropriate pin handling and meets electrical characteristic requirements (connect each input-only port to V_{DD} or V_{SS} through a resistor).

Note 2. V_{DD} must not be lower than the reset release voltage (V_{LVD0}) that is specified for the LVD0.

3.2 List of Pins to be Used

Table 3-1 lists the pins to be used and their functions.

Table 3-1 Pins to be Used and Their Functions

Pin name	I/O	Function
P20 / ANI0	Input	A/D converter analog input port

Caution In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

4. Software Explanation

4.1 Setting of Option Byte

Table 4-1 shows the option byte settings.

Table 4-1 Option Byte Settings

Address	Setting Value	Contents
000C0H / 020C0H	11101111B	Disables the watchdog timer. (Counting stopped after reset)
000C1H / 020C1H	11111011B	LVD0 detection voltage: reset mode At rising edge TYP. 2.970 V (2.88 V to 3.06 V) At falling edge TYP. 2.910 V (2.82 V to 3.00 V)
000C2H / 020C2H	11101000B	HS mode, High-speed on-chip oscillator clock (f_{IH}): 32 MHz
000C3H / 020C3H	10000100B	Enables on-chip debugging

4.2 List of Variables

Table 4-2 lists global variables.

Table 4-2 Global Variables

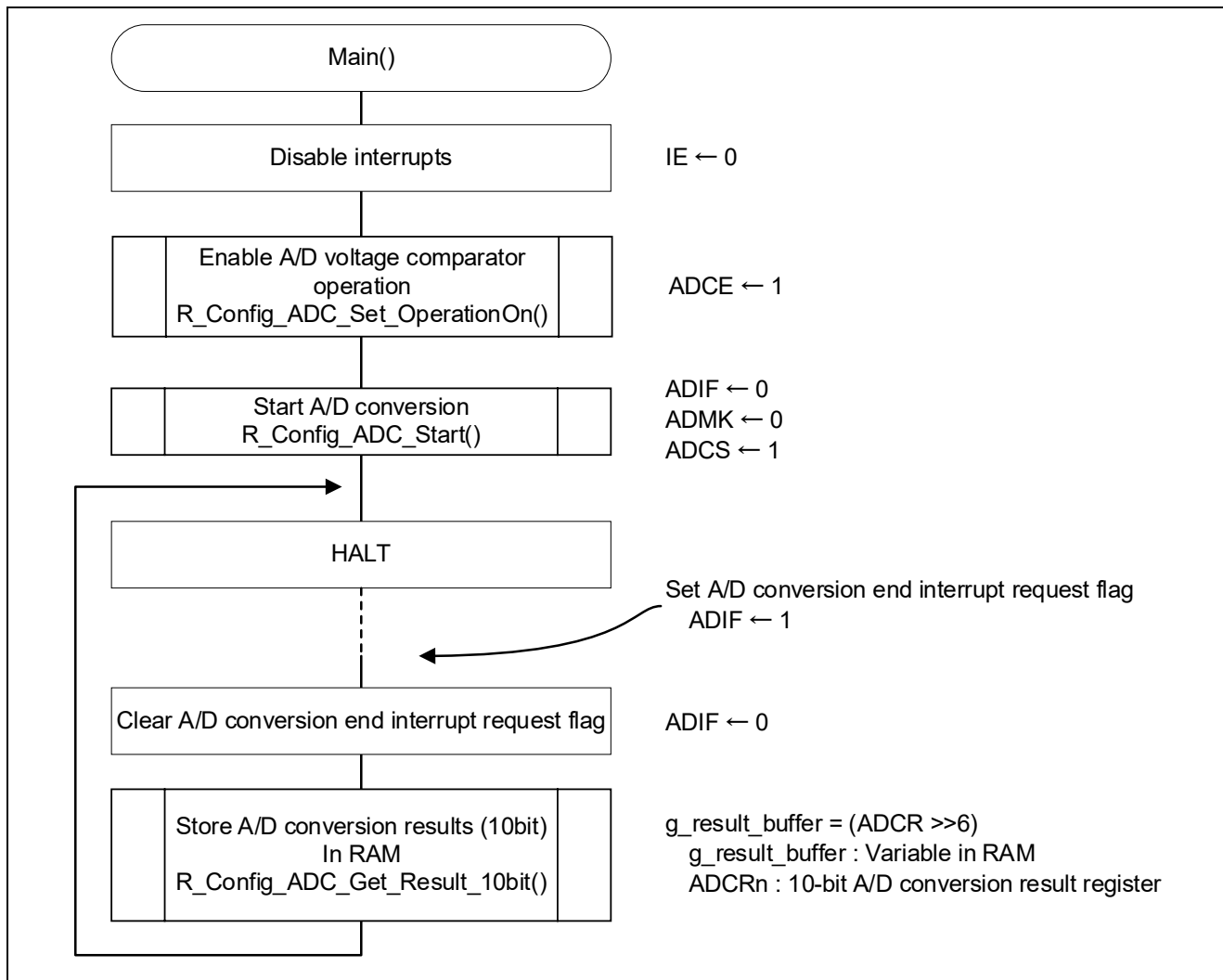
Type	Variable Name	Description	Function Used
Unsigned short	g_result_buffer	A/D conversion result storage area	main()

4.3 Flowchart

4.3.1 Main Processing Function

Figure 4-1 shows the flowchart of the main processing.

Figure 4-1 Main Processing Function



5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RL78/G22 User's Manual: Hardware (R01UH0896J)

RL78 family user's manual software (R01US0015J)

The latest versions can be downloaded from the Renesas Electronics website.

Technical update

The latest versions can be downloaded from the Renesas Electronics website.

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2023.02. 02	-	First Edition
1.01	2023.04. 07	5	Operation Confirmation Conditions update
1.02	2023.08. 04	5	Operation Confirmation Conditions update

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1. Precaution against Electrostatic Discharge (ESD)

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2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
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