RL78/L23

3ch IH Control using Timer KB

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Introduction

This application note describes IH control using the 16-bit timers KB40, KB41, and KB42 on the RL78/L23 microcontroller.
The 16-bit timers KB40, KB41, and KB42 are capable of generating PWM output suitable for IH control. Each timer includes a Timer Restart Function, which allows the output to automatically restart in synchronization with external signals, and an IH Control PWM Output Function, which disables restarts during a predefined active period to ensure a stable output pulse width.

Target Device

RL78/L23

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

This application note uses 16-bit timers KB40, KB41, and KB42 to output PWM waveforms from the TKBO01, TKBO11, and TKBO21 pins. PWM output from each pin is switched in turn in 10ms increments.

The duty ratio of PWM output is sequentially switched in 4 steps of 20%, 40%, 80%, and 0% by pressing the switch (INTP0).

Table 1.1 shows the peripheral functions used and their applications. Figure 1.1 shows the operation overview diagram, and Figure 1.2 shows the PWM output function for IH control.

Table 1.1 Peripheral Function to be Used and Its Use

Peripheral Function	Use
16-bit timer KB40	PWM output for IH control
16-bit timer KB41	PWM output for IH control
16-bit timer KB42	PWM output for IH control
External interrupt INTP0	Detect switch press
External interrupt INTP3	Restart of PWM output for IH control
External interrupt INTP4	Restart of PWM output for IH control
External interrupt INTP5	Restart of PWM output for IH control
External interrupt INTP6	Forced stop of PWM output for IH control
Timer array unit (TAU) channel 0	Generates a 10ms cycle

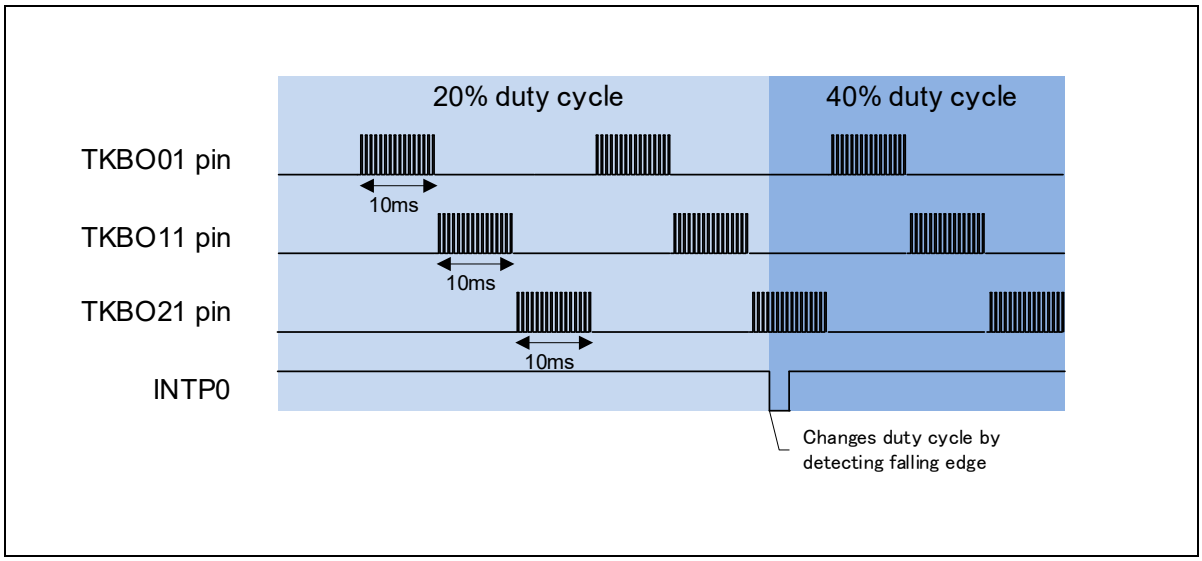

Figure 1.1 Operation Overview Diagram

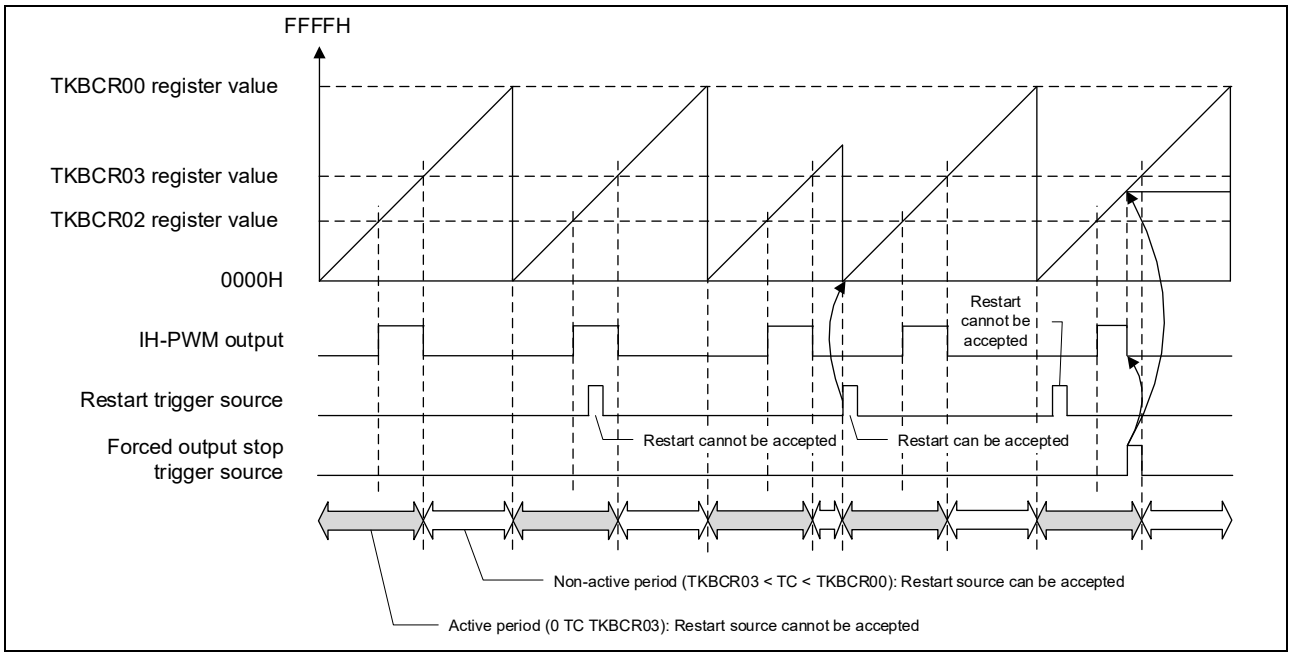

Figure 1.2 PWM output function for IH control

1.1 Detailed Specifications

This section describes the initial settings and processing of the sample code.

(1) Initialize External Interrupts

<Setting conditions>

- Set INTP0 to trigger on the falling edge.
- Set INTP3 to trigger on the falling edge.
- Set INTP4 to trigger on the falling edge.
- Set INTP5 to trigger on the falling edge.
- Set INTP6 to trigger on the rising edge.

(2) Initialize the TAU

<Setting conditions>

- Set the interval time for channel 0 to 10ms.

(3) Initialize 16-bit timer KB40

＜Setting conditions＞

- Set the TKBCR00 register to 1599. (This sets the PWM output period to 50μs.)
- Set the TKBCR01 register to 0.
- Set the TKBCR02 register to 32.
- Set the TKBCR03 register to 32.
- Enable the IH control PWM output function.
- Set the restart function trigger to the external interrupt signal (INTP3).
- Enable output on the TKBO01 pin.
- Set the default level of the TKBO01 pin to Low, and the active level to High.
- Enable forced output stop function 1.
- Set the trigger for forced output stop function 1 to the external interrupt signal (INTP6).
- Set the output level to Low when forced output stop function 1 is executed.

(4) Initialize 16-bit timer KB41

<Setting conditions>

- Set the TKBCR10 register to 1599. (This sets the PWM output period to 50 μs.)
- Set the TKBCR11 register to 0.
- Set the TKBCR12 register to 32.
- Set the TKBCR13 register to 32.
- Enable the IH control PWM output function.
- Set the restart function trigger to the external interrupt signal (INTP4).
- Enable output on the TKBO11 pin.
- Set the default level of the TKBO11 pin to Low, and the active level to High.

- Enable forced output stop function 1.
- Set the trigger for forced output stop function 1 to the external interrupt signal (INTP6).
- Set the output level to Low when forced output stop function 1 is executed.

(5) Initialize 16-bit timer KB42

<Setting conditions>

- Set the TKBCR20 register to 1599. (This sets the PWM output period to 50μs.)
- Set the TKBCR21 register to 0.
- Set the TKBCR22 register to 32.
- Set the TKBCR23 register to 32.
- Enable the IH control PWM output function.
- Set the restart function trigger to the external interrupt signal (INTP5).
- Enable output on the TKBO21 pin.
- Set the default level of the TKBO21 pin to Low, and the active level to High.
- Enable forced output stop function 1.
- Set the trigger for forced output stop function 1 to the external interrupt signal (INTP6).
- Set the output level to Low when forced output stop function 1 is executed.

(6) After initializing the peripheral functions, enable TAU channel 0 and enable external interrupt INTP0.

(7) Enter HALT mode and wait for an interrupt request from TAU channel 0.

(8) When the interrupt request cancels HALT mode, set the compare value of 16-bit timer KB40 and enable its operation.

Stop 16-bit timers KB41 and KB42. At this point, the high-level width of the PWM output is not maintained, and the output remains Low.

(9) Repeat steps (7) and (8) to output PWM signals sequentially from each pin using 16-bit timers KB40, KB41, and KB42 at 10ms intervals.

(10) When the switch is pressed, the PWM duty cycle is changed. The duty cycle transitions in the following order: 20% → 40% → 80% → 0%.

(11) When a forced output stop signal from external interrupt INTP6 is detected, the forced output stop function halts the PWM output.

2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/L23 (R7F100LPL)
Operating frequency	● High-speed on-chip oscillator (HOCO) clock: 32MHz ● CPU/peripheral hardware clock: 32MHz
Operating voltage	● 3.3V ● LVD0 operations (V_{LVD0}): Reset mode Rising edge TYP. 1.90V Falling edge TYP. 1.86V
Integrated development environment (CS+)	CS + V8.13.00 from Renesas Electronics Corporation
C compiler (CS+)	CC-RL V1.15.00 from Renesas Electronics Corporation
Integrated development environment (e2 studio)	e2 studio V2025-04.1 (25.4.1) from Renesas Electronics Corporation
C compiler (e2 studio)	CC-RL V1.15.00 from Renesas Electronics Corporation
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V5.20.1 from IAR Systems
C compiler (IAR)	IAR C/C++ Compiler for Renesas RL78 V5.20.1.2826 from IAR Systems
Board used	RL78/L23 Fast Prototyping Board (RTK7RLL230S00WS1BJ)

3. Hardware

3.1 Hardware Example

Figure 4.1 shows the hardware configuration used in this application note.

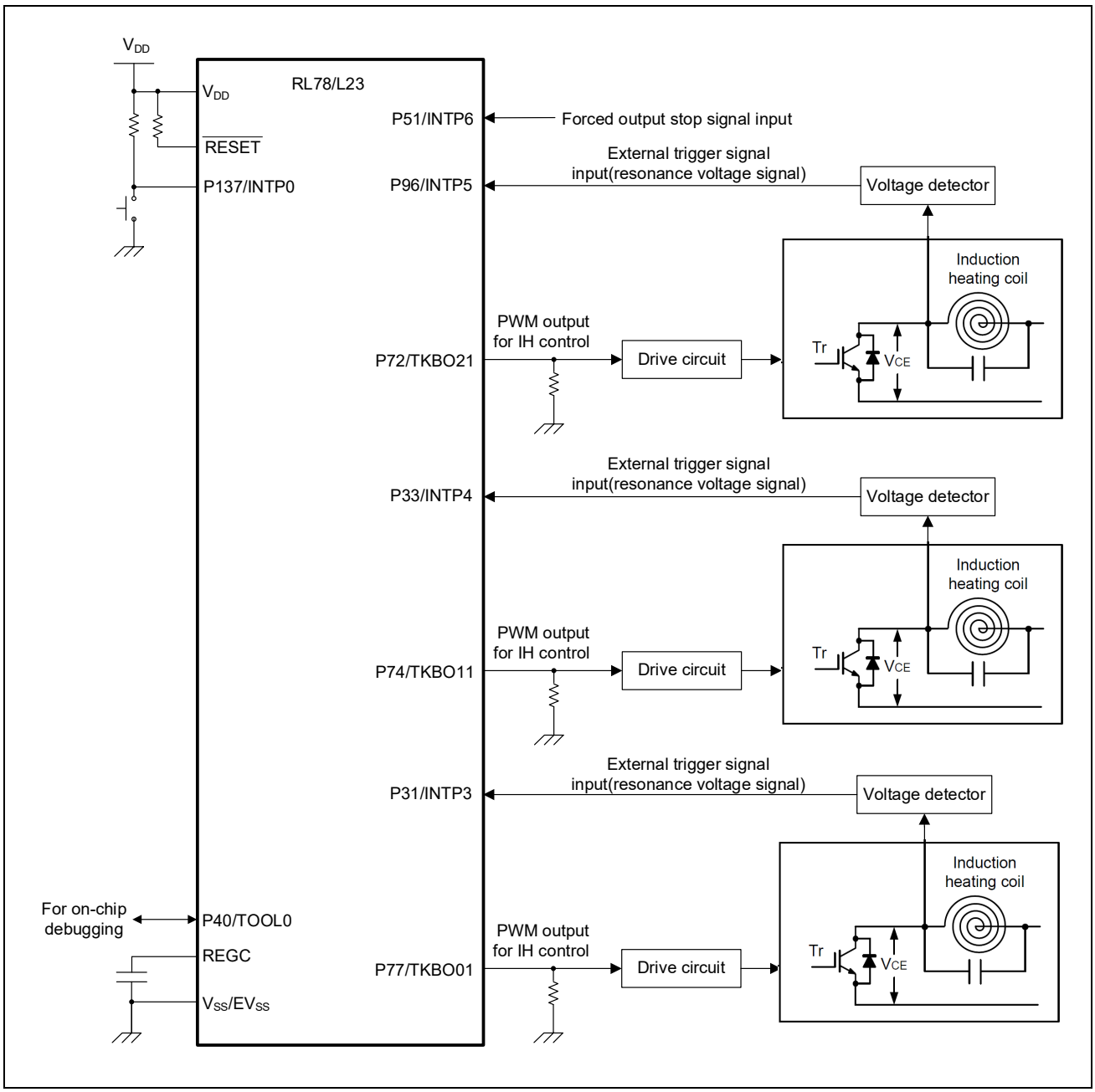

Figure 4.1 Hardware Configuration

Cautions:1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. V_{DD} must be held at not lower than the reset release voltage (V_{LVD0}) that is specified as LVD0.

3.2 List of Pins to be Used

Table 3.1 lists the pins to be used and their functions.

Table 3.1 Pins to be Used and their Functions

Pin Name	I/O	Description
P31/INTP3	Input	Restart signal input for 16-bit timer KB40
P33/INTP4	Input	Restart signal input for 16-bit timer KB41
P51/INTP6	Input	Forced output stop signal input for 16-bit timers KB40, KB41, and KB42
P72/TKBO21	Output	PWM output for 16-bit timer KB42.
P74/TKBO11	Output	PWM output for 16-bit timer KB41.
P77/TKBO01	Output	PWM output for 16-bit timer KB40.
P96/INTP5	Input	Restart signal input for 16-bit timer KB42
P137/INTP0	Input	switch input

4. Software

4.1 Option Byte Settings

Table 4.1 lists the option byte settings.

Table 4.1 Option Byte Settings

Address	Value	Description
000C0H/040C0H	11101111B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/040C1H	11111110B	LVD0 operating mode: reset mode Detection voltage: Rising edge 1.90V Falling edge 1.86V
000C2H/040C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/040C3H	10000100B	Enables the on-chip debugger.

4.2 List of Constants

Table 4.2 lists the constants used in the sample code.

Table 4.2 List of Constants

Constant	Setting	Description
CLEAR	0	Flag clear value
SET	1	Flag set value
KB40	0	Status value of 16-bit timer KB40
KB41	1	Status value of 16-bit timer KB41
KB42	2	Status value of 16-bit timer KB42
DUTY_0	0	Status value for 0% duty cycle
DUTY_20	1	Status value for 20% duty cycle
DUTY_40	2	Status value for 40% duty cycle
DUTY_80	3	Status value for 80% duty cycle

4.3 List of Variables

Table 4.3 lists global variables.

Table 4.3 List of Global Variables

Type	Variable Name	Contents	Function Used
static pwm_data	g_duty[4]	PWM output duty cycle setting value Initial values are duty cycle setting values for 0%, 20%, 40%, and 80%	main
uint8_t	g_interrupt_flag	Interrupt flag	main、 r_Config_TAU0_0_interrupt
uint8_t	g_pwm_ch	Status of 16-bit timer KB channel	main
uint8_t	g_duty_status	Duty cycle status	main、 r_Config_INTC_intp0_interrupt

4.4 List of Functions

Table 4.4 lists the functions.

Table 4.4 List of Functions

Function Name	Outline
main	Main processing
r_igbt_outdrv	IGBT output driver setup processing
r_igbt_width_set	IGBT output setup processing
r_Config_TAU0_0_interrupt	TAU0 channel0 interrupt processing
r_Config_INTC_intp0_interrupt	External interrupt processing

4.5 Function Specifications

This section describes the specifications for the functions that are used in this sample program.

[Function Name] main

Synopsis	Main processing	
Header	r_cg_macrodriver.h、Config_INTC.h、Config_TKB0.h、Config_TKB1.h、Config_TKB2.h、Config_TAU0_0.h、Pin.h、r_cg_tau_common.h、r_cg_tkb_common.h、r_cg_userdefine.h	
Declaration	void r_main_userinit(void);	
Explanation	PWM waveforms are output from TKBO01, TKBO11, and TKBO21 pins using 16-bit timers KB40, KB41, and KB42. The PWM output is switched sequentially at 10ms intervals.	
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] r_igbt_outdrv

Synopsis	IGBT output driver setup processing	
Header	r_cg_macrodriver.h、Config_INTC.h、Config_TKB0.h、Config_TKB1.h、Config_TKB2.h、Config_TAU0_0.h、Pin.h、r_cg_tau_common.h、r_cg_tkb_common.h、r_cg_userdefine.h	
Declaration	void r_rtc_operation_start(void);	
Explanation	Calculate the values to be set in each compare register.	
Arguments	uint8_t ch	16-bit timer KB channel
	uint16_t period	Period
	uint16_t ton_width	High width
	uint8_t delay_time	Delay time
Return value	None	
Remarks	None	

[Function Name] r_igbt_width_set

Synopsis	IGBT output setup processing	
Header	r_cg_macrodriver.h、Config_INTC.h、Config_TKB0.h、Config_TKB1.h、Config_TKB2.h、Config_TAU0_0.h、Pin.h、r_cg_tau_common.h、r_cg_tkb_common.h、r_cg_userdefine.h	
Declaration	void r_handle_watch_display(void);	
Explanation	Perform setup processing for starting and changing IGBT output.	
Arguments	uint8_t ch	16-bit timer KB channel
	uint16_t tkbcrX0_calc	Register setting values for TKBCR00, TKBCR10, and TKBCR20
	uint16_t tkbcrX2_calc	Register setting values for TKBCR02, TKBCR12, and TKBCR22
	uint16_t tkbcrX3_calc	Register setting values for TKBCR03, TKBCR13, and TKBCR23
Return value	None	
Remarks	None	

[Function Name] r_Config_TAU0_0_interrupt

Synopsis	TAU channel0 interrupt processing
Header	r_cg_macrodriver.h、r_cg_userdefine.h、Config_TAU0_0.h
Declaration	#pragma interrupt r_Config_TAU0_0_interrupt(vect=INTTM00)
Explanation	Set the interrupt flag.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_Config_INTC_intp0_interrupt

Synopsis	External interrupt processing
Header	r_cg_macrodriver.h、r_cg_userdefine.h、Config_INTC.h
Declaration	#pragma interrupt r_Config_INTC_intp0_interrupt(vect=INTP0)
Explanation	Update the duty cycle status.
Arguments	None
Return value	None
Remarks	None

4.6 Flowcharts

4.6.1 Main Processing

Figures 4.1 and 4.2 shows the flowchart of the main processing.

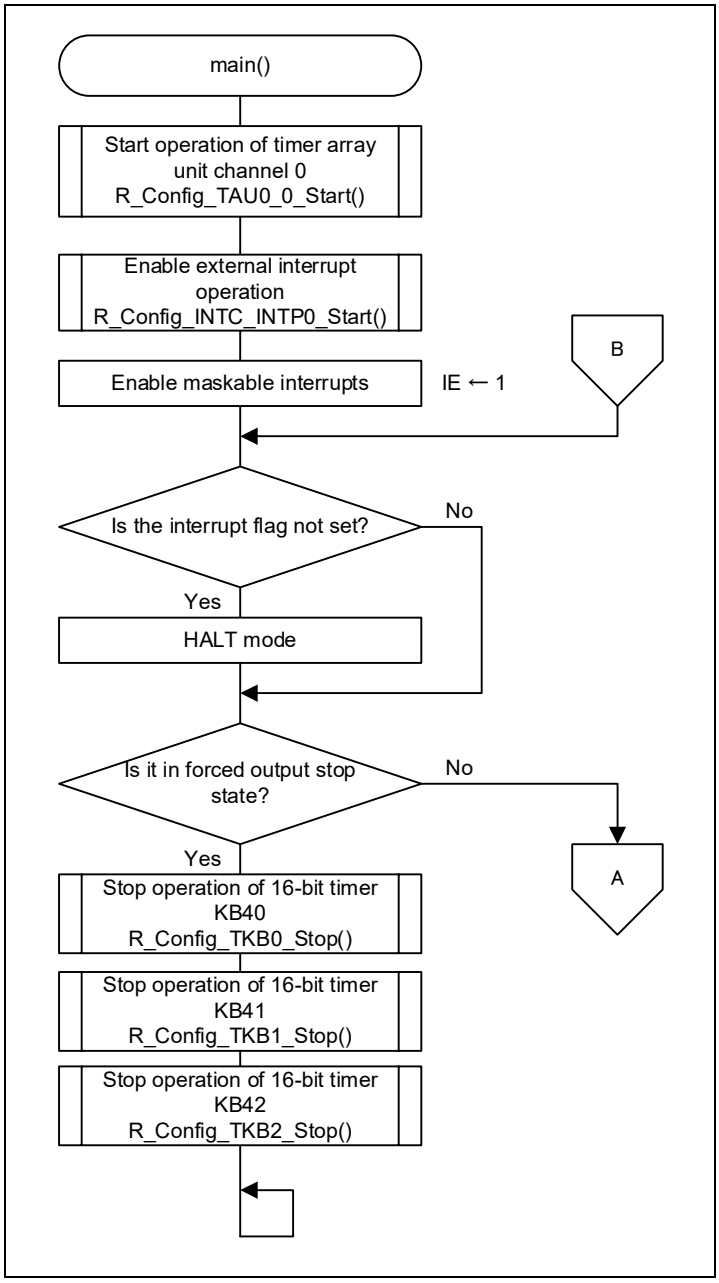

Figure 4.1 Main Processing (1/2)

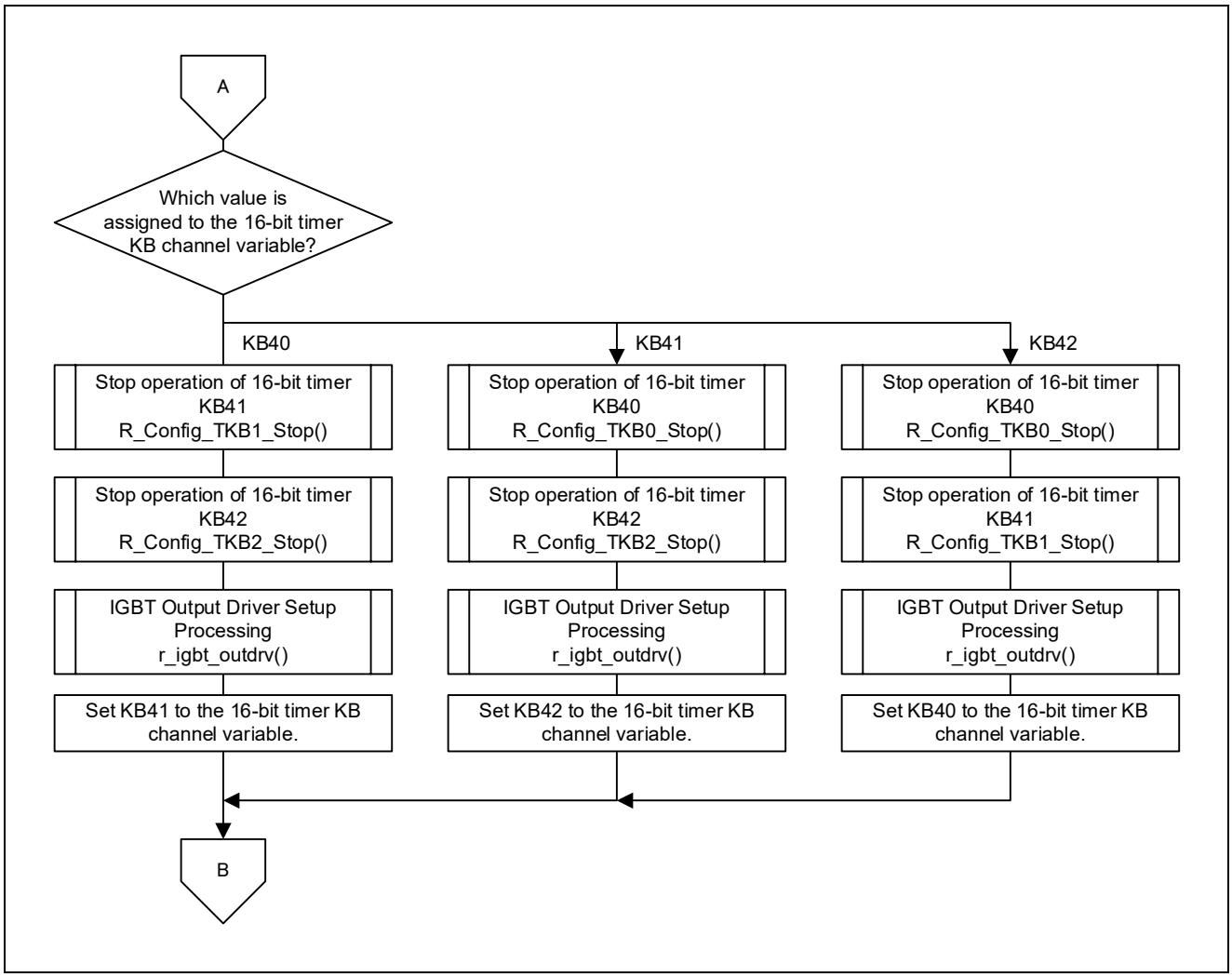

Figure 4.2 Main Processing (2/2)

4.6.2 IGBT Output Driver Setup Processing

Figure 4.3 shows the flowchart of the IGBT output driver setup processing.

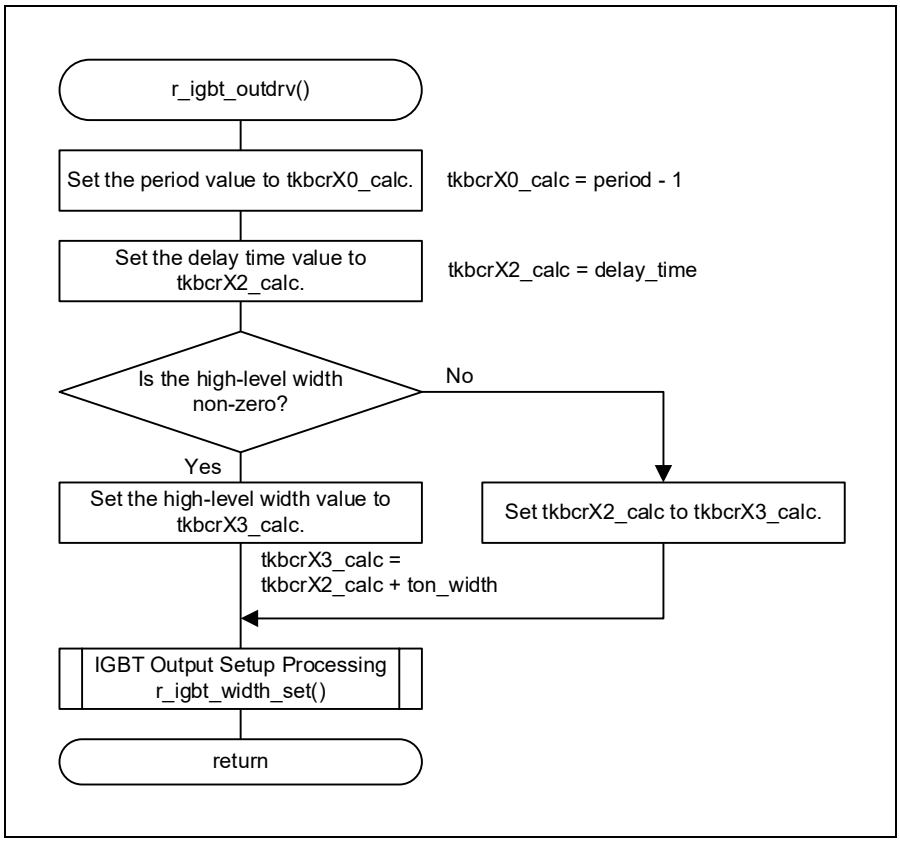

Figure 4.3 IGBT Output Driver Setup Processing

4.6.3 IGBT Output Setup Processing

Figure 4.4 shows the flowchart of the IGBT output setup processing.

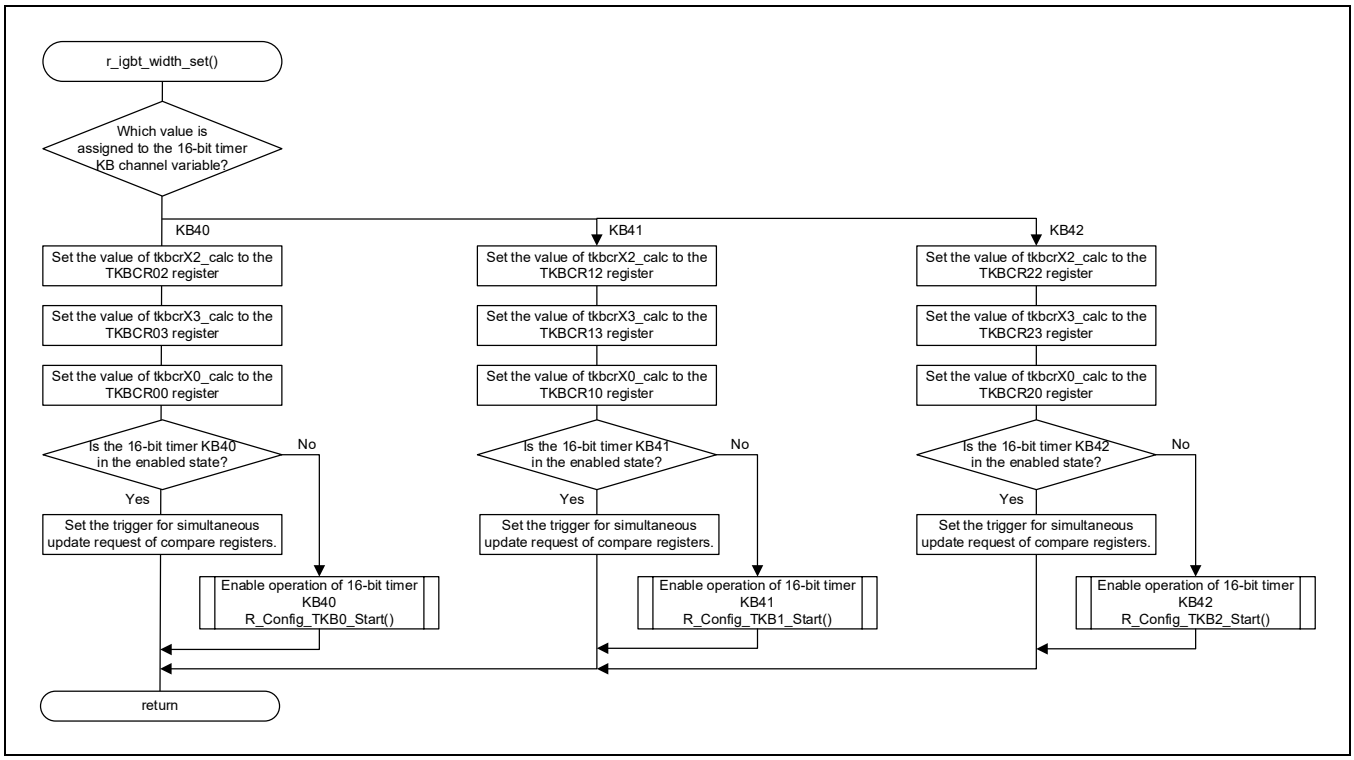

Figure 4.4 IGBT Output Setup Processing

4.6.4 TAU Channel0 Interrupt Processing

Figure 4.5 shows the flowchart of the TAU channel0 interrupt processing.

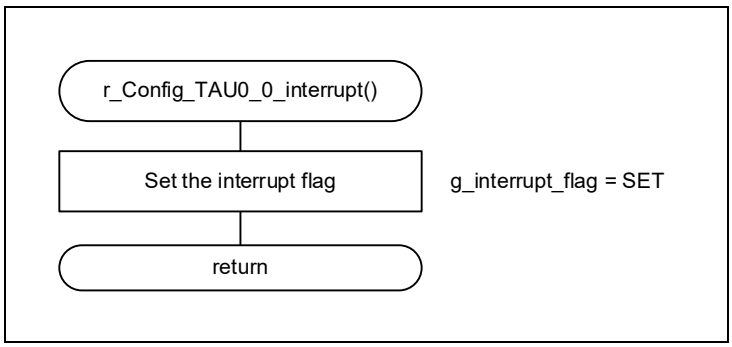

Figure 4.5 TAU Channel0 Interrupt Processing

4.6.5 External Interrupt Processing

Figure 4.6 shows the flowchart of the external interrupt processing.

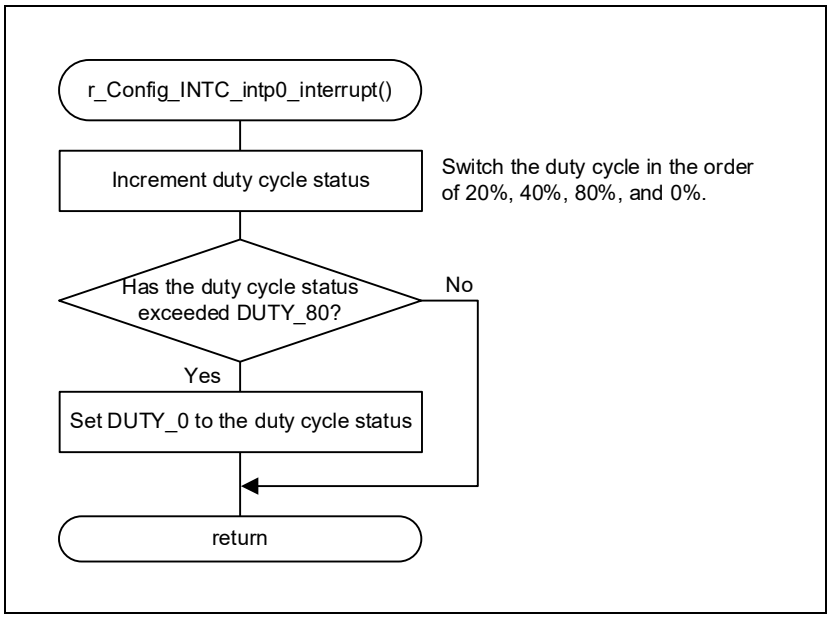

Figure 4.6 External Interrupt Processing

5. Sample Code

The sample code is available on the Renesas Electronics Website.

6. Documents for Reference

RL78/L23 User's Manual: Hardware (R01UH1082E)

RL78 Family User's Manual: Software (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Aug.27, 2025	-	First edition issued

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2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
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   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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