RTK0EE0017D11004BJ

Design guidelines for circuit boards with the external front-end module

Introduction

This document gives guidelines for designing circuit boards that incorporate the RF transceiver and the front-end module.
This document explains the daughter board design of the evaluation kit as an example. The evaluation kit consists of a mother board (RTK0EE0013D12002BJ) and a daughter board (RTK0EE0017D11004BJ). The RTK0EE0017D11004BJ consists of MCU (RX65N), RF transceiver (R9A06G062GNP), and front-end module (SKY66122-11).

Note: Descriptions in this application note are examples for reference. Following the guidelines does not guarantee the quality of characteristic signals. In attempting to use this device in your actual system, extensively consider and evaluate the system as a whole. Choosing to use the device in your system is at your own responsibility.

Target Device

R9A06G062GNP

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1. Overview

This document explains the daughter board design of the evaluation kit as an example. The evaluation kit consists of a mother board (RTK0EE0013D12002BJ) and a daughter board (RTK0EE0017D11004BJ). The RTK0EE0017D11004BJ consists of MCU (RX65N), RF transceiver (R9A06G062GNP), and front-end module (SKY66122-11).

The RF characteristics are greatly affected by the design method. Therefore, in order to obtain the original RF characteristics, it is recommended to design board according to the precautions described in this document.

1.1 Related documents

Also refer to the following document related to this application note.

R02UH0006EJ0120 : R9A06G062GNP Sub-GHz Transceiver User’s Manual: Hardware

R35AN0013EJ0100 : R9A06G062GNP Design Guidelines for Circuit Boards with the Sub-GHz Transceiver

1.2 Appearance of the evaluation kit

The appearance of the evaluation kit is shown in Figure 1-1.

Figure 1-1 : Appearance of the evaluation kit

1.3 Appearance of the RTK0EE0017D11004BJ (Daughter board)

The appearance of the RTK0EE0017D11004BJ is shown in Figure 1-2.

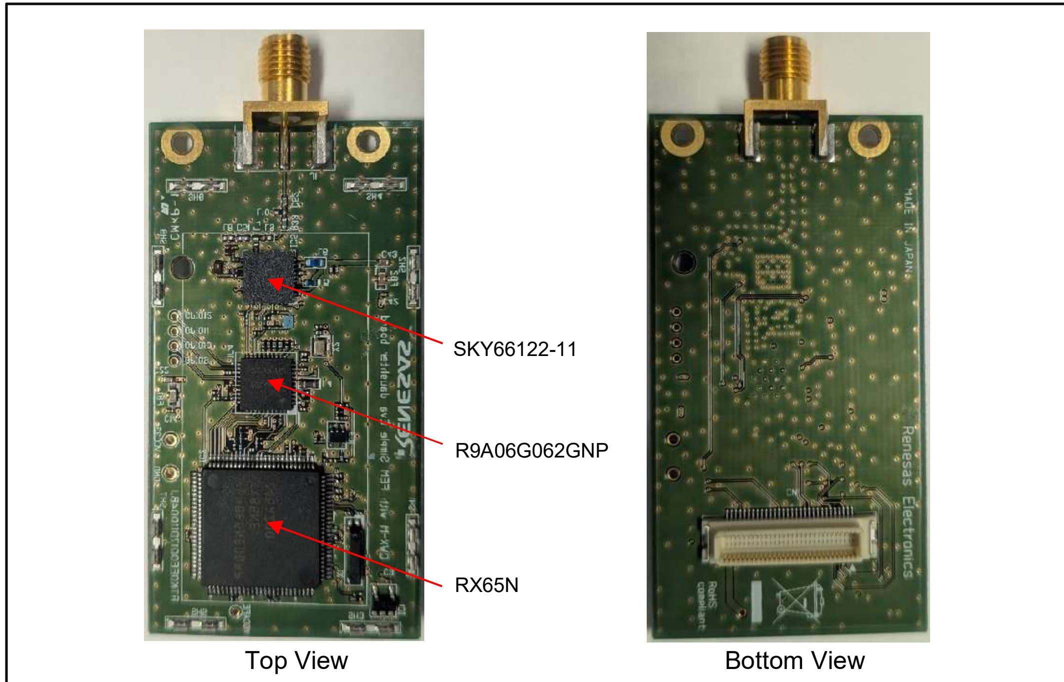

Figure 1-2 : Appearance of the RTK0EE0017D11004BJ (Daughter board)

1.4 Appearance of the RTK0EE0013D12002BJ (Mother board)

The appearance of the RTK0EE0013D12002BJ is shown in Figure 1-3.

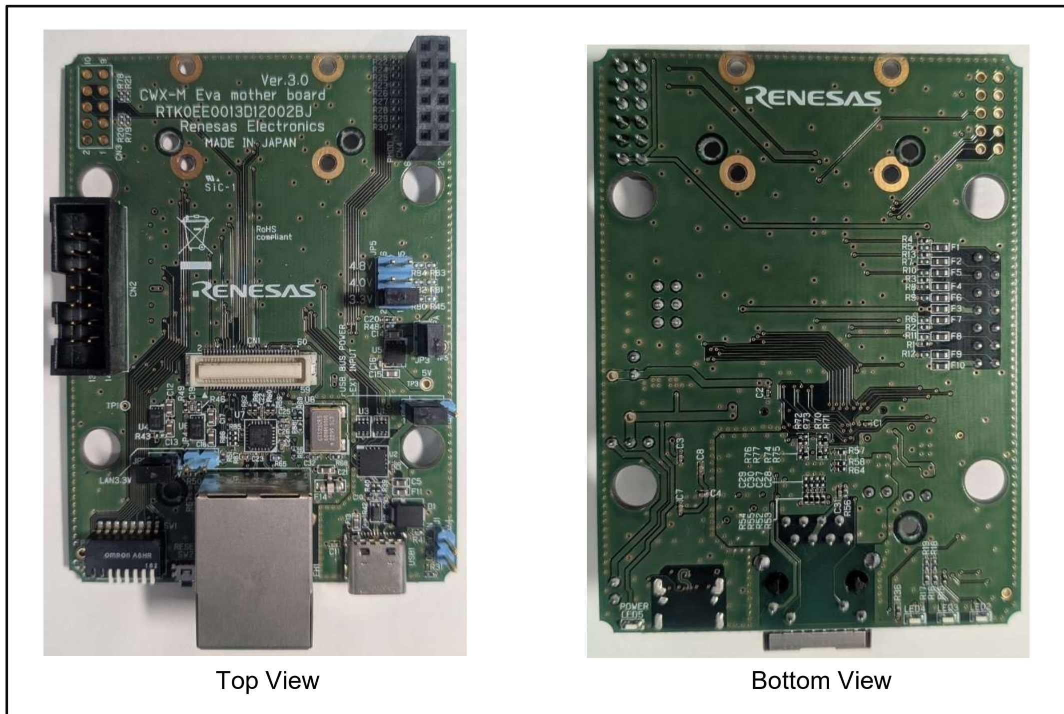

Figure 1-3 : Appearance of the RTK0EE0013D12002BJ (Mother board)

2. Circuit design

This chapter explains the circuit design when using the RF transceiver IC (R9A06G062GNP) and a front-end module (SKY66122-11). It also explains some of the circuit design related to the interface with the MCU.

For the detail circuit design of SKY66122-11 peripheral circuit, refer to the manufacturer's data sheet.

2.1 Interface of front-end module (SKY66122-11)

Table 2-1 shows the outline of SKY66122-11 pins and connection examples with the RF transceiver IC.

Table 2-1 : Outline of SKY66122-11 pins and connection examples

Pin	Pin Name	Description	Connection
1	CPS	Path select control	R9A06G062GNP : Pin14(GPIO8)
2	CTX	Transmit / Receive control	R9A06G062GNP : Pin13(GPIO7)
3	GND	Ground	Ground
4	PA_IN	Input to PA	R9A06G062GNP : Pin23(RFOUT) Connect to TX SAW filter output pin Refer to chapter 2.2.
5	GND	Ground	Ground
6	GND	Ground	Ground
7	TX_FLT	Source for external TX filter	50 Ω termination
8	GND	Ground	Ground
9	T/R	Transmit and receive	R9A06G062GNP : Pin21(RFIN) Refer to chapter 2.2.
10	GND	Ground	Ground
11	CSD	Shutdown control	RX65N : Pin74(I/O port function) (Pull down this signal line with 56kΩ)
12	GND	Ground	Ground
13	GND	Ground	Ground
14	LNA_IN	LNA input	Connect to RX SAW filter output pin
15	GND	Ground	Ground
16	RX_FLT	Source for external RX filter	Connect to RX SAW filter input pin
17	GND	Ground	Ground
18	VDET	Power detector output	Connect to AD function pin of MCU
19	GND	Ground	Ground
20	ANT	Antenna	Antenna
21	GND	Ground	Ground
22	GND	Ground	Ground
23	GND	Ground	Ground
24	GND	Ground	Ground
25	GND	Ground	Ground
26	GND	Ground	Ground
27	GND	Ground	Ground
28	GND	Ground	Ground
29	VCC2	Power supply	Connect to power supply
30	GND	Ground	Ground
31	VCC0	Decoupling capacitor	Connect to decoupling capacitor
32	GND	Ground	Ground
33	VCC1	Power supply	Connect to power supply
34	GND	Ground	Ground
35	VSUP1	General voltage supply	Connect to power supply
36	GND	Ground	Ground
Die Pad	GND	Ground	Ground

2.2 RF signal line

2.2.1 TX attenuator circuit

It is recommended to mount an attenuator circuit on the TX signal line between the RF transceiver and SKY66122-11. Figure 2-1 shows the mounting position of the attenuator.
It extends the variable range of the TX power. The RF transceiver has the power variable range of -15 to + 15 dBm and about 30 dB. However, since the TX gain of SKY66122-11 is about 30 dB, even if the gain of the RF transceiver is varied, the output of SKY66122-11 remains saturated, and the variable range of the TX power is narrowed. The variable range of the TX power is extended by mounting the attenuator.

2.2.2 TX SAW filter circuit

It is recommended to mount the SAW filter on TX signal line to meet radio wave regulations. Figure 2-1 shows the mounting position of the TX SAW filter.

2.2.3 RX SAW filter circuit

It is recommended to mount the SAW filter on RX signal line to consideration of RX intermodulation from other systems (esp. cellular system). Figure 2-1 shows the mounting position of the RX SAW filter.

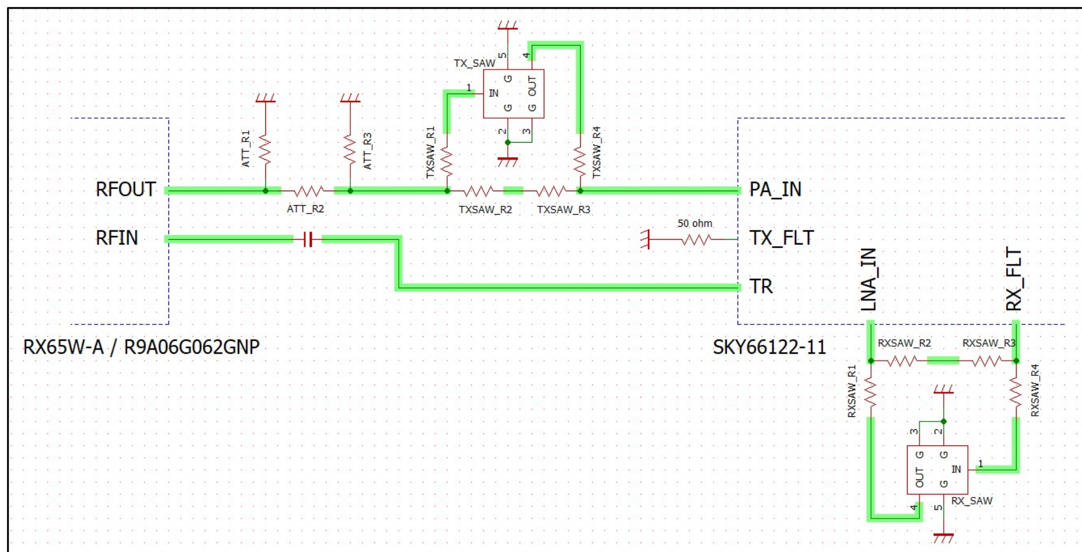

Figure 2-1 : Example of RF signal line

Table 2-2 : Examples of the component values (RF signal line)

Item	FCC	ETSI	ARIB
TX attenuator	5dB ATT_R1 : 180 ohm ATT_R2 : 30 ohm ATT_R2 : 180 ohm	10dB ATT_R1 : 100 ohm ATT_R2 : 68 ohm ATT_R2 : 100 ohm	5dB ATT_R1 : 180 ohm ATT_R2 : 30 ohm ATT_R2 : 180 ohm
TX SAW	Mounted ex. B39921B2672P810 TXSAW_R1 : 0 ohm TXSAW_R2 : NM TXSAW_R3 : NM TXSAW_R4 : 0 ohm	Not mounted TXSAW_R1 : NM TXSAW_R2 : 0 ohm TXSAW_R3 : 0 ohm TXSAW_R4 : NM	Mounted ex. B39931B2645P810 TXSAW_R1 : 0 ohm TXSAW_R2 : NM TXSAW_R3 : NM TXSAW_R4 : 0 ohm
RX SAW	Mounted ex. B39921B2672P810 RXSAW_R1 : 0 ohm RXSAW_R2 : NM RXSAW_R3 : NM RXSAW_R4 : 0 ohm	Mounted ex. B39871B2600P810 RXSAW_R1 : 0 ohm RXSAW_R2 : NM RXSAW_R3 : NM RXSAW_R4 : 0 ohm	Mounted ex. B39931B2645P810 RXSAW_R1 : 0 ohm RXSAW_R2 : NM RXSAW_R3 : NM RXSAW_R4 : 0 ohm

2.3 Antenna signal line

2.3.1 LC filter circuit

It is recommended to add an LC filter and a notch filter to the ANT pin of the SKY66122-11.This is to suppress harmonics of the fundamental wave. Figure 2-2 shows an example of the antenna signal line circuit. Table 2-3 shows examples of the component values in the initial condition.

2.3.2 Antenna matching circuit

When using a monopole antenna instead of a dipole antenna, it is recommended to mount antenna matching components on the board. Figure 2-2 shows the circuit example of the antenna matching components. Table 2-3 shows examples of the component values in the initial condition.

In the initial condition, R1, R2, and R3 are not used as the antenna matching components. Adjust the component values by customer according to the antenna characteristics to be used.

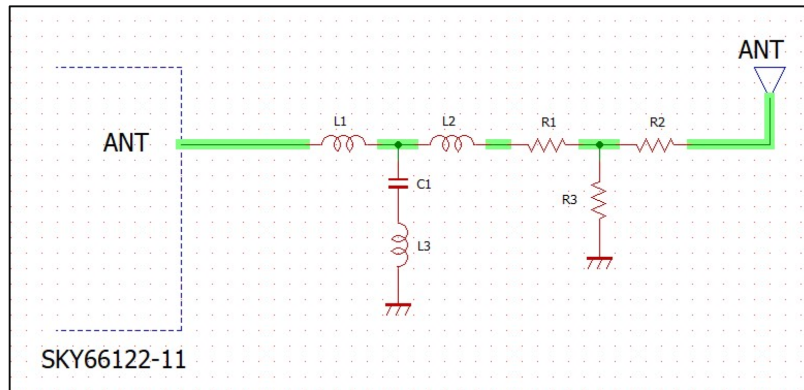

Figure 2-2 : Example of Antenna signal line

Table 2-3 : Examples of the component values (Antenna signal line)

Item	L1 [nH]	L2 [nH]	C1 [pF]	L3 [nH]	R1 [ohm]	R2 [ohm]	R3 [ohm]
LC & notch filter	5.6	5.6	2.0	3.0			
Antenna matching					0	0	NM

2.4 SPI signal line

It is recommended to mount the filter on SPI signal line. The SPI signal frequency is 24MHz. In a wireless environment, this prevents degradation of RX characteristics caused by 24MHz harmonics being input to the antenna.

Figure 2-3 shows an example of the circuit configuration around the SPI. The R9A06G062GNP has the SIN, SOUT, SCLK, and SEN pins for the SPI signals. The R9A06G062GNP is connected with the external master microcontroller and operates as a slave device. Some transfer rates for the SPI may lead to the harmonic components at integer multiples of the SCLK signal frequency adversely affecting the operation within the desired bandwidth. We recommend inserting damping resistors or low-pass filters for suppressing the harmonic components in response to the state of the spurious emissions from the SCLK signal for the SPI.

Table 2-4 lists examples of the constants for the circuit when the clock signal for communications is at 24 MHz.

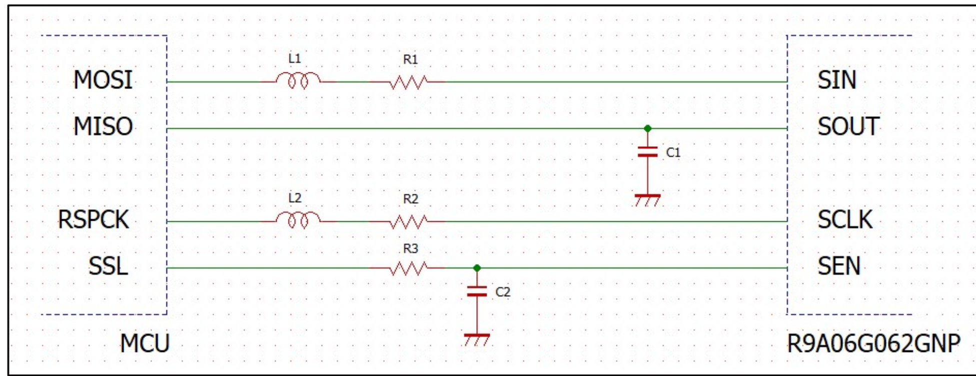

Figure 2-3 : Example of the SPI signal line

Table 2-4 : Examples of the component values (SPI signal line)

Item	L1 [nH]	R1 [ohm]	C1 [pF]	L2 [nH]	R2 [ohm]	R3 [ohm]	C2 [pF]
SIN	100	300					
SOUT			6				
SCLK				100	300		
SEN						22	6

2.5 Reference clock circuit

2.5.1 Using a 48MHz TCXO

Figure 2-4 shows an example of the standard configuration of a circuit with the use of a temperature-compensated crystal oscillator (TCXO). To suppress the harmonic components, we recommend adjusting the voltage amplitude value of output from the 48-MHz TCXO. The voltage amplitude adjustment uses the capacitance division of C1 and C2. Connect a capacitor (C3) to the XOUT pin.
Table 2-5 lists typical values of the constants for the circuit with the use of the NT1612SA from NDK as the TCXO. Before final determination of the constants, we recommend you proceed with sufficient evaluation from the various relevant viewpoints, such as the type of TCXO and the stray capacitance generated by the patterns for your own PCB.

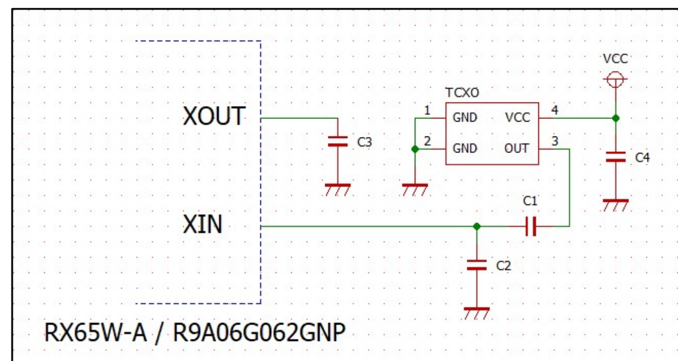

Figure 2-4 : Example of reference clock circuits (TCXO)

Table 2-5 : Examples of the component values (TCXO)

TCXO	C1 [pF]	C2 [pF]	C3 [pF]	C4 [uF]
NT1612SA	9	18	1000	0.1

The RTK0EE0017D11004BJ evaluation kit does not use a crystal oscillator. For the circuit design of the crystal oscillator, please refer to the following application note.

R35AN0013EJ0100 : R9A06G062GNP Design Guidelines for Circuit Boards with the Sub-GHz Transceiver

2.5.2 Using a CKOUT pin

Figure 2-5 shows an example of the circuit configuration using CKOUT pin. The R9A06G062GN has a function that outputs a 16MHz clock, which is the 48MHz reference clock divided by 3, from the CKOUT pin. This clock can be used as the MCU's main clock.
May be the harmonic components at integer multiples of the CKOUT signal frequency adversely affecting the operation within the desired bandwidth. We recommend inserting damping resistors or low-pass filters for suppressing the harmonic components in response to the state of the spurious emissions from the CKOUT signal.
Table 2-6 lists examples of the constants for the circuit.

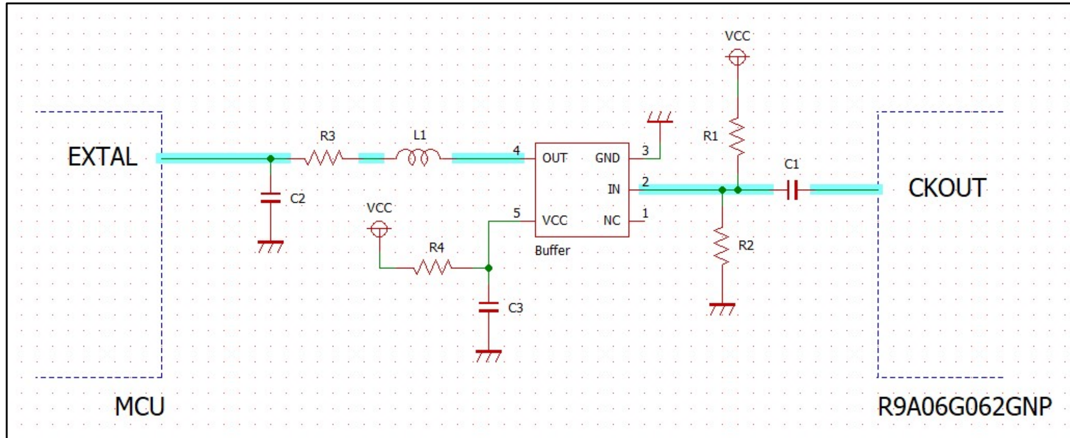

Figure 2-5 : Example of reference clock circuits (CKOUT)

Table 2-6 : Examples of the component values (CKOUT)

Buffer	L1 [nH]	C1 [pF]	C2 [pF]	C2 [uF]	R1 [ohm]	R2 [ohm]	R3 [ohm]	R4
SN74LVC1G34DCK	100	1000	NM	0.1	8.2k	8.2k	160	BLM03AG700SN1

When the CKOUT function is not used, an external crystal oscillator can be used as the MCU's main clock. In that case, please refer to the MCU user's manual.

2.6 DC-DC converter circuit

Figure 2-6 shows an example of the external circuit configuration for the DC-DC converter. Connect the grounds for capacitors C1 to the GND_DDC pin along the shortest possible paths.
Table 2-7 lists examples of the constants for the DC-DC converter circuit.

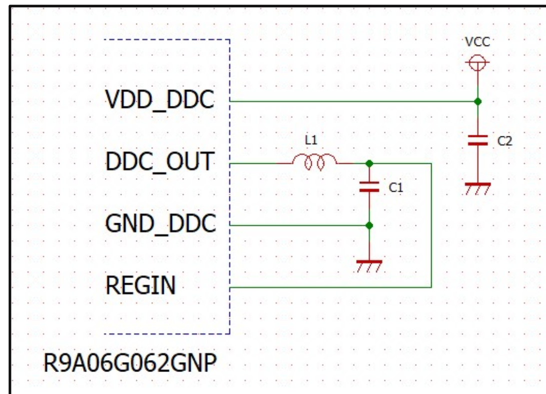

Figure 2-6 : Example of DC-DC converter circuits

Table 2-7 : Examples of the component values (DC-DC converter circuits)

L1 [uH]	C1 [uF]	C2 [uF]
10 (MLZ1608M100WT)	1	0.1

2.7 Power supply circuit

When sharing the power supply for each IC, it is recommended to separate the power supply with a noise filter or ferrite beads. Figure 2-7 shows an example of the power supply circuit using the noise filter. Table2-8 shows examples of the component values.

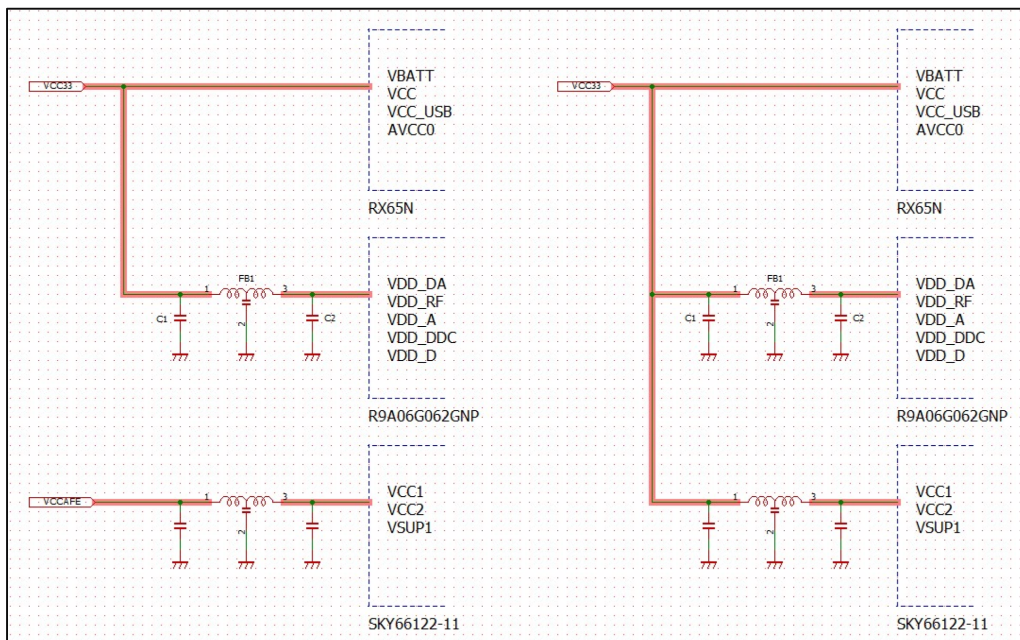

Figure 2-7 : Example of the power supply circuit

Table 2-8 : Examples of the component values (Power supply circuit)

FB1	C1 [uF]	C2 [uF]
NFM18CC222R1C3	1	4.7

3. Layout design

This chapter explains the layout design when using a RF transceiver (R9A06G062GNP) and a front-end module (SKY66122-11).

For the detail layout design of SKY66122-11 peripheral circuit, refer to the manufacturer's data sheet.

We recommend the application of the same principles for the pattern layout of a board as those applied on the evaluation board from Renesas.
As is the case with the evaluation board from Renesas, a PCB with four wiring layers is recommended.

- PCB material : FR-4
  Board thickness : 1.6 mm
  Number of layers : Four
- Major layer configuration (main intended use)
  First layer : signal lines, second layer : ground, third layer : VDD, forth layer : ground, signal lines, or ground and signal lines

The board layer structure is shown in Figure 3-1 and Figure 3-2. This daughter board is designed with a 4-layer board.

Board material : ELC-4765 (SUMITOMO BAKELITE CO.,LTD.)

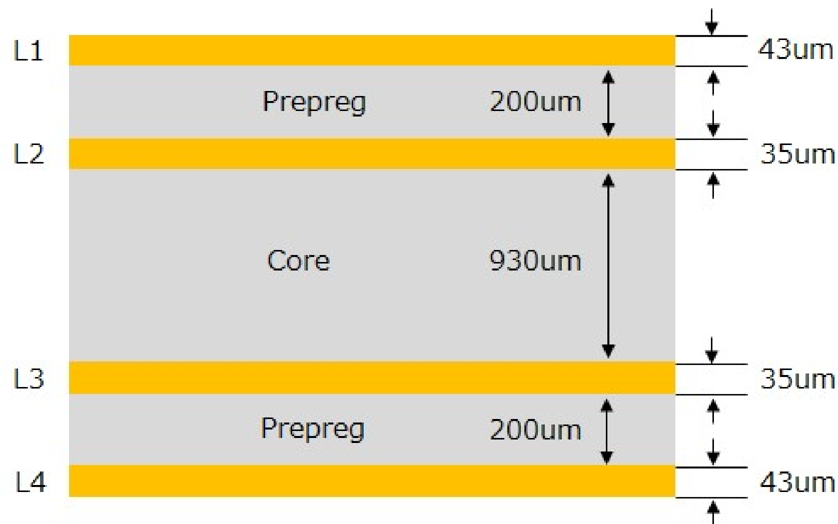

Figure 3-1 : Board layer structure

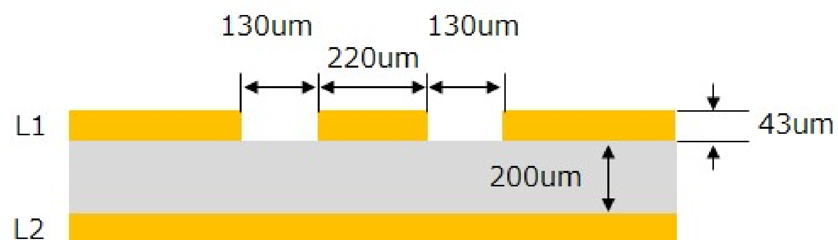

Figure 3-2 : RF unit 50 ohm impedance line

3.1 RF signal line

Points to note in the design of the wiring patterns around the RF signal lines are as follows.

- Use coplanar lines for the RF signals and design the wiring patterns to maintain characteristic impedances of 50 ohms.
- Place as many via holes as possible around the coplanar lines and secure the widest possible ground regions.
- Do not place the lines for different signals in the second layer just below the RF signal lines.
- The GND_A0 (pin 22) and GND_A1 (pin 24) pins are wired outside the IC and used as the GND for the coplanar lines.
- Secure the widest possible ground regions for the GND_A0 (pin 22) and GND_A1 (pin 24) pins. Connect these pins to the exposed die pad in the surface layer along the shortest possible paths and connect the pins to the ground (second) layer through as many via holes as possible, and such that the wiring lengths become as short as possible.

Figure 3-3 shows an example of the layout around the RF signal lines.

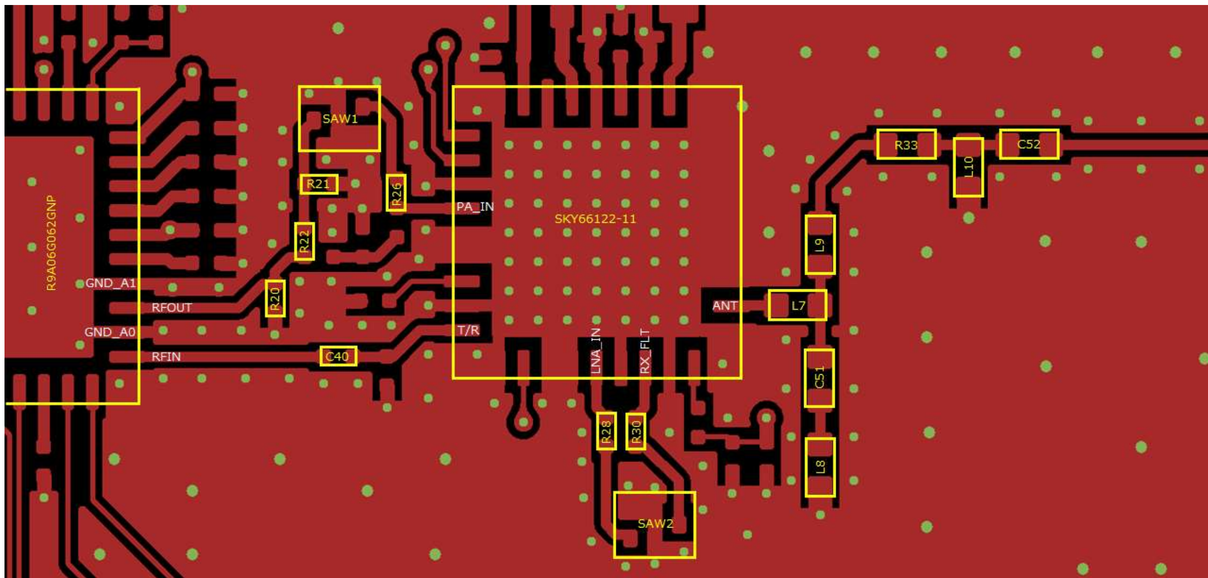

Figure 3-3 : Examples of layout around the RF signal lines

3.2 SPI signal line

Points to note in the design of the wiring patterns around the SPI signal lines are as follows.

- The SPI lines must be wired as short as possible.
- The components of SOUT(Pin2) must be placed on R9A06G062GNP side, and the components of SIN(Pin1) / SCLK(Pin3) / SEN(Pin4) must be placed on the MCU side.

Figure 3-4 shows an example of the layout around the SPI signal lines.

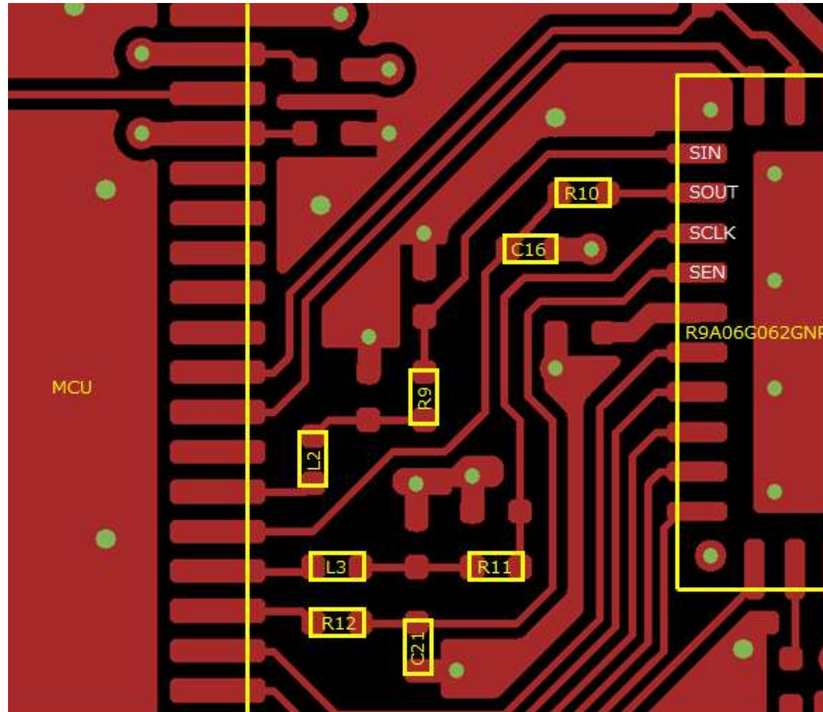

Figure 3-4 : Examples of layout around the SPI signal lines

3.3 TCXO circuit

Points to note in the design of the wiring patterns for the TCXO circuits are as follows.

- Do not place signal lines other than those for the XIN and XOUT pins around the TCXO.
  Especially, do not place the power supply line of the front-end module(FEM) around the TCXO. This is because the TCXO output may couple into the FEM, resulting in unwanted spurious signals.

- Place as wide surface GND area as possible between the TCXO and FEM.

- Proceed with sufficient evaluation of your system in detail before determining the constants for the circuits related to the TCXO.

Figure 3-5 shows an example of the layout around the TCXO circuits.

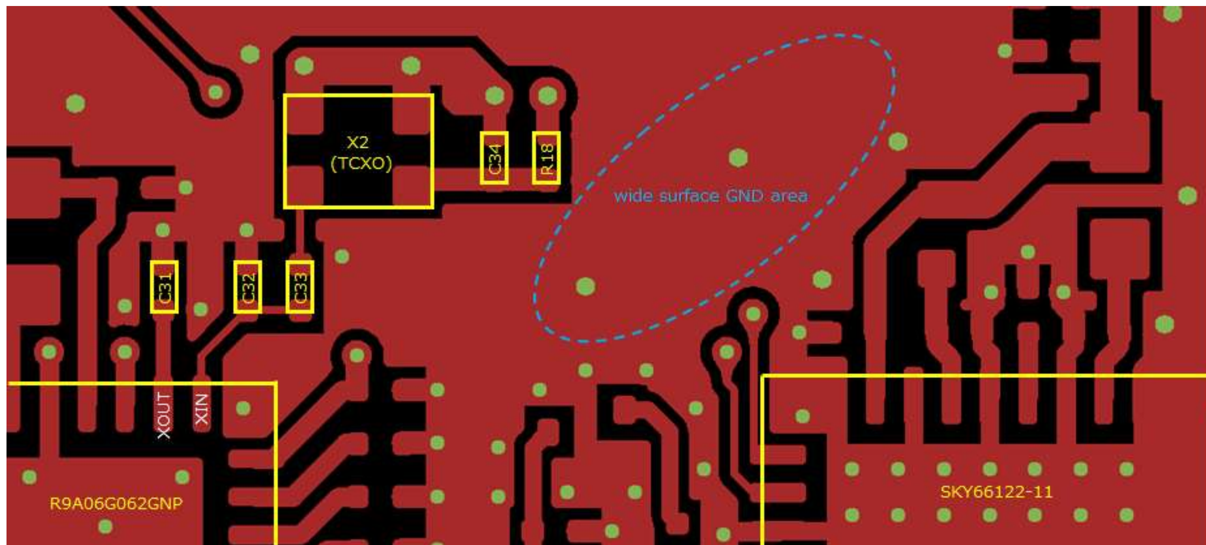

Figure 3-5 : Example of layout around the TCXO circuits

The RTK0EE0017D11004BJ evaluation kit does not use a crystal oscillator. For the layout design of the crystal oscillator, please refer to the following application note.

R35AN0013EJ0100 : R9A06G062GNP Design Guidelines for Circuit Boards with the Sub-GHz Transceiver

3.4 DC-DC converter circuit

Points to note in the design of the feedback loop patterns for the output line of the DC-DC converter are as follows.

- Do not place signal lines around the REGIN (pin 34), GND_DDC (pin 35), DDC_OUT (pin 36), and VDD_DDC (pin 37) pins.
- Make the wiring loop between the REGIN and DDC_OUT pins as short as possible.
- Place capacitor C27 as close as possible to the VDD_DDC pin.
- Place grounds for capacitors C27 and C28 such that they can be connected to the GND_DDC pin along the shortest possible paths on the ground surface.
- Place the board ground from GND_DDC (pin 35) in the loop between REGIN (pin 34) and DDC_OUT (pin 36), and place one or more via.

Figure 3-6 shows an example of the layout around the DC-DC converter circuits.

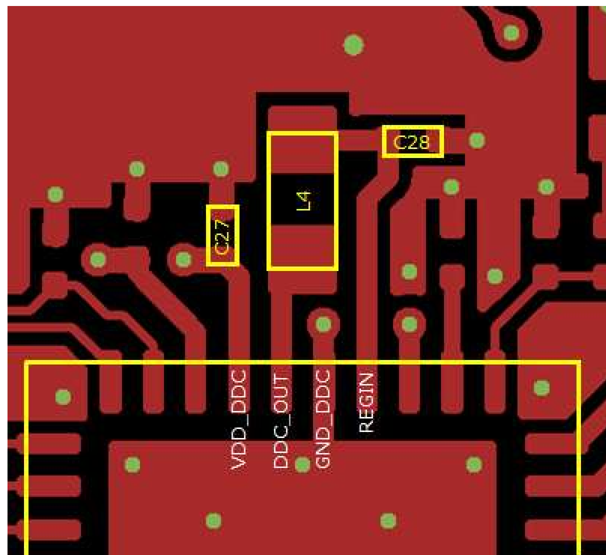

Figure 3-6 : Example of layout around the DC-DC converter circuits

3.5 Power supply circuit

3.5.1 RF transceiver (R9A06G062GNP)

Points to note in the design of the pattern layouts for power supply circuits on the board are as follows.

- Place bypass capacitors close to the respective power supply pins such that the wiring lengths are as short as possible.
- Place via holes for grounds close to grounds for the bypass capacitors such that the grounds can be connected to the ground (second) layer through the via holes along the shortest possible paths. One or more GND via holes must be placed for one bypass capacitor.
- Unless otherwise specified, keep wiring runs to power supply pins as thick as possible in consideration of keeping the impedances low.

Figure 3-7 shows an example of the layout around power supply circuits for the RF transceiver.

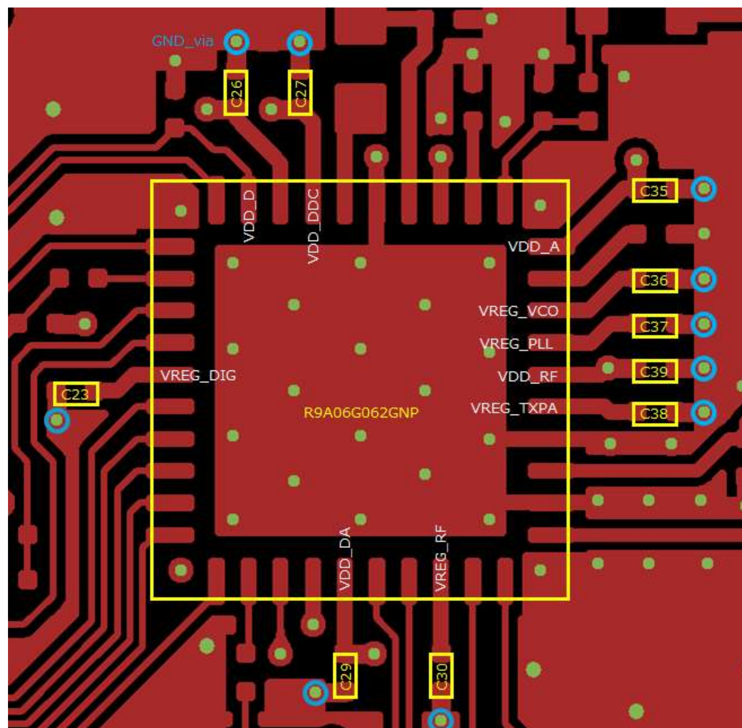

Figure 3-7 : Example of the layout around power supply circuits (RF transceiver)

3.5.2 Front-end module (SKY66122-11)

Points to note in the design of the pattern layouts for power supply circuits on the board are as follows.

- Place bypass capacitors close to the respective power supply pins such that the wiring lengths are as short as possible.
- Place via holes for grounds close to grounds for the bypass capacitors such that the grounds can be connected to the ground (second) layer through the via holes along the shortest possible paths. One or more GND via holes must be placed for one bypass capacitor.
- Unless otherwise specified, keep wiring runs to power supply pins as thick as possible in consideration of keeping the impedances low.

Figure 3-8 shows an example of the layout around power supply circuits for the front-end module.

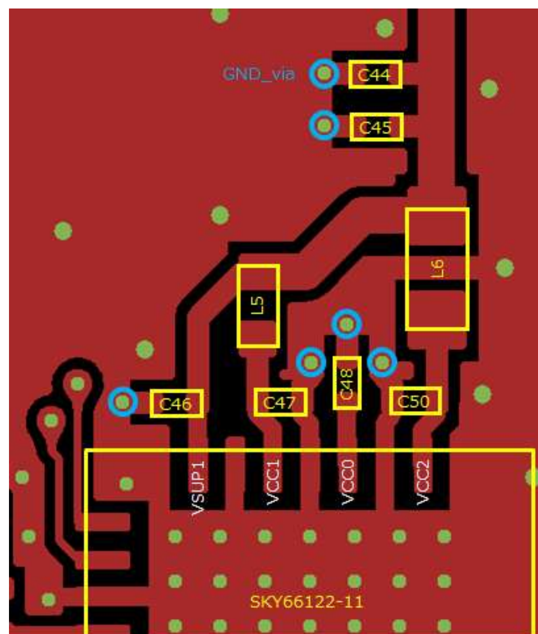

Figure 3-8 : Example of the layout around power supply circuits (front-end module)

3.6 Ground

3.6.1 RF transceiver (R9A06G062GNP)

Points to note in the design of the wiring patterns for grounds are as follows.

- The RF transceiver's exposed die pad and RF circuit GND must have as many GND vias as possible and short between the top layer and the bottom layer to have low impedance.
- Use the second layer as the ground layer. It is recommended that the second layer be solid plane GND.
- Connect the GND_A0 (pin 22), GND_A1 (pin 24), and GND_DDC (pin 35) pins to the exposed die pad in the surface layer and connect them to the ground (second) layer through via holes along the shortest possible paths.
- Do not place signal lines under the exposed die pad.

Figure 3-9 shows an example of the layout around grounds for the RF transceiver.

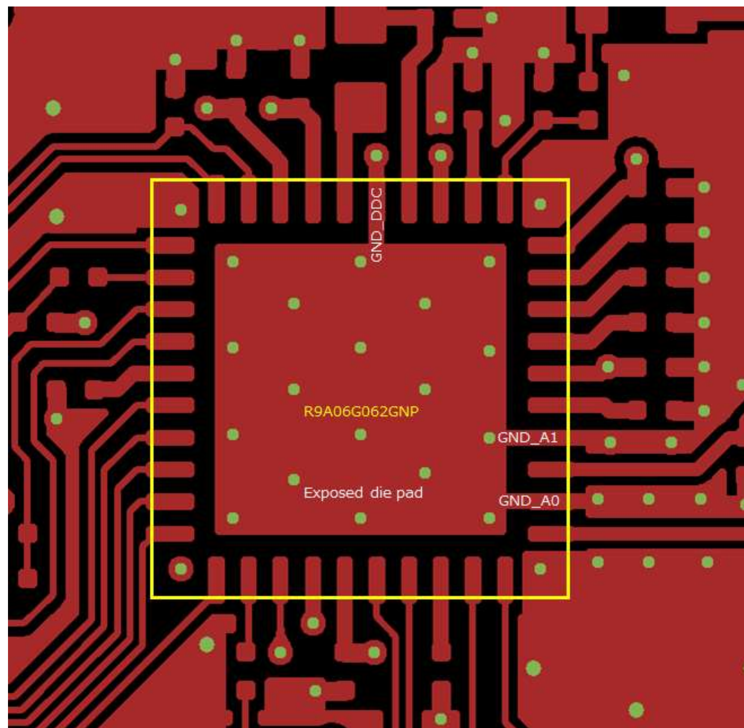

Figure 3-9 : Example of layout around grounds (RF transceiver)

3.6.2 Front-end module (SKY66122-11)

Points to note in the design of the wiring patterns for grounds are as follows.

- The front-end module's exposed die pad and RF circuit GND must have as many GND vias as possible and short between the top layer and the bottom layer to have low impedance.

- Use the second layer as the ground layer. It is recommended that the second layer be solid plane GND.

- Connect the GND(pin5), GND(pin6), GND(pin8), GND(pin10), GND(pin12), GND(pin13), GND(pin15), GND(pin17), GND(pin19), GND(pin21), GND(pin22), GND(pin23), GND(pin24), GND(pin25), GND(pin26), GND(pin27), GND(pin28), GND(pin30), GND(pin32), GND(pin34) and GND(pin 36) pins to the exposed die pad in the surface layer and connect them to the ground (second) layer through via holes along the shortest possible paths.

- Do not place signal lines under the exposed die pad.

Figure 3-10 shows an example of the layout around grounds for front-end module.

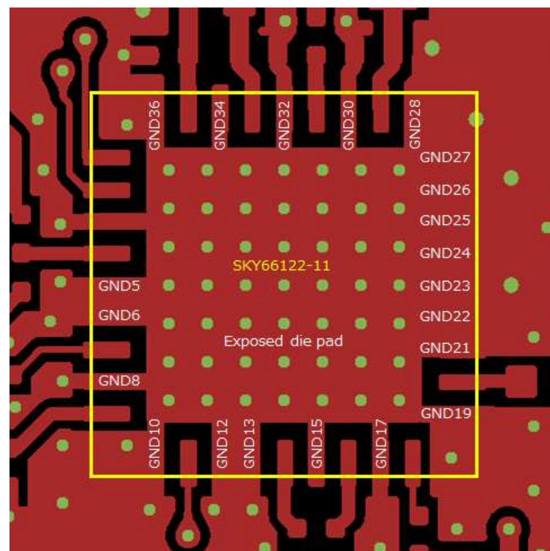

Figure 3-10 : Example of layout around grounds (front-end module)

3.6.3 The outer periphery of the board

The outer periphery of the board must be surrounded by GND patterns, and as many GND vias as possible must be placed. This is the area framed in yellow in Figure 3-10.

This is to prevent radio wave radiation from the board.

Figure 3-11 shows an example of the layout around the outer periphery of the board.

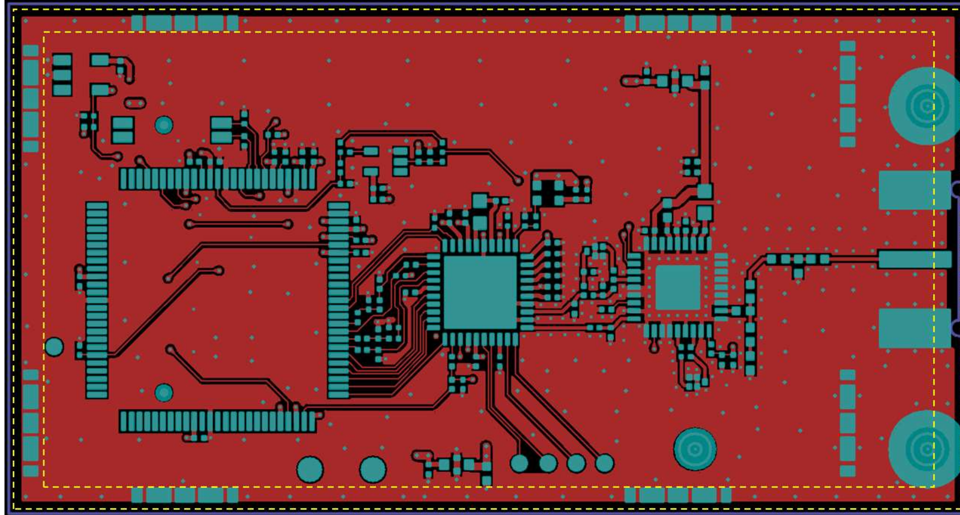

Figure 3-11 : Example of layout around the outer periphery of the board

3.6.4 Metal case

It is recommended to install a metal case in the RF circuit area. This is to prevent spurious radiation from board patterns other than the antenna.

In tests using antenna, spurious that did not exist in the wired condition may be found. Especially when aiming for FCC certification of the module, shielding must be installed.

When shielding the RF circuit, connect the outer periphery of the metal case to the board GND as much as possible. It is necessary to connect the outer periphery of the metal case to the board GND at intervals of at least λ/2. (When shielding 10GHz spurious, it is 1.5 cm or less.)

3.6.5 Connection of mother board and daughter board

When combining a mother board and a daughter board, such as the evaluation kit introduced in this document, it is recommended to strengthen the GND connection between the two boards.

Depending on how the parent board and daughter board are connected, the board may act as an antenna and radiate unwanted signals generated within the board.

If unwanted signals radiated from the board are input through the antenna, RX characteristics may degrade.

Figure 3-12 shows an example of connecting GND between two boards.

The left figure shows the case when the GND connection is not strengthened. The GND connection is at the PCB connector only. In this case, unwanted signals may be radiated from the board.

The right figure shows the case when the GND connection is strengthened. The GND connection is strengthened using metal screws. In this case, no unwanted signals are radiated from the board.

If metal screws are used, the board resist must be removed from the connection area.

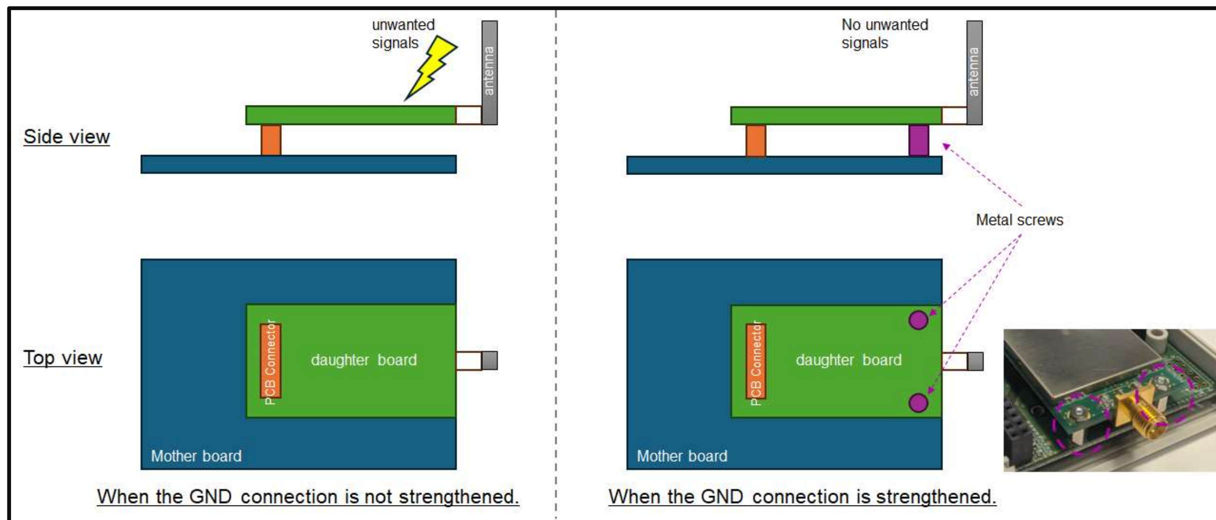

Figure 3-12 : Example of connecting GND between two boards

4. Circuit Diagram for Reference

4.1 Circuit diagram

Figure 4-1 is a circuit diagram of the RTK0EE0017D11004BJ evaluation kit for reference.

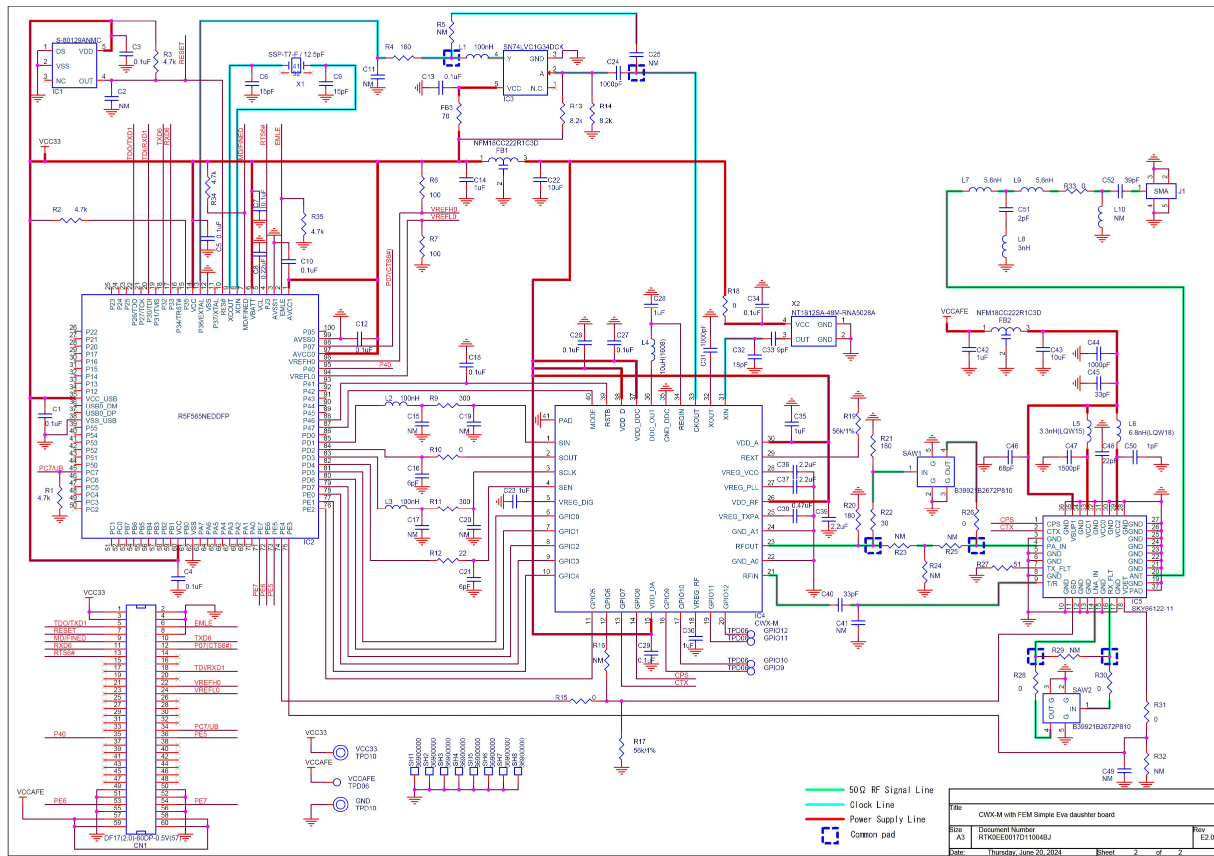

Figure 4-1 Circuit diagram

4.2 Bill of materials

Table 4-1 bill of materials in the reference diagram of circuits shown in Figure 4-1.

Table 4-1 Bill of materials

Patrs ID	Reference	Type	Patrs number	Manufacture	Note
CN1	DF17(2.0)-60DP-0.5V(57)	Connector	DF17(2.0)-60DP-0.5V(57)	HIROSE	
C1,C3,C4,C5,C7,C10,C12,C13,C18,C26,C27,C29,C34	0.1uF	Capacitor	GRM033R61C104KE84D	Murata	C0603/X5R/10%/16V
C2,C11,C15,C17,C19,C20,C25,C41,C49	NM	Capacitor	-	-	Not mounted, C0603
C6,C9	15pF	Capacitor	GRM0332C1H150JA01D	Murata	C0603/CH/5%/50V
C8	0.22uF	Capacitor	GRM033R61A224KE90D	Murata	C0603/X5R/10%/10V
C14,C23,C28,C30,C35,C42	1uF	Capacitor	CL03A105KP3NSNC	SAMSUNG	C0603/X5R/10%/10V
C16,C21	6pF	Capacitor	GRM0335C1H6R0BA01D	Murata	C0603/C0G/±0.1pF/50V
C22,C43	10uF	Capacitor	GRM155R61A106ME11D	Murata	C1005/X5R/20%/10V
C24,C31,C44	1000pF	Capacitor	GRM033R71H102KA12D	Murata	C0603/X7R/10%/50V
C32	18pF	Capacitor	GRM0332C1H180JA01D	Murata	C0603/CH/5%/50V
C33	9pF	Capacitor	GRM0335C1H9R0BA01D	Murata	C0603/C0G/±0.1pF/50V
C36,C37,C39	2.2uF	Capacitor	GRM033R61A225KE47D	Murata	C0603/X5R/10%/10V
C38	0.47uF	Capacitor	LMK063BBJ474KPLF	Taiyo yuden	C0603/X5R/10%/10V
C40,C45	33pF	Capacitor	GRM0332C1H330JA01D	Murata	C0603/CH/5%/50V
C46	68pF	Capacitor	GRM0332C1H680JA01D	Murata	C0603/CH/5%/50V
C47	1500pF	Capacitor	GRM033R71H152KA12D	Murata	C0603/X7R/10%/50V
C48	22pF	Capacitor	GRM0332C1H220JA01D	Murata	C0603/CH/5%/50V
C50	1pF	Capacitor	GRM0335C1H1R0BA01D	Murata	C0603/C0G/±0.1pF/50V
C51	2pF	Capacitor	GRM1555C1H2R0BA01D	Murata	C1005/C0G/±0.1pF/50V
C52	39pF	Capacitor	CL05C390JB5NNNC	SAMSUNG	C1005/C0G/5%/50V
FB1,FB2	NFM18CC222R1C3D	EMI Filter	NFM18CC222R1C3D	Murata	2200pF/16V/1608
FB3	70	Ferrite bead	BLM03AG700SN1	Murata	0603
IC1	S-80129ANMC	Delay IC	S-80129ANMC-JCOxU	SII	SOT-23-5
IC2	R5F565NEDDFP	MCU	R5F565NEDDFP	RENESAS	100-Pin, LFQFP
IC3	SN74LVC1G34DCK	Buffer	SN74LVC1G34DCK	TI	SC70-5
IC4	CWX-M	RF transceiver	R9A06G062GNP	RENESAS	40-Pin, HVQFN
IC5	SKY66122-11	Front-end module	SKY66122-11	Skyworks	36-pin, 6 x 6 x 0.9 mm
J1	SMA	SMA connector	73251-1150	MOLEX	1.57 End Launch
L2,L3,L1	100nH	Inductor	LQP03TNR10H02D	Murata	L0603
L4	10uH(1608)	Inductor	MLZ1608M100WT	TDK	L1608
L5	3.3nH(LQW15)	Inductor	LQW15AN3N3C80	Murata	L1005
L6	6.8nH(LQW18)	Inductor	LQW18AN6N8C00	Murata	L1608
L7,L9	5.6nH	Inductor	LQG15HS5N6B02D	Murata	L1005
L8	3nH	Inductor	LQG15HS3N0B02D	Murata	L1005
L10	NM	Inductor	-	-	Not mounted, L1005
R1,R2,R3,R34,R35	4.7k	Resistor	RK73B1HTTC472J	KOA	R0603
R4	160	Resistor	RK73B1HTTC161J	KOA	R0603
R6,R7	100	Resistor	RK73B1HTTC101J	KOA	R0603
R5,R16,R29,R32	NM	Resistor	-	-	Not mounted, R0603
R10,R15,R18,R26,R28,R30,R31	0	Resistor	RK73Z1HTTC	KOA	R0603
R9,R11	300	Resistor	RK73B1HTTC301J	KOA	R0603
R12	22	Resistor	RK73B1HTTC220J	KOA	R0603
R13,R14	8.2k	Resistor	RK73B1HTTC822J	KOA	R0603
R17,R19	56k/1%	Resistor	RK73H1HTTC5602F	KOA	R0603/1%
R20	180 (for FCC/ARIB) 100 (for ETSI)	Resistor	RK73B1HTTC181J (for FCC/ARIB) RK73B1HTTC101J (for ETSI)	KOA	R0603
R21	180 (for FCC/ARIB) NM (for ETSI)	Resistor	RK73B1HTTC181J (for FCC/ARIB) Not mounted (for ETSI)	KOA	R0603
R22	30 (for FCC/ARIB) NM (for ETSI)	Resistor	RK73B1HTTC300J (for FCC/ARIB) Not mounted (for ETSI)	KOA	R0603
R23	NM (for FCC/ARIB) 68 (for ETSI)	Resistor	Not mounted (for FCC/ARIB) RK73B1HTTC680J (for ETSI)	KOA	R0603
R24	NM (for FCC/ARIB) 100 (for ETSI)	Resistor	Not mounted (for FCC/ARIB) RK73B1HTTC101J (for ETSI)	KOA	R0603
R25	NM (for FCC/ARIB) 0 (for ETSI)	Resistor	Not mounted (for FCC/ARIB) RK73Z1HTTC (for ETSI)	KOA	R0603
R26	0 (for FCC/ARIB) NM (for ETSI)	Resistor	RK73Z1HTTC (for FCC/ARIB) Not mounted (for ETSI)	KOA	R0603
R27	51	Resistor	RK73B1HTTC510J	KOA	R0603
R33	0	Resistor	RK73Z1ETTP	KOA	R1005
SAW1	B39921B2672P810 (for FCC) B39931B2645P810 (for ARIB) NM (for ETSI)	SAW filter	B39921B2672P810 (for FCC) B39931B2645P810 (for ARIB) Not mounted (for ETSI)	Qualcomm	5-pin, 1.4 x 1.1 x 0.45 mm
SAW2	B39921B2672P810 (for FCC) B39931B2645P810 (for ARIB) B39871B2600P810 (for ETSI)	SAW filter	B39921B2672P810 (for FCC) B39931B2645P810 (for ARIB) B39871B2600P810 (for ETSI)	Qualcomm	5-pin, 1.4 x 1.1 x 0.45 mm
X1	SSP-T7-F / 12.5pF	Crystal resonator	SSP-T7-F / 12.5pF	SII	-40 to +85deg-C
X2	NT1612SA-48M-RNA5028A	TCXO	NT1612SA-48M-RNA5028A	NDK	Clipped sine wave
SH1,SH2,SH3,SH4,SH5,SH6,SH7,SH8	36900000	Shield Clip	36900000	Würth Elektronik	6.5 x 0.8 x 1.28 mm

5. Configuration of Application Note

This Application Note contains the following contents listed in Table 5-1 and Table 5-2.

Table 5-1 : Configuration of Application Note-1

File organization	Description
r01an8154ej0100-rtk0ee0017d11004bj(R9A06G062GNP).pdf	This application note
r01an8154ej0100-rtk0ee0017d11004bj-hw-design	
01_Daughter board	
01_Circuit_Diagram	
RTK0EE0017D11004BJ_Circuit_Diagram.pdf	Circuit diagram
02_Parts_List	
RTK0EE0017D11004BJ_Parts_List.pdf	Parts list
03_Gerber_Data	
RTK0EE0017D11004BJ_LA.G01	L1: Analog signal, Parts layer
RTK0EE0017D11004BJ_L2.G02	L2: GND layer
RTK0EE0017D11004BJ_L3.G03	L3: Power supply, GND layer
RTK0EE0017D11004BJ_LB.G04	L4: Digital signal, GND layer
RTK0EE0017D11004BJ_RA.G05	L1: Resist
RTK0EE0017D11004BJ_RB.G06	L4: Resist
RTK0EE0017D11004BJ_SA.G07	L1: Silk
RTK0EE0017D11004BJ_SB.G08	L4: Silk
RTK0EE0017D11004BJ_GA.G09	Dimensions
RTK0EE0017D11004BJ_MA.G11	L1: Solder Mask
RTK0EE0017D11004BJ_MB.G12	L4: Solder Mask
RTK0EE0017D11004BJ_HO.dr1	Drill data
04_Board_Layout_Diagram	
RTK0EE0017D11004BJ_Board_Layout_Diagram.pdf	Board layout diagram
05_Board_Design_Checklist	
RTK0EE0017D11004BJ_Board_Design_Checklist.xlsx	Board design checklist

Table 5-2 : Configuration of Application Note-2

File organization	Description
r01an8154ej0100-rtk0ee0017d11004bj(R9A06G062GNP).pdf	This application note
r01an8154ej0100-rtk0ee0017d11004bj-hw-design	
02_Mother board	
01_Circuit_Diagram	
RTK0EE0013D12002BJ_Circuit_Diagram.pdf	Circuit diagram
02_Parts_List	
RTK0EE0013D12002BJ_Parts_List.pdf	Parts list
03_Gerber_Data	
RTK0EE0013D12002BJ_LA.G01	L1: Signal, Parts layer
RTK0EE0013D12002BJ_L2.G02	L2: GND layer
RTK0EE0013D12002BJ_L3.G03	L3: Power supply layer
RTK0EE0013D12002BJ_LB.G04	L4: Signal, Parts layer
RTK0EE0013D12002BJ_RA.G05	L1: Resist
RTK0EE0013D12002BJ_RB.G06	L4: Resist
RTK0EE0013D12002BJ_SA.G07	L1: Silk
RTK0EE0013D12002BJ_SB.G08	L4: Silk
RTK0EE0013D12002BJ_GA.G09	Dimensions
RTK0EE0013D12002BJ_MA.G11	L1: Solder Mask
RTK0EE0013D12002BJ_MB.G12	L4: Solder Mask
RTK0EE0013D12002BJ_HO.dr1	Drill data
04_Board_Layout_Diagram	
RTK0EE0013D12002BJ_Board_Layout_Diagram.pdf	Board layout diagram

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Nov.28.2025	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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