RX Family

Ethernet Hardware Design Guide

Introduction

This application note describes precautions when designing boards that use the Ethernet functions. Note that the information in this document is based on the corresponding information for the Ethernet communication board developed at Renesas for internal evaluation.

Target Device

RX64M Group
RX71M Group
RX72M Group
RX72N Group

Contents

1. Board Design

1.1 Layer Structure

An RX MCU, as well as a physical layer chip (PHY-LSI), an SDRAM, etc. are mounted on the Ethernet communication board. Taking into consideration the large number of wiring patterns, the need for noise suppression for specific signals, the size of the board, and the like, the board was designed with a six-layer structure.

The layer structure of the Ethernet communication board is shown in Table 1. Note that, in order to perform noise suppression for specific signals*1, layer L2 has been made the ground layer, and layer L5 has been made the power supply layer.

Note 1. Refers to the MII/RMII signals in Table 2 and the SDRAM address/data bus and control signals

Table 1 Ethernet Communication Board Layer Structure

Layer	Usage
L1	Component surface (signal layer)
L2	Ground layer
L3	Signal layer
L4	Signal layer
L5	Power supply layer
L6	Solder surface (signal layer)

Table 2 MII/RMII Signals

MII	RMII
ETn_TX_CLK	—
ETn_RX_CLK	REF50CKn
ETn_ERXD3 to ETn_ERXD0	RMIIn_RXD1 to RMIIn_RXD0
ETn_ETXD3 to ETn_ETXD0	RMIIn_TXD1 to RMIIn_TXD0

1.2 Component Layout

The component layout of the Ethernet communication board is shown in Figure 1, and precautions during layout are described below.

- The maximum SDCLK frequency of the SDRAM is 80 MHz*1, so when mounting the SDRAM, give priority to placing it in the vicinity of an RX MCU.
- Lay out the components such that the SDRAM data bus and the media independent interface (MII) or reduced media independent interface (RMII) signals (particularly ET1_RX_CLK on MII channel 1) are as short as possible and do not run alongside one another. In particular, be sure that the signal patterns of ET1_RX_CLK and D5/D6 (of the SDRAM data bus) do not run parallel to one another. (See Figure 1.)
- Lay out the components such that other lines do not run alongside the data bus and the MII or RMII signals either.

Note 1. The maximum SDCLK frequency of RX64M and RX71M group is 60 MHz.

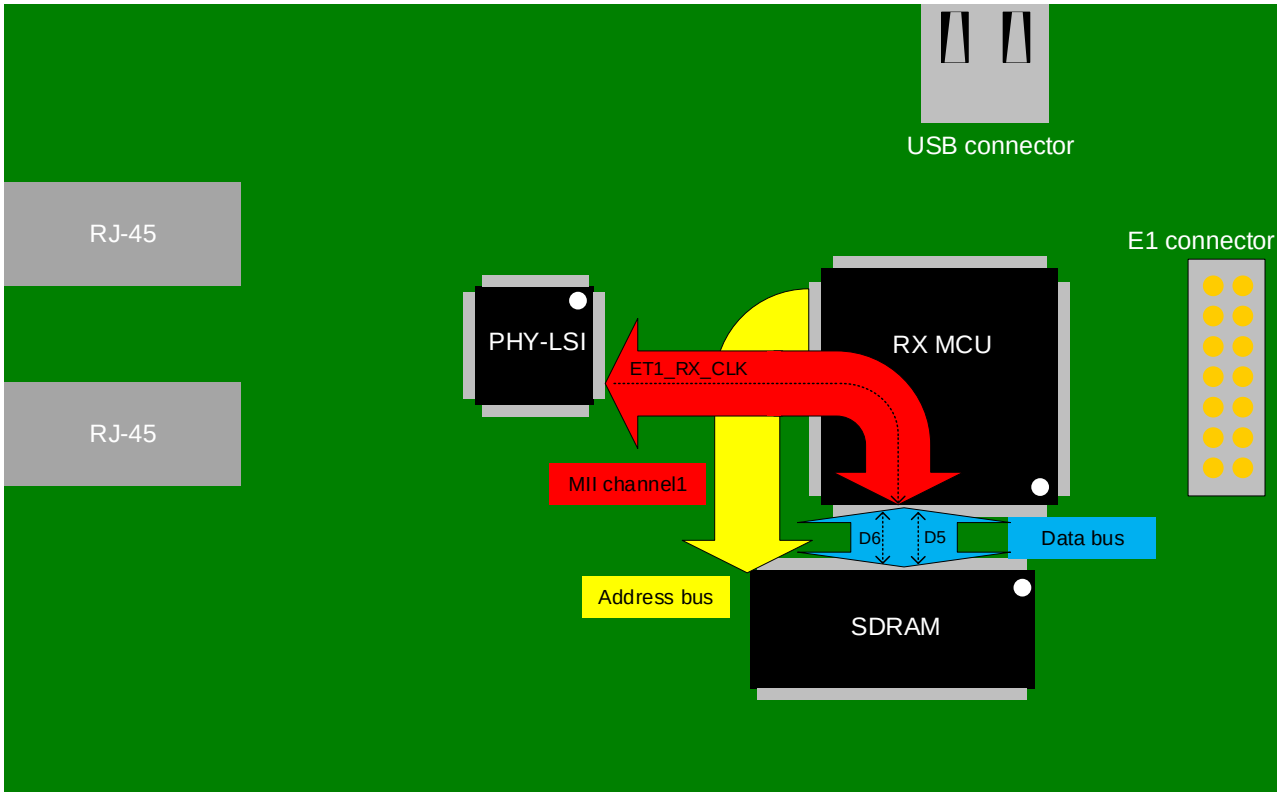


Figure 1 Component Layout

1.3 Pattern Design

1.3.1 MII/RMII/SDRAM Signal Patterns

The following are some precautions for when designing MII, RMII, and SDRAM signal patterns. Note that the MII and RMII signals in this section refer to the signals shown in Table 2.

1. Give priority to wiring D7 to D0 (particularly D5 and D6) of the data bus of the SDRAM on layer L1, and to making it as short as possible. (See (1) in Figure 2.)
2. In order to allow the return current from the SDRAM and MII/RMII signals to readily return, make layer L2 the ground layer.
3. As a result of having given priority to D7 to D0 of the data bus of the SDRAM, it will not be possible to wire the MII signals (particularly ET1_RX_CLK) on layer L1 alone. For this reason, wire it on layers L1 and L3 instead. Note that when layer L3 is used, the return current can readily return since the ground layer (layer L2) is immediately above. (See (2) in Figure 2.)
4. The components have been laid out with priority given to wiring D7 to D0 of the data bus of the SDRAM. As a result, it will not be possible to wire D15 to D8 of the data bus on layer L1 alone. For this reason, wire it on layers L1 and L3 instead. Note that when layer L3 is used, the return current can readily return since the ground layer (layer L2) is immediately above. (See (3) in Figure 2.)
5. As a result of having wired the SDRAM data bus and the MII signals on layers L1 and L3, it will not be possible to wire the SDRAM address bus on those layers. For this reason, wire it on layers L1 and L4 instead. (See (4) in Figure 2.)
6. Wire the signals other than those mentioned above on layer L6.
7. Design the inter-layer thicknesses, with the exception of that between layers L3 and L4, to be one-third the distance (H) between patterns running alongside one another (i.e., to be 1/3H) in order to allow return currents to readily return. (See Figure 3.) In addition, the inter-layer thickness affects impedance, so if there are signals subject to impedance control, take this into account when designing the board thicknesses. In the case of the Ethernet communication control board, based on impedance control and the board thicknesses that were possible for the board manufacturer that was asked to do the design, an inter-layer thickness of 0.1 mm was used, except for between layers L3 and L4.
8. Make the thickness between layers L3 and L4 substantial in order to prevent the effects of coupling. In the case of the Ethernet communication board, this thickness was decided by subtracting the inter-layer thickness between layers L1 and L3 and that between layers L4 and L6 from the board thickness. Given that the board thickness was 1.4 mm, an inter-layer thickness of 0.8 mm between layers L3 and L4 was used.
9. Design the distance between the SDRAM signal pattern and the MII/RMII signal pattern based on the 3W rule (i.e., a distance of at least 2W+α for a line width of W). (See Figure 4.)
10. Impedance control is necessary for the SDRAM and MII/RMII signals. Design the board with a characteristic impedance of 50Ω ±10%. In the case of the Ethernet communication board, a line width of 0.16 mm was used for layers L1 and L6, and a line width of 0.12 mm was used for layers L3 and L4.
11. When wiring the MII channel 1 signal from an RX MCU, avoid having the lines run alongside those of the SDRAM signals. In particular, be sure to lay out the patterns from an RX MCU such that the ET1_RX_CLK and D5 and D6 signals run in the opposite directions. (See Figure 5.)
12. Design the board such that, on the ground layer (power supply layer) along the return current path, there are no GND (power supply) slits or ground (power supply) separations. (See Figure 6.)

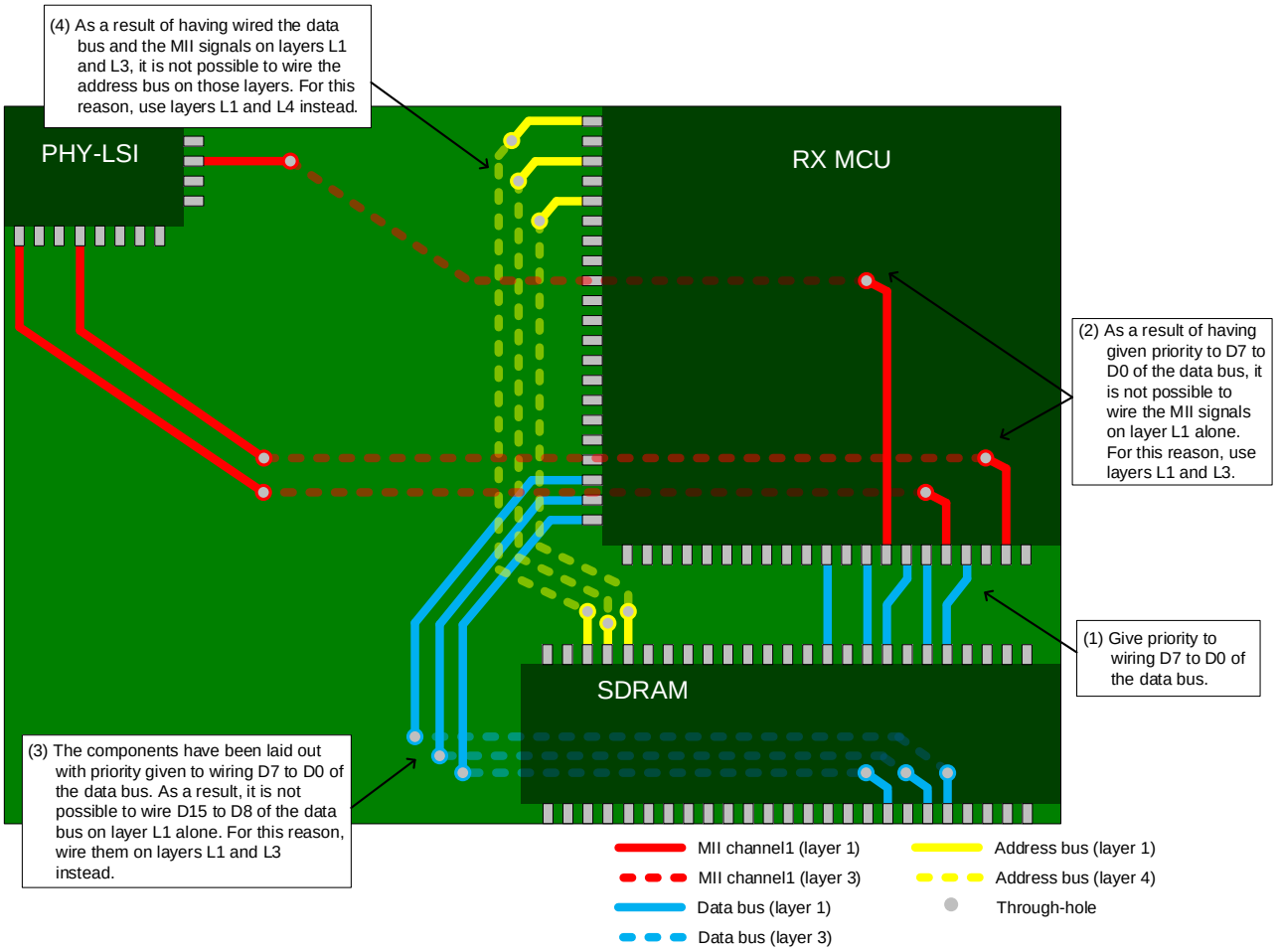


Figure 2 Pattern Layout Image (Transparency Diagram from Perspective of Layer L1)

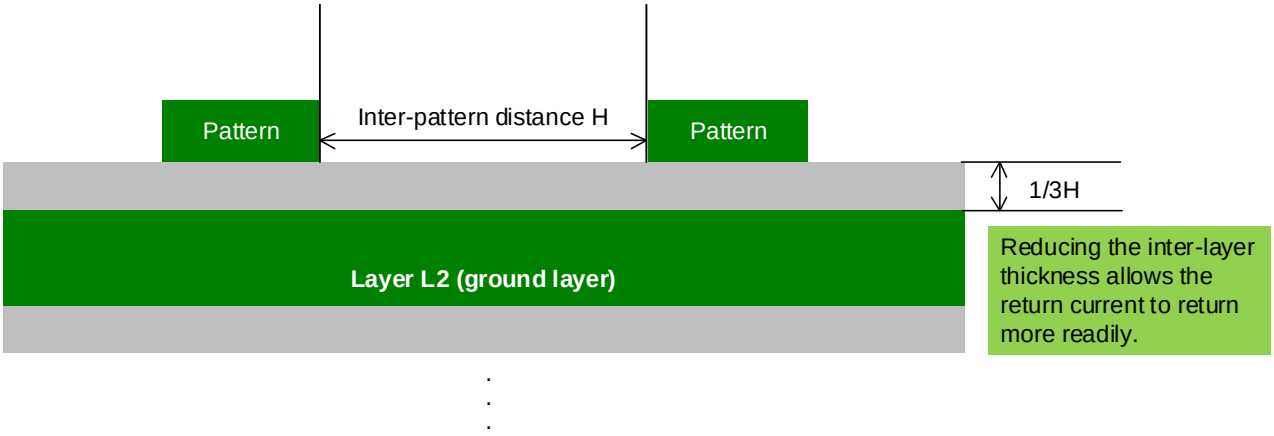


Figure 3 Return Current (Inter-layer Distance)

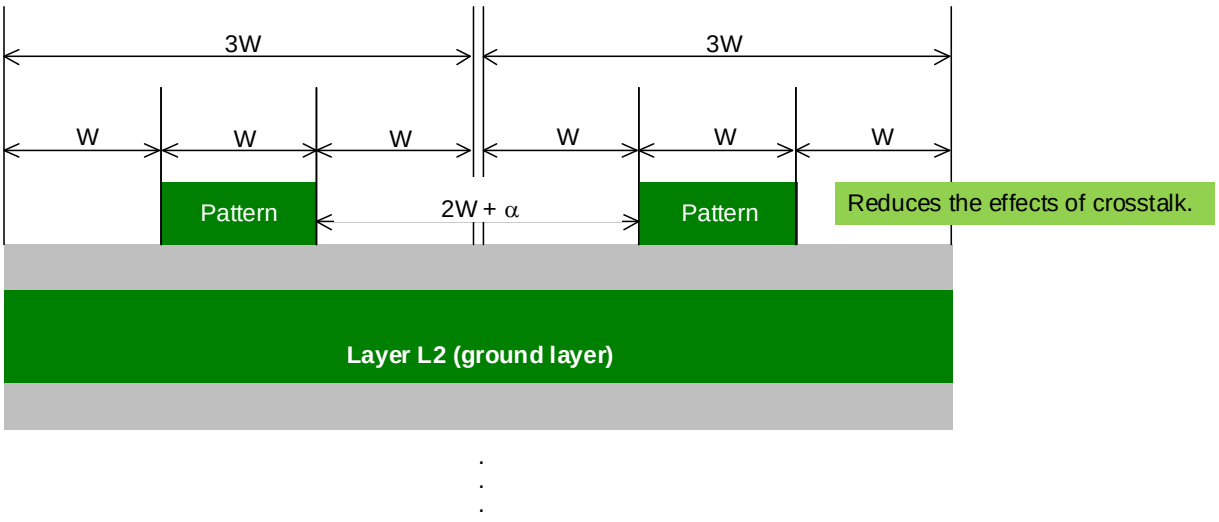


Figure 4 The 3W Rule

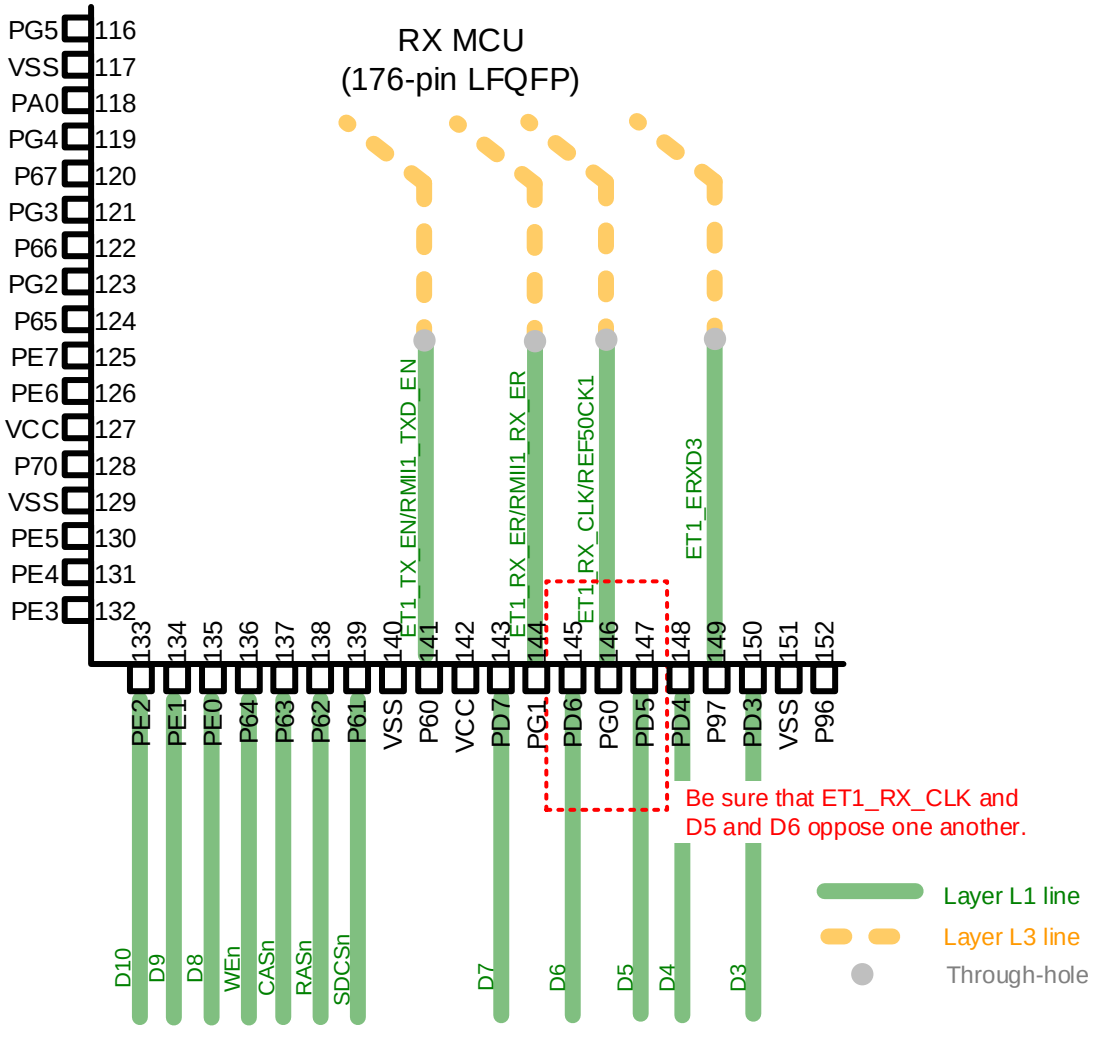
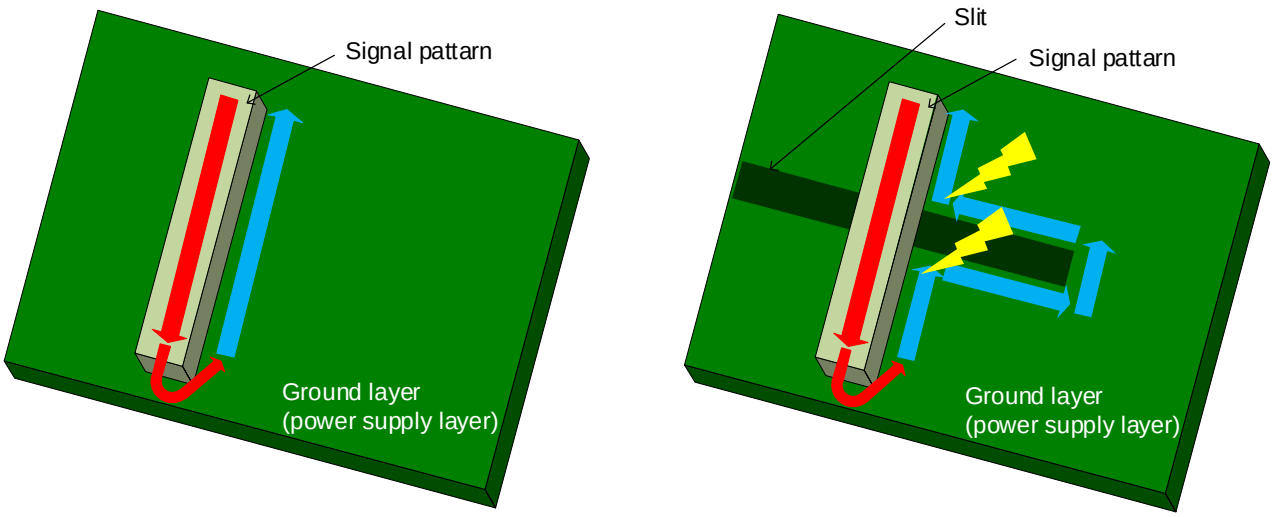


Figure 5 Wiring Example



(a) If there are no obstructions on the return current path, disturbances will not arise in the magnetic field and noise will be suppressed

(b) If there are obstructions on the return current path, the magnetic field will be disturbed and noise will arise due to the presence of slits and separations

Figure 6 Return Current (Facilitated by Ground Layer)

1.3.2 MDI Signals

The following are some precautions for when designing patterns for the medium dependent interface signal (MDI signal).

- Do not place the MDI signal lines near any other signals (both on the same layer and on different layers).
- Make the MDI signal lines as short as possible.
- Impedance control is necessary for the MDI signals. For the characteristic impedance required by the MDI transmission path, follow the guidelines of the manufacturer of the PHY chip being used.
- Make all differential signals isometric using differential pairs.
- Lay out components on the MDI signals such that the differential pairs are symmetric. (See Figure 7.)
- Lay out the termination network in accordance with the guidelines of the hardware manufacturer.

(a) Symmetric placement (good)

(b) Symmetric placement (bad)

Figure 7 Layout of Components on Differential Signal Transmission Paths

2. Board Specifications

The following are the board specifications for the Ethernet communication board developed in accordance with this guide.

- Board layers: 6
- Board thickness: 1.43 mm
- Per-layer signal details:
  Layer L1 Ethernet signals (MII/RMII/MDI), data bus,*1 address bus,*1 strobe signal*1
  Layer L2 Ground layer
  Layer L3 Ethernet signals (MII/RMII), data bus,*1 strobe signal*1
  Layer L4 Power supply, address bus*1
  Layer L5 Power supply layer
  Layer L6 Ethernet signals (MDI), strobe signal*1

Note 1. SDRAM signals

- Pattern specifications
  — Normal pattern width is 0.15 mm.
  — Pattern width of specific MII/RMII/SDRAM signals that are noise-suppressed is 0.16 mm for layers L1 and L6, and 0.12 mm for layers L3 and L4.
  — Pattern width of specific MDI signals that are noise-suppressed is 0.1 mm.

- Layer structure:

Layer	Thickness (mm)	Material
1	0.025	Copper plating
	0.018	Copper foil
	0.100	Prepreg
2	0.035	Copper foil
	0.100	Core material
3	0.035	Copper foil
	0.800	Prepreg
4	0.035	Copper foil
	0.100	Core material
5	0.035	Copper foil
	0.100	Prepreg
6	0.018	Copper foil
	0.025	Copper plating

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Nov.11.16	—	First edition issued
1.01	Jan.31.20	1 2 to 10	Changed the group name to “RX Family” in the document title. Added RX72M group and RX72N group to the target device. Changed “the RX64M and RX71M” to “RX MCU” int this document.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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