RX23E-A Group

Analog Front End Typical Characteristics

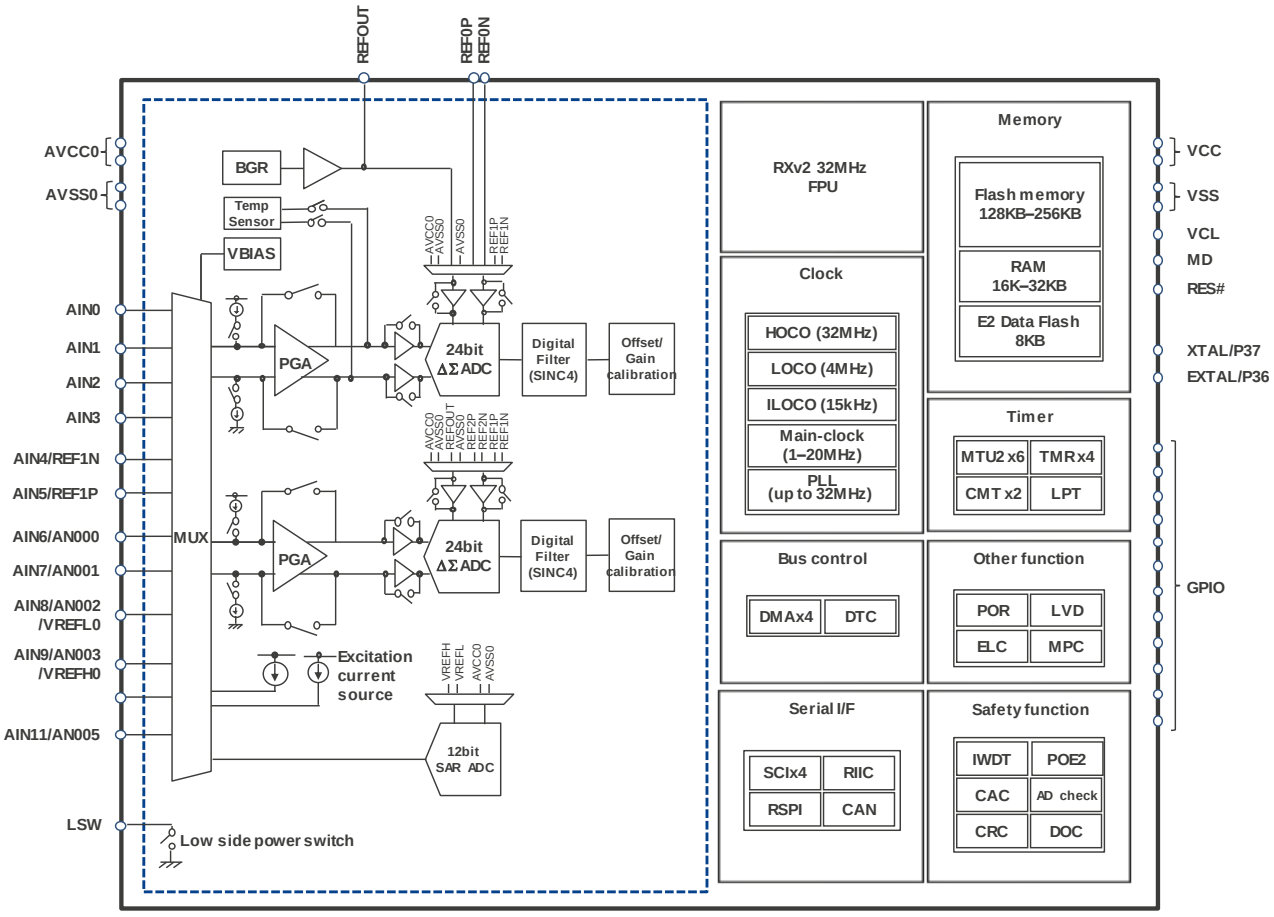
Summary

This document describes typical analog characteristics of 24bit Δ-Σ A/D converter (DSAD) and Analog Front End (AFE) integrated in RX23E-A.

Measurement conditions are described as below, unless otherwise specified.
AVCC0=5V, Ta=25°C, External VREF=2.5V, Normal mode, OPCR.DSADLVM bit=0 (*1)

See below for the meaning of abbreviations contained in this document.

Gain=1(DSAD)	:	PGA disabled / Buffer disabled
Gain=1(BUF)	:	PGA disabled / Buffer enabled
Gain=1(PGA)	:	PGA enabled / Buffer enabled
PRB	:	Positive Reference Buffer
NRB	:	Negative Reference Buffer



Target Device

RX23E-A

*1 OPCR.DSADLVM bit selects the operating voltage for Δ-ΣA/D. When the AVCC0 voltage is lower than 3.6 V, set it to 1. To use Δ-ΣA/D with high precision, set the AVCC0 voltage to 3.6 V or higher, and set this bit to 0.

Contents

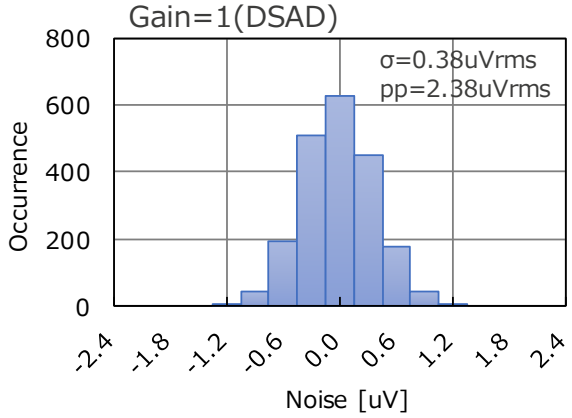
1. RX23E-A Analog Front End Features

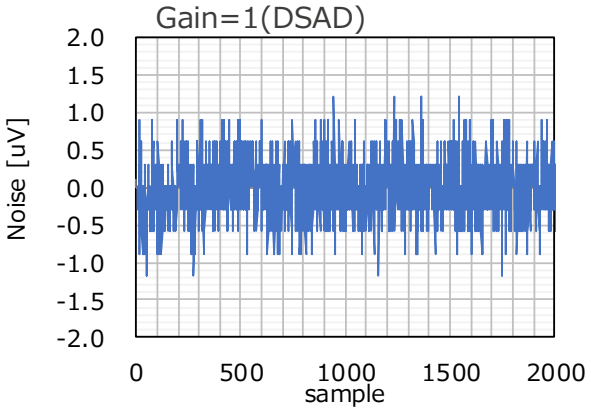
- Two 24-bit delta-sigma A/D converters
  A/D converter with up to 23-bit effective resolution (gain = 1, output data rate = 7.6 SPS)
- High-precision programmable gain instrumentation amplifier,
  30 nVRMS (gain = 128, output data rate = 7.6 SPS)
- Rail-to-rail programmable gain instrumentation amplifier (gain = 1 to 128)
- Two operating modes and programmable data rates,
  Normal mode: Output data rate of 7.6 SPS to 15625 SPS,
  Low power mode: Output data rate of 1.9 SPS to 3906 SPS
- Offset drift 10 nV/°C (gain = 128)
- Gain drift 1 ppm/°C (gain = 1 (PGA), gain = 2 to 128)
- Up to six differential inputs, 11 single-ended inputs
- Fourth-order sinc filter
- Simultaneous 50 Hz/60 Hz rejection (output data rate = 10, 54 SPS)
- Offset error and gain error calibration
- Inter-unit A/D conversion synchronized start
- Delta-sigma A/D input disconnect detection assist
- Delta-sigma A/D reference voltage external input
- Voltage reference output voltage: 2.5 V, temperature drift: 10 ppm/°C, output current: ±10 mA
- Excitation current sources: Up to four, Output current: 50 µA to 1000 µA,
  current matching: ±0.2%, drift matching: 5 ppm/°C
- Bias voltage generator output voltage: (AVCC0 + AVSS0)/2
- Temperature sensor: Accuracy ±5°C
- Low-side switch: 10 Ω on-resistance
- Low power-supply-voltage detectors
- Delta-sigma A/D input voltage fault detectors
- Delta-sigma A/D reference voltage fault detectors and disconnect detectors
- Excitation current source disconnect detectors

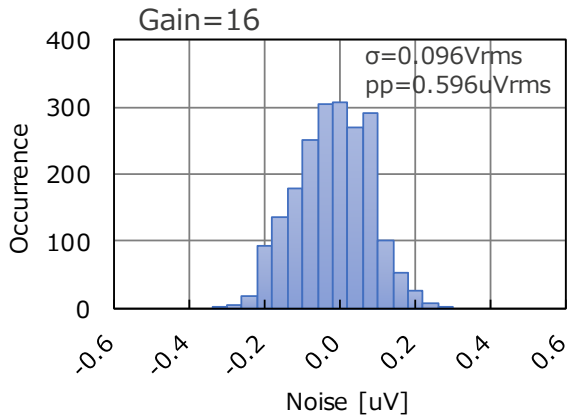
2. 24bit Delta-Sigma A/D Converter

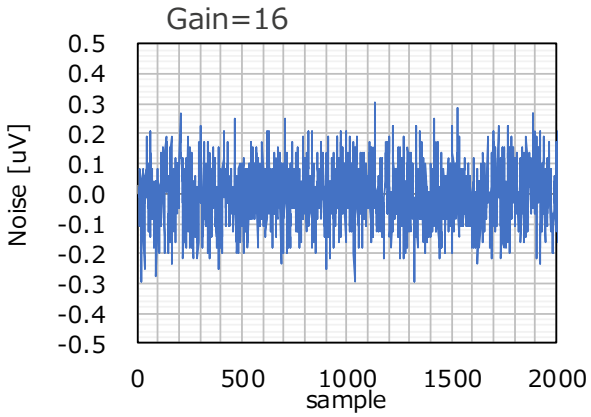
2.1 Noise histogram, Time domain waveform

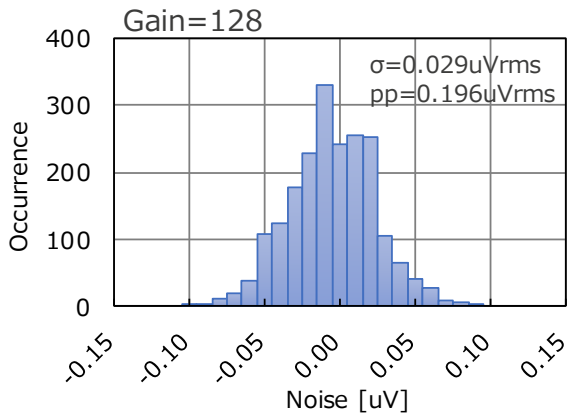
AVCC0=5V, Ta=25°C
Normal mode, Data rate=7.629sps, External VREF=2.5V, AIN=0V

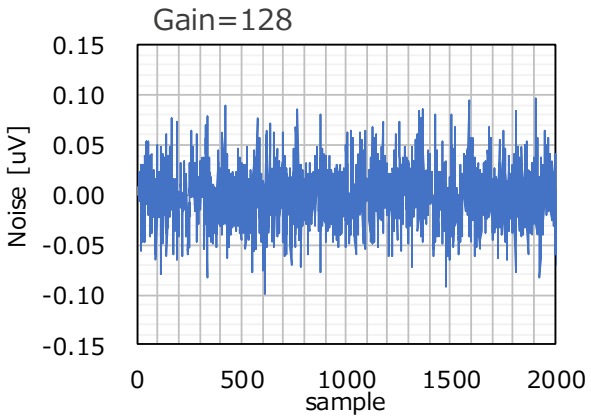




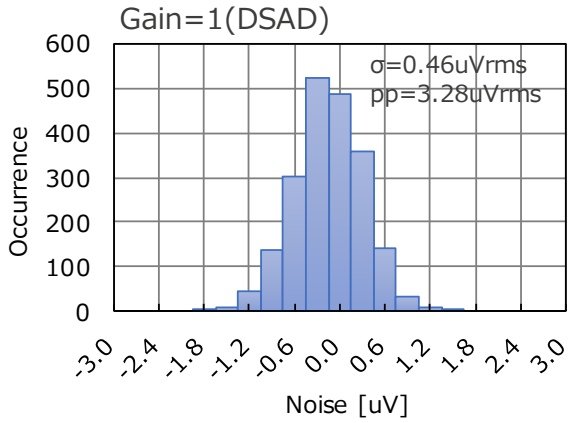


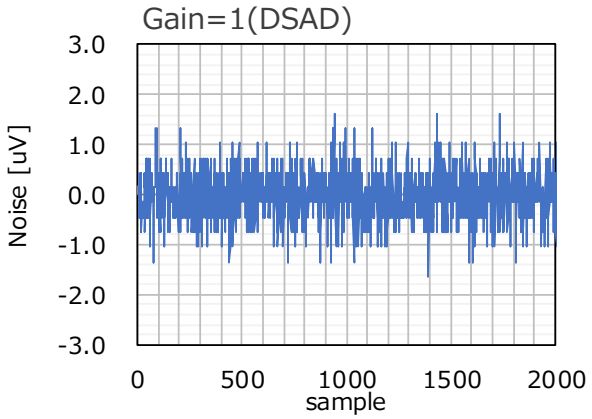


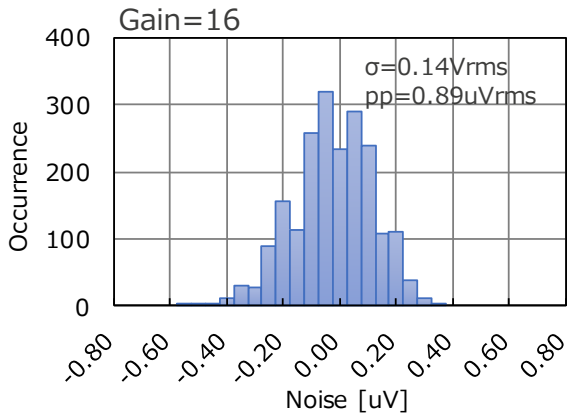


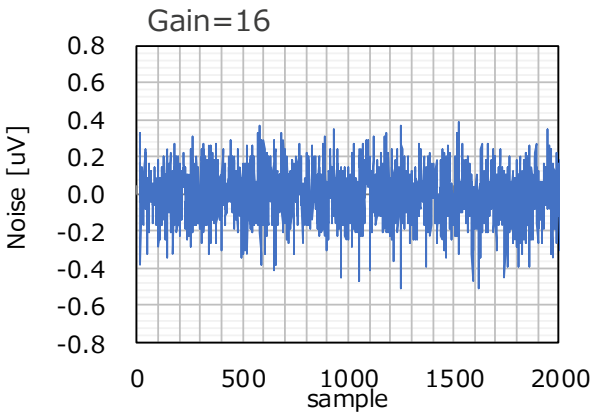


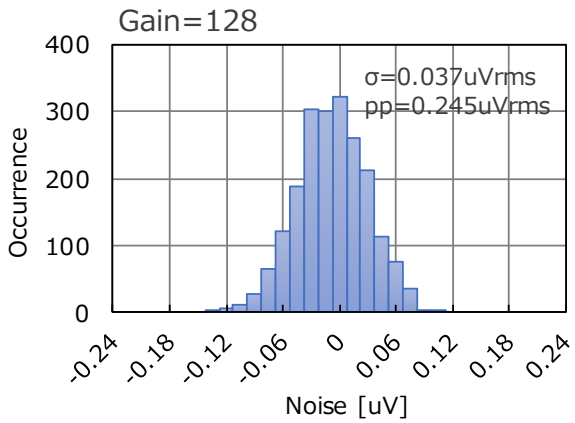
AVCC0=5V, Ta=25°C
Low power mode, Data rate=7.629ps, External VREF=2.5V, AIN=0V

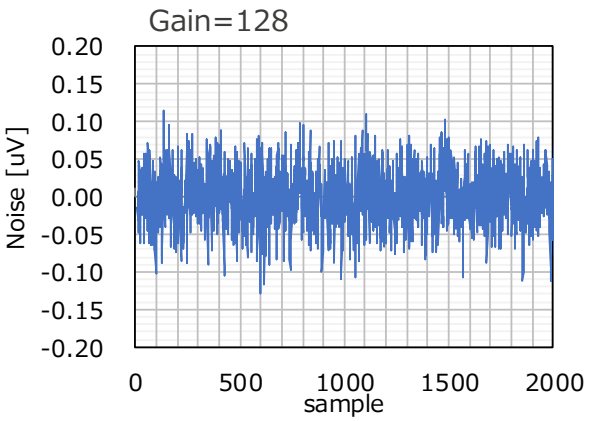






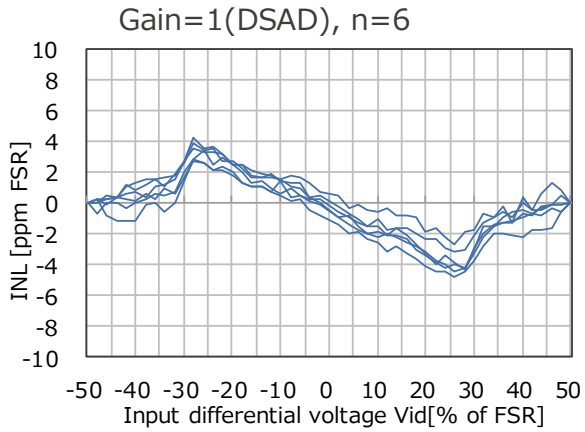


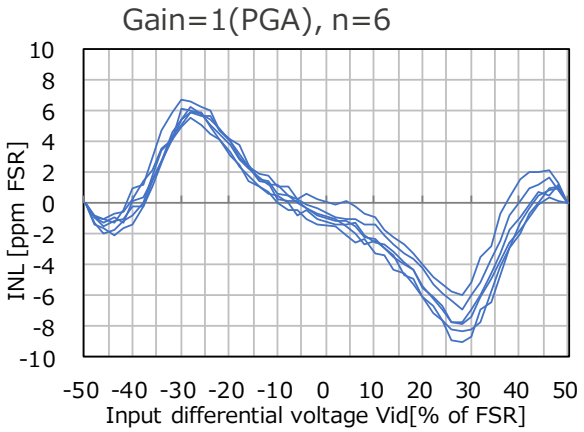


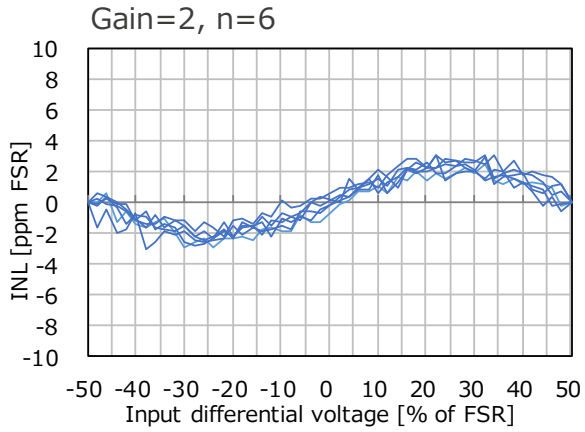


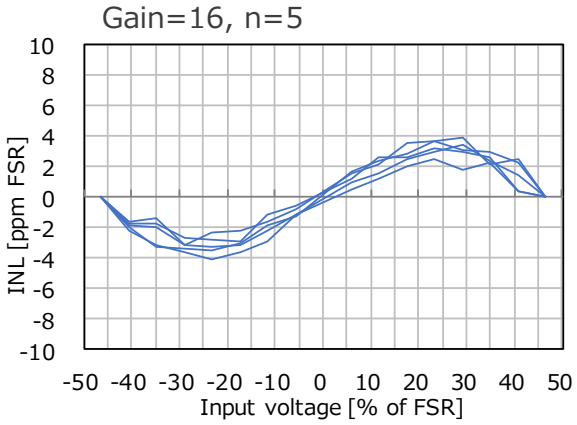
2.2 Integral nonlinearity error (INL)

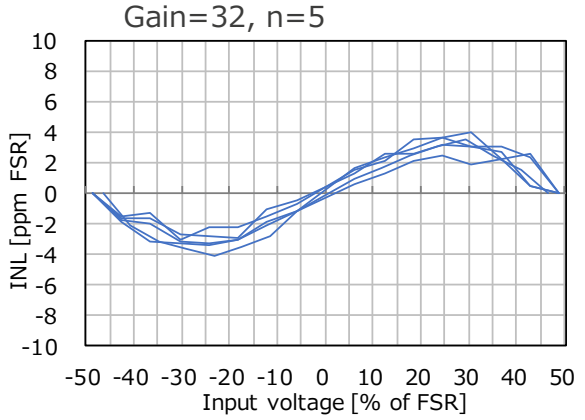
AVCC0=5V, Ta=25°C
Normal mode, External VREF=2.5V

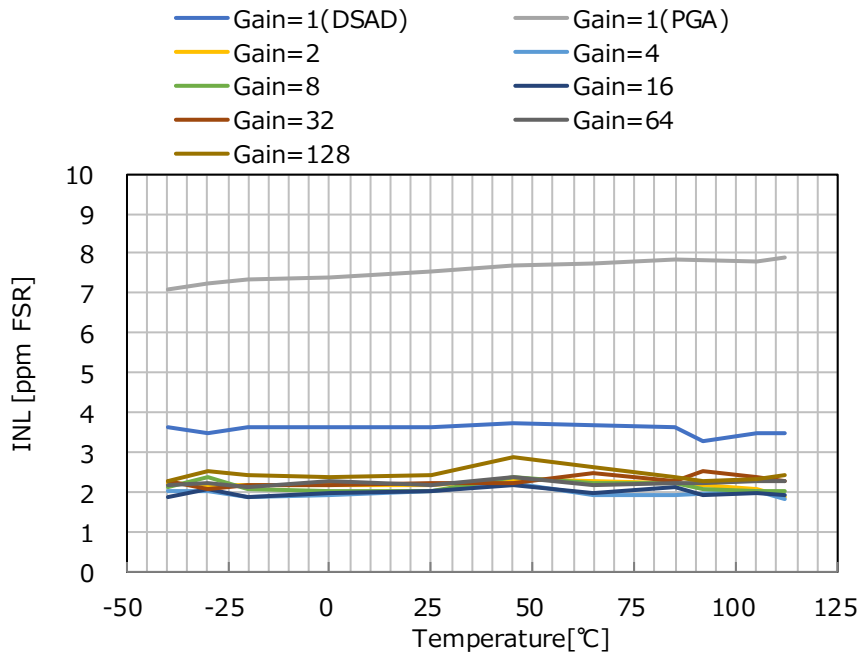


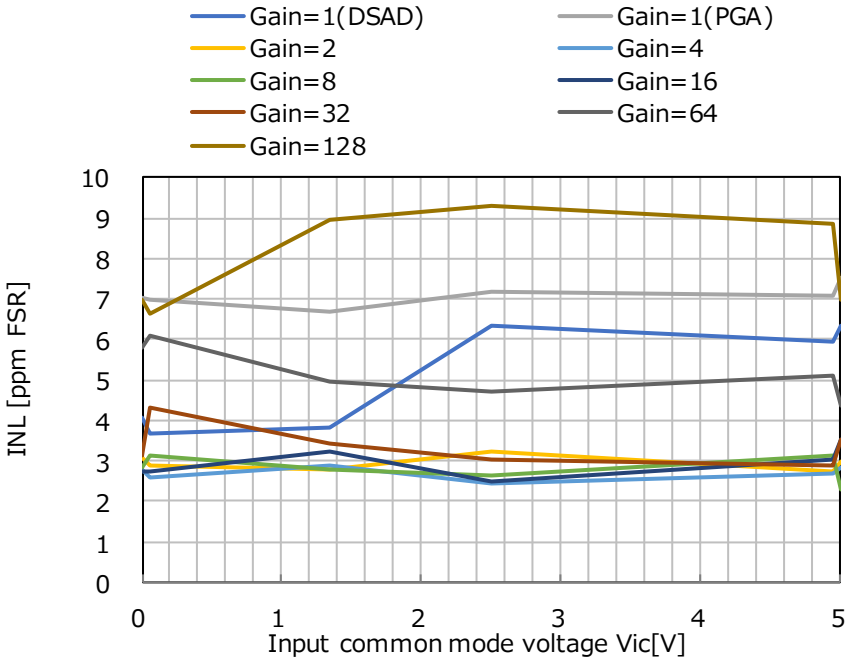






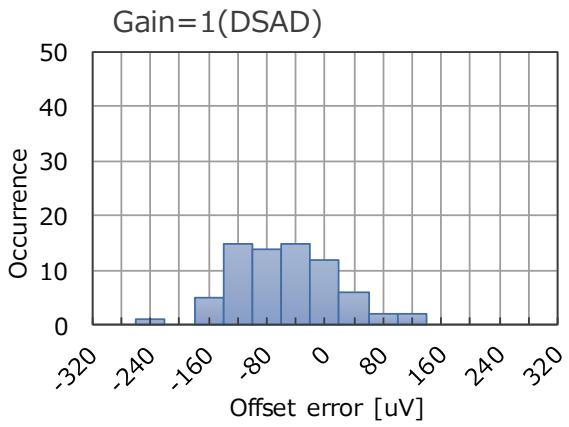


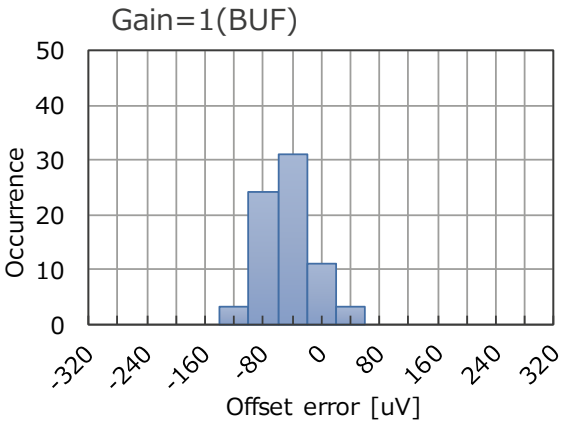

Gain=1(DSAD)
Gain=1(PGA)
Gain=2
Gain=4
Gain=8
Gain=16
Gain=32
Gain=64
Gain=128
INL [ppm FSR]
10
9
8
7
6
5
4
3
2
1
0
-50
-25
0
25
50
75
100
125
Temperature[℃]

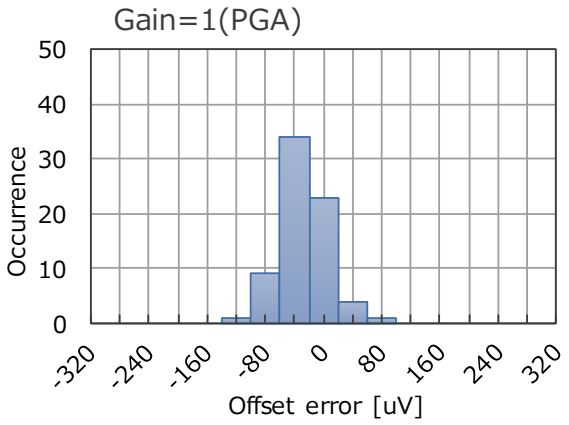

Gain=1(DSAD)
Gain=1(PGA)
Gain=2
Gain=4
Gain=8
Gain=16
Gain=32
Gain=64
Gain=128
INL [ppm FSR]
10
9
8
7
6
5
4
3
2
1
0
0
1
2
3
4
5
Input common mode voltage Vic[V]

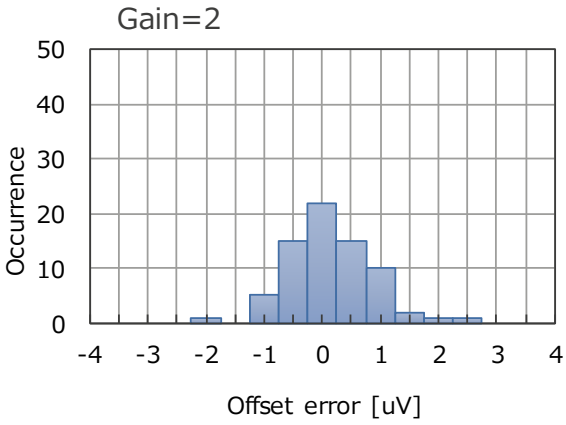
2.3 Offset error histogram

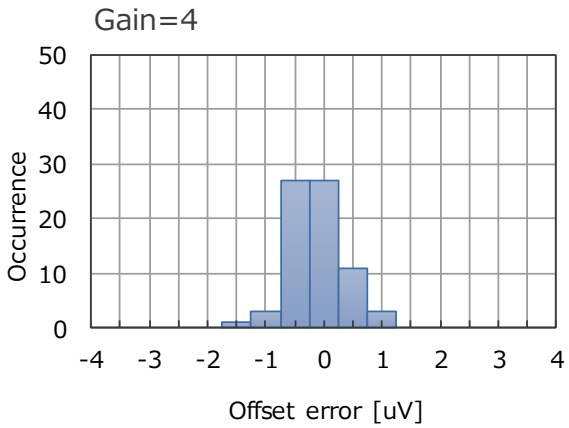
AVCC0=5V, Ta=25°C, n=72
After factory calibration of offset errors

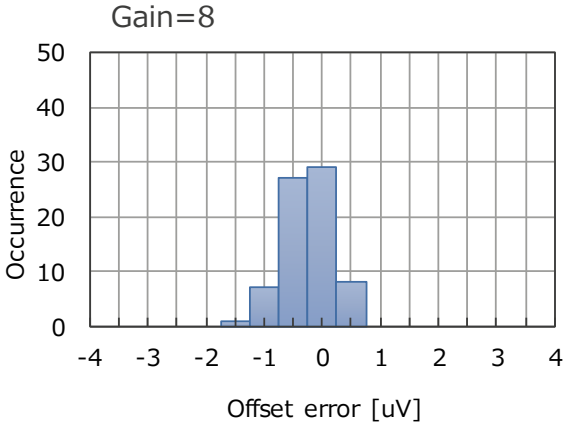


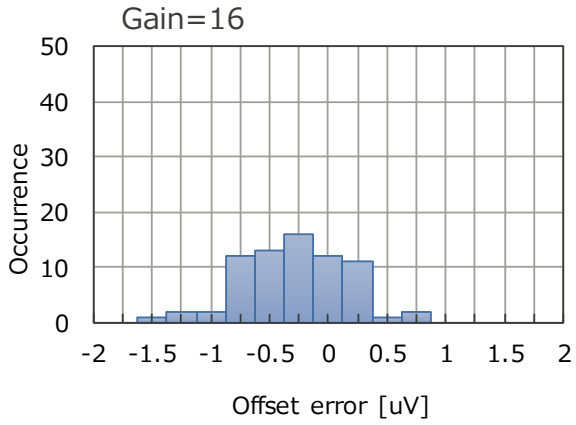


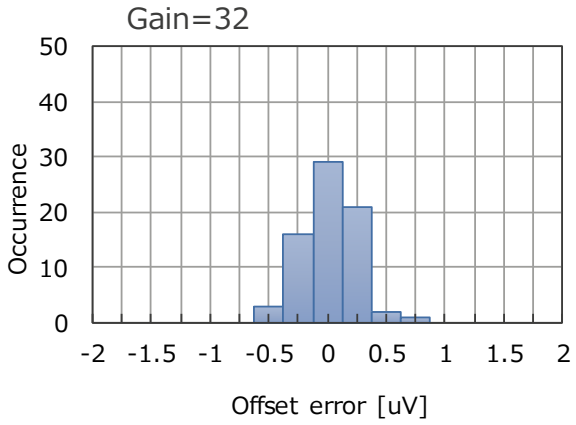


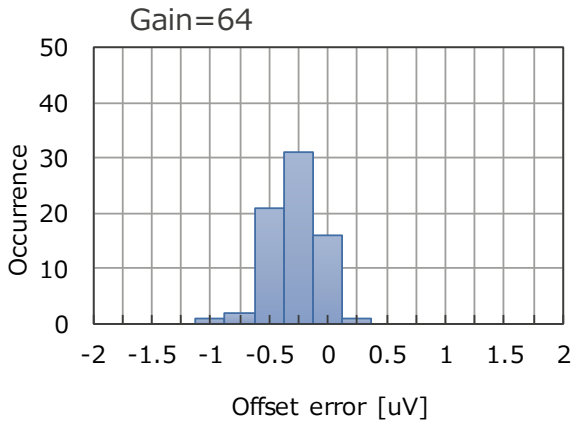


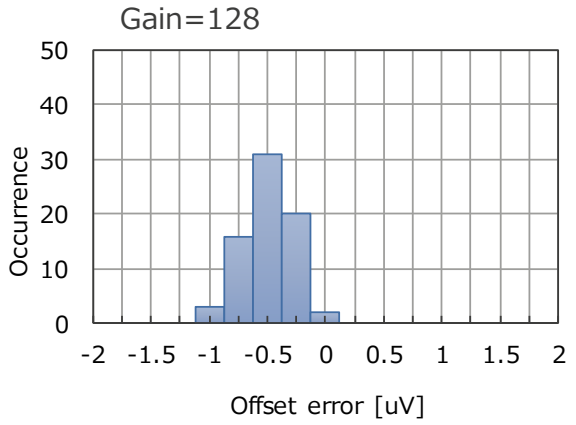





Gain=16
Occurrence
50
40
30
20
10
0
-2 -1.5 -1 -0.5 0 0.5 1 1.5 2
Offset error [uV]

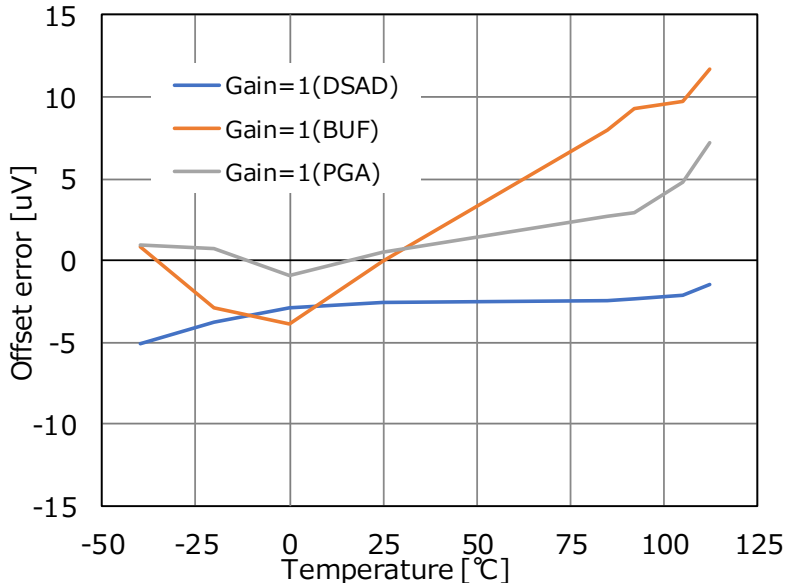

Gain=32
Occurrence
50
40
30
20
10
0
-2 -1.5 -1 -0.5 0 0.5 1 1.5 2
Offset error [uV]

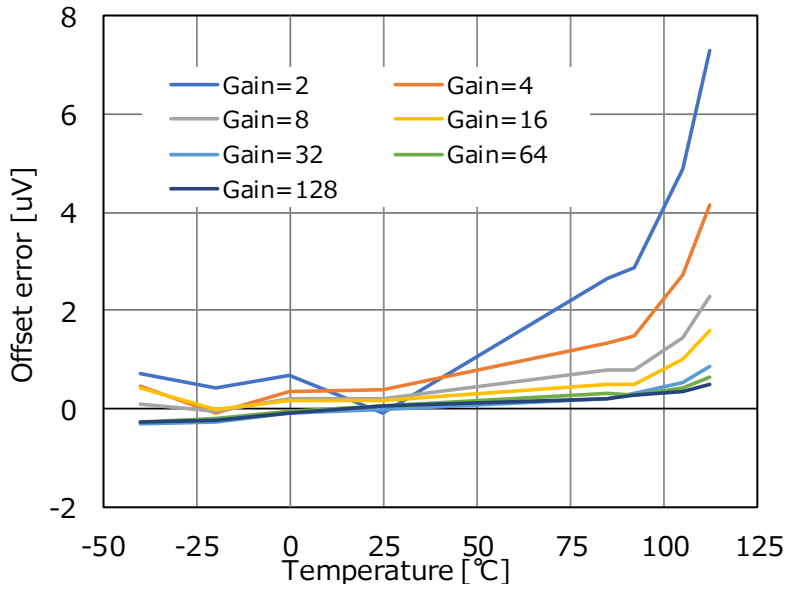

Gain=64
Occurrence
50
40
30
20
10
0
-2 -1.5 -1 -0.5 0 0.5 1 1.5 2
Offset error [uV]


Gain=128
Occurrence
50
40
30
20
10
0
-2 -1.5 -1 -0.5 0 0.5 1 1.5 2
Offset error [uV]

2.4 Offset error temperature drift

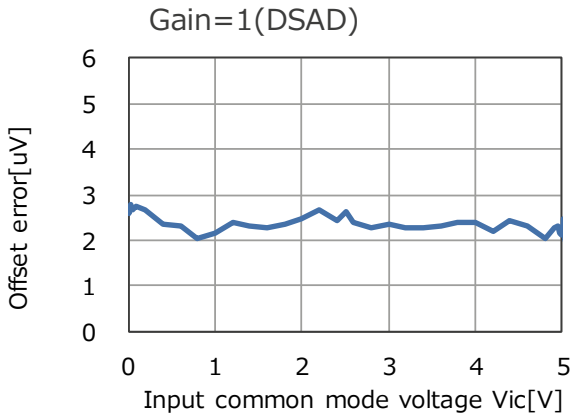
AVCC0=5V, Ta=25°C

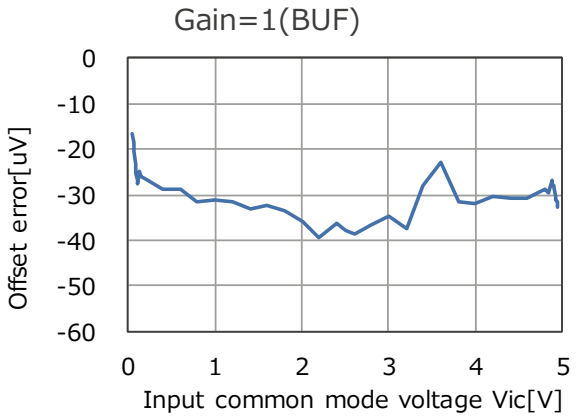


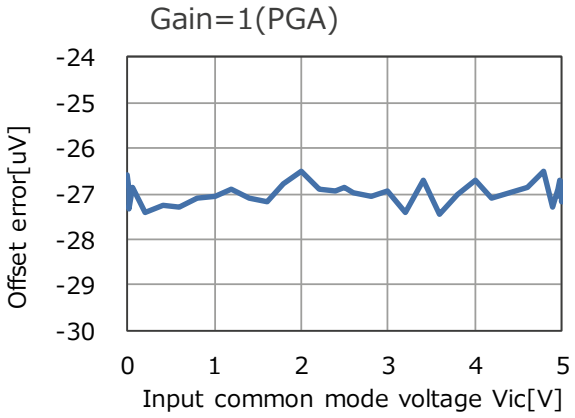


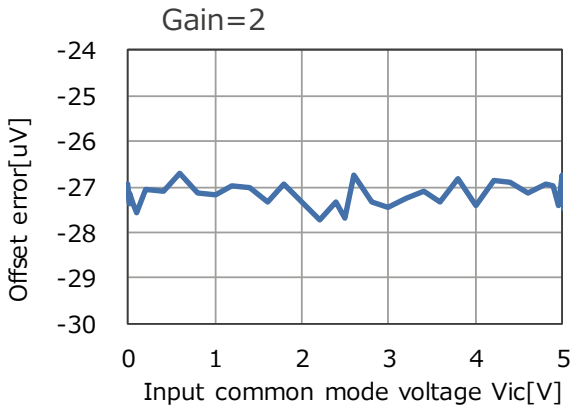
2.5 Offset error - Input common mode voltage

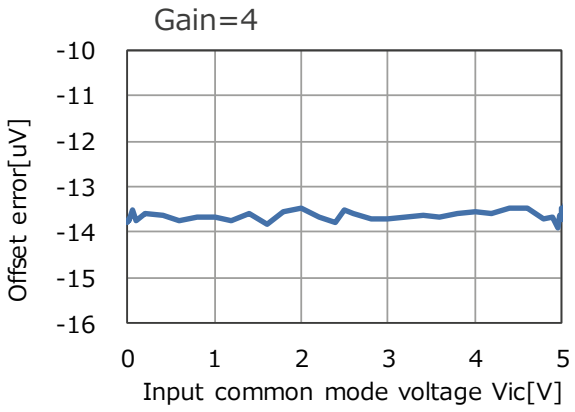
AVCC0=5V, Ta=25°C
Before calibration of offset errors

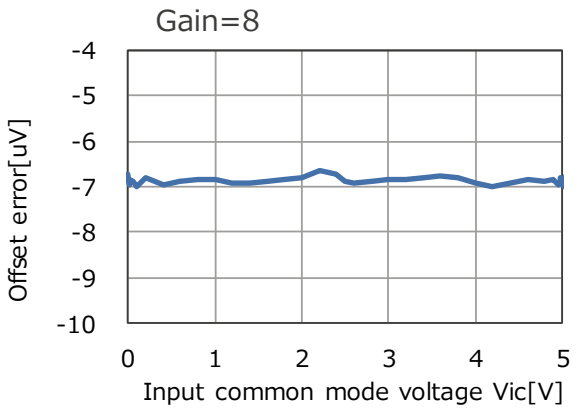


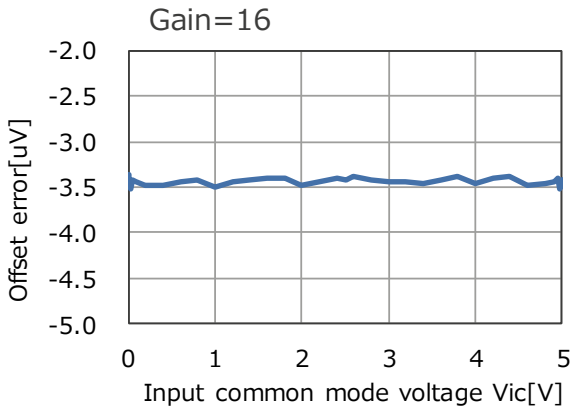


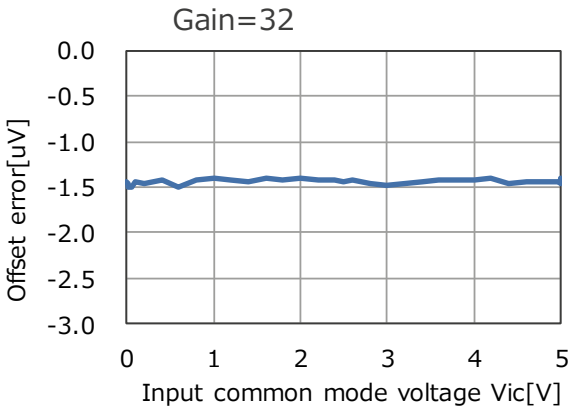


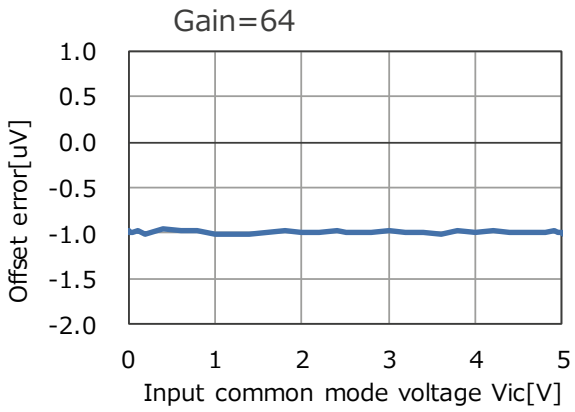


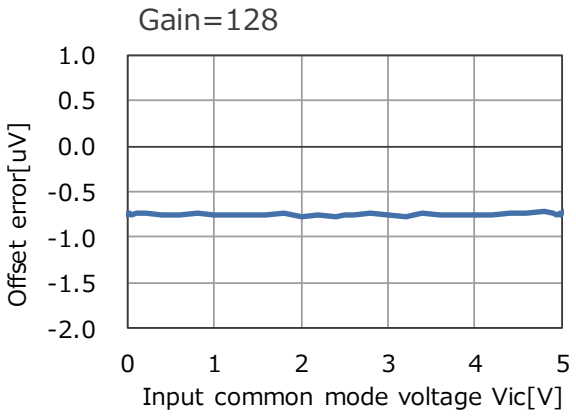





Gain=16
-2.0
-2.5
-3.0
-3.5
-4.0
-4.5
-5.0
Offset error[uV]
0
1
2
3
4
5
Input common mode voltage Vic[V]

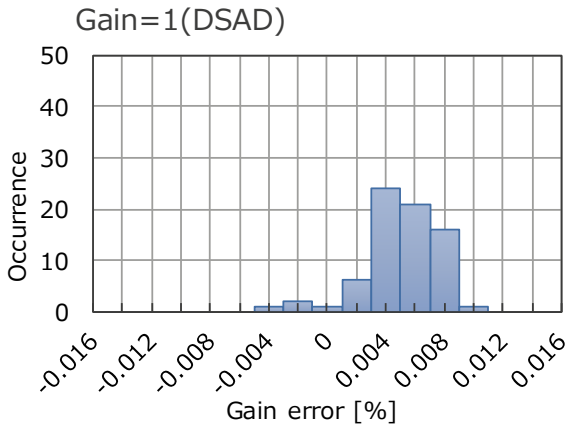

Gain=32
0.0
-0.5
-1.0
-1.5
-2.0
-2.5
-3.0
Offset error[uV]
0
1
2
3
4
5
Input common mode voltage Vic[V]

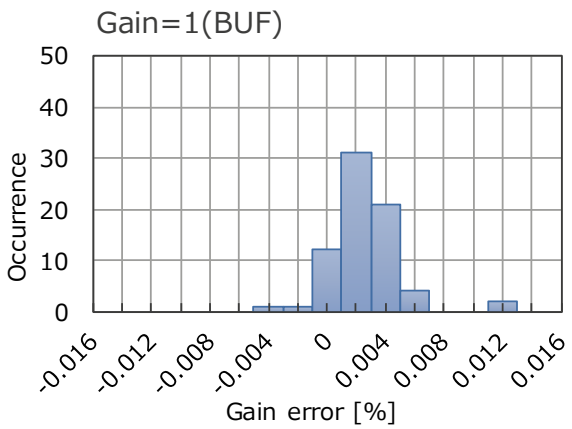

Gain=64
1.0
0.5
0.0
-0.5
-1.0
-1.5
-2.0
Offset error[uV]
0
1
2
3
4
5
Input common mode voltage Vic[V]

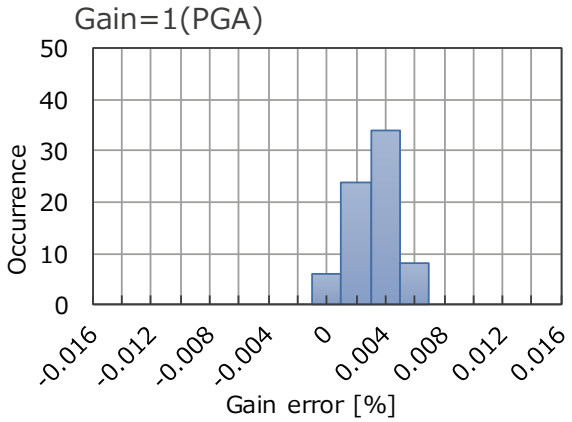

Gain=128
1.0
0.5
0.0
-0.5
-1.0
-1.5
-2.0
Offset error[uV]
0
1
2
3
4
5
Input common mode voltage Vic[V]

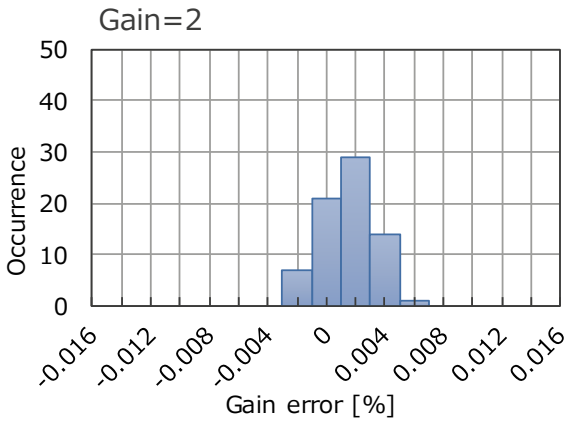
2.6 Gain error histogram

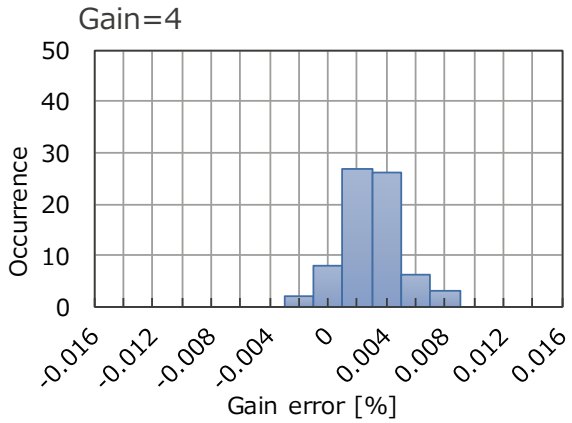
AVCC0=5V, Ta=25°C, n=72
After factory calibration of gain errors

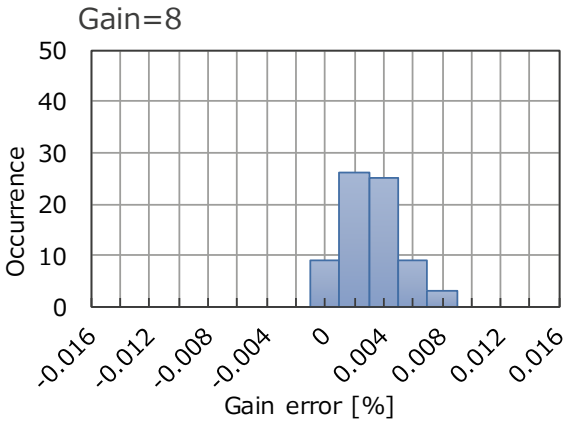


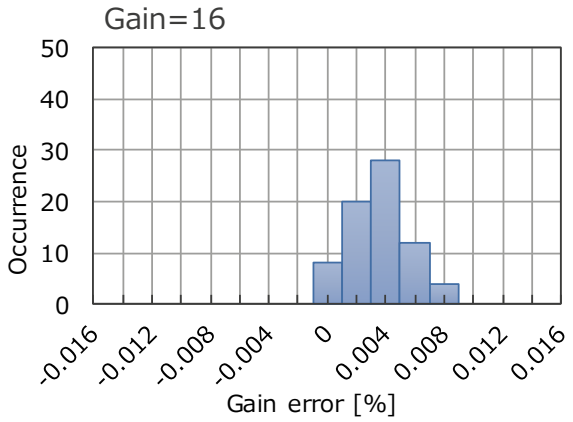


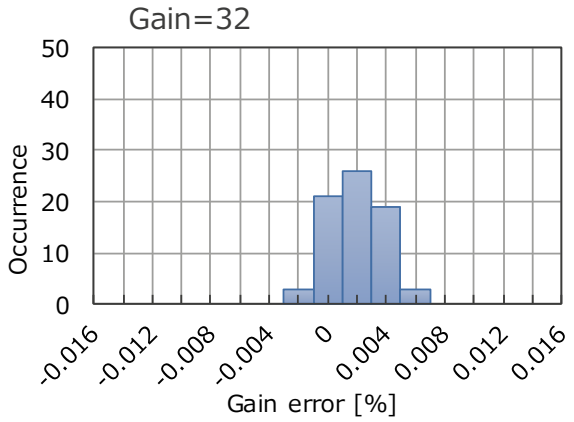


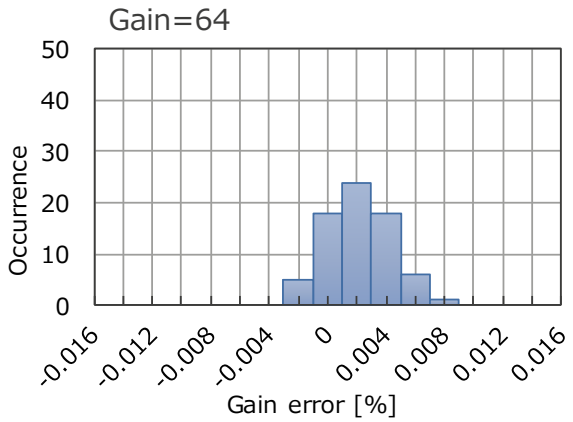


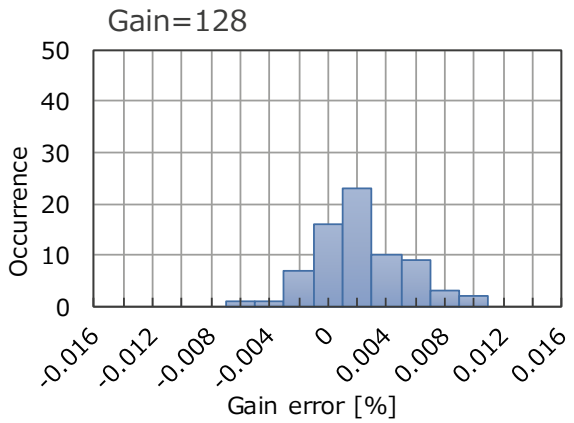





Gain=16
Occurrence
50
40
30
20
10
0
-0.016
-0.012
-0.008
-0.004
0
0.004
0.008
0.012
0.016
Gain error [%]

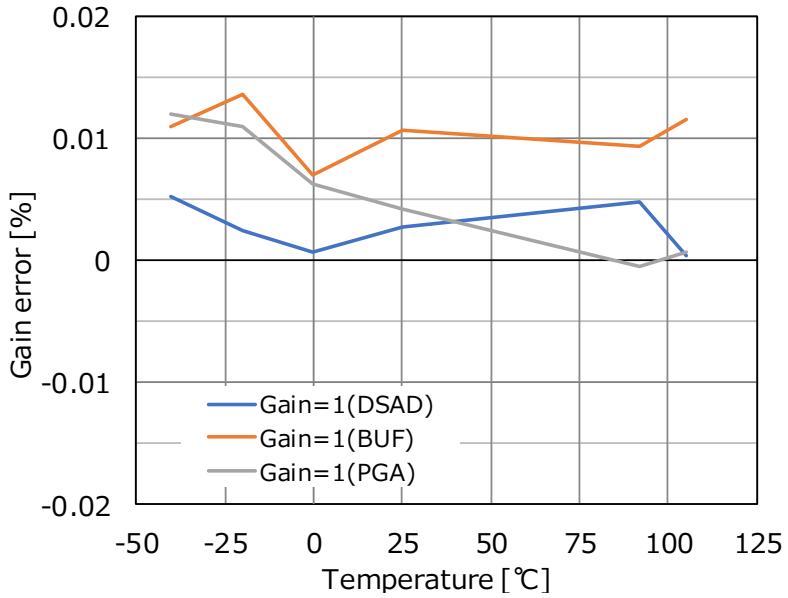

Gain=32
Occurrence
50
40
30
20
10
0
-0.016
-0.012
-0.008
-0.004
0
0.004
0.008
0.012
0.016
Gain error [%]

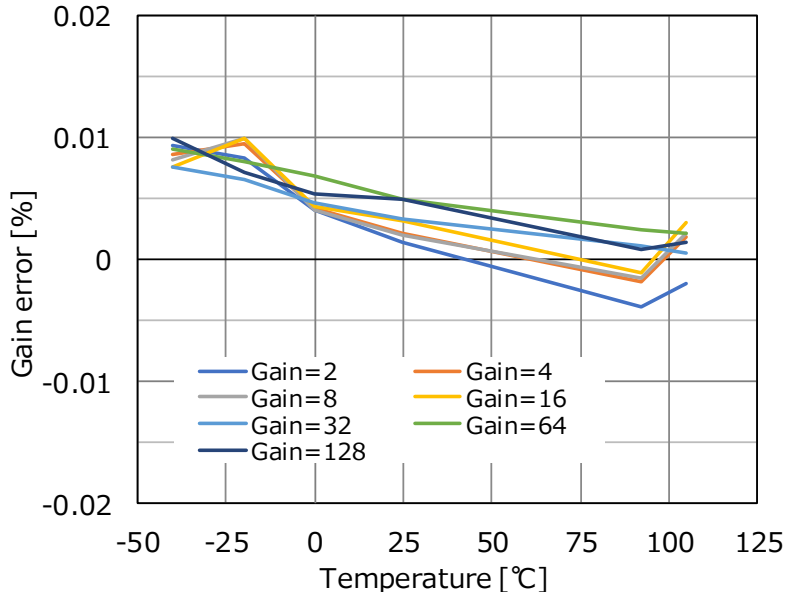

Gain=64
Occurrence
50
40
30
20
10
0
-0.016
-0.012
-0.008
-0.004
0
0.004
0.008
0.012
0.016
Gain error [%]


Gain=128
Occurrence
50
40
30
20
10
0
-0.016
-0.012
-0.008
-0.004
0
0.004
0.008
0.012
0.016
Gain error [%]

2.7 Gain error temperature drift

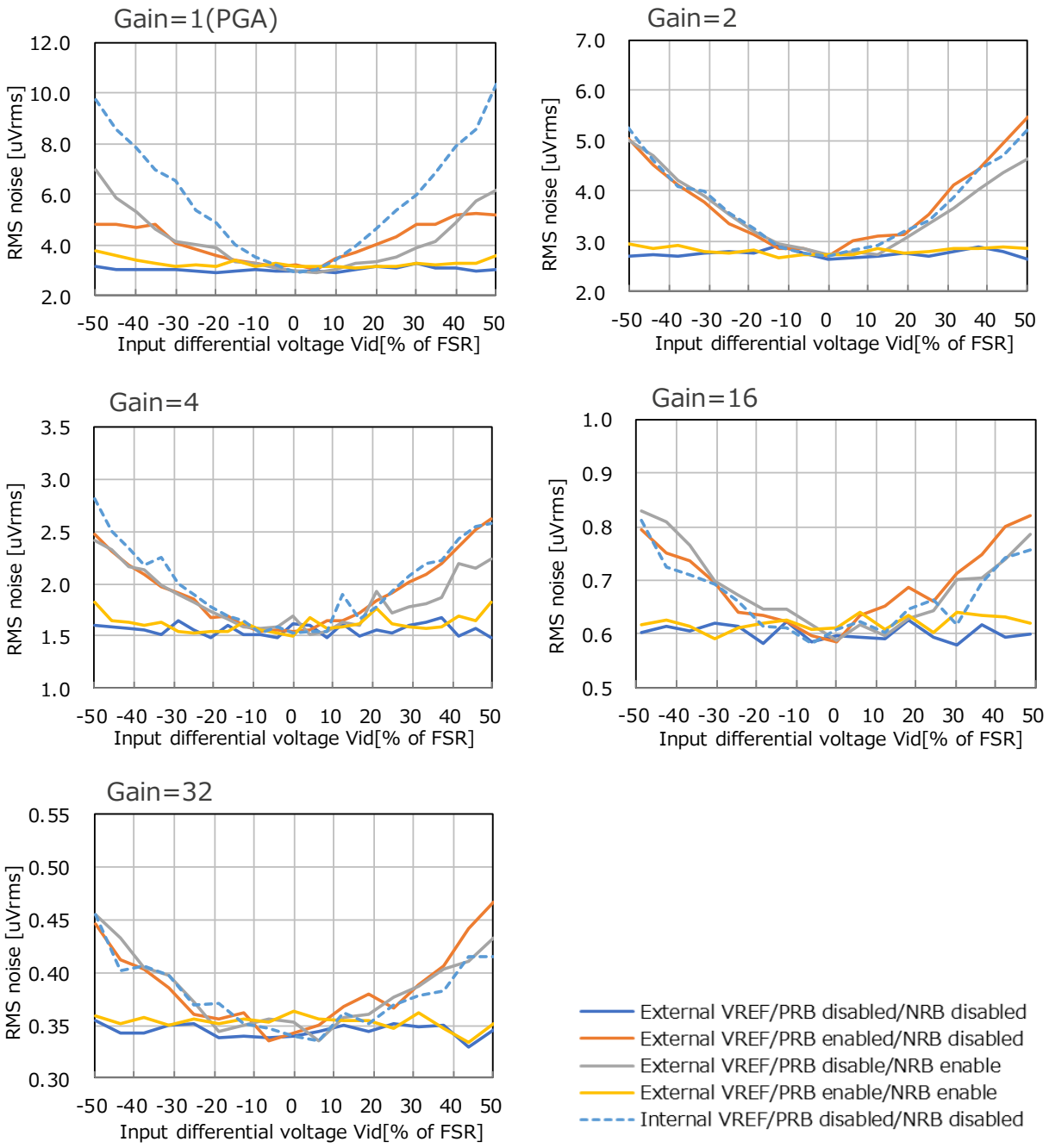
AVCC0=5V, Ta=25°C





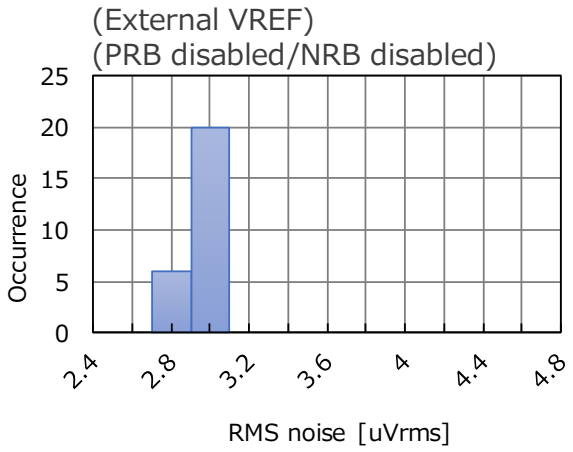
2.8 RMS noise – Input differential voltage

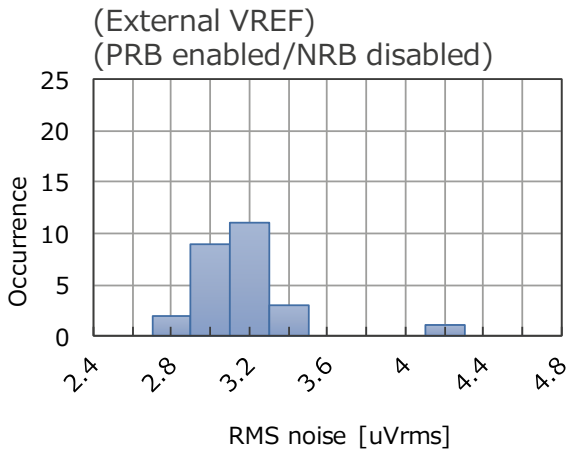
AVCC0=5V, Ta=25°C
Normal mode, Date Rate=244sps, VREF=2.5V

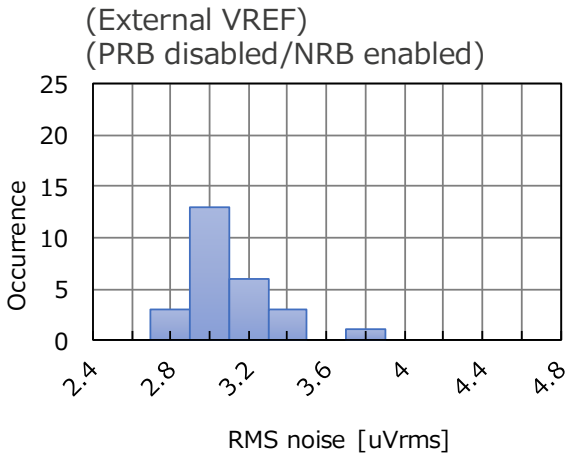


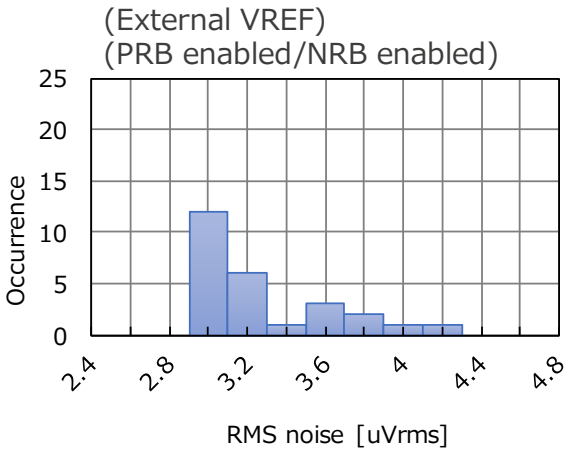
2.9 RMS noise VREF dependence histogram

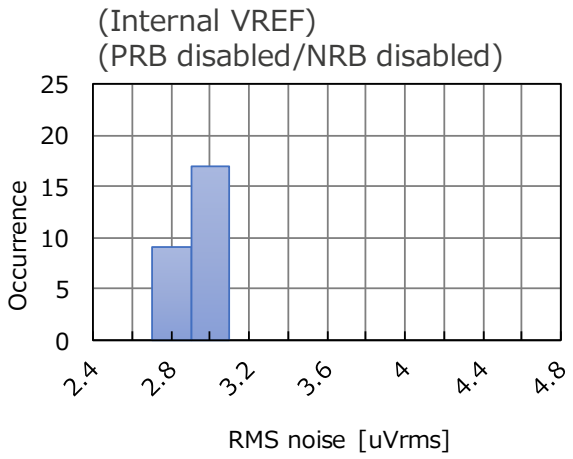
AVCC0=5V, Ta=25°C, n=26
Normal mode, Date Rate=244sps, VREF=2.5V, Vid=0V, Gain=1(PGA)



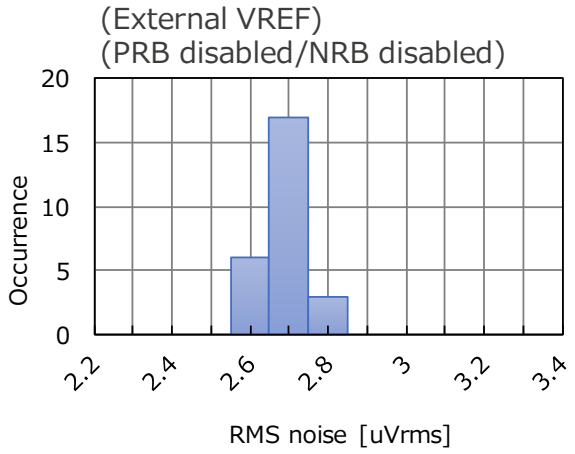


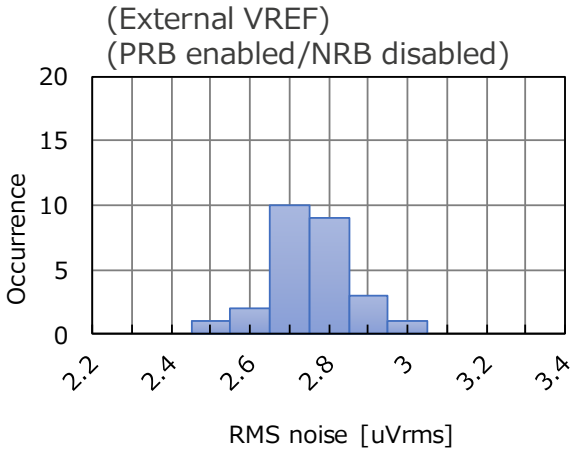


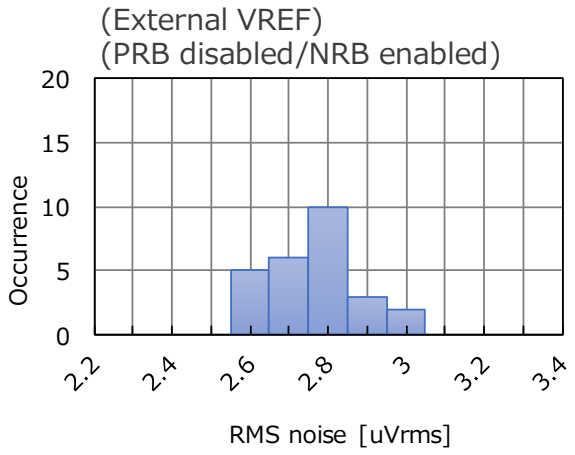


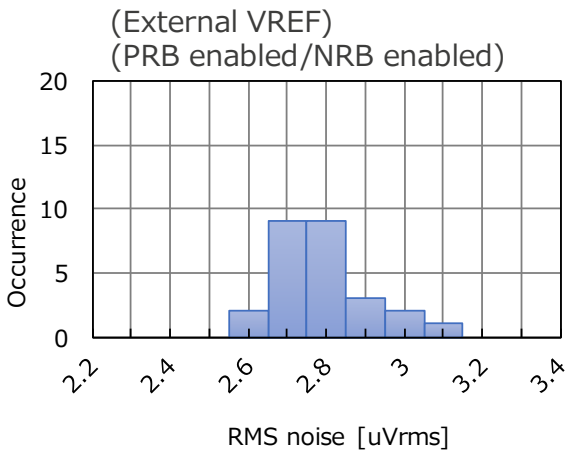


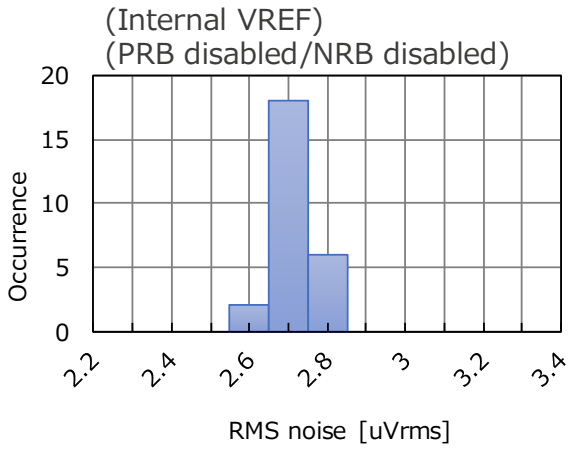
AVCC0=5V, Ta=25°C, n=26
Normal mode, Date Rate=244sps, VREF=2.5V, Vid=0V, Gain=4



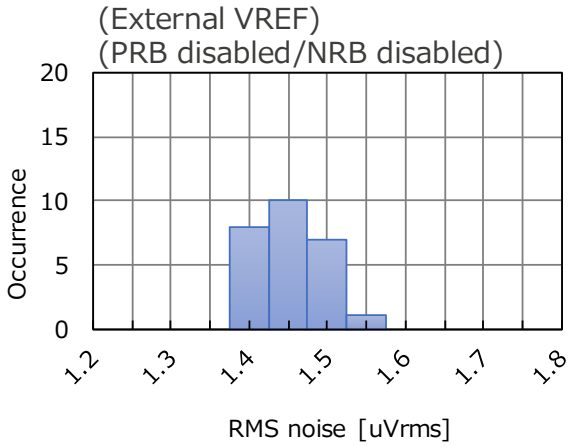


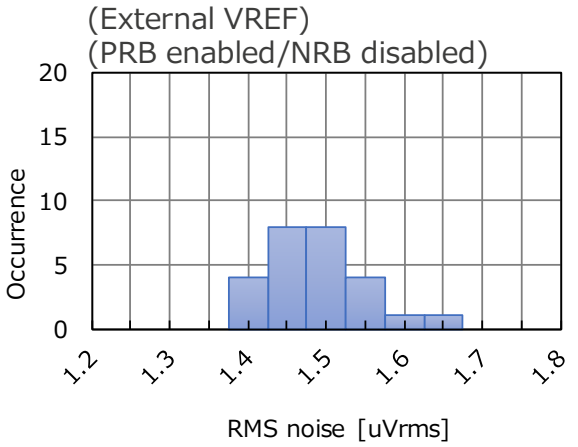


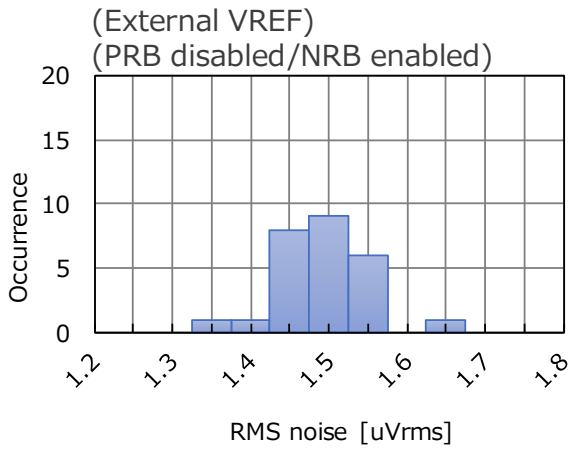


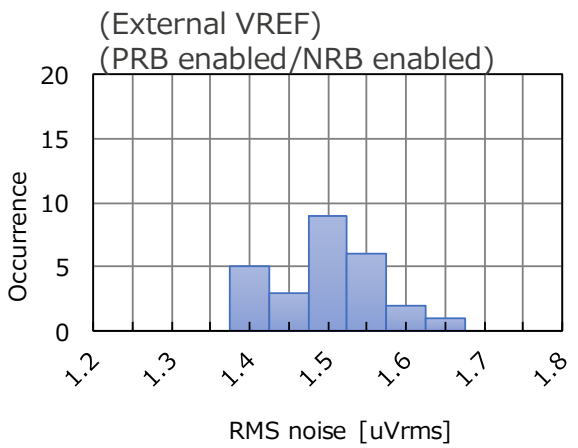


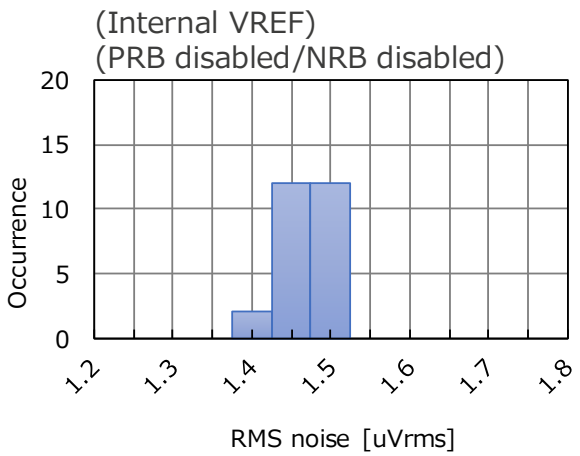
AVCC0=5V, Ta=25°C, n=26
Normal mode, Date Rate=244sps, VREF=2.5V, Vid=0V, Gain=2







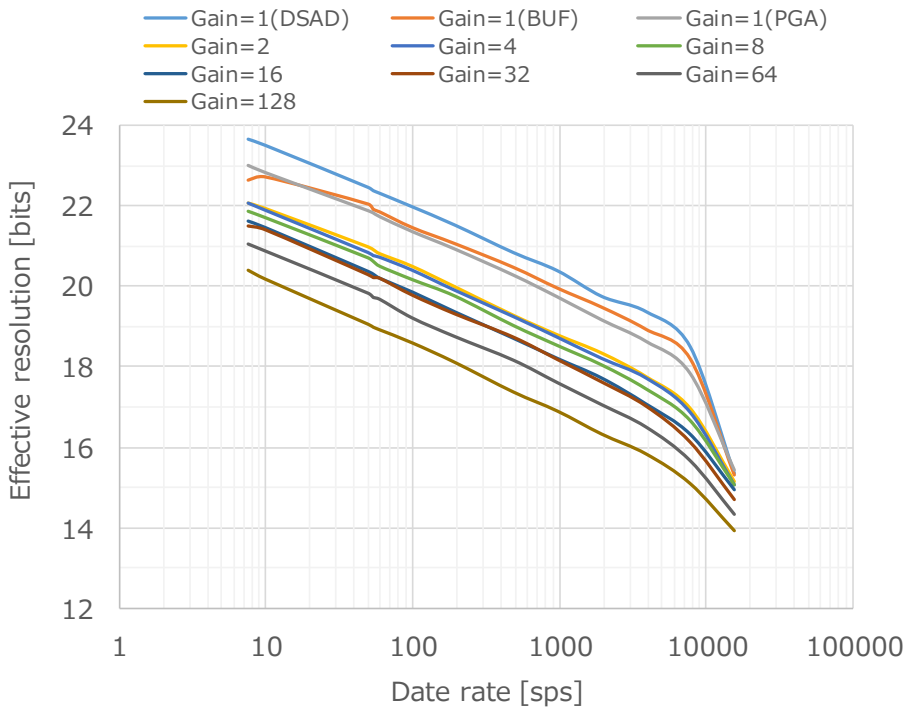




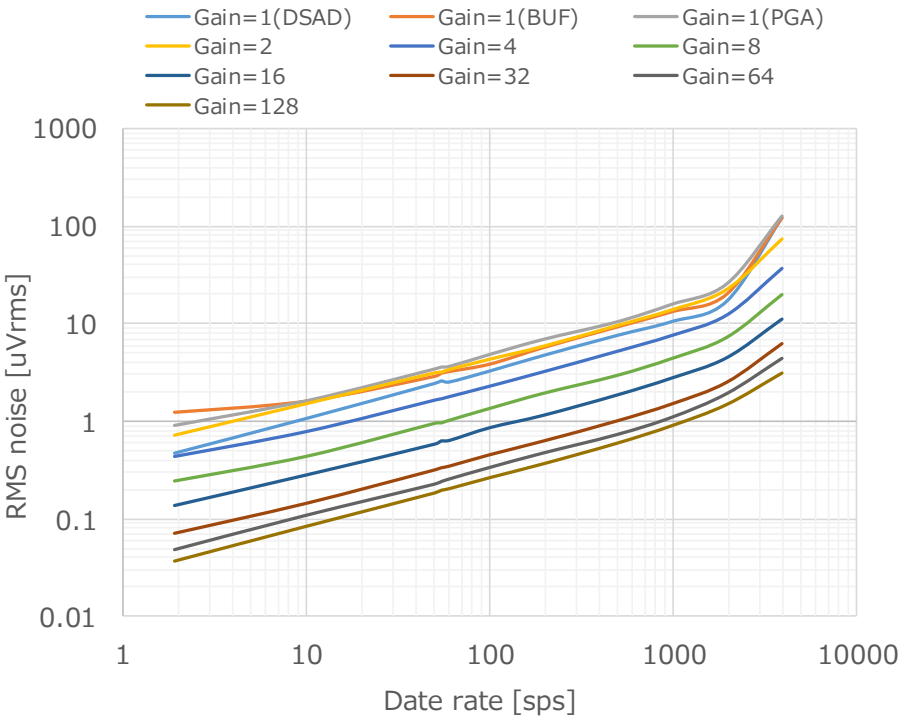
2.10 RMS noise – Date rate

AVCC0=5V, Ta=25°C
External VREF=2.5V

(Normal mode)



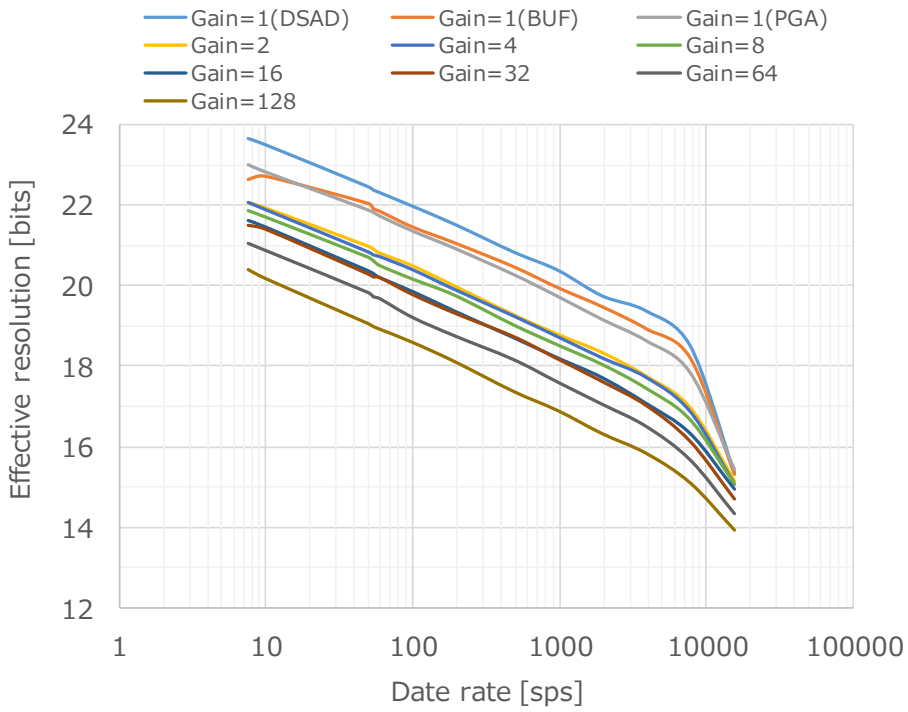
(Low power mode)



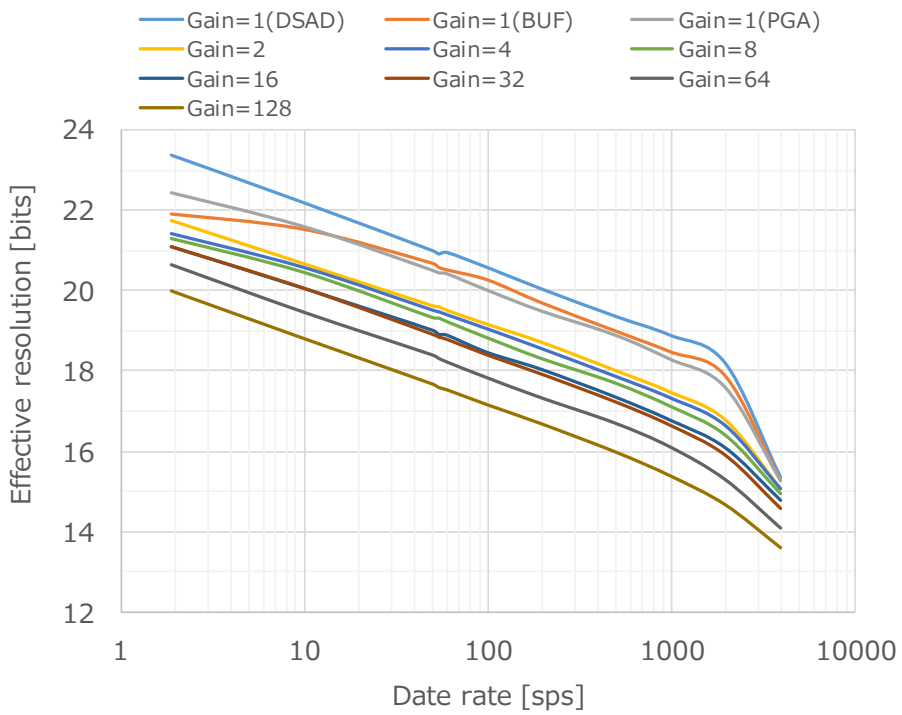
2.11 Effective resolution－Date rate

AVCC0=5V, Ta=25°C
External VREF=2.5V

(Normal mode)



(Low power mode)



2.12 Noise table (Normal mode)

AVCC0=5V, Ta=25°C, Normal mode, Modulator Clock=500kHz, External VREF=2.5V, AIN=0V

RMS noise[uVrms] (Peak-to-peak noise[uVpp])

Date rate [sps]	OSR	PGA gain									
		Gain=1 (DSAD)	Gain=1 (BUF)	Gain=1 (PGA)	Gain=2	Gain=4	Gain=8	Gain=16	Gain=32	Gain=64	Gain=128
7.6	65,536	0.383 (2.39)	0.740 (4.48)	0.601 (3.89)	0.563 (3.59)	0.284 (2.02)	0.166 (1.08)	0.097 (0.60)	0.052 (0.34)	0.036 (0.28)	0.029 (0.20)
10	50,048	0.426 (2.64)	0.701 (4.84)	0.680 (4.40)	0.618 (4.18)	0.322 (2.53)	0.185 (1.15)	0.108 (0.71)	0.056 (0.40)	0.041 (0.27)	0.033 (0.20)
50	9,984	0.878 (5.42)	1.117 (7.59)	1.308 (9.76)	1.196 (7.59)	0.667 (5.15)	0.369 (2.51)	0.230 (1.69)	0.121 (0.92)	0.084 (0.61)	0.072 (0.52)
54	9,216	0.929 (6.35)	1.225 (9.71)	1.359 (10.5)	1.254 (9.52)	0.702 (4.85)	0.392 (2.85)	0.240 (1.70)	0.127 (0.88)	0.090 (0.59)	0.076 (0.51)
60	8,320	0.973 (7.31)	1.279 (8.99)	1.450 (10.7)	1.345 (9.27)	0.723 (4.50)	0.426 (3.30)	0.258 (1.48)	0.129 (1.07)	0.093 (0.59)	0.080 (0.58)
100	4,992	1.228 (8.67)	1.673 (11.4)	1.873 (13.0)	1.673 (9.76)	0.904 (5.96)	0.536 (3.46)	0.327 (2.41)	0.172 (1.19)	0.128 (0.96)	0.100 (0.68)
195	2,560	1.681 (12.7)	2.206 (18.6)	2.530 (16.7)	2.378 (16.7)	1.277 (8.45)	0.710 (4.65)	0.460 (3.15)	0.238 (1.55)	0.176 (1.16)	0.139 (0.90)
488	1,024	2.697 (17.3)	3.311 (22.4)	3.954 (29.3)	3.881 (27.4)	2.007 (13.5)	1.175 (8.52)	0.723 (4.73)	0.355 (2.28)	0.264 (1.80)	0.231 (1.55)
977	512	3.691 (27.5)	4.740 (29.0)	5.758 (36.5)	5.442 (35.7)	2.871 (20.0)	1.656 (12.0)	1.025 (6.67)	0.522 (3.53)	0.389 (2.57)	0.321 (2.21)
1,953	256	5.734 (35.3)	6.572 (42.5)	8.535 (55.3)	7.438 (48.9)	4.130 (28.2)	2.308 (15.8)	1.434 (9.34)	0.768 (4.85)	0.567 (4.05)	0.476 (2.71)
3,906	128	7.446 (51.1)	9.607 (65.8)	12.32 (70.0)	11.15 (76.5)	5.778 (38.6)	3.476 (27.2)	2.237 (14.7)	1.162 (7.83)	0.831 (5.98)	0.669 (4.21)
7,813	64	13.60 (102)	15.91 (110)	21.39 (143)	19.22 (120)	10.43 (67.6)	5.971 (39.0)	3.760 (26.4)	2.161 (13.9)	1.482 (11.0)	1.112 (6.96)
15,625	32	120.5 (644)	117.5 (720)	112.5 (735)	67.81 (347)	36.42 (218)	17.96 (109)	9.766 (58.7)	5.812 (37.6)	3.726 (22.2)	2.498 (16.9)

Effective resolution [Bits] (Noise free resolution [Bits])

Date rate [sps]	OSR	PGA gain									
		Gain=1 (DSAD)	Gain=1 (BUF)	Gain=1 (PGA)	Gain=2	Gain=4	Gain=8	Gain=16	Gain=32	Gain=64	Gain=128
7.6	65,536	23.6 (21.0)	22.6 (20.0)	23.0 (20.3)	22.1 (19.4)	22.1 (19.2)	21.8 (19.1)	21.6 (19.0)	21.5 (18.8)	21.0 (18.1)	20.4 (17.6)
10	50,048	23.5 (20.9)	22.7 (19.9)	22.8 (20.1)	22.0 (19.2)	21.9 (18.9)	21.7 (19.1)	21.5 (18.7)	21.4 (18.6)	20.9 (18.2)	20.2 (17.6)
50	9,984	22.4 (19.8)	22.0 (19.3)	21.9 (19.0)	21.0 (18.3)	20.8 (17.9)	20.7 (17.9)	20.4 (17.5)	20.3 (17.4)	19.8 (17.0)	19.0 (16.2)
54	9,216	22.4 (19.6)	21.9 (18.9)	21.8 (18.9)	20.9 (18.0)	20.8 (18.0)	20.6 (17.7)	20.3 (17.5)	20.2 (17.5)	19.7 (17.0)	19.0 (16.2)
60	8,320	22.3 (19.4)	21.8 (19.0)	21.7 (18.8)	20.8 (18.0)	20.7 (18.1)	20.5 (17.5)	20.2 (17.7)	20.2 (17.2)	19.7 (17.0)	18.9 (16.1)
100	4,992	22.0 (19.1)	21.5 (18.7)	21.4 (18.6)	20.5 (18.0)	20.4 (17.7)	20.2 (17.5)	19.9 (17.0)	19.8 (17.0)	19.2 (16.3)	18.6 (15.8)
195	2,560	21.5 (18.6)	21.1 (18.0)	21.0 (18.2)	20.0 (17.2)	19.9 (17.2)	19.8 (17.0)	19.4 (16.6)	19.3 (16.6)	18.8 (16.0)	18.1 (15.4)
488	1,024	20.8 (18.1)	20.5 (17.7)	20.3 (17.4)	19.3 (16.5)	19.3 (16.5)	19.0 (16.2)	18.7 (16.0)	18.8 (16.1)	18.2 (15.4)	17.4 (14.6)
977	512	20.4 (17.5)	20.0 (17.3)	19.7 (17.1)	18.8 (16.1)	18.7 (15.9)	18.5 (15.7)	18.2 (15.5)	18.2 (15.4)	17.6 (14.9)	16.9 (14.1)
1,953	256	19.7 (17.1)	19.5 (16.8)	19.2 (16.5)	18.4 (15.6)	18.2 (15.4)	18.1 (15.3)	17.7 (15.0)	17.6 (15.0)	17.1 (14.2)	16.3 (13.8)
3,906	128	19.4 (16.6)	18.9 (16.2)	18.6 (16.1)	17.8 (15.0)	17.7 (15.0)	17.5 (14.5)	17.1 (14.4)	17.0 (14.3)	16.5 (13.7)	15.8 (13.2)
7,813	64	18.5 (15.6)	18.2 (15.4)	17.8 (15.1)	17.0 (14.3)	16.9 (14.2)	16.7 (14.0)	16.3 (13.5)	16.1 (13.5)	15.7 (12.8)	15.1 (12.5)
15,625	32	15.3 (12.9)	15.3 (12.7)	15.4 (12.7)	15.2 (12.8)	15.1 (12.5)	15.1 (12.5)	15.0 (12.4)	14.7 (12.0)	14.4 (11.8)	13.9 (11.2)

2.13 Noise table (Low power mode)

AVCC0=5V, Ta=25°C, Low Power mode, Modulator Clock=125kHz, External VREF=2.5V, AIN=0V

RMS noise[uVrms] (Peak-to-peak noise[uVpp])

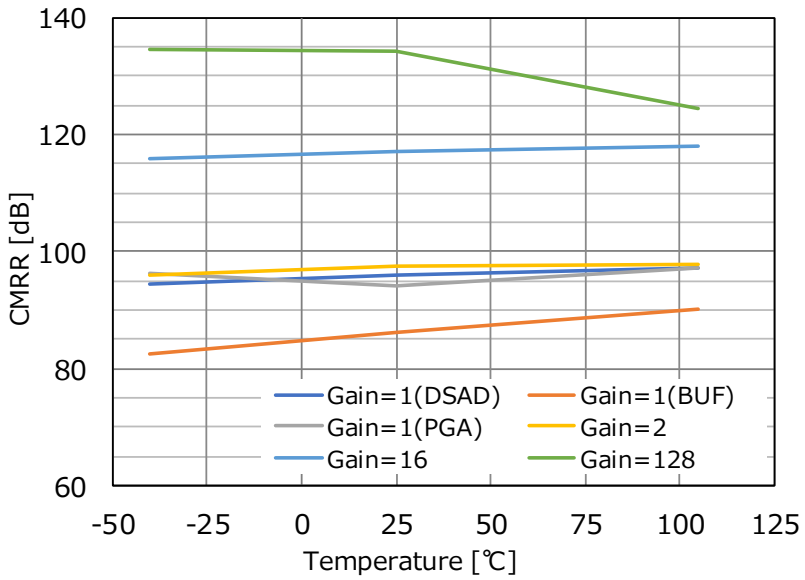
Date rate [sps]	OSR	PGA gain									
		Gain=1 (DSAD)	Gain=1 (BUF)	Gain=1 (PGA)	Gain=2	Gain=4	Gain=8	Gain=16	Gain=32	Gain=64	Gain=128
1.9	65,536	0.463 (3.29)	1.236 (6.58)	0.892 (5.38)	0.708 (4.63)	0.444 (2.62)	0.245 (1.72)	0.140 (0.90)	0.070 (0.47)	0.048 (0.34)	0.038 (0.25)
10	12,512	1.053 (7.03)	1.606 (11.9)	1.596 (11.4)	1.492 (10.6)	0.797 (5.27)	0.437 (2.86)	0.286 (1.79)	0.143 (1.00)	0.109 (0.72)	0.085 (0.61)
50	2,496	2.412 (15.7)	2.883 (18.4)	3.390 (21.7)	3.093 (22.5)	1.669 (11.0)	0.954 (5.96)	0.592 (3.86)	0.317 (2.35)	0.228 (1.69)	0.187 (1.22)
54	2,304	2.558 (19.4)	3.098 (20.5)	3.544 (23.9)	3.139 (19.4)	1.719 (11.3)	0.962 (6.39)	0.637 (3.92)	0.333 (2.12)	0.242 (1.81)	0.199 (1.39)
60	2,080	2.491 (16.3)	3.230 (20.8)	3.598 (26.4)	3.348 (25.0)	1.810 (13.6)	1.024 (7.38)	0.645 (4.50)	0.346 (2.30)	0.257 (1.88)	0.207 (1.37)
100	1,248	3.237 (21.7)	3.843 (26.6)	4.794 (32.5)	4.274 (27.1)	2.319 (15.3)	1.357 (9.35)	0.872 (6.37)	0.454 (2.98)	0.338 (2.29)	0.268 (1.83)
195	640	4.663 (37.7)	5.666 (37.7)	6.826 (46.5)	5.799 (39.7)	3.245 (21.3)	1.930 (12.9)	1.164 (7.50)	0.627 (4.61)	0.474 (3.31)	0.371 (2.68)
488	256	7.451 (46.6)	9.151 (62.5)	10.30 (70.9)	9.404 (59.6)	5.216 (35.7)	2.934 (20.2)	1.869 (13.6)	1.006 (6.13)	0.729 (5.46)	0.599 (4.56)
977	128	10.37 (72.4)	13.13 (83.1)	15.63 (111)	13.71 (93.3)	7.605 (63.0)	4.383 (30.3)	2.796 (18.0)	1.510 (9.78)	1.099 (7.60)	0.908 (7.23)
1,953	64	16.80 (117)	19.92 (153)	25.41 (177)	22.23 (138)	12.30 (94.9)	7.226 (50.9)	4.520 (30.6)	2.531 (16.2)	1.927 (13.6)	1.499 (11.1)
3,906	32	120.9 (720)	120.4 (761)	126.6 (634)	73.29 (507)	36.82 (216)	19.83 (124)	11.22 (78.4)	6.332 (39.1)	4.427 (27.3)	3.143 (20.0)

Effective resolution [Bits] (Noise free resolution [Bits])

Date rate [sps]	OSR	PGA gain									
		Gain=1 (DSAD)	Gain=1 (BUF)	Gain=1 (PGA)	Gain=2	Gain=4	Gain=8	Gain=16	Gain=32	Gain=64	Gain=128
1.9	65,536	23.4 (20.5)	21.9 (19.5)	22.4 (19.8)	21.8 (19.0)	21.4 (18.9)	21.3 (18.5)	21.1 (18.4)	21.1 (18.4)	20.6 (17.8)	20.0 (17.3)
10	12,512	22.2 (19.4)	21.5 (18.6)	21.6 (18.7)	20.7 (17.9)	20.6 (17.9)	20.5 (17.7)	20.1 (17.4)	20.1 (17.3)	19.5 (16.7)	18.8 (16.0)
50	2,496	21.0 (18.3)	20.7 (18.0)	20.5 (17.8)	19.6 (16.8)	19.5 (16.8)	19.3 (16.7)	19.0 (16.3)	18.9 (16.0)	18.4 (15.5)	17.7 (15.0)
54	2,304	20.9 (18.0)	20.6 (17.8)	20.4 (17.7)	19.6 (17.0)	19.5 (16.8)	19.3 (16.6)	18.9 (16.3)	18.8 (16.2)	18.3 (15.4)	17.6 (14.8)
60	2,080	20.9 (18.2)	20.5 (17.8)	20.4 (17.5)	19.5 (16.6)	19.4 (16.5)	19.2 (16.4)	18.9 (16.1)	18.8 (16.1)	18.2 (15.3)	17.5 (14.8)
100	1,248	20.6 (17.8)	20.3 (17.5)	20.0 (17.2)	19.2 (16.5)	19.0 (16.3)	18.8 (16.0)	18.5 (15.6)	18.4 (15.7)	17.8 (15.1)	17.2 (14.4)
195	640	20.0 (17.0)	19.7 (17.0)	19.5 (16.7)	18.7 (15.9)	18.6 (15.8)	18.3 (15.6)	18.0 (15.4)	17.9 (15.1)	17.3 (14.5)	16.7 (13.8)
488	256	19.4 (16.7)	19.0 (16.2)	18.9 (16.1)	18.0 (15.4)	17.9 (15.1)	17.7 (14.9)	17.4 (14.5)	17.3 (14.6)	16.7 (13.8)	16.0 (13.1)
977	128	18.9 (16.1)	18.5 (15.8)	18.3 (15.4)	17.5 (14.7)	17.3 (14.3)	17.1 (14.3)	16.8 (14.1)	16.7 (14.0)	16.1 (13.3)	15.4 (12.4)
1,953	64	18.2 (15.4)	17.9 (14.9)	17.6 (14.8)	16.8 (14.2)	16.6 (13.7)	16.4 (13.6)	16.1 (13.3)	15.9 (13.2)	15.3 (12.5)	14.7 (11.8)
3,906	32	15.3 (12.8)	15.3 (12.6)	15.3 (12.9)	15.1 (12.3)	15.1 (12.5)	14.9 (12.3)	14.8 (12.0)	14.6 (12.0)	14.1 (11.5)	13.6 (10.9)

2.14 Common Mode Rejection Ratio (CMRR)

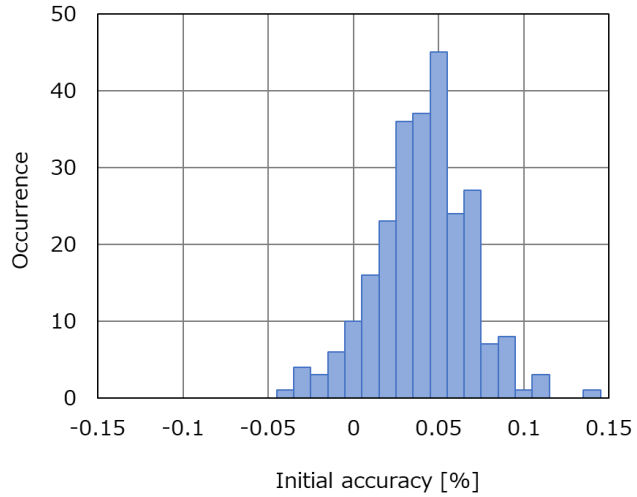
AVCC0=5V



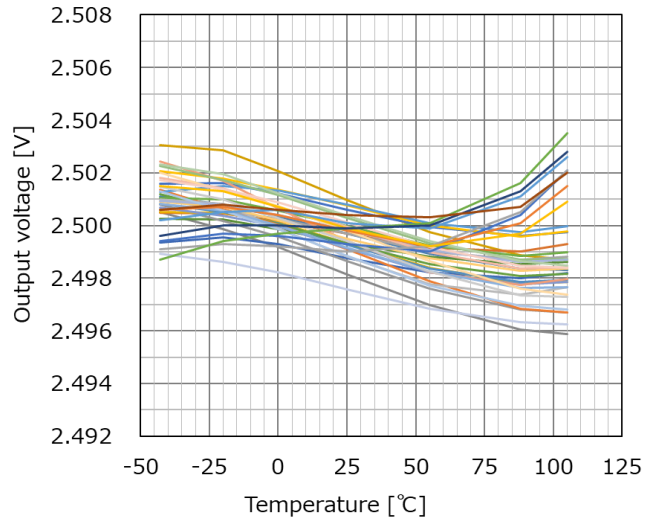
3. Voltage Reference (VREF)

3.1 Initial accuracy, Temperature drift, Load regulation

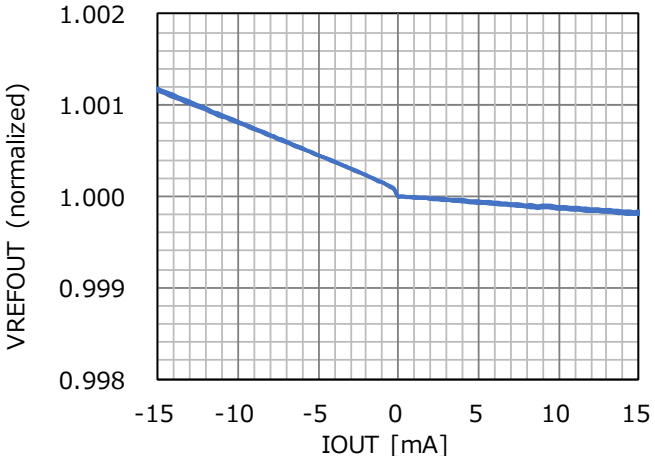
AVCC0=5V, Ta=25°C



AVCC0=5V



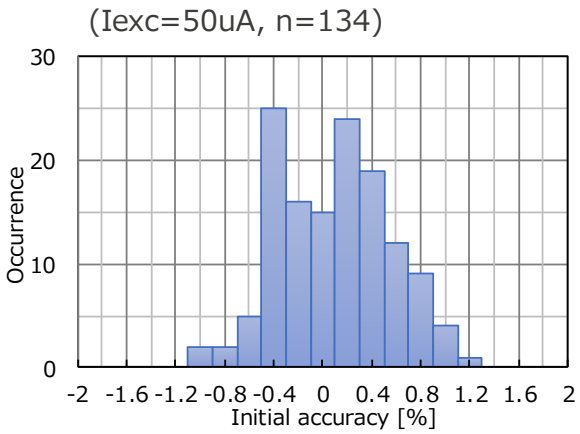
(Ta=25℃)

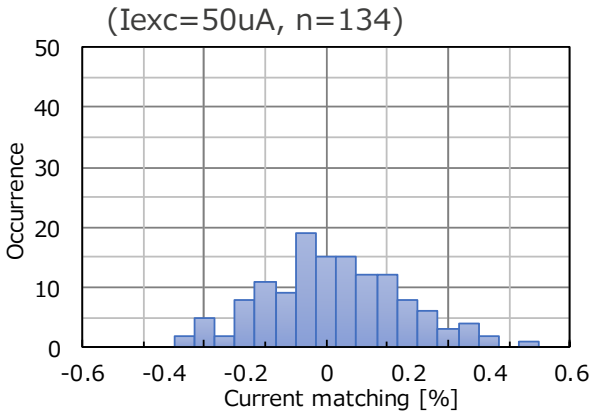


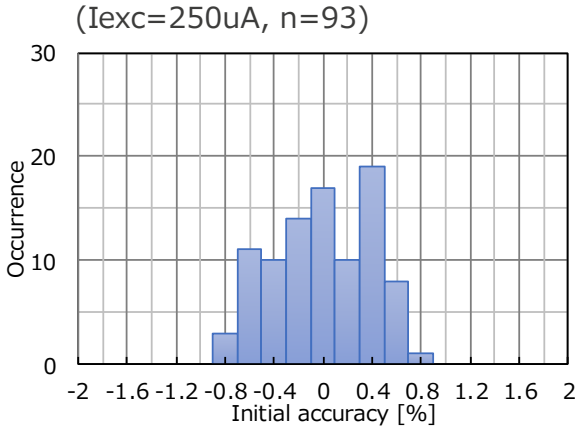
4. Excitation Current Source (IEXC)

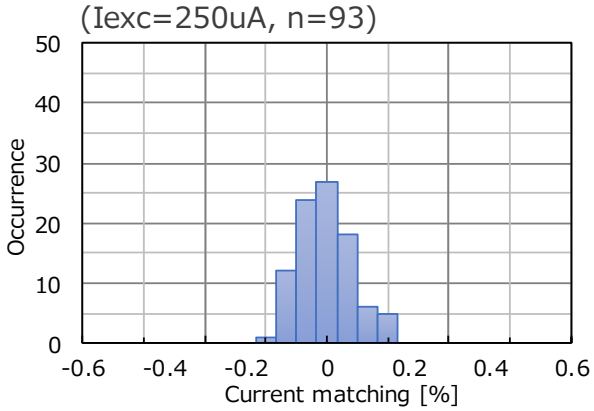
4.1 Initial accuracy, Current matching

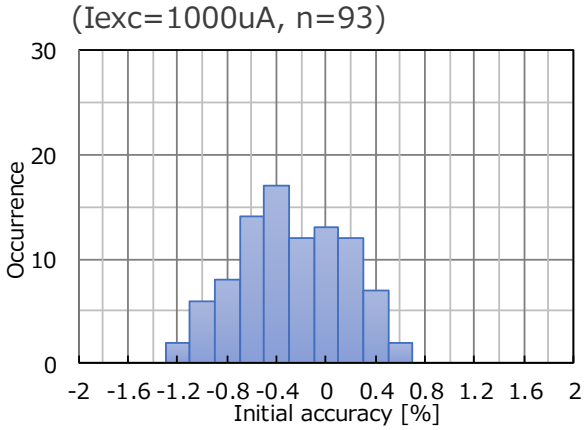
AVCC0=5V, Ta=25°C

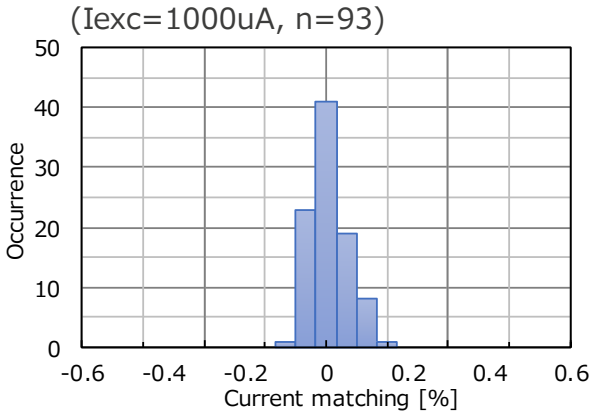






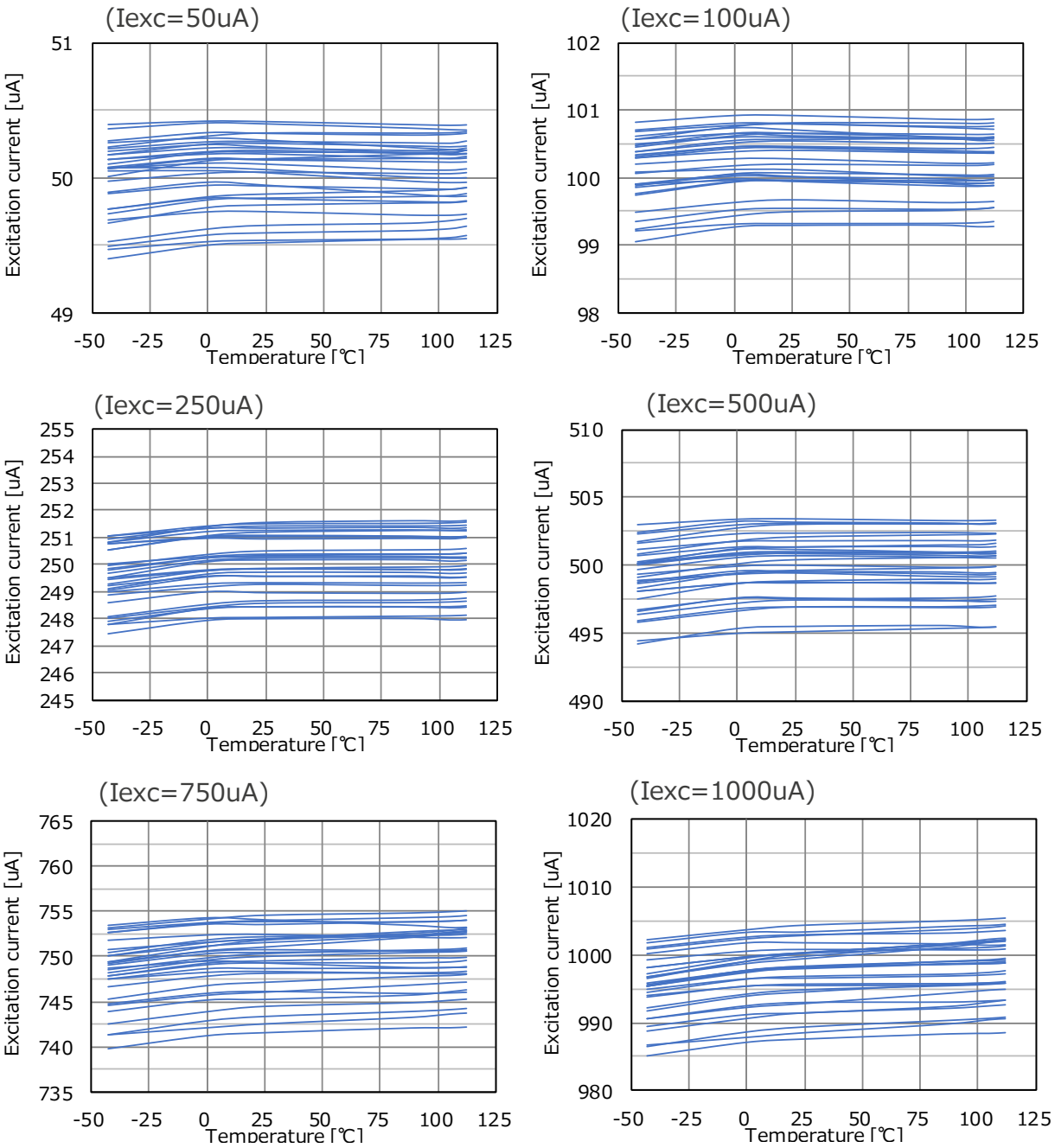






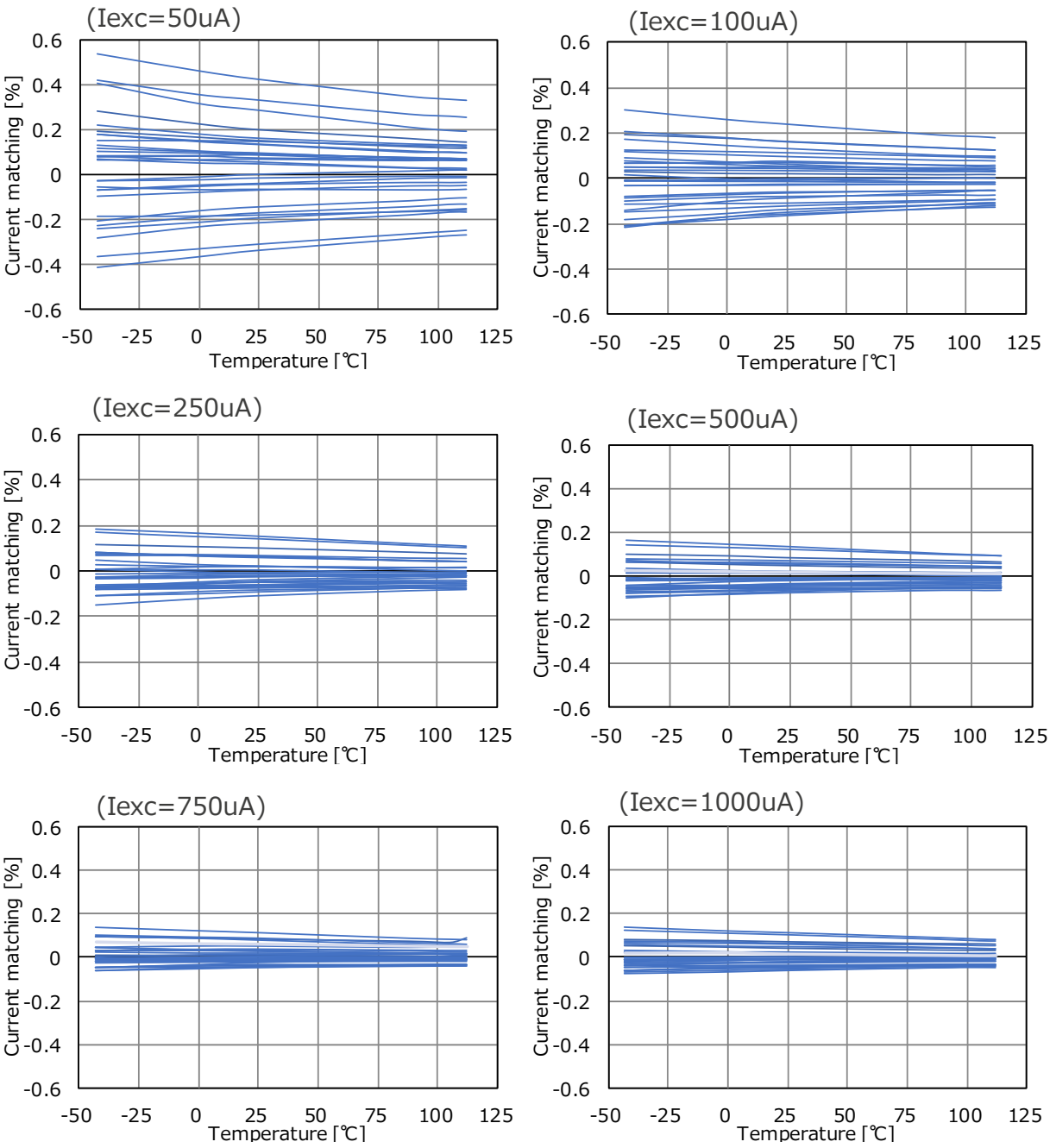
4.2 Temperature drift

AVCC0=5V, n=30



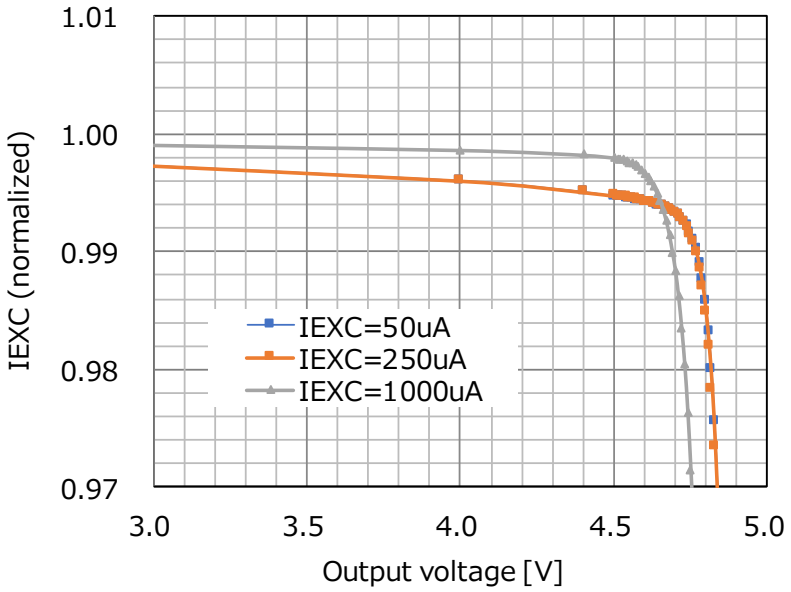
4.3 Drift matching

AVCC0=5V, n=30



4.4 Load regulation

AVCC0=5V, Ta=25°C

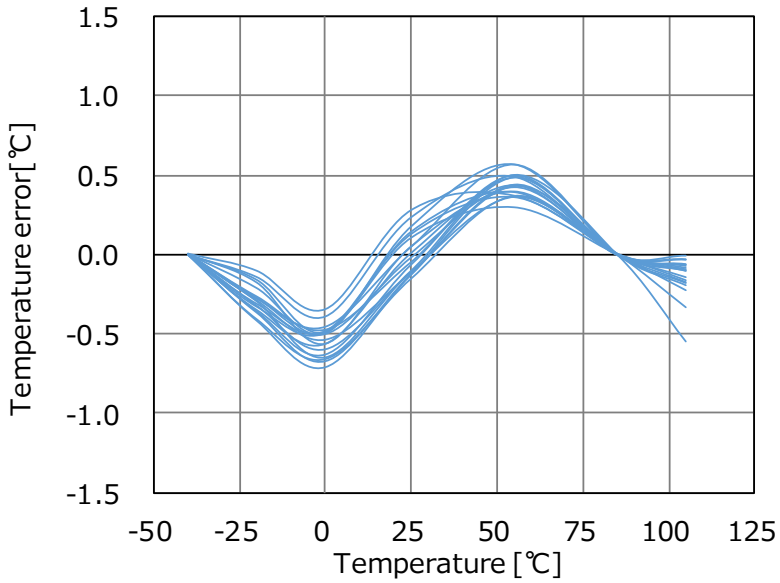


5. Temperature sensor (TEMPS)

5.1 Temperature error

AVCC0=5V

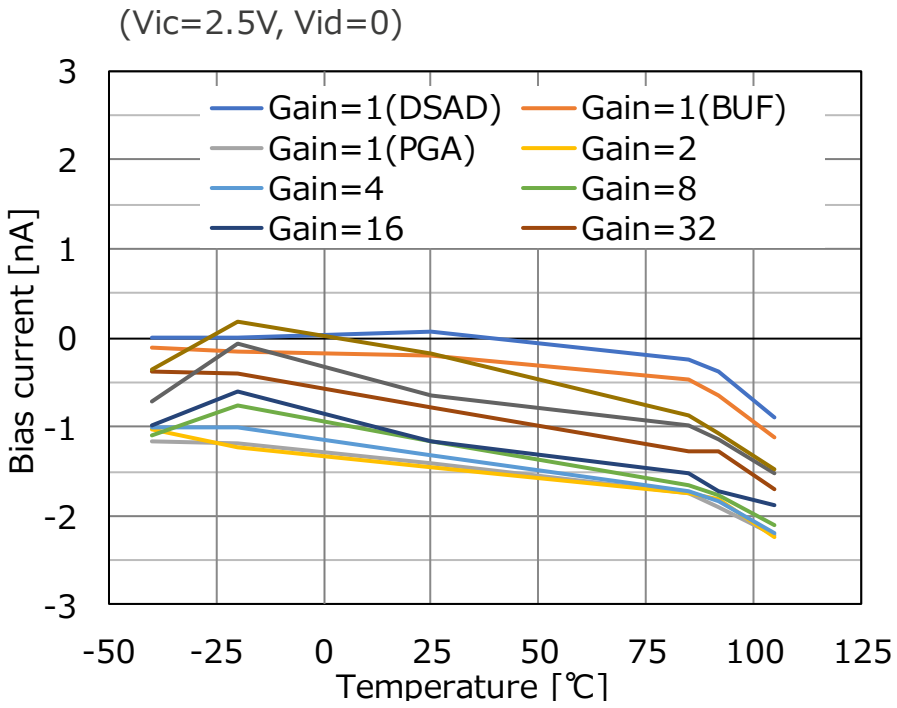
(n=18, Not include measurement uncertainty)

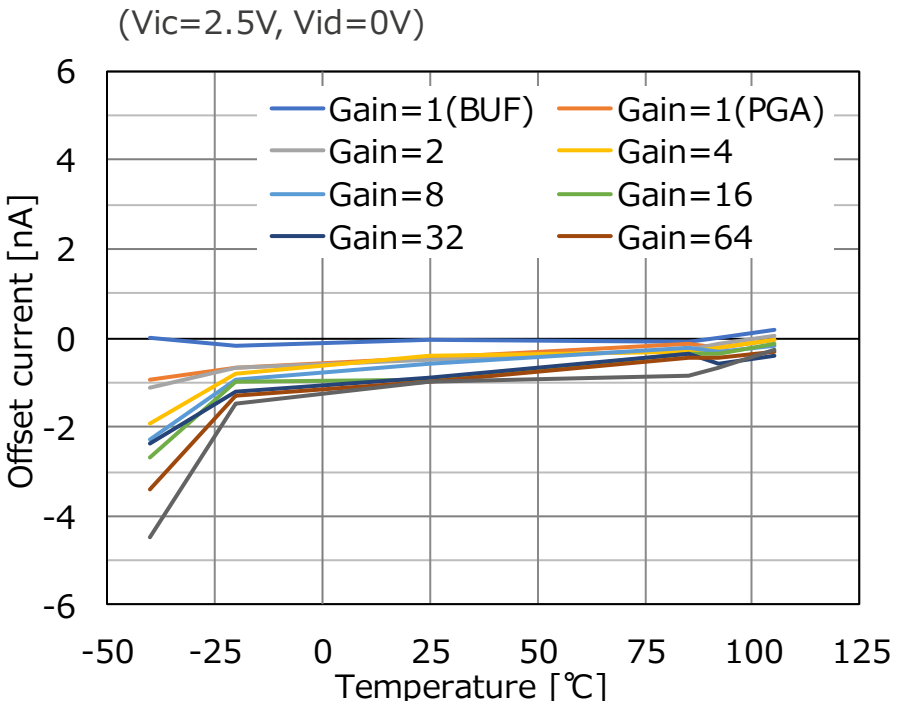


6. 24-bit Delta-Sigma A/D Converter Analog Input

6.1 Input current temperature dependence

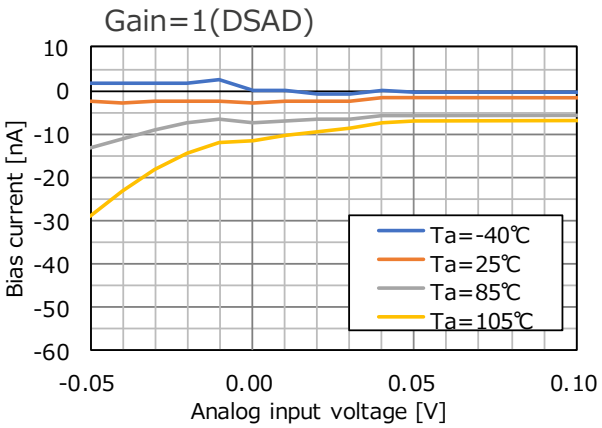
AVCC0=5V, Normal mode

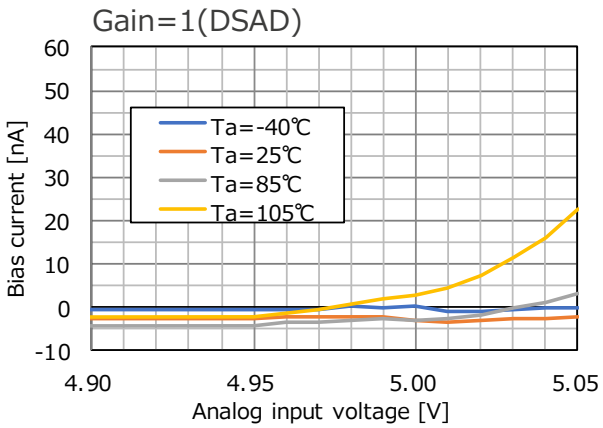


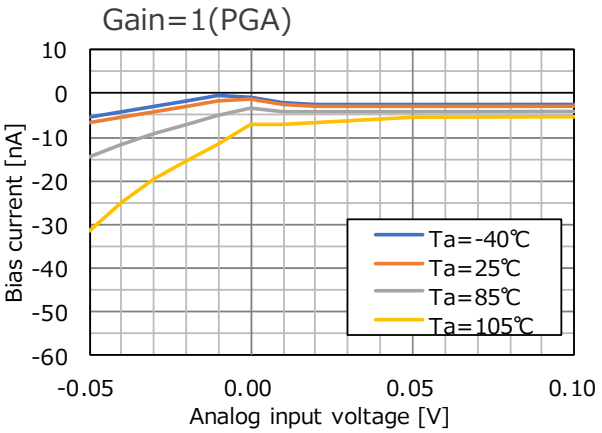


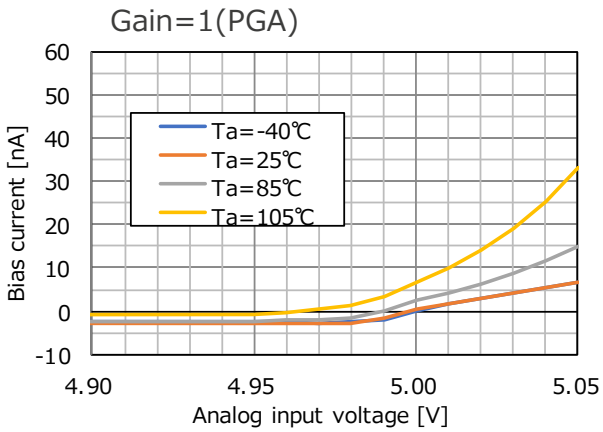
6.2 Input bias current – Input voltage

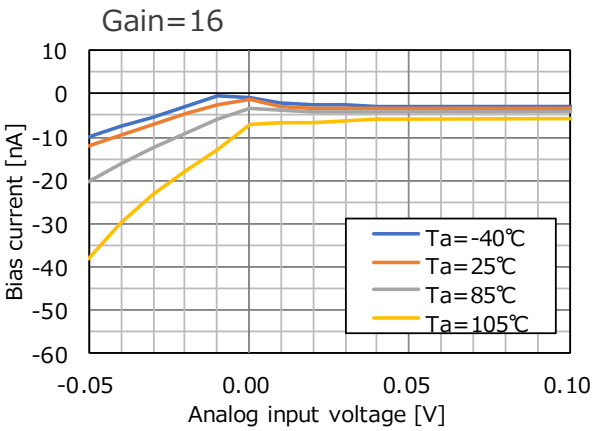
AVCC0=5V, Normal mode

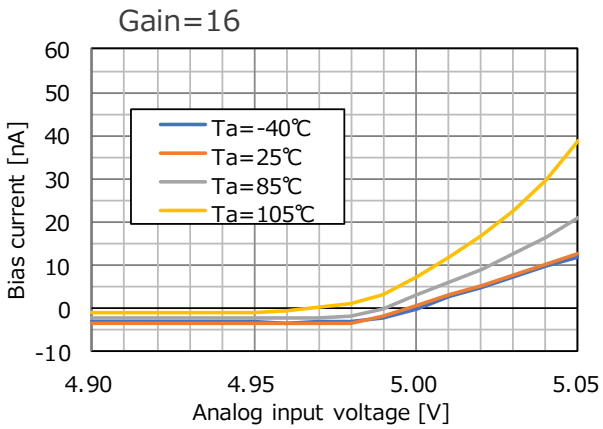


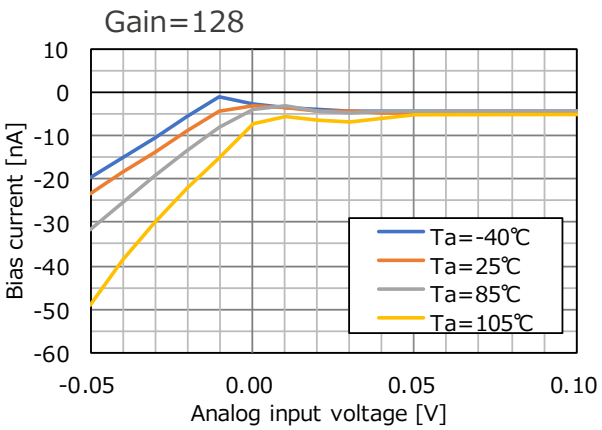


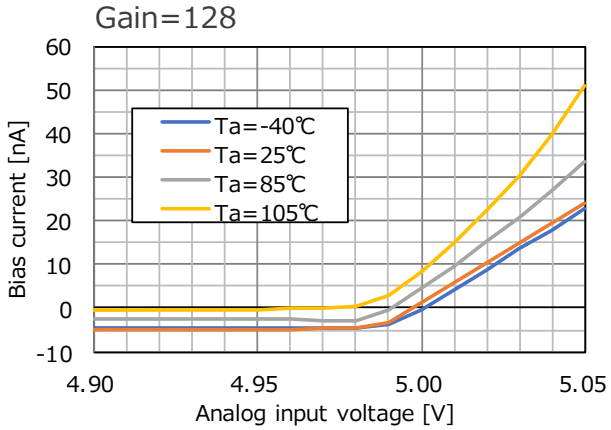






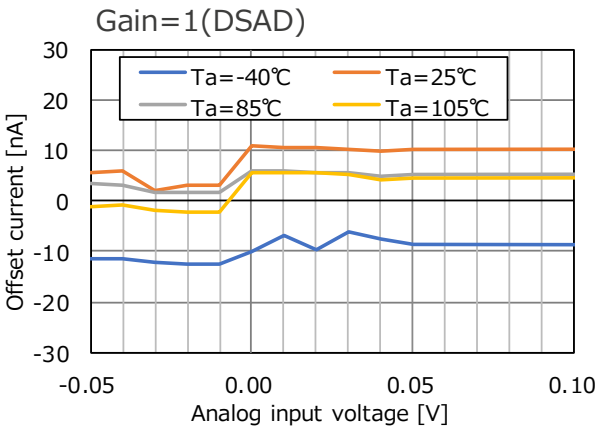


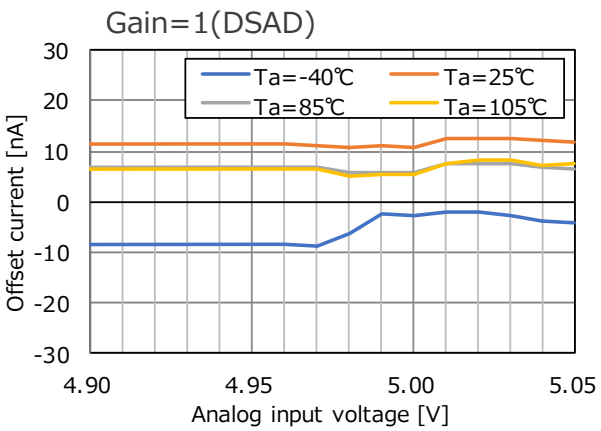


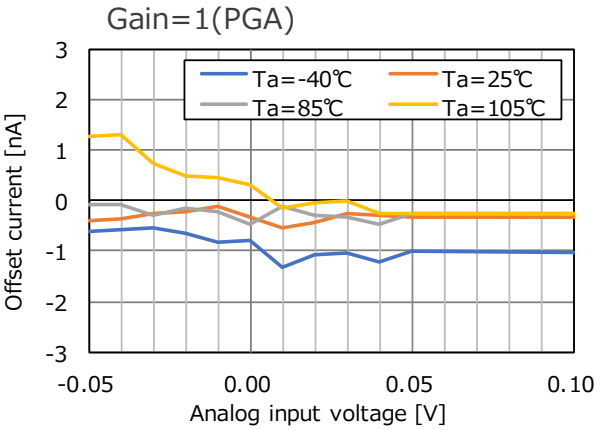


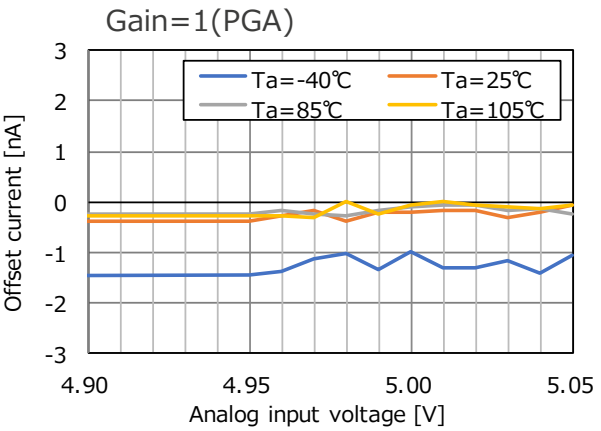
6.3 Input offset current - Input voltage

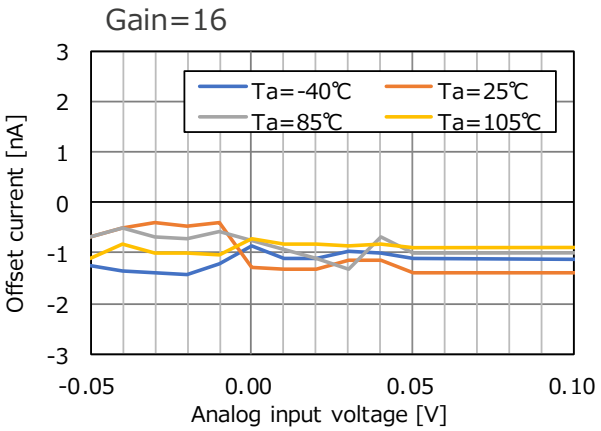
AVCC0=5V, Normal mode

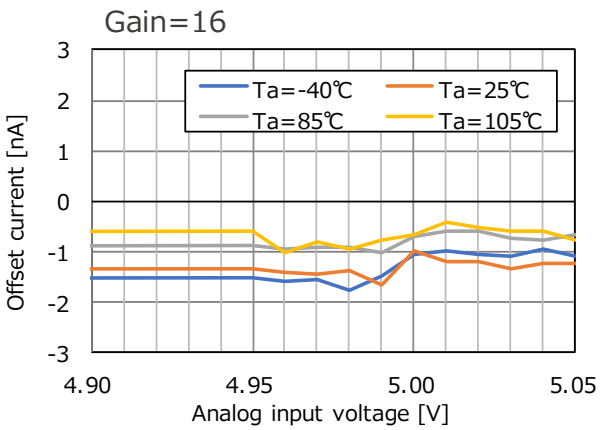


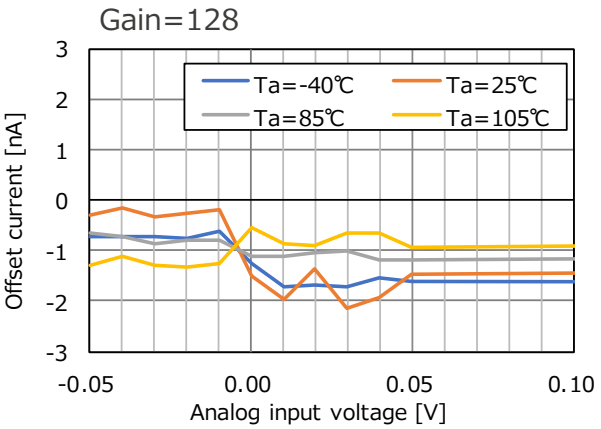


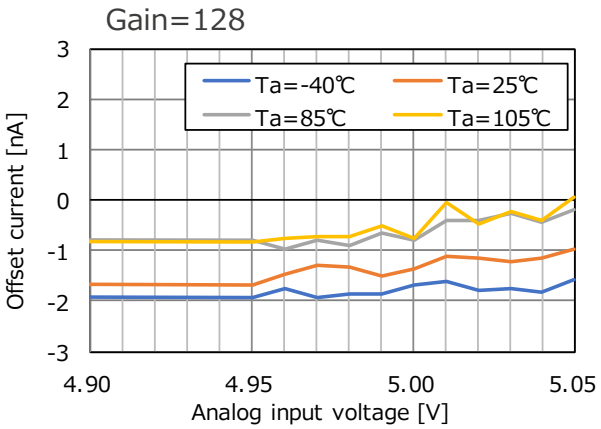








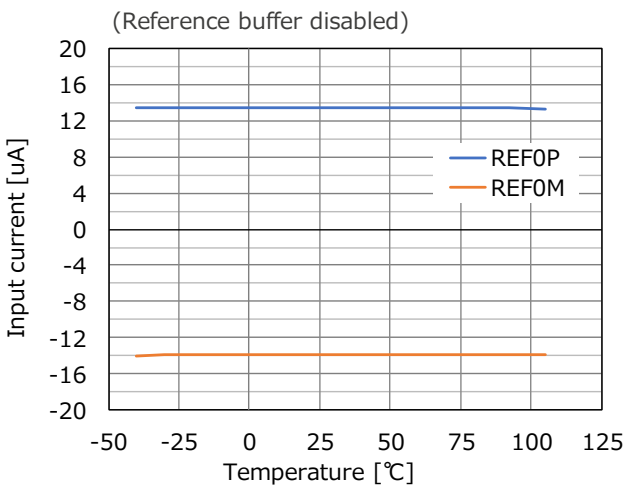


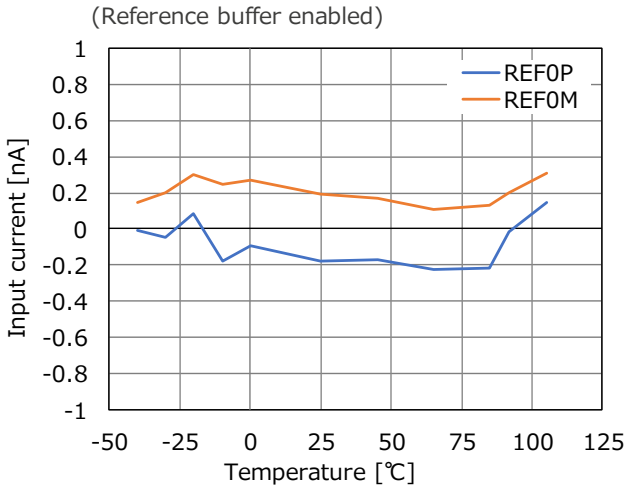


7. External Reference Input

7.1 Input current temperature dependence

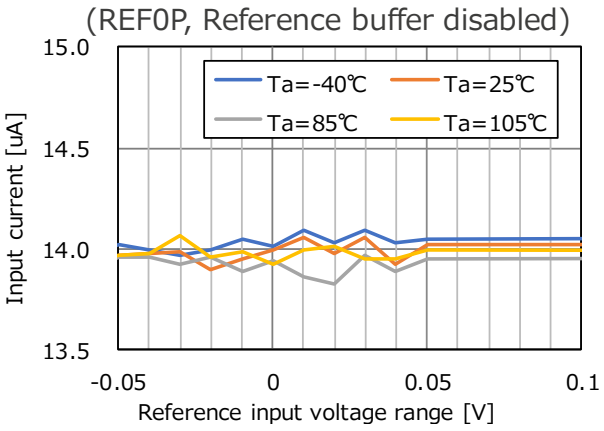
AVCC0=5V, VREF=2.5V

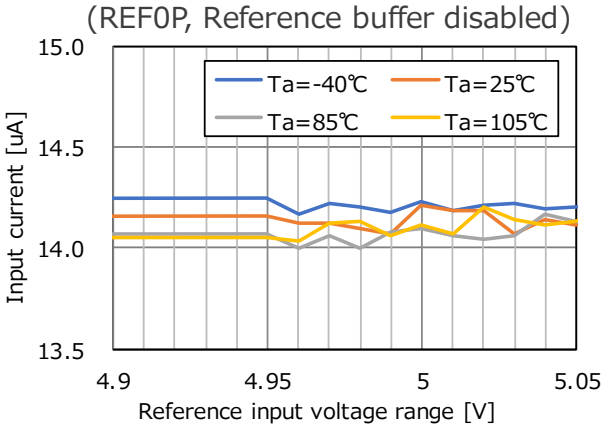


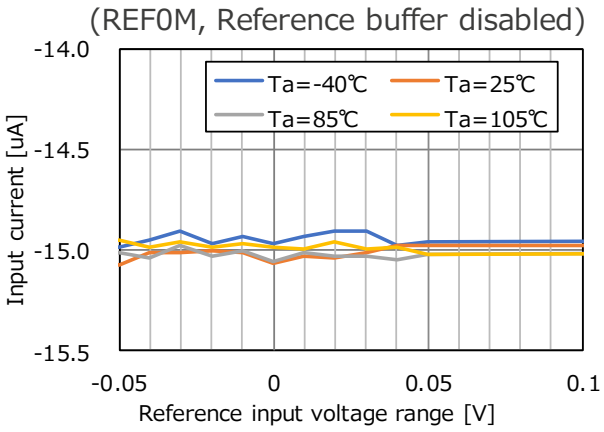


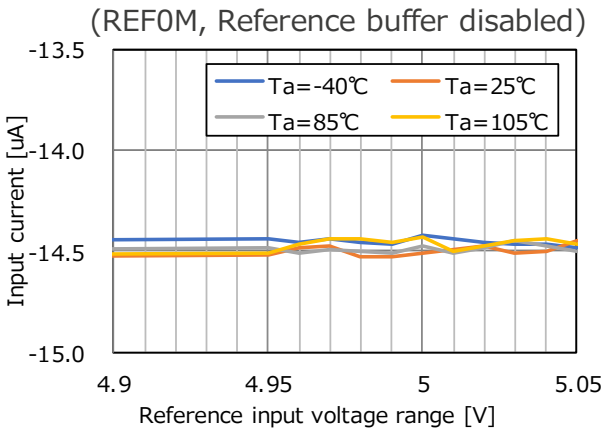
7.2 Input current – Input voltage

AVCC0=5V, VREF=2.5V





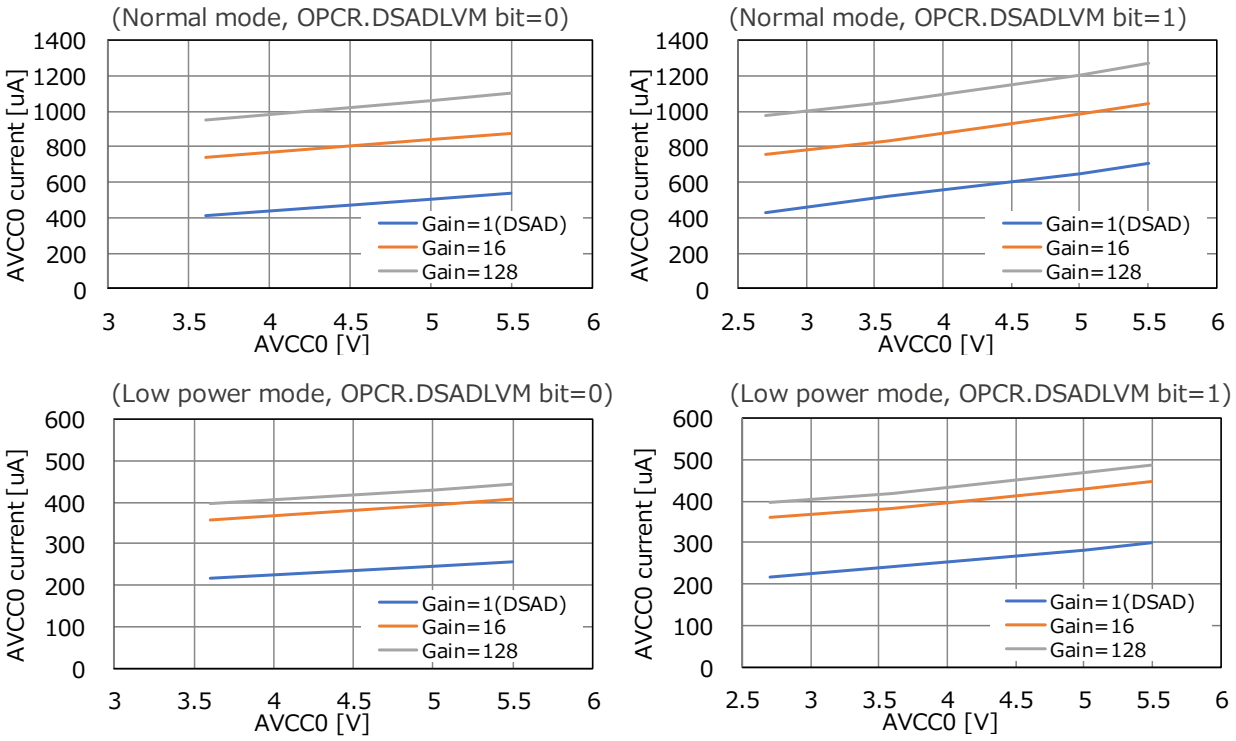




8. Operating Current

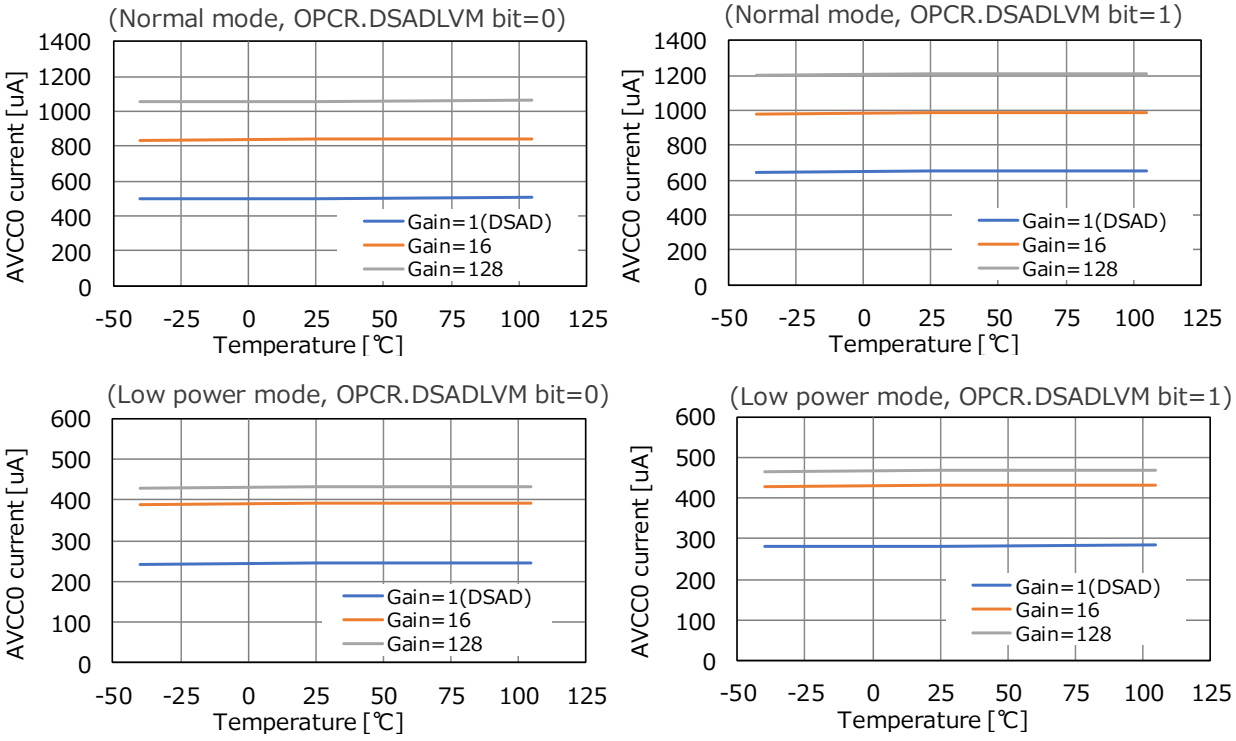
8.1 24-bit Delta-Sigma A/D converter operating current – AVCC0

Ta=25°C

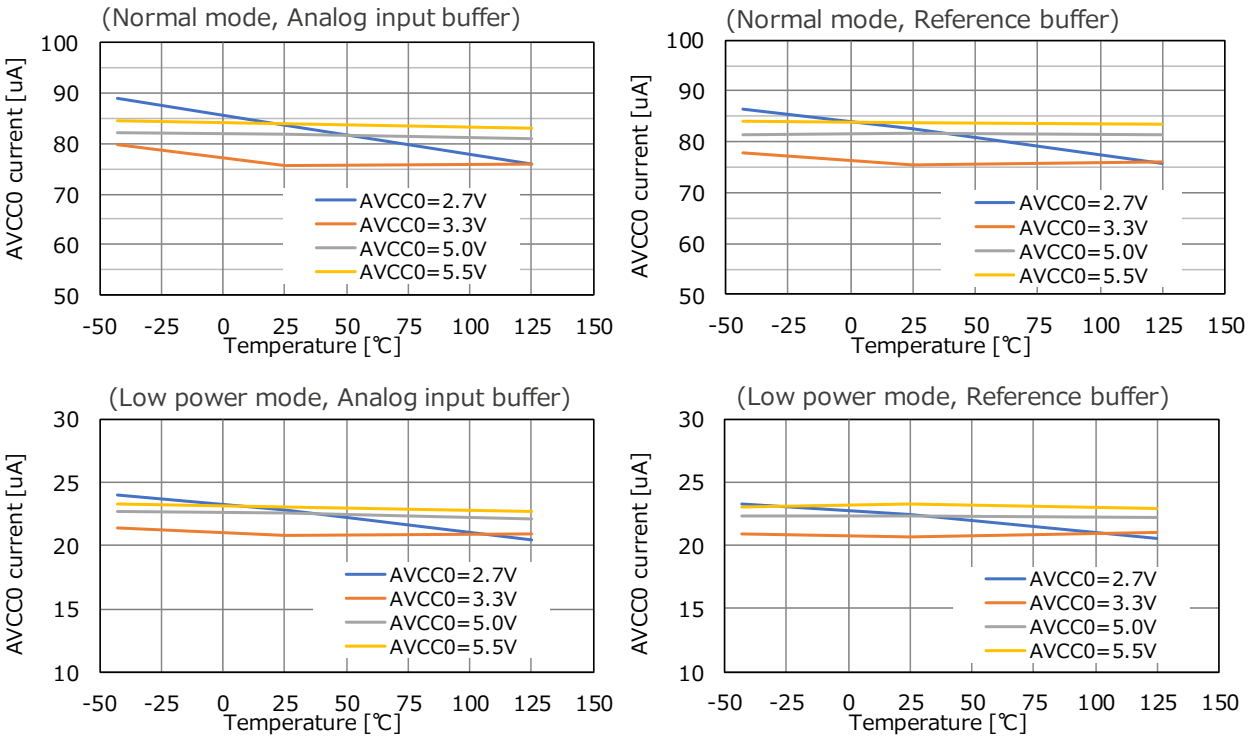


8.2 24-bit Delta-Sigma A/D converter operating current temperature dependence

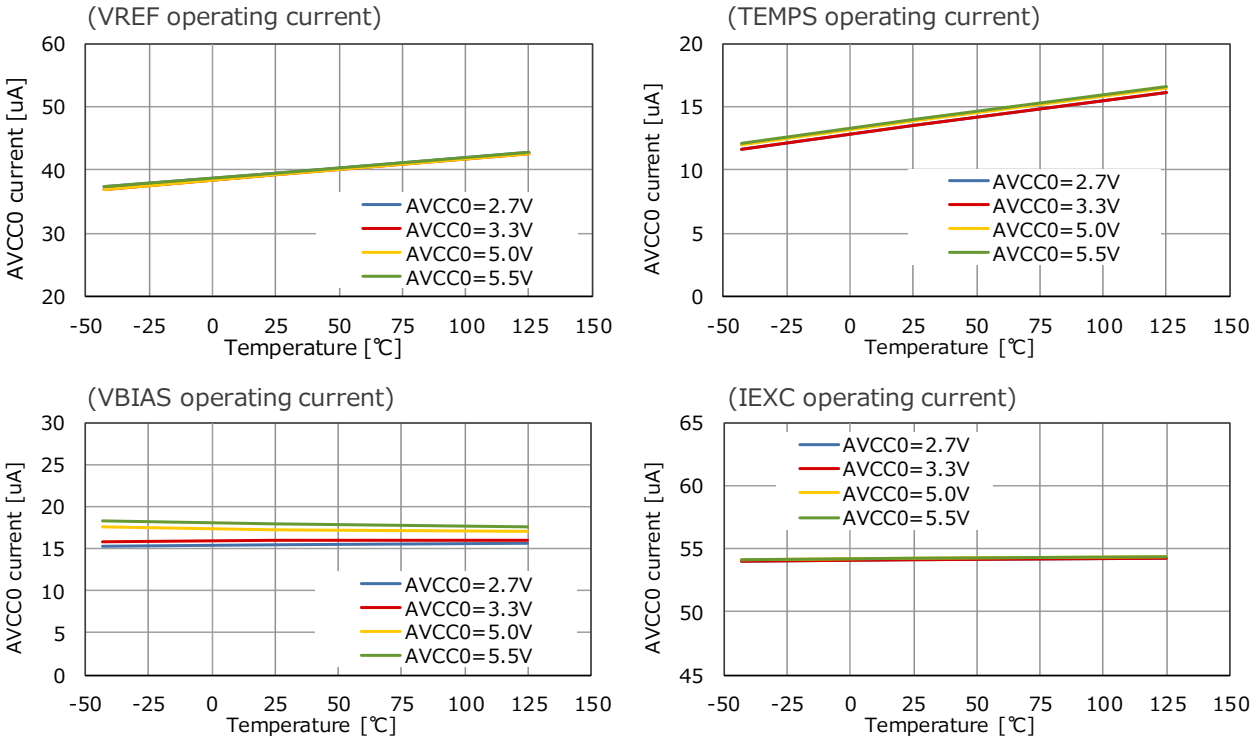
AVCC0=5V



8.3 Buffer operating current temperature dependence



8.4 Voltage reference (VREF), Temperature sensor (TEMPS), Bias voltage generator (VBIAS), Excitation current source (IEXC)

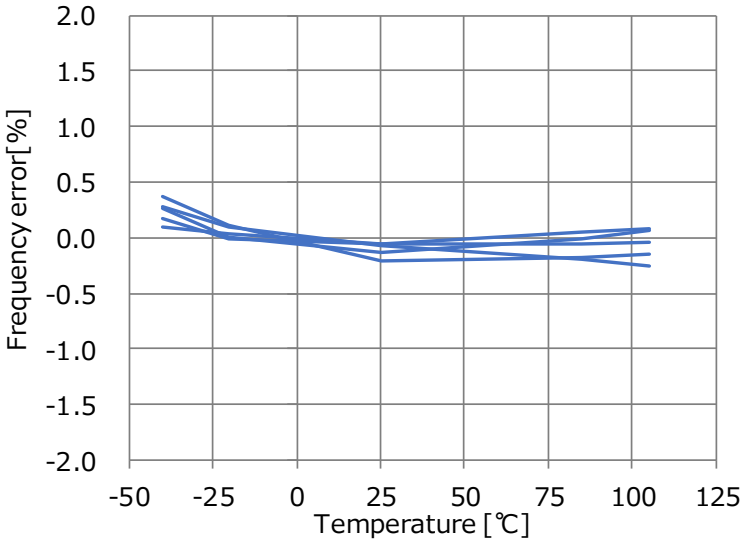


9. High-Speed On-Chip Oscillator (HOCO)

9.1 Temperature drift

AVCC0=5V

(n=5, Normalized at 32MHz)

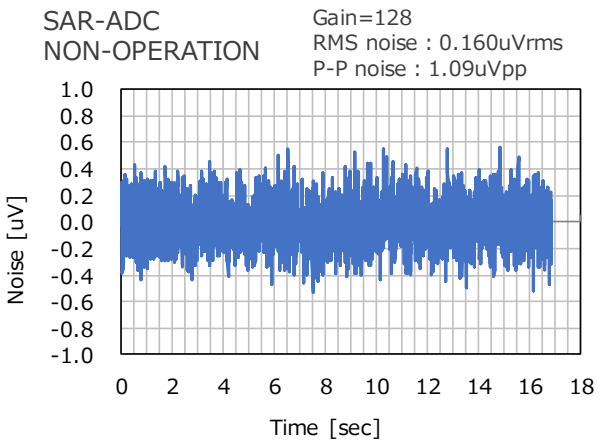


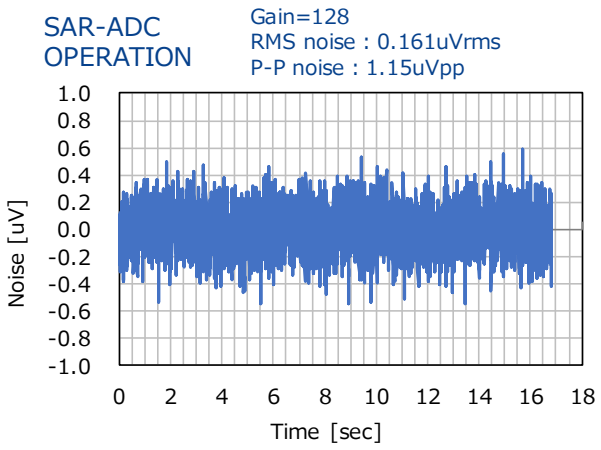
10. Interference

10.1 From 12bit SAR-ADC

AVCC=5V, Ta=25°C, External CLK=8MHz
Normal mode, Date rate=244sps, External VREF=2.5V, AIN=0V
12bit SAR-ADC : Input=AVCC, Sampling time=7.5us, Discharge ON

Condition	Peak-to-peak noise[uVpp] (RMS noise[uVrms])			
	Gain=1 (DSAD)	Gain=1 (PGA)	Gain=16	Gain=128
SAR-ADC NON-OPERATION	**12.5 (1.90)**	**19.7 (3.01)**	**3.50 (0.508)**	**1.09 (0.160)**
SAR-ADC OPERATION	13.7 (1.92)	21.5 (3.01)	3.32 (0.509)	1.15 (0.161)

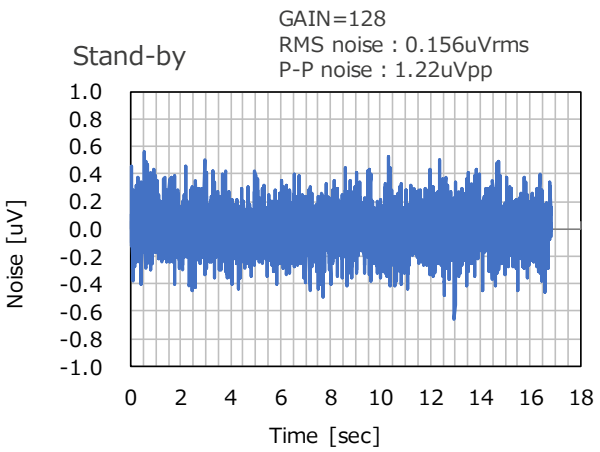


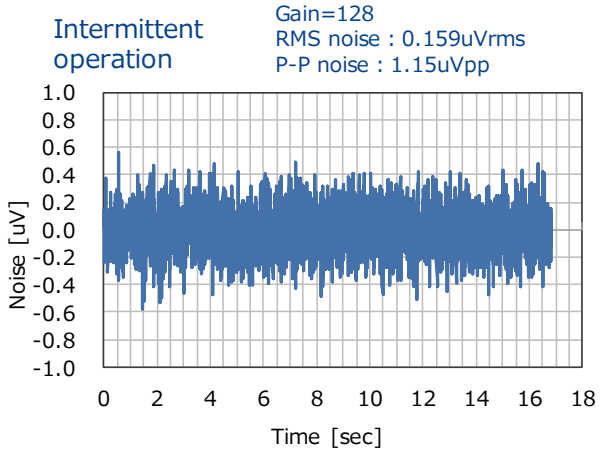


10.2 From MCU

AVCC=5V, Ta=25°C, External CLK=8MHz
Normal mode, Date rate=244sps, External VREF=2.5V, AIN=0V

Condition	Peak-to-peak noise[uVpp] (RMS noise[uVrms])			
	Gain=1 (DSAD)	Gain=1 (PGA)	Gain=16	Gain=128
Stand-by	13.1 (1.92)	18.8 (2.91)	3.69 (0.514)	1.22 (0.156)
Continuous operation (IIR filter)	**13.4 (1.99)**	**19.1 (2.91)**	**3.58 (0.513)**	**1.07 (0.159)**
Intermittent operation (Multiplication<->Stand-by)	**13.7 (1.99)**	**19.7 (2.89)**	**3.50 (0.499)**	**1.15 (0.159)**

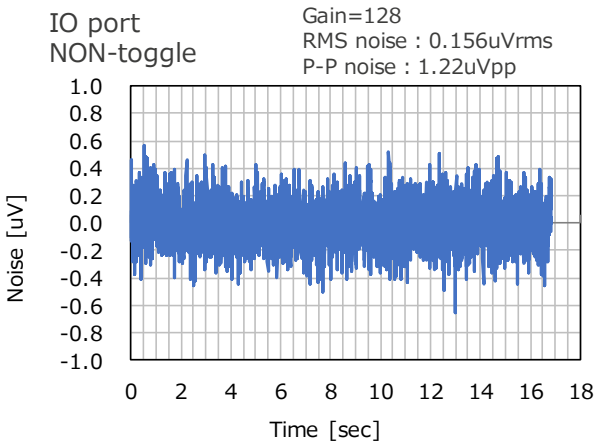


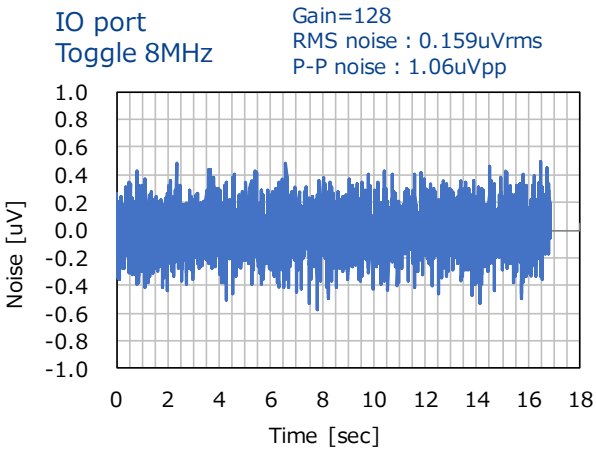


10.3 From IO port

VCC=AVCC=5V, Ta=25°C, External CLK=8MHz
Normal mode, Date rate=244sps, External VREF=2.5V, AIN=0V
IO port：PC14~17(Four terminals), Toggle frequency=8MHz, Cload=30pF

Condition	Peak-to-peak noise[uVpp] (RMS noise[uVrms])			
	Gain=1 (DSAD)	Gain=1 (PGA)	Gain=16	Gain=128
IO port NON-toggle	13.1 (1.92)	18.8 (2.91)	3.69 (0.514)	1.22 (0.156)
IO port Toggle 8MHz	**13.4 (1.99)**	**19.1 (2.91)**	**3.58 (0.513)**	**1.07 (0.159)**





Revision history

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 03, 2020	-	First release
2.00	Nov. 10, 2021	4	1. RX23E-A Analog Front End Features Voltage reference output voltage, temperature drift, changed
		26	3.1 Initial accuracy, Temperature drift, changed

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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