RX23T Group

Motor Control Function Migration Guide (RX210, RX62T or RX63T to RX23T)

R01AN3669EJ0100
Rev.1.00
Mar 09, 2017

Introduction

When migrating motor control functions from the RX210, RX62T or RX63T to the RX23T, there are a number of points regarding hardware and software that should be borne in mind.

The points related to hardware are described in 1, Points Regarding Pin Settings, and the points related to software are described in 2, Points Regarding Function Settings.

For points of difference regarding registers, refer to the separate application note “Points of Difference Between RX23T Group and RX62T Group” (R01AN2823EJxxxx). (The revision number is represented by “xxxx”. Make sure to refer to the latest revision of the application note.)

This application note applies to the 64-pin versions of the above products.

Target Device

RX23T

Contents

1. Points Regarding Pin Settings

1.1 Clock

1.1.1 Oscillator Pin

The main clock frequency of the RX23T may be in the range 1 MHz to 20 MHz.

When migrating from the RX210, RX62T or RX63T, the previous setting may be used unchanged.

The main clock frequency ranges of the three microcontrollers are shown below.

	RX210	RX62T	RX63T	RX23T
Main clock frequency	1 MHz to 20 MHz	8 MHz to 12.5 MHz	4 MHz to 16 MHz	1 MHz to 20 MHz

1.2 VCL Pin (External Capacitor)

On the RX210, RX62T and RX63T the VCL pin should be connected to a 0.1 μF smoothing capacitor for internal power supply stabilization, and on the RX23T it should be connected to a 4.7 μF smoothing capacitor for this purpose.

The capacitor should be located near the VCL pin.

1.3 PLLVCC Pin

On the RX62T a 22 μF bypass capacitor should be inserted between the PLLVCC (pin number 20) and PLLVSS (pin number 22) pins. The RX23T does not have a PLLVCC pin.

On the RX23T a 0.1 μF bypass capacitor should be inserted between the VCC (pin number 20) and VSS (pin number 22) pins.

In both cases, the bypass capacitor should be located as close as possible to the power supply pins, and the connecting pattern lines should be as short and as thick as possible.

1.4 12-Bit A/D Converter

Important points when migrating software that uses up to ten A/D input pin channels on the RX210, RX62T or RX63T to the RX23T are described below.

1.4.1 A/D Input Pins

The 12-bit A/D converter module of the RX23T comprises one unit with 10 analog input channels assigned to pins AN000 to AN007, AN016, and AN017.

When migrating from the RX210, change the assignments of pins AN008 to AN013 on the RX210 to unused pins among AN000 to AN007, AN016, and AN017 on the RX23T. There are some functional points of difference, however, and caution is therefore necessary.

When migrating from the RX62T, pins AN000 to AN003 on the RX23T can be used in the same manner as pins AN000 to AN003 on the RX62T. Change the assignments of pins AN100 to AN103 on the RX62T to pins among AN004 to AN007, AN016 , and AN017 on the RX23T. There are some functional points of difference, however, and caution is therefore necessary.

When migrating from the RX63T, pins AN000 to AN007 on the RX23T can be used in the same manner as pins AN000 to AN007 on the RX63T.

A list of the 12-bit A/D converter input pin assignments of the three microcontrollers is shown below.

	Pin Assignment			
Pin Function	**RX210**	**RX62T**	**RX63T**	**RX23T**
AN000	P40	P40	P40	P40
AN001	P41	P41	P41	P41
AN002	P42	P42	P42	P42
AN003	P43	P43	P43	P43
AN004	P44	—	P44	P44
AN005	—	—	P45	P45
AN006	P46	—	P46	P46
AN007	—	—	P47	P47
AN008	PE0	—	—	—
AN009	PE1	—	—	—
AN010	PE2	—	—	—
AN011	PE3	—	—	—
AN012	PE4	—	—	—
AN013	PE5	—	—	—
AN016	—	—	—	P11
AN017	—	—	—	P10
AN100	—	P44	—	—
AN101	—	P45	—	—
AN102	—	P46	—	—
AN103	—	P47	—	—

1.4.2 ADST Bit Status Output Pins

The ADST bit status output pin functionality has been extended on the RX23T.

The ADST bit (A/D conversion start bit) indicates whether A/D conversion is stopped (0) or started (1). The following pins can be used to check the AD conversion state.

P02/ADST0 Pin and PD6/ADST0 Pin

For details of ADST bit change conditions, refer to section 29, 12-Bit A/D Converter (S12ADE), in RX23T Group User's Manual: Hardware.

1.4.3 A/D Converter Input Clock

On the RX210, RX63T and RX23T the peripheral module clock (S12AD clock) (PCLKD) is used as the A/D conversion clock (ADCLK).

The RX62T does not have a peripheral module clock D (PCLKD), so when migrating to the RX23T it is necessary to add settings for peripheral module clock D (PCLKD).

1.4.4 Pins Supporting Channel-Dedicated Sample-and-Hold Function

On the RX210, RX63T and RX23T pins AN000 to AN002 support the channel-dedicated sample-and-hold function.

On the RX62T it is possible to use the channel-dedicated sample-and-hold function on both channels 0 to 2 (AN000 to AN002) of S12AD0 and channels 0 to 2 (AN100 to AN102) of S12AD1, but on the RX23T it is not possible in such cases to use the channel-dedicated sample-and-hold function on channels 0 to 2 (AN100 to AN102) of S12AD1.

1.4.5 Pins Supporting Designation for Group A Priority Control

On the RX23T pins AN000 to AN007, AN016, and AN017 support designation for group A priority control.

During basic operation in group scan mode, all other trigger inputs are ignored during scan operation on group A or group B. When group A priority control is enabled, in contrast, if a trigger input for group A is received during A/D conversion operation on group B, A/D conversion on group B halts so that A/D conversion on group A can proceed.

The RX63T supports group A priority control, but this function is not supported on the RX210 and RX62T.

1.5 Timers

Important points when migrating software that performs one-motor PWM output control using the complementary PWM mode of the multi-function timer pulse unit (MTU) of the RX62T or RX63T to the RX23T are described below.

1.5.1 PWM Output Pins

When migrating from the RX210, the PWM output pins used for complementary PWM mode must be changed.

When migrating from the RX62T or RX63T, the pins of the RX23T can be used in the same manner as those of the RX62T or RX63T.

The PWM output pins used in complementary PWM mode are listed below.

Channel	Output Pin	Description
MTU3	MTIOC3B	PWM output pin 1
	MTIOC3D	PWM output pin 1’ (PWM output 1 negative-phase waveform output)
MTU4	MTIOC4A	PWM output pin 2
	MTIOC4C	PWM output pin 2’ (PWM output 2 negative-phase waveform output)
	MTIOC4B	PWM output pin 3
	MTIOC4D	PWM output pin 3’ (PWM output 3 negative-phase waveform output)

The port assignments on the three microcontrollers of the PWM output pins in complementary PWM mode are listed below.

		Port Assignment			
Channel	Output Pin	RX210 (Applies to TFLGA and LQFP)	RX62T	RX63T	RX23T
MTU3	MTIOC3B	P17/PC5/PB7	P71	P71	P71
	MTIOC3D	P16/PC4/PB6	P74	P74	P74
MTU4	MTIOC4A	PA0/PB3/PE2	P72	P72	P72
	MTIOC4C	PB1/PE5/PE1	P75	P75	P75
	MTIOC4B	P30/P54/PC2/PE3	P73	P73	P73
	MTIOC4D	P31/P55/PC3/PE4	P76	P76	P76

1.5.2 A/D Conversion Start Request Frame Synchronization Signal Output Pins

On the RX23T the functionality of the A/D conversion start request frame synchronization signal output pins has been extended.

The A/D conversion start request frame synchronization signal allows monitoring, using an external pin, of the timing of the generation of A/D conversion start request signals. The pins that can be used to check the timing of the generation of A/D conversion start request signals are as follows:

PB2/ADSM0 Pin

After the A/D conversion start request signal to be monitored is selected in A/D conversion start request select register 0 (TADSTRGR0) of the multi-function timer pulse unit (MTU), a high-level pulse signal is output on the ADSM0 pin when an A/D conversion start request signal is generated, and a low-level pulse signal is output on the ADSM0 pin on the timer cycle used to generate the A/D conversion start request signal.

1.6 Protection Functions

1.6.1 POE Input Pins

The important points when migrating software that performs one-motor PWM output control using the complementary PWM mode of the multi-function timer pulse unit (MTU), and input on pins POE0# from the RX210, RX62T or RX63T to the RX23T, are described below.

When migrating from the RX210, assignment of the POE0# pin must be changed.

When migrating from the RX62T or RX63T to the RX23T, pins POE0# can be used in the same manner.

The pin assignments of the POE input pins of the three microcontrollers are listed below.

	Port Assignment			
Input Pin	**RX210**	**RX62T**	**RX63T**	**RX23T**
POE0#	PC4	P70	P70	P70
POE1#	PB5	—	—	—
POE2#	PA6	—	—	—
POE3#	PB3	—	—	—
POE8#	P30/P17/PE3	PB4	PB4	PB4
POE10#	—	PE2	PE2	PE2
POE11#	—	—	PB5	—

Note that on the RX210 high-impedance control by POE takes effect regardless of the MTU pin selection settings in the port mode register (PMR). High-impedance control cannot be applied to pins selected as general I/O ports.

On the RX62T, RX63T, and RX23T high-impedance control by POE takes effect regardless of the setting of the port mode register (PMR).

The high-impedance target pins in case of POE detection on the three microcontrollers are listed below.

POE Detection	High-Impedance Target Pins			
	RX210	**RX62T**	**RX63T**	**RX23T**
POE0	MTU complementary PWM output pins (MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D)	MTU complementary PWM output pins (MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4C, MTIOC4B, MTIOC4D) *1	MTU complementary PWM output pins (MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4C, MTIOC4B, MTIOC4D, or (MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7C, MTIOC7B, MTIOC7D) *2	MTU complementary PWM output pins (MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) *3
POE1	MTU complementary PWM output pins (MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D)	—	—	—
POE2	MTU complementary PWM output pins (MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D)	—	—	—
POE3	MTU complementary PWM output pins (MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D)	—	—	—
POE8	MTU0 output pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D)	MTU0 pins (MTIOC0A-A, MTIOC0A-B, MTIOC0B-A, MTIOC0B-B, MTIOC0C, MTIOC0D) *4	MTU0 pins (MTIOC0A, TIOC0B, MTIOC0C, MTIOC0D) *4	MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) *5
POE10	—	GPT0 and GPT1 pins (GTIOC0A-B, GTIOC0B-B, GTIOC1A-B, GTIOC1B-B, GTIOC2A-B) *6	GPT0 and GPT1 pins (GTIOC0A, GTIOC0B, GTIOC1A, GTIOC1B) *6	*7

POE Detection	High-Impedance Target Pins			
	RX210	RX62T	RX63T	RX23T
POE11	—	—	GPT2 and GPT3 pins (GTIOC2A, GTIOC2B, GTIOC3A, GTIOC3B) *8	—

Note 1. By means of register settings, the MTU complementary PWM output pins (pins MTU6 and MTU7), MTU0 pin, and GPT pin can be put in the high-impedance state.
Note 2. By means of register settings, the MTU0 pin and GPT pin can be put in the high-impedance state.
Note 3. By means of register settings, the MTU0 pin can be put in the high-impedance state.
Note 4. By means of register settings, the MTU complementary PWM output pins (pins MTU3 and MTU4, and pins MTU6 and MTU7), and the GPT pin can be put in the high-impedance state.
Note 5. By means of register settings, the MTU complementary PWM output pins (pins MTU3 and MTU4) can be put in the high-impedance state.
Note 6. By means of register settings, the MTU complementary PWM output pins (pins MTU3 and MTU4, and pins MTU6 and MTU7), MTU0 pin, GPT2 pin, and GPT3 pin can be put in the high-impedance state
Note 7. By means of register settings, the MTU complementary PWM output pins (pins MTU3 and MTU4), the MTU0 pin can be put in the high-impedance state.
Note 8. By means of register settings, the MTU complementary PWM output pins (pins MTU3 and MTU4, or pins MTU6 and MTU7), the MTU0 pin, the GPT0 pin, and the GPT1 pin can be put in the high-impedance state.

1.6.2 LVD Input Pin

On the RX210, RX62T, RX63T, and RX23T the VCC pin is used as the input pin of the voltage detection circuit (LVD).

1.6.3 Comparator Input Pins

Comparator detection input pins CMPA1, CMPA2, CMPB0, and CMPB1, and reference voltage setting input pins CVREFA, CVREFB0, and CVREFB1, used by comparator A and comparator B on the RX210, are not present on the RX23T.

On the RX23T changes must be made to the comparator detection input pins (CMPC00 to CMPC02, CMPC10 to CMPC12, and CMPC20 to CMPC22), the internal reference voltage (AVCC0), the reference voltage setting input pins (CVREFC0 and CVREFC1), and the on-chip D/A converter output voltage.

The reference voltage setting input pins CVREFL and CVREFH of the RX62T and RX63T are not present on the RX23T. In addition, on the RX23T pins AN000 to AN002 and AN100 to AN102 cannot be used as comparator detection input pins, and AVCC0 cannot be used as a reference voltage setting input pin.

On the RX23T the comparator detection input pins are CMPC00 to CMPC02, CMPC10 to CMPC12, and CMPC20 to CMPC22; the internal reference voltage (AVCC0); the reference voltage setting input pins are CVREFC0 and CVREFC1; and the on-chip D/A converter output voltage must be changed.

Also, if AN000 to AN002 and AN100 to AN102 are assigned as comparator detection input pins, these pin function settings must be changed to CMPC00 to CMPC02, CMPC10 to CMPC12, and CMPC20 to CMPC22.

The comparator input pins of the three microcontrollers are listed below.

	RX210		RX62T		RX63T		RX23T	
Type	Pin	Port Assignment	Pin	Port Assignment	Pin	Port Assignment	Pin	Port Assignment
Comparator detection input pins	CMPA1	PE3	AN000	P40	AN000	P40	CMPC00 (AN000)	P40
	CMPA2	PE4	AN001	P41	AN001	P41	CMPC01 (AN003)	P43
	CMPB0	PE1	AN002	P42	AN002	P42	CMPC02 (AN006)	P46
	CMPB1	PA3	AN100	P44	—	—	CMPC10 (AN001)	P41
	—	—	AN101	P45	—	—	CMPC11 (AN004)	P44
	—	—	AN102	P46	—	—	CMPC12/CMPC22 (AN007)	P47
	—	—	—	—	—	—	CMPC20 (AN002)	P42
	—	—	—	—	—	—	CMPC21 (AN005)	P45
	—	—	—	—	—	—	AVCC0 (internal reference voltage)	(57Pin)
Reference voltage setting input pins	CVREFA	PA1	CVREFL	P43	CVREFL	P43	CVREFC0 (AN016)	P11
	CVREFB0	PE2	CVREFH	P47	CVREFH	P47	CVREFC1 (AN017)	P10
	CVREFB1	PA4	3-bit D/A converter output voltage	—	3-bit D/A converter output voltage	—	On-chip 8-bit D/A converter output voltage	—

Note: Items in parentheses are multiplexed analog pins.

2. Points Regarding Function Settings

2.1 Clocks

2.1.1 Main Clock Oscillator

On the RX210, RX62T, RX63T, and RX23T the available methods of supplying a clock signal to the main clock oscillator are connection to a resonator and input of an external clock signal.

When migrating software, keep in mind that on the RX62T and RX63T it was not possible to change the main clock oscillator oscillation source by means of a register setting, whereas on the RX23T the oscillation source can be changed using the MOSEL (main clock oscillator switch) bit in the main clock oscillator forced oscillation control register (MOFCR).

When migrating from the RX210, switching the oscillation source of the main clock oscillator is accomplished on the RX23T as well by setting the main clock oscillator switch (MOSEL) bit in the main clock oscillator forced oscillation control register (MOFCR).

On the RX62T the main clock oscillator is the clock source of the system clock (ICLK) and peripheral module clock (PCLK).

On the RX23T, as on the RX210 and RX63T, either the main clock oscillator or the on-chip oscillator clock can be selected as the clock source of the system clock (ICLK), peripheral module clock (PCLK), etc.

On the RX23T clock source selection is accomplished by setting the CKSEL[2:0] (clock source select) bits in system clock control register 3 (SCKCR3).

The on-chip oscillator clock oscillation frequencies that can be used as the clock source on the RX210, RX63T and RX23T are listed below.

	RX210	RX62T	RX63T	RX23T
High-speed on-chip oscillator (HOCO)	32 MHz/ 36.864 MHz/ 40 MHz/ 50 MHz	—	—	32 MHz
Low-speed on-chip oscillator (LOCO)	125 KHz	—	125 KHz	4 MHz

On the RX23T the system clock (ICLK) setting requires that a setting be made to the MEMWAIT (memory wait cycle setting) bits in the memory wait cycle setting register (MEMWAIT).

On the RX62T a single peripheral module clock (PCLK) was supplied to all peripheral modules, but on the RX23T, as on the RX210 and RX63T, the peripheral module clock functionality has been extended.

The applications of the peripheral module clock of the RX23T are listed below.

Peripheral Module Clock Type	Application
Peripheral module clock A (PCLKA)	The multi-function timer pulse unit (MTU)
Peripheral module clock B (PCLKB)	Peripheral clock for modules other than the multi-function timer pulse unit (MTU) and 12-bit A/D converter (S12AD)
Peripheral module clock D (PCLKD)	12-bit A/D converter (S12AD)

On the RX62T the division ratios of the system clock (ICLK) and the peripheral module clock (PCLK) were specified by the settings of ICK[3:0] and PCK[3:0] in the system clock control register (SCKCR), but on the RX23T the division ratios of the system clock (ICLK) and the peripheral module clocks (PCLKA, PCLKB, and PCLKD) are specified by the settings of ICK[3:0], PCKA[3:0], PCKB[3:0], and PCKD[3:0], respectively, in the peripheral module clock system clock control register (SCKCR).

For details, refer to section 9, Clock Generation Circuit, in RX23T Group User's Manual: Hardware.

2.1.2 Memory Wait Cycles

On the RX23T the system clock (ICLK) setting requires that a setting be made to the MEMWAIT (memory wait cycle setting) bits in the memory wait cycle setting register (MEMWAIT).

The memory wait cycle setting register (MEMWAIT) controls ROM wait cycles.

The MEMWAIT setting conditions stipulate that the MEMWAIT bit must not be set to 0 (no wait states) when a system clock (ICLK) frequency higher than 32 MHz is selected.

Also, it is not necessary to set the MEMWAIT bit to 1 (wait states) when a system clock (ICLK) frequency of 32 MHz or lower is selected.

For details of the setting restrictions for the MEMWAIT bits, refer to section 9, Clock Generation Circuit, in RX23T Group User's Manual: Hardware.

The setting restrictions for the MEMWAIT bits are summarized below.

	Operating Power Control State		
	High-Speed Operating Mode		Middle-Speed Operating Mode
MEMWAIT Bits	ICLK ≤ 32 MHz	ICLK > 32 MHz	
0	Can be set.	Cannot be set.	Can be set.
1	Can be set.	Can be set.	Cannot be set.

2.2 Port Settings

The I/O ports of the RX23T can function as general I/O ports, I/O for peripheral functions, or as interrupt input pins.

Each port can also function as a peripheral module I/O pin, interrupt input pin, etc. After a reset it becomes an input port, but the function can be changed by means of register settings. The settings of the various ports are determined by the I/O port registers and the on-chip peripheral module registers.

On the RX23T, as on the RX210 and RX63T, port function settings are made in the pin function control registers of the multi-function pin controller (MPC) and the I/O port mode register (PMR). On the RX62T the priority level of output port functions is determined by the various functions, and input ports transfer signals to all functions for which the input setting is selected.

For details of the supported settings of each port of the RX23T, refer to section 19, Multi-Function Pin Controller (MPC), in RX23T Group User's Manual: Hardware.

2.3 A/D Conversion

2.3.1 Single-Shunt Current Detection

The settings necessary to perform A/D conversion at two user-defined locations, during the timer counter peak to trough or trough to peak interval, are described below.

Note that since it is necessary to give priority to shunt current detection over other A/D conversion operations, group scan mode is selected as the scan mode, the shunt current analog input is assigned to group A, group A priority control is enabled, and double trigger mode is selected for the A/D conversion trigger.

1. Set the scan mode select (ADCS[1:0]) bits in the A/D control register (ADCSR) to 01b (group scan mode).
2. In the A/D control register (ADCSR), set the double trigger mode select (DBLE) bit to 1 (double trigger mode selected) and the double trigger channel select (DBLANS [4:0]) bits to specify a channel as the analog input to be used as the double trigger target.
3. To select the A/D conversion start trigger for group A, set the A/D conversion start trigger select (TRSA[5:0]) bits in the A/D conversion start trigger select register (ADSTRGR) to 001011b (compare match of MTU4.TADCORA and MTU4.TCNT or compare match of MTU4.TADCORB and MTU4.TCNT).
4. Set the trigger start enable (TRGE) bit in the A/D control register (ADCSR) to 1 (start of A/D conversion by synchronous or asynchronous trigger enabled).
5. In the timer A/D converter start request cycle set buffer register of MTU4 (TADCOBRA or TADCOBRB), set the counter value for A/D conversion start requests.
6. In the timer A/D converter start request control register (TADCR) of MTU4, set the MTU4.TADCOBRA/B transfer timing select (BF[1:0]) bits to specify the A/D conversion start request cycle timing of transfers from the timer A/D converter start request cycle set buffer register (TADCOBRA or TADCOBRB) to the timer A/D converter start request cycle set register (TADCORA or TADCORB).
7. In the timer A/D converter start request control register (TADCR) of MTU4, set bits DT4BE, UT4BE, DT4AE, and UT4AE to specify the A/D conversion start request cycle.
8. Set the group A priority control setting (PGS) bit in the A/D group scan priority control register (ADGSPCR) to 1 (operation with group A priority control).

2.3.2 Three-Shunt Current Detection

The settings necessary to perform A/D conversion at timer counter peak or trough are described below.

Note that since it is necessary to give priority to shunt current detection over other A/D conversion operations, group scan mode is selected as the scan mode, the shunt current analog input is assigned to group A, and group A priority control is enabled.

1. In A/D channel select register A0 (ADANSA0), select analog inputs AN000 to AN002 as channels on which A/D conversion will be performed for group A.

2. Set the channel-dedicated sample-and-hold circuit bypass select (SHANS[2:0]) bits in the sample-and-hold circuit control register (ADSHCR) to specify that the channel-dedicated sample-and-hold circuits are used for AN000 to AN002.

3. Set the scan mode select (ADCS[1:0]) bits in the A/D control register (ADCSR) to 01b (group scan mode).

4. When A/D conversion takes place at timer counter peaks, set the A/D conversion start trigger select (TRSA[5:0]) bits in the A/D conversion start trigger select register (ADSTRGR) to 000100b (MTU3.TGRA compare match/input capture (peak)).
   When A/D conversion takes place at timer counter troughs, set the A/D conversion start trigger select (TRSA[5:0]) bits in the A/D conversion start trigger select register (ADSTRGR) to 000101b (MTU4.TGRA compare match/input capture, or MTU4.TCNT underflow (trough) in complementary PWM mode).

5. When A/D conversion takes place at timer counter peaks, set the A/D converter start request enable (TTGE) bit in the timer interrupt enable register (TIER) of MTU3 to 1 (A/D conversion start request generation enabled).
   When A/D conversion takes place at timer counter troughs, set the A/D converter start request enable 2 (TTGE2) bit in the timer interrupt enable register (TIER) of MTU4 to 1 (A/D conversion start request generation by MTU4.TCNT underflow (trough) enabled).

6. Set the channel-dedicated sample-and-hold circuit sampling time setting (SSTSH[7:0]) bits in the sample-and-hold circuit control register (ADSHCR) to specify the sampling time.

7. Set the trigger start enable (TRGE) bit in the A/D control register (ADCSR) to 1 (start of A/D conversion by synchronous or asynchronous trigger enabled).

8. Set the group A priority control setting (PGS) bit in the A/D group scan priority control register (ADGSPCR) to 1 (operation with group A priority control).

2.3.3 Bus Voltage

Obtaining the bus voltage involves A/D conversion in continuous scan mode.

The settings necessary to perform bus voltage A/D conversion using different A/D conversion triggers than in shunt current detection are described below.

Note that since the priority of bus voltage A/D conversion is lower than that for shunt current detection, etc., and since the A/D conversion trigger settings used differ from those for shunt current detection, group scan mode is selected as the scan mode, the shunt current analog input is assigned to group A, group A priority control is enabled, and the bus voltage is assigned to group B.

For shunt current detection settings, refer to 2.3.1, Single-Shunt Current Detection, and 2.3.2, Three-Shunt Current Detection.

1. Set the scan mode select (ADCS[1:0]) bits in the A/D control register (ADCSR) to 01b (group scan mode).
2. In A/D channel select register B0 (ADANSB0) or A/D channel select register B1 (ADANSB1), select the analog input channels on which A/D conversion will be performed for group B.
3. Set the A/D conversion start trigger select for group B (TRSB[5:0]) bits in the A/D conversion start trigger select register (ADSTRGR) to 111111b (trigger source deselection state).
4. Set the group A priority control setting (PGS) bit in the A/D group scan priority control register (ADGSPCR) to 1 (operation with group A priority control).
5. Set the group B restart setting (GBRSCN) bit in the A/D group scan priority control register (ADGSPCR) to 1 (scanning for group B is restarted after having been discontinued due to group A priority control).
6. Set the group B single scan continuous start setting (GBRP) bit in the A/D group scan priority control register (ADGSPCR) to 1 (single scan for the group B is continuously activated).

2.3.4 Channel-Dedicated Sample-and-Hold Function

The channel-dedicated sample-and-hold function is used to perform A/D conversion of analog input on all selected channels once only after sample-and-hold takes place.

This allows simultaneous sampling of multiple channels, for example for three-shunt current detection.

On the RX23T the channel-dedicated sample-and-hold function can be used on analog input channels AN000 to AN002.

The channel-dedicated sample-and-hold settings are described below.

1. Set the channel-dedicated sample-and-hold circuit bypass select (SHANS[2:0]) bits in the sample-and-hold circuit control register (ADSHCR) to enable use of the channel-dedicated sample-and-hold circuit for the channels on which the function is to be enabled.
2. Set the channel-dedicated sample-and-hold circuit sampling time setting (SSTSH[7:0]) bits in the sample-and-hold circuit control register (ADSHCR) to specify the sampling time.

2.3.5 Group A Priority Control

During basic operation in group scan mode, all other trigger inputs are ignored during scan operation on group A or group B. When group A priority control is enabled, in contrast, if a trigger input for group A is received during A/D conversion operation on group B, A/D conversion on group B halts so that A/D conversion on group A can proceed.

The settings for enabling group A priority control are described below.

1. Set the scan mode select (ADCS[1:0]) bits in the A/D control register (ADCSR) to 01b (group scan mode).
2. In A/D channel select register A0 (ADANSA0) or A/D channel select register A1 (ADANSA1), select the analog input channels on which A/D conversion will be performed for group A.
3. In A/D channel select register B0 (ADANSB0) or A/D channel select register B1 (ADANSB1), select the analog input channels on which A/D conversion will be performed for group B.
4. Set the A/D conversion start trigger select for group A (TRSA[5:0]) bits in the A/D conversion start trigger select register (ADSTRGR) to specify the group A A/D conversion start trigger.
5. Set the A/D conversion start trigger select for group B (TRSB[5:0]) bits in the A/D conversion start trigger select register (ADSTRGR) to specify the group B A/D conversion start trigger.
6. Set the group A priority control setting (PGS) bit in the A/D group scan priority control register (ADGSPCR) to 1 (operation with group A priority control).

2.3.6 A/D Conversion Status Output (ADST Bit Status Output)

On the RX23T the ADST bit status output pins can be used to check the A/D conversion status.

To enable ADST bit status output (pin P02/ADST0 or PD6/ADST0), set the pin function select bits in the pin function select register of the multi-function pin controller (MPC), and set the pin mode control bit in the port mode register (PMR) of the I/O port to 1 (use pin as I/O port for peripheral functions).

2.4 Timer (MTU)

2.4.1 Complementary PWM

In complementary PWM mode it is possible to specify dead time for output PWM waveforms. The dead time is the period during which the upper and lower arm transistors are set to the inactive level in order to prevent short-circuiting of the arms. Three sets of (positive-phase and negative-phase) PWM waveforms, or six phases in total, can be output with dead time by combining MTU3 and MTU4. PWM waveforms without dead time can also be output.

In complementary PWM mode, pins MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, and MTIOC4D function as PWM output pins, and the MTIOC3A pin can be set to toggle output synchronized with the PWM cycle.

MTU3.TCNT and MTU4.TCNT function as up/down-counters.

To enable complementary PWM mode on the RX23T, as on the RX210, RX62T and RX63T, in the timer mode register of MTU3 set the mode select (MD[3:0]) bits to a value of 1101b to 1111b, the buffer operation A (BFA) bit to 1 (TGRA and TGRC registers used together for buffer operation), and the buffer operation B (BFB) bit to 1 (TGRB and TGRD registers used together for buffer operation).

Also, the timer mode register names differ: the MTU3 timer mode register (TMDR) on the RX210 corresponds to MTU3 timer mode register 1 (TMDR1) on the RX23T, RX62T, and RX63T.

Note that the MTU6 and MTU7 of the RX62T and RX63T are not present on the RX23T.

To produce left-right asymmetric PWM output in complementary PWM mode on the RX23T, it is necessary to set the double buffer select (DRS) bit in timer mode register 2 (TMDR2A) to 1 (double buffer function enabled) and to specify different values for buffer register B (MTU3.TGRE, MTU4.TGRE, and MTU4.TGRF) and buffer register A (MTU3.TGRD, MTU4.TGRC, and MTU4.TGRD).

Note that settings should be made for buffer register A (MTU3.TGRD, MTU4.TGRC, and MTU4.TGRD) and for buffer register B (MTU3.TGRE, MTU4.TGRE, and MTU4.TGRF) at the same time.

When transferring buffer register data, write to MTU4.TGRD last.

For details of setting values, refer to section 20, Multi-Function Timer Pulse Unit (MTU3c), in RX23T Group User's Manual: Hardware.

2.4.2 Timer A/D Conversion Start Request

In complementary PWM mode on the RX23T, as on the RX210, RX62T, and RX63T, MTU3.TGRA compare match (peak), MTU4.TCNT underflow (trough), or compare match on channels other than MTU3 and MTU4 can be used as the A/D conversion start request.

To perform A/D conversion at two user-defined locations, during the timer counter peak to trough or trough to peak interval, make one of the following combinations of settings to bits DT4BE, UT4BE, DT4AE, and UT4AE in the MTU4 timer A/D conversion start request control register (TADCR).

	DT4BE Down-Count TRG4BN Enable Bit	UT4BE Up-Count TRG4BN Enable Bit	DT4AE Down-Count TRG4AN Enable Bit	UT4AE Up-Count TRG4AN Enable Bit
Combination 1	Enabled (1)	Disabled (0)	Enabled (1)	Disabled (0)
Combination 2	Enabled (1)	Disabled (0)	Disabled (0)	Enabled (1)
Combination 3	Disabled (0)	Enabled (1)	Enabled (1)	Disabled (0)
Combination 4	Disabled (0)	Enabled (1)	Disabled (0)	Enabled (1)

It is also necessary to specify the A/D conversion start trigger by making the settings specified in step 3, and to specify the A/D conversion start request cycle by making the settings specified in step 5, of 2.3.1, Single-Shunt Current Detection.

The settings for performing A/D conversion at either the peak or trough of the timer counter are described below.

Performing A/D Conversion at the Peak of the Timer Counter

Set the A/D conversion start trigger select (TRSA[5:0]) bits in the A/D conversion start trigger select register (ADSTRGR) to 000100b (MTU3.TGRA compare match/input capture (peak)) to specify the A/D conversion start trigger, and set the A/D converter start request enable (TTGE) bit in the MTU3 timer interrupt enable register (TIER) to 1 (A/D conversion start request generation enabled).

Performing A/D Conversion at the Trough of the Timer Counter

Set the A/D conversion start trigger select (TRSA[5:0]) bits in the A/D conversion start trigger select register (ADSTRGR) to 000101b (MTU4.TGRA compare match/input capture, or MTU4.TCNT underflow (trough) in complementary PWM mode) to specify the A/D conversion start trigger, and set the A/D converter start request enable 2 (TTGE2) bit in the MTU4 timer interrupt enable register (TIER) to 1 (A/D conversion request at MTU4.TCNT underflow (trough) enabled).

2.4.3 A/D Conversion Start Request Frame Synchronization Signal Output

The RX23T can output an A/D conversion start request frame synchronization signal.

The A/D conversion start request frame synchronization signal enables external pins to be used to monitor the A/D conversion start request signal generation timing. Make the following settings to enable A/D conversion start request frame synchronization signal output (on pin PB2/ADSM0).

1. Set the appropriate pin function select bit in the pin function select register of the multi-function pin controller (MPC).

2. Set the pin mode control bit in the port mode register (PMR) of the I/O port to 1 (peripheral function).

3. Set the A/D conversion start request select for ADSM0 pin output frame synchronization signal generation (TADSTRS0[4:0]) bits in A/D conversion start request select register 0 (TADSTRGR0) of the multi-function timer pulse unit (MTU) to specify the A/D conversion start request to be used to generate output of the frame synchronization signal on the ADSM0 pin.

For details of setting values, refer to section 20, Multi-Function Timer Pulse Unit (MTU3c), in RX23T Group User's Manual: Hardware.

2.5 Protection Functions

2.5.1 POE

The port output enable (POE) function can be used to place output pins of the MTU in the high-impedance state under various conditions.

The conditions under which MTU output pins can be placed in the high-impedance state using the port output enable (POE) function on the RX23T are summarized below.

Condition
Change of input pin state. Input received on POE0#, POE8#, or POE10# pin.
Shorting of output pins. • Output signal level (active level) matched for one cycle or more on MTU complementary PWM output pins MTIOC3B and MTIOC3D (indicating a short). • Output signal level (active level) matched for one cycle or more on MTU complementary PWM output pins MTIOC4A and MTIOC4C (indicating a short). • Output signal level (active level) matched for one cycle or more on MTU complementary PWM output pins MTIOC4B and MTIOC4D (indicating a short).
Bit in software port output enable register (SPOER) set to 1 (place pins in high-impedance state).
Clock generation circuit oscillation stop detected.
Comparator detection by comparator (CMPC).

On the RX210 it was possible to put MTU output pins in the high-impedance state from the event link controller (ELC), but the event link controller (ELC) is not present on the RX23T.

POE1# and POE3# are present on the RX210 but not on the RX23T. When migrating software that uses POE1# or POE3# to put MTU3 or MTU4 pins in the high-impedance state, it is necessary to make changes to use POE0# on the RX23T.

When migrating software that uses the comparator output detection function of the comparator on the RX210, be aware that the high-impedance state control functionality for MTU output pins has been extended on the RX23T.

When migrating from the RX62T, the POE function on the RX23T can be used in the same manner.

POE11#, present on the RX63T, is not present on the RX23T. When migrating software that uses POE11# to put MTU3, MTU4, or MTU0 pins in the high-impedance state, it is necessary to make changes to use POE0# or POE8# on the RX23T.

To enable high-impedance control by comparing the output level of MTU3 pins (MTIOC3B/MTIOC3D) or MTU4 pins (MTIOC4A and MTIOC4C or MTIOC4B and MTIOC4D) in complementary PWM mode on the RX23T, set the pin output active level in active level register 1 (ALR1) and enable high-impedance control for MTU3 or MTU4 pins in port output enable control register 2 (POECR2).

Among the registers used by the POE function, the following can be written to only once after a reset.

It is necessary to use byte or word access when making settings.

- Input level control/status registers 1, 3, 4, and 6 (ICSR1, ICSR3, ICSR4, and ICSR6)
- Output level control/status register 1 (OCSR1)
- Active level register 1 (ALR1)
- Port output enable control registers 1, 2, 4, and 5 (POECR1, POECR2, POECR4, and POECR5)
- Port output enable comparator request select register (POECMPSEL)

For details of POE register settings, refer to section 21, Port Output Enable 3 (POE3b), in RX23T Group User's Manual: Hardware.

2.5.2 LVD

The voltage detection circuit (LVD) monitors the voltage input on the VCC pin. The VCC input voltage can be monitored using a software program.

It is possible to generate an internal reset or interrupt when a specified detection voltage value is detected.

The voltage detection circuit of the RX23T supports three LVD functions: voltage monitoring 0, voltage monitoring 1, and voltage monitoring 2.

The specifications of the voltage detection circuit of the RX23T are listed below.

Item		Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2
	Detection target	Voltage drops past Vdet0.	When voltage rises above or drops below Vdet1.	When voltage rises above or drops below Vdet2.
	Detection voltage	Voltage selectable from 2 levels using OFS1 register.	Voltage selectable from 9 levels using LVDLVLR.LVD1LVL[3:0] bits.	Voltage selectable from 4 levels using LVDLVLR.LVD2LVL[1:0] bits.
	Monitor flag	None	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1.	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2.
			LVD1SR.LVD1DET flag: Vdet1 passage detection.	LVD2SR.LVD2DET flag: Vdet2 passage detection.
Processing when voltage detected	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC: CPU restart after specified duration when VCC > Vdet0.	Reset when Vdet1 > VCC: CPU restart after specified duration when VCC > Vdet1 or Vdet1 > VCC (selectable).	Reset when Vdet2 > VCC: CPU restart after specified duration when VCC > Vdet2 or Vdet2 > VCC (selectable).
	Interrupts	None	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Selectable between non-maskable or maskable interrupt.	Selectable between non-maskable or maskable interrupt.
			Interrupt request issued both when Vdet1 > VCC and when VCC > Vdet1, or when Vdet1 > VCC or VCC > Vdet1.	Interrupt request issued both when Vdet2 > VCC and when VCC > Vdet2, or when Vdet2 > VCC or VCC > Vdet2.

On the RX210 it was possible to switch the voltage monitoring 2 voltage detection voltage level among several voltage detection target voltages, VCC , and the comparator A2 (CMPA2) pin input voltage, but such switching is not supported on the RX23T.

When migrating software from the RX62T, be aware that on the RX23T adds a new monitoring function (voltage monitoring 0) to the two supported on the RX62T (voltage monitoring 1 and voltage monitoring 2). On the RX23T monitoring by the voltage monitoring 1 and voltage monitoring 2 functions can be checked using the voltage monitoring 1 circuit status register (LVD1SR) and voltage monitoring 2 circuit control register 1 (LVD2CR1), respectively.

When migrating software that uses the voltage detection circuit (LVD) of the RX210, RX62T or RX63T, it is necessary to change the detection voltage level settings on the RX23T.

On the RX23T the voltage monitoring 0 detection voltage level can be set in option function select register 1 (OFS1). The voltage detection 1 and voltage detection 2 detection voltage levels can be set in the voltage detection level select register (LVDLVLR).

For details of the voltage detection circuit (LVD), refer to section 7, Option-Setting Memory, and section 8, Voltage Detection Circuit (LVDAb), in RX23T Group User's Manual: Hardware.

The detection voltage level settings supported by the three microcontrollers are listed below.

Detection Voltage Level	RX210	RX62T	RX63T	RX23T
Voltage monitoring 0 detection voltage level	Selectable from 4 levels	Function not implemented.	Fixed at 1 level	Selectable from 2 levels
Voltage monitoring 1 detection voltage level	Selectable from 16 levels	Fixed at 1 level	Fixed at 1 level	Selectable from 9 levels
Voltage monitoring 2 detection voltage level	Selectable from 16 levels. Fixed at 1 level for CMPA2 pin.	Fixed at 1 level	Fixed at 1 level	Selectable from 4 levels

2.5.3 Comparator Reference Voltage

On the RX23T comparator C (CMPC) compares the reference input voltage and analog input voltage. The reference input voltage and analog input voltage comparison result can be read by software or output to an external pin. It is also possible to generate an interrupt request when the comparison result changes.

The comparator C reference input voltage of the RX23T is selectable from the inputs to pins CVREFC0 and CVREFC1, and the output of the on-chip D/A converter.

To switch the reference input voltage on the RX23T, set the CVRS[1:0] (reference input voltage select) bits in the comparator reference voltage select register (CMPSEL1).

Note that when the CVRS[1:0] (reference input voltage select) bits in the comparator reference voltage select register (CMPSEL1) are set to 10b (on-chip D/A converter output voltage selected as reference input voltage), it is also necessary to make settings to the D/A converter for generating comparator C reference voltage (DA).

The D/A converter for generating comparator C reference voltage (DA) outputs an 8-bit conversion result based on the AVCC0 pin input voltage and the value of D/A data register 0 (DADR0), using the following formula.

Formula: (DADR0 register value ÷ 256) × AVCC0

D/A conversion starts when the D/A output enable 0 (DAOE0) bit in the D/A control register (DACR) of the D/A converter for generating comparator C reference voltage (DA) is set to 1 (D/A conversion enabled).

For details, refer to section 30, D/A Converter for Generating Comparator C Reference Voltage (DA), and section 31, Comparator C (CMPC), in RX23T Group User's Manual: Hardware.

3. Points of Difference

3.1 Comparison of Functions

A comparative listing of the functions of the RX210, RX62T, RX63T, and RX23T is presented below.

Type	Module/Function	Item	Description	RX210 [64-Pin Version]	RX62T [64-Pin Version]	RX63T [64-Pin Version]	RX23T [64-Pin Version]
Clocks	Clock generation circuit	Oscillator	Main clock oscillator	1 MHz to 20 MHz	8 MHz to 12.5 MHz	4 MHz to 16 MHz	1 MHz to 20 MHz
			Subclock oscillator	32.768 KHz	—	—	—
			High-speed on-chip oscillator (HOCO)	32 MHz/ 36.864 MHz/ 40 MHz/ 50 MHz	—	—	32 MHz
			Low-speed on-chip oscillator (LOCO)	125 KHz	—	125 KHz	4 MHz
			PLL frequency synthesizer	○	○	○	○
			IWDT-dedicated on-chip oscillator	125 KHz	125 KHz	125 KHz	15 KHz
		Settings	System clock (ICLK)	○	○	○	○
			Peripheral module clock (PCLK)	—	○	—	—
			Peripheral module clock (PCLKA)	—	—	○	○
			Peripheral module clock (PCLKB)	○	—	○	○
			AD clock (PCLKC)	—	—	○	—
			S12AD clock (PCLKD)	○		○	○
			FlashIF clock (FCLK)	○	—	○	○
			External bus clock (BCLK)	—	—	—	—
		Operating frequency	System clock (ICLK)	50 MHz max.	100 MHz max.	100 MHz max.	40 MHz max.
			Peripheral module clock (PCLK)	—	50 MHz max.	—	—
			Peripheral module clock (PCLKA)	—	—	100 MHz max.	40 MHz max.
			Peripheral module clock (PCLKB)	32 MHz max.	—	50 MHz max.	40 MHz max.
			AD clock (PCLKC)	—		100 MHz max.	—
			S12AD clock (PCLKD)	50 MHz max.		50 MHz max.	40 MHz max.
			FlashIF clock (FCLK)	32 MHz max.	—	50 MHz max.	32 MHz max.
			External bus clock (BCLK)	—	—	—	—
	ROM	ROM access wait	ROM access wait setting	—	—	—	○

Type	Module/Function	Item	Description	RX210 [64-Pin Version]	RX62T [64-Pin Version]	RX63T [64-Pin Version]	RX23T [64-Pin Version]
Interrupts	Interrupt controller (ICU)	Symbol		ICUb	ICU	ICUb	ICUb
		Interrupt sources	External interrupt sources (IRQ pins)	7	4	6	6
			Software interrupt sources	1	1	1	1
			Non-maskable interrupt sources (NMI pins)	6	3	6	5
		Non-maskable interrupts	NMI pin interrupt	○	○	○	○
			Oscillation stop detection interrupt	○	○	○	○
			Voltage monitoring interrupt	—	○	—	—
			Voltage monitoring 1 interrupt	○	—	○	○
			Voltage monitoring 2 interrupt	○	—	○	○
			WDT underflow/ refresh error	○	—	○	—
			IWDT underflow/ refresh error	○	—	○	○
		Priority setting	Support for 16 interrupt priority levels	○	○	○	○
I/O ports	General I/O ports	Ports	Input/output	48	37	39	50
			Input	1	9	9	1
			Open-drain output	35	2	10	42
			Large-current output	—	6	—	8
			5 V tolerant	2	—	39	2
			Pull-up resistors	48	—	—	50
Multi-function pin controller	Multi-function pin controller (MPC)	I/O functions	Support for selecting from multiple pins for I/O functions	○	—	○	○

Type	Module/Function	Item	Description	RX210 [64-Pin Version]	RX62T [64-Pin Version]	RX63T [64-Pin Version]	RX23T [64-Pin Version]
Timer	Multi-function timer pulse unit (MTU)	Symbol		MTU2a	MTU3	MTU3	MTU3c
		Channels	16 bits/channel	6 channels	8 channels	8 channels	6 channels
		Pulse I/O	Pulse I/O channels (max. supported pulse I/O channels)	16	24	16	16
			Pulse input channels (max. supported pulse input channels)	3	3	3	3
		Division ratio	Clock pin	PCLK	ICLK	PCLKA	PCLKA
			Divide-by-1	○	○	○	○
			Divide-by-2	—	—	—	○
			Divide-by-4	○	○	○	○
			Divide-by-8	—	—	—	○
			Divide-by-16	○	○	○	○
			Divide-by-32	—	—	—	○
			Divide-by-64	○	○	○	○
			Divide-by-256	○	○	○	○
			Divide-by-1024	○	○	○	○
		External clock input	MTCLKA	○	○	○	○
			MTCLKB	○	○	○	○
			MTCLKC	○	○	○	○
			MTCLKD	○	○	○	○
			MTIOC1A	—	—	—	○
		Input capture function	Transfer of TCNT value to TGR at input edge detection	○	○	○	○
		Output compare function	0 output, 1 output, toggle output	○	○	○	○
		Synchronous operation	Simultaneous overwriting of multiple TCNT values (synchronous preset)	○	○	○	○
		Buffer operation	Use of TGRC and TGRD registers as buffer registers	○	○	○	○
		Cascade connection operation	Connection of 16-bit counters from different channels to function as a 32-bit counter	○	○	○	○
		PWM mode	Output of PWM waveforms from output pins	○	○	○	○

Type	Module/Function	Item	Description	RX210 [64-Pin Version]	RX62T [64-Pin Version]	RX63T [64-Pin Version]	RX23T [64-Pin Version]
Timer	Multi-function timer pulse unit (MTU)	Phase counting mode	16-bit mode	○	○	○	○
			32-bit mode	○	○	○	○
		Reset-synchronized PWM mode	PWM waveforms (positive-phase and negative-phase) that share a common wave transition point	○	○	○	○
		Complementary PWM output mode	Output of non-overlapping waveforms for 3-phase inverter control	○	○	○	○
			Automatic dead time setting	○	○	○	○
			Support for setting PWM duty ratio to any value from 0 to 100%	○	○	○	○
			A/D conversion request delaying function	○	○	○	○
			Peak/trough interrupt skipping function	○	○	○	○
			Double buffer function	—	○	○	○
		External pulse width measurement	External pulse width measurement	○	○	○	○
		Dead time compensation counter	Measurement of delay in output waveforms and application to duty ratio	○	○	○	○
		Trigger generation	A/D converter conversion start trigger generation	○	○	○	○
			A/D conversion start skipping function	○	○	○	○
		A/D conversion start timing measurement	A/D conversion start request frame synchronization signal	—	—	—	○
		Interrupt sources	Interrupt sources	28	38	38	28

Type	Module/Function	Item	Description	RX210 [64-Pin Version]	RX62T [64-Pin Version]	RX63T [64-Pin Version]	RX23T [64-Pin Version]
Timer	Port output enable (POE)	Symbol		POE2a	POE3	POE3	POE3b
		High-impedance control	High-impedance control of MTU waveforms output pins	○	○	○	○
			High-impedance control of GPT waveforms output pins	—	○	○	—
		Activation sources	Activation by POE0 input pin	○	○	○	○
			Activation by POE1 input pin	○	—	—	—
			Activation by POE2 input pin	○	—	—	—
			Activation by POE3 input pin	○	—	—	—
			Activation by POE4 input pin	—	—	○	—
			Activation by POE8 input pin	○	○	○	○
			Activation by POE10 input pin	—	—	○	○
			Activation by POE11 input pin	—	○	○	—
			Activation by POE12 input pin	—	—	○	—
			Activation at detection of clock generation circuit oscillation stop	○	○	○	○
			Activation by comparison of output level of MTU complementary PWM output pins	○	○	○	○
			Activation at detection of output short (GPT large-current pins)	—	○	—	—
			Activation at detection of output short (GPT output pins)	—	—	○	—
			Activation by event signal of event link controller (ELC)	○	—	—	—
			Activation at comparator detection	○	○	○	○
			Activation by software (register)	○	○	○	○

Type	Module/Function	Item	Description	RX210 [64-Pin Version]	RX62T [64-Pin Version]	RX63T [64-Pin Version]	RX23T [64-Pin Version]
Timer	General PWM timer (GPT)	Symbol		—	GPT	GPT	—
		Channels	16 bits/channel	—	4 channels	4 channels	—
		I/O	Input pins	—	1	1	—
			I/O pins	—	6	8	—
		Division ratio	Clock pin	—	ICLK	PCLKA	—
			Divide-by-1	—	○	○	—
			Divide-by-2	—	○	○	—
			Divide-by-4	—	○	○	—
			Divide-by-8	—	○	○	—
		External clock input		—	○	○	—
		Count operation	Up-count or down-count (saw-wave)	—	○	○	—
			Up/down-count (triangle-wave)	—	○	○	—
		Output compare/ input capture registers	Output compare registers that also function as input capture registers	—	○	○	—
		Compare/ buffer registers	Support for setting compare match registers as buffer registers	—	○	○	—
		Cycle set registers/ buffer registers	Support for setting cycle set registers as buffer registers	—	○	○	—
		Input capture function	Transfer of count values to GTCCRA or GTCCRB at input edge detection	—	○	○	—
		Synchronous operation	Support for simultaneous count clear or start on multiple channels	—	○	○	—
		Phase shift start	Support for setting count value of channels before count operation start and starting count operation with phase differential	—	○	○	—

Type	Module/Function	Item	Description	RX210 [64-Pin Version]	RX62T [64-Pin Version]	RX63T [64-Pin Version]	RX23T [64-Pin Version]
Timer	General PWM timer (GPT)	Automatic dead time setting function	Automatic setting of compare match value for negative-phase waveforms with dead time based on compare match value and dead time value for positive-phase waveforms	—	○	○	—
		PWM mode	Output of PWM waveforms on output pins	—	○	○	—
		Buffer operation	Support for compare match using buffer registers	—	○	○	—
		One-shot operation	Support for with fixed buffer operation	—	○	○	—
		Trigger generation	A/D conversion start trigger	—	○	○	—
		PWM delay generation function	Support for controlling PWM output rise/fall timing at resolution of 1/32 of PCLKA	—	—	—	—
	8-bit timer (TMR)	Symbol		TMR	—	—	TMR
		Channels	8 bits/channel	2 channels × 2 units	—	—	2 channels × 2 units
		Division ratio	Clock pin	PCLK	—	—	PCLK
			Divide-by-1	○	—	—	○
			Divide-by-2	○	—	—	○
			Divide-by-8	○	—	—	○
			Divide-by-32	○	—	—	○
			Divide-by-64	○	—	—	○
			Divide-by-1024	○	—	—	○
			Divide-by-8192	○	—	—	○
		Output	Support for pulse output or PWM output with user-specified duty ratio	○	—	—	○
		Cascade connection operation	Support for use as 16-bit timer using cascade connection of 2 channels	○	—	—	○
		A/D conversion trigger	Support for generation of A/D converter conversion start trigger	—	—	—	○
		SCI baud rate clock generation	SCI5	○	—	—	○
			SCI6	○	—	—	—
			SCI12	○	—	—	—
		Event link function	Output	○	—	—	—
			Input	○	—	—	—

Type	Module/Function	Item	Description	RX210 [64-Pin Version]	RX62T [64-Pin Version]	RX63T [64-Pin Version]	RX23T [64-Pin Version]
Timer	Compare match timer (CMT)	Symbol		CMT	CMT	CMT	CMT
		Units	(16-bit × 2 channels) × number of units	2	2	2	2
		Count clock	Input count clock	PCLK	PCLK	PCLK	PCLK
			Divide-by-8	○	○	○	○
			Divide-by-32	○	○	○	○
			Divide-by-128	○	○	○	○
			Divide-by-512	○	○	○	○
		Event link function	Output	○	—	—	—
			Input	○	—	—	—
A/D converters	12-bit A/D converter (S12AD)	Symbol		S12ADb	S12ADA	S12ADB	S12ADE
		Channels × units	Channels	16 channels × 1 unit	4 channels × 2 units	8 channels × 1 unit	10 channels × 1 unit
		Resolution	Bit width	12-bit	12-bit	12-bit	12-bit
		Conversion time per channel	When A/D conversion clock When ADCLK = 50 MHz and AVCC0 = 4.0 V to 5.5 V	1.0 µs	1.0 µs	1.0 µs	—
			When ADCLK = 40 MHz	—	—	—	1.0 µs
			When A/D conversion clock ADCLK = 25 MHz and AVCC0 = 3.0 V to 3.6 V	—	2.0 µs	2.0 µs	—
		Division ratio	A/D conversion clock	ADCLK	PCLK	ADCLK	ADCLK
			Divide-by-1	ADCLK is set by the clock generation circuit (CPG).	○	ADCLK is set by the clock generation circuit (CPG).	ADCLK is set by the clock generation circuit (CPG).
			Divide-by-2		○		
			Divide-by-4		○		
			Divide-by-8		○		
		Operating modes	Single mode	—	○	—	—
			Single-cycle scan mode	○	○	○	○
			Continuous scan mode	○	○	○	○
			Group scan mode	○	○	○	○
			Group A priority control (group scan mode only)	—	—	○	○
			Group A priority control groups	—	—	2	2

Type	Module/Function	Item	Description	RX210 [64-Pin Version]	RX62T [64-Pin Version]	RX63T [64-Pin Version]	RX23T [64-Pin Version]
A/D converters	12-bit A/D converter (S12AD)	A/D conversion start method	Triggering by temperature sensor	○	—	—	—
			Triggering by event link controller (ELC)	○	—	—	—
		A/D conversion accuracy	Support for specifying A/D data register bit accuracy (storage at 12-bit, 10-bit, or 8-bit accuracy)	— (12-bit fixed)	○	○	— (12-bit fixed)
			Support for A/D data register format selection (flush-right or flush-left)	○	○	○	○
			A/D-converted value addition function	○	—	○	○
		Self-diagnostic functions	Internal self-diagnostics using analog input voltage (VREFL0)	○	○	○	○
			Internal self-diagnostics using analog input voltage (VREFH0 × 1/2)	○	○	○	○
			Internal self-diagnostics using analog input voltage (VREFH0 × 1)	○	○	○	○
		Programmable gain amplifiers		1 channel (for temperature sensor)	3 channels × 2 units	—	—
		Input signal amplification function using programmable gain amplifier	Gain: 2.0×	—	○	—	—
			Gain: 2.5×	—	○	—	—
			Gain: 3.077×	—	○	—	—
			Gain: 3.636×	—	○	—	—
			Gain: 4.0×	—	○	—	—
			Gain: 4.444×	—	○	—	—
			Gain: 5.0×	—	○	—	—
			Gain: 5.714×	—	○	—	—
			Gain: 6.667×	—	○	—	—
			Gain: 10.0×	—	○	—	—
			Gain: 13.333×	—	○	—	—

Type	Module/Function	Item	Description	RX210 [64-Pin Version]	RX62T [64-Pin Version]	RX63T [64-Pin Version]	RX23T [64-Pin Version]
Comparator	Comparator	Symbol		CMPA/ CMPB	—	—	CMPC
		Comparators		2 channels × 2 units	3 channels × 2 units	3 channels × 1 unit	3 channels
		Function settings	Low-level comparator	—	○	○	—
			High-level comparator	—	○	○	—
			Window comparator	○	○	○	○
		Response speed	REFH response time (tCR)	—	1 µs	500 ns	—
			REFL response time (tCF)	—	1 µs	500 ns	—
			[Comparator A] Comparator output delay time Falling edge VI = LVREF − 110 mV	3 µs	—	—	—
			[Comparator A] Comparator output delay time Falling edge VI < LVREF − 1 V	2µs	—	—	—
			[Comparator A] Comparator output delay time Rising edge VI = LVREF + 160 mV	3 µs	—	—	—
			[Comparator A] Comparator output delay time Rising edge VI > LVREF + 1 V	1.5 µs	—	—	—
			[Comparator B] Comparator output delay time VI = VREF + 100 mV	1 µs	—	—	—
			[CMPC] VOD = 100 mV t CMPCTL.CDFS = 0 tcr	—	—	—	200 ns
			[CMPC] VOD = 100 mV t CMPCTL.CDFS = 0 tcf	—	—	—	200 ns

4. Sample Code

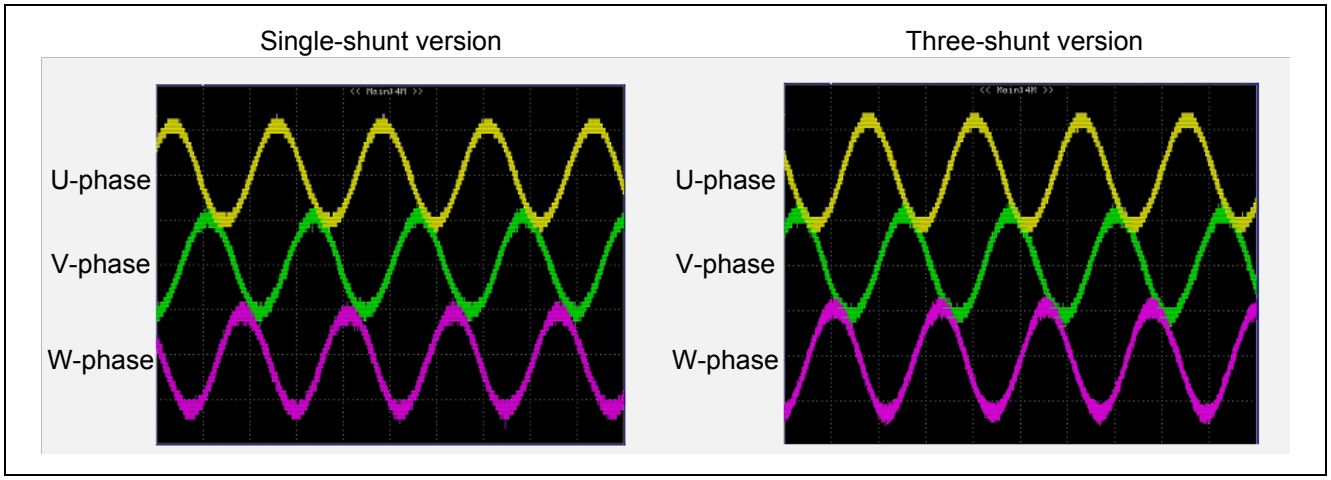
4.1 Summary

The sample code is provided to illustrate, when creating a program that uses the RX23T to control two motors, how to generate left-right symmetric (three-shunt version) and left-right asymmetric (single-shunt version) PWM output using complementary PWM mode 3 of the MTU; how to make settings for A/D conversion using the group scan function, with different timings for group A and group B; and how to make settings for the protection functions.

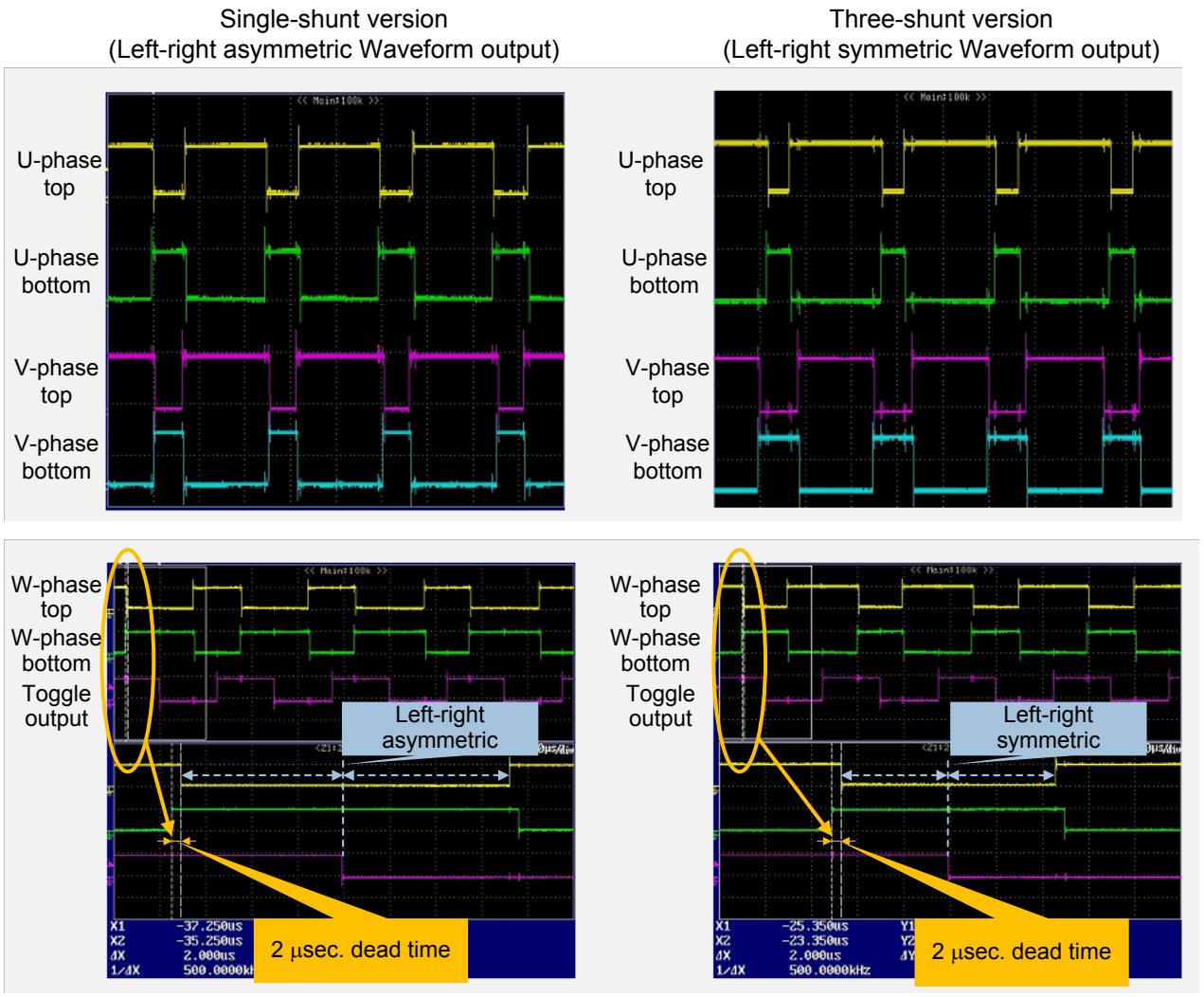
Note that the settings used in the sample code are such that the data results in sine waves when each PWM output phase undergoes CR filtering. The output waveforms are shown below.

The sample code is intended only for reference, and Renesas makes no guarantee regarding its operation. When making use of the sample code, make sure to perform sufficient testing in a suitable environment.

< Sine Wave After CR Filtering >



< PWM Output Waveforms >



Note: Toggle output: Toggles waveform output in synchronization with the PWM cycle.

4.2 Development and Operation Confirmation Environment

The development and operation confirmation environment of the sample code is summarized below.

< CS+ >

tem	Description
MCU used	R5F523T5ADFM (Package: PLQP0064KB-A)
Operating voltage	5 V
Integrated development environment	Renesas Electronics Corporation CS+ for CC V4.01.00 [05 Sep 2016]
C compiler	Renesas Electronics Corporation CC - RX V2.05.0
	Compiler options: -isa=rxv2 –fpu -lang=c99 -include=Include -output=obj -debug -optimize=max –speed -nologo -Xcref=%BuildModeName%
iodefine.h version	Version 1.1 (2015-07-13)
Board used	Renesas Starter Kit for RX23T (Product No.: RTK500523TC00000BR)

< e^2 studio >

Item	Description
MCU used	R5F523T5ADFM (Package: PLQP0064KB-A)
Operating voltage	5 V
Integrated development environment	Renesas Electronics Corporation e^2studio Version: 5.2.0.020
C compiler	Renesas Electronics Corporation CC - RX V2.05.0
	Compiler options: -isa=rxv2 –fpu -include="C:\PROGRA~1\Renesas\RX\2_5_0/include" -debug -optimize=max -speed -nologo -define=__RX -nomessage -alias=noansi
iodefine.h version	Version 1.1 (2015-07-13)
Board used	Renesas Starter Kit for RX23T (Product No.: RTK500523TC00000BR)
Remarks	Sample code created with reference to Software Migration Guide: CS+ to e^2 studio Migration.

4.3 Peripheral Functions

The peripheral function used in the sample code and their applications are listed below.

Peripheral Function	Application
Ports	• Test port output (for processing timing measurement) • SW1 input (PWM output start switch) • SW2 input (PWM output stop switch) • ADST bit (A/D conversion start bit) status output • A/D conversion start request frame synchronization signal (ADSM0) output
Multi-function timer pulse unit 3 (MTU3c)	• Toggle waveform output synchronized with the PWM cycle • Complementary PWM output (single-shunt version: left-right asymmetric, three-shunt version: left-right symmetric)
12-bit A/D converter (S12ADE)	For A/D value acquisition (acquisition of shunt current, bus voltage, and other A/D values)
D/A converter for generating comparator C reference voltage (DA)	Generates reference input voltage for comparator C (CMPC).
Comparator C (CMPC)	Outputs comparator detection result when overvoltage is detected.
Port output enable 3 (POE3b)	Puts PWM output pins in high-impedance state when overcurrent or overvoltage is detected.
Voltage detection circuit (LVDAb)	Applies a reset when a voltage drop is detected.

(1) Ports

1. Test port output (for processing timing measurement)
   Outputs high at start, and low at finish, of MTU3 peak interrupt processing.
2. SW1 input (PWM output start switch) and SW2 input (PWM output stop switch)
   Starts and stops PWM output in response to SW1 and SW2 input, respectively.
3. ADST bit (A/D conversion start bit) status output
   Used to check the A/D conversion status.
4. A/D conversion start request frame synchronization signals (ADSM0)
   Used to check the timing of A/D conversion start request signal generation.

(2) Multi-function timer pulse unit 3 (MTU3c)

Toggles waveform output in synchronization with the PWM cycle (MTIOC3A).
Uses complementary PWM mode 3 to generate six-phase PWM output with triangle-wave modulation and dead time (MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4C, MTIOC4B, and MTIOC4D).
The sample code generates PWM output with a 125 µsec. cycle, low-active, and 2 µsec. dead time.
In the single-shunt version of the sample code, the double buffer function is enabled and different values are set for buffer A and buffer B, resulting in left-right asymmetric PWM output.
In the three-shunt version of the sample code, the double buffer function is disabled, resulting in left-right symmetric PWM output.

(3) 12-bit A/D converter (S12ADE)

The group scan function is used, with the shunt current value assigned to group A and the bus voltage value and other A/D values assigned to group B, and A/D conversion is performed with different timing for each.
In the single-shunt version of the sample code, group A is set to double trigger mode, A/D conversion takes places with two different timings on the selected channel, and the converted values are stored in different registers (redundant registers for A/D data).
In the three-shunt version of the sample code, the channel-dedicated sample-and-hold function is used on group A, and sampling is performed on three channels with the same timing.

(4) D/A converter for generating comparator C reference voltage (DA)

AVCC0 is used as the input, and a value equal to 90% of the input value is output as the comparator reference voltage.

(5) Comparator C (CMPC)

The output from the D/A converter for generating comparator C reference voltage (DA) is used as the input, and when it exceeds the CMPC analog input voltage, the comparator detection result is output and a POE control signal is output.

(6) Port output enable 3 (POE3b)

Overcurrent detection (falling-edge detection on POE0# pin), comparator detection, or output short detection occurs, the pins on which PWM output is in progress are put into the high-impedance state.

(7) Voltage detection circuit (LVDAb)

A reset is generated when the power supply voltage drops to 2.51 V or less. The reset source can be acquired from reset status register 0 (RSTSR0).

4.4 Sample Code Specifications

The basic specifications of the sample code are listed below.

No.	Category	Item	Setting
1	Clock settings	Using HOCO	32 MHz
		PCLKA (max. 40 MHz)	32 MHz
		PCLKB (max. 40 MHz)	32 MHz
		PCLKD (max. 40 MHz)	32 MHz
		ICLK (max. 40 MHz)	32 MHz
		FCLK (max. 32 MHz)	32 MHz
		Memory wait cycles	No wait states
2	Ports	SW1	PWM output start
		SW2	PWM output stop
3	MTU3c	Operation mode	Complementary PWM mode 3 (transfer at peaks and/or troughs)
		Double buffer function	Enabled
		Carrier frequency	8 KHz (cycle: 125 µsec.)
		Dead time	2 µsec.
		PWM active output	Low-active
		PWM output values	Use table that generates left-right asymmetric (1.25 µsec. gap between left and right) output of U-phase, V-phase, and W-phase (shingle-shunt).
		PWM output values	Use table that generates left-right symmetric output of U-phase, V-phase, and W-phase (three-shunt).
		Toggle output synchronized with PWM cycle	Enabled

No.	Category	Item	Setting
4	12-bits A/D converter (S12ADE)	Double trigger mode	Enabled (single-shunt)
		Group scan mode	Enabled
			Group A: AN002 (single-shunt) Group A: AN000, AN001, AN002 (three-shunt)
			Group B: AN003, AN005, AN007
		Group A priority control	Enabled
		A/D conversion triggers	A/D conversion start request (TRG4AN) at MTU4.TCNT down-count A/D conversion start request (TRG4BN) at MTU4.TCNT down-count (single-shunt)
			MTU4.TCNT underflow (trough) (three-shunt)
		Buffer register update timing	MTU4.TADCORA and MTU4.TADCORB updated from cycle set buffer register at peaks
		Channel-dedicated sample-and-hold	Enabled: AN002 (single-shunt) AN000, AN001, AN002 (three-shunt)
		Sampling time	0.4 µsec.
		A/D conversion start request frame synchronous signal output	Compare match of MTU4.TADCORB and MTU4.TCNT Compare match of MTU4.TADCORB and MTU4.TCNT (single-shunt)
			MTU4.TCNT underflow (trough) (three-shunt)
		ADST bit status output	Enabled
5	D/A converter for generating comparator C reference voltage (DA)	DA conversion result	Value equal to 90% of AVCC0 output as comparator reference voltage
6	Comparator (CMPC)	Reference voltage	Input by on-chip D/A converter
		Operation when detected	POE control signal output
			Comparator external pin output enabled
7	Port output enable 3 (POE3b)	Detection condition	POE#0 falling edge detection
			Comparator detection
		Operation when detected	Put MTU ports in high-impedance state
8	Voltage detection circuit (LVDAb)	Detection condition	Voltage drop (2.51 V) detection (using voltage monitoring 0)

4.5 Hardware

4.5.1 Pins Used

The pins used by the sample code are listed below.

Pin Name	Pin	I/O	Description
MTIOC3B	P71	Output	PWM output pin 1
MTIOC3D	P74	Output	PWM output pin 1’ (PWM output 1 negative-phase waveform output)
MTIOC4A	P72	Output	PWM output pin 2
MTIOC4C	P75	Output	PWM output pin 2’ (PWM output 2 negative-phase waveform output)
MTIOC4B	P73	Output	PWM output pin 3
MTIOC4D	P76	Output	PWM output pin 3’ (PWM output 3 negative-phase waveform output)
ADST0	P02	Output	ADST bit status output pin
ADSM0	PB2	Output	A/D conversion start request frame synchronization signal pin
COMP1	P23	Output	Comparator output pin
—	P22	Output	Test port output pin (for processing timing measurement)
AN003	P43	Input	Group B bus voltage detection A/D pin
AN005	P43	Input	Group B A/D pin 1
AN007	P47	Input	Group B A/D pin 2
AN000	P40	Input	Shunt current detection A/D pin (three-shunt)
AN001	P41	Input	Shunt current detection A/D pin (three-shunt)
AN002	P42	Input	Shunt current detection A/D pin (single-shunt/three-shunt)
—	PD6	Input	SW1: PWM output start
—	P00	Input	SW2: PWM output stop
POE0#	P70	Input	POE0# input pin
CMPC11	P44	Input	Comparator input pin

4.6 Software

4.6.1 Operation Overview

The sample code starts PWM output when SW1 is pressed following a reset, and stops PWM output when SW2 is pressed.

The 8 kHz carrier frequency of the complementary PWM output waveforms has dead time of 2 µsec.

In the single-shunt version output consists of left-right asymmetric (1.25 µsec. gap between left and right) waveforms, and in the three-shunt version output consists of left-right symmetric waveforms.

The MTU and 12-bit A/D converter are used in combination to perform A/D conversion processing.

The group scan function is used with the 12-bit A/D converter to accomplish A/D conversion using different timings for group A and group B. In the single-shunt version the double trigger mode on group A is used, A/D conversion takes places with two different timings on the selected channel, and the converted values are stored in different registers (redundant registers for A/D data). In the three-shunt version A/D conversion uses simultaneous sampling on three channels at the underflow (trough) of MTU4.TCNT.

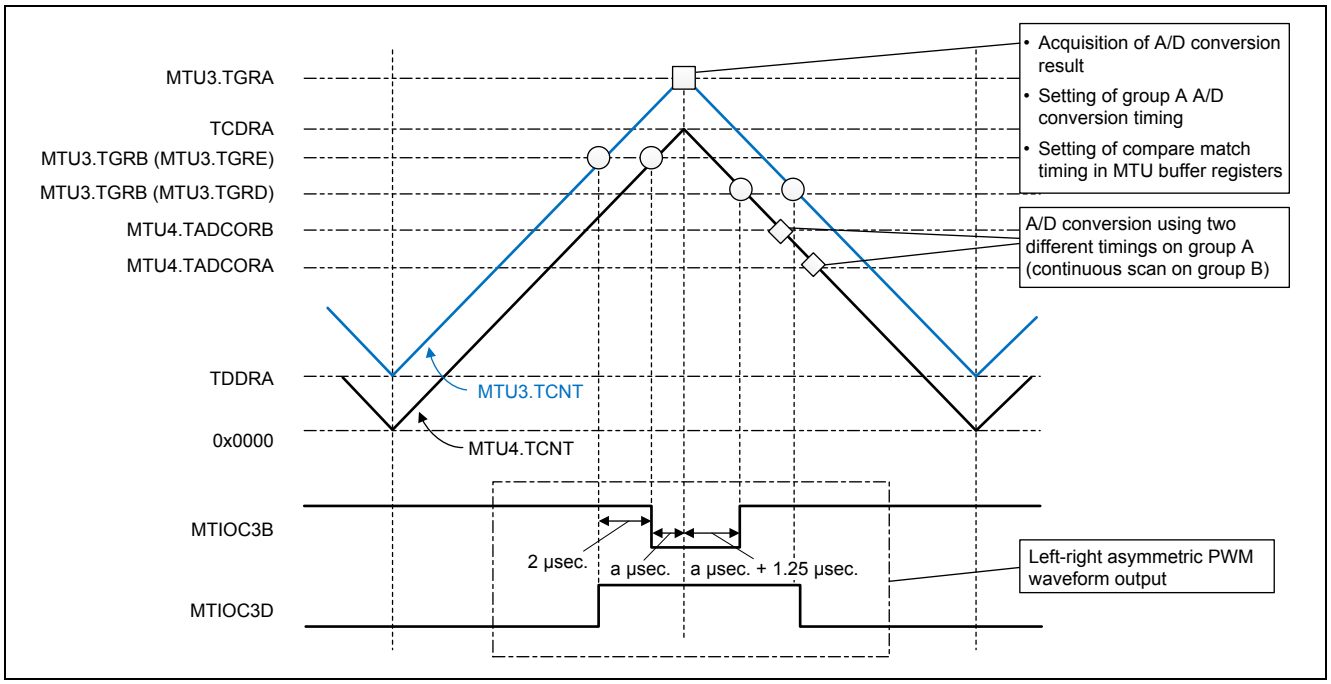
The POE function puts the PWM output pins in the high-impedance state when POE0# input occurs or when comparator output is detected.

The LVD function generates a reset when the voltage drops below 2.51 V.

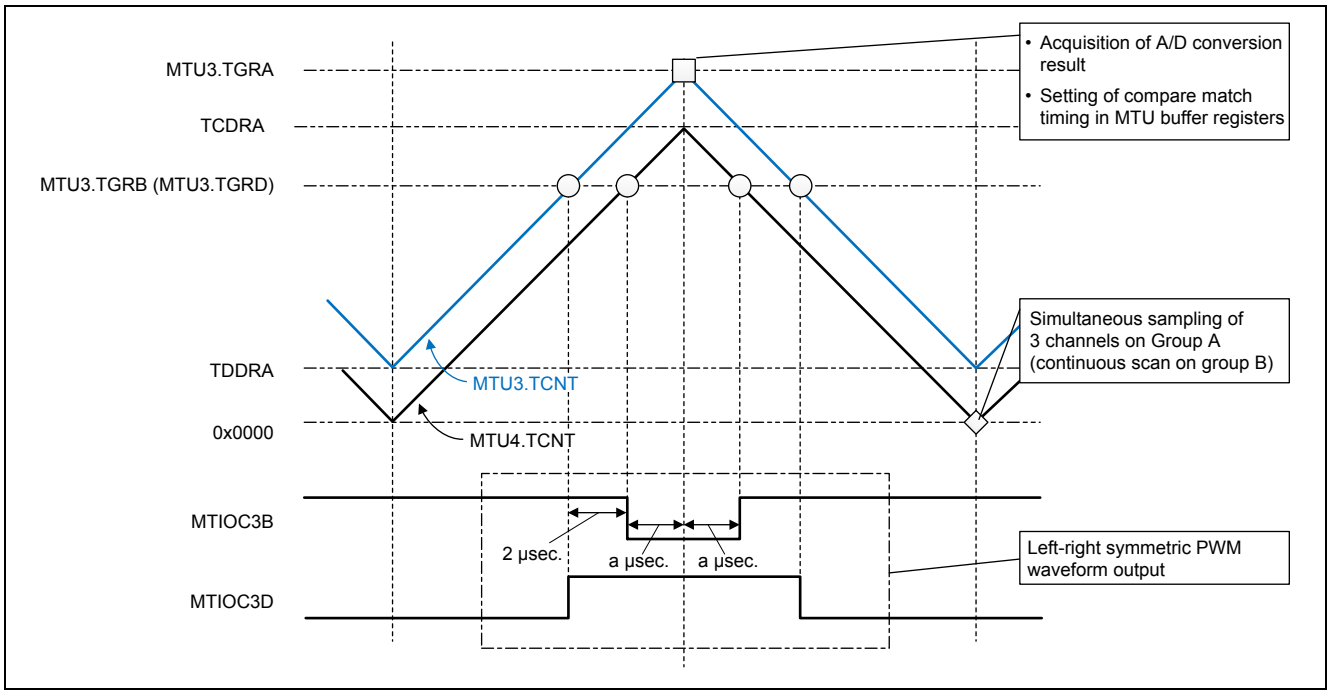
In addition, reset status register 0 (RSTSR0) can be used to obtain the reset source.

The A/D conversion timing and PWM output of the sample code (single-shunt and three-shunt versions) are shown below.

< Single-shunt version >



< Three-shunt version >



4.6.2 File Configuration

File Name	Description	Remarks
app.h	reg.c and app.c header file	
reg.c	Register access processing	
app.c	Main processing routine, setting of PWM duty	
intprg.c	Interrupt handler	
dbsct.c	Section definition file	
vecttbl.c	Vector table definition file	
iodefine.h	Register definition header file	
typedefine.h	Type definition header file	
vect.h	Vector definition header file	
stacksct.h	Stack definition header file	

4.6.3 List of Constants

Constants are listed below.

Constant Name	Setting Value	Description
DEF_FLAG_OFF	0	Flag state: off
DEF_FLAG_ON	1	Flag state: on
DEF_CLOCK_FREQ_Hz	32000000	Clock frequency
DEF_CARRIER_FREQ_Hz	8000	PWM cycle
DEF_DEADTIME_CNT_NUM	DEF_CLOCK_FREQ_NUM * 2 / 1000000	Dead time setting value
DEF_CARRIER_COUNT_NUM	DEF_CLOCK_FREQ_NUM / DEF_CARRIER_FREQ_NUM	PWM cycle count value
DEF_HALF_CARRIER_COUNT_NUM	DEF_CARRIER_COUNT_NUM / 2	Value equal to 1/2 of PWM cycle count value
MTU_AD_GET_TIMING1	800	Shunt current acquisition timing 1 (single-shunt only)
MTU_AD_GET_TIMING2	1600	Shunt current acquisition timing 1 (single-shunt only)
DEF_PWM_TABLE_MAX	360	PWM table element count

Constant tables are listed below.

Constant Name	Description
g_table_pwm_duty_u_1	U-phase PWM output timing table 1
g_table_pwm_duty_u_2	U-phase PWM output timing table 2 (single-shunt only)
g_table_pwm_duty_v_1	V-phase PWM output timing table 1
g_table_pwm_duty_v_2	V-phase PWM output timing table 2 (single-shunt only)
g_table_pwm_duty_w_1	W-phase PWM output timing table 1
g_table_pwm_duty_w_2	W-phase PWM output timing table 2 (single-shunt only)

4.6.4 List of Variables

Global variables are listed below.

Type	Variable Name	Description
unsigned char	g_val_reset_fact	For reset source storage
unsigned short	g_val_pwm_duty_table_case_num	PWM duty table setting count
unsigned short	g_val_dc_voltage	For bus voltage A/D storage (AN003)
unsigned short	g_val_ad_an005	For A/D value storage 1 (AN005)
unsigned short	g_val_ad_an007	For A/D value storage 2 (AN007)
unsigned long	g_val_enable_flag	PWM control flag
unsigned short	g_val_shunt_ad_1	For shunt current A/D value storage 1 (single-shunt (AN002)/three-shunt (AN000))
unsigned short	g_val_shunt_ad_2	For shunt current A/D value storage 2 (single-shunt (AN002)/three-shunt (AN001))
unsigned short	g_val_shunt_ad_3	For shunt current A/D value storage 3 (three-shunt) (AN002)

4.6.5 Functions

Functions are listed below.

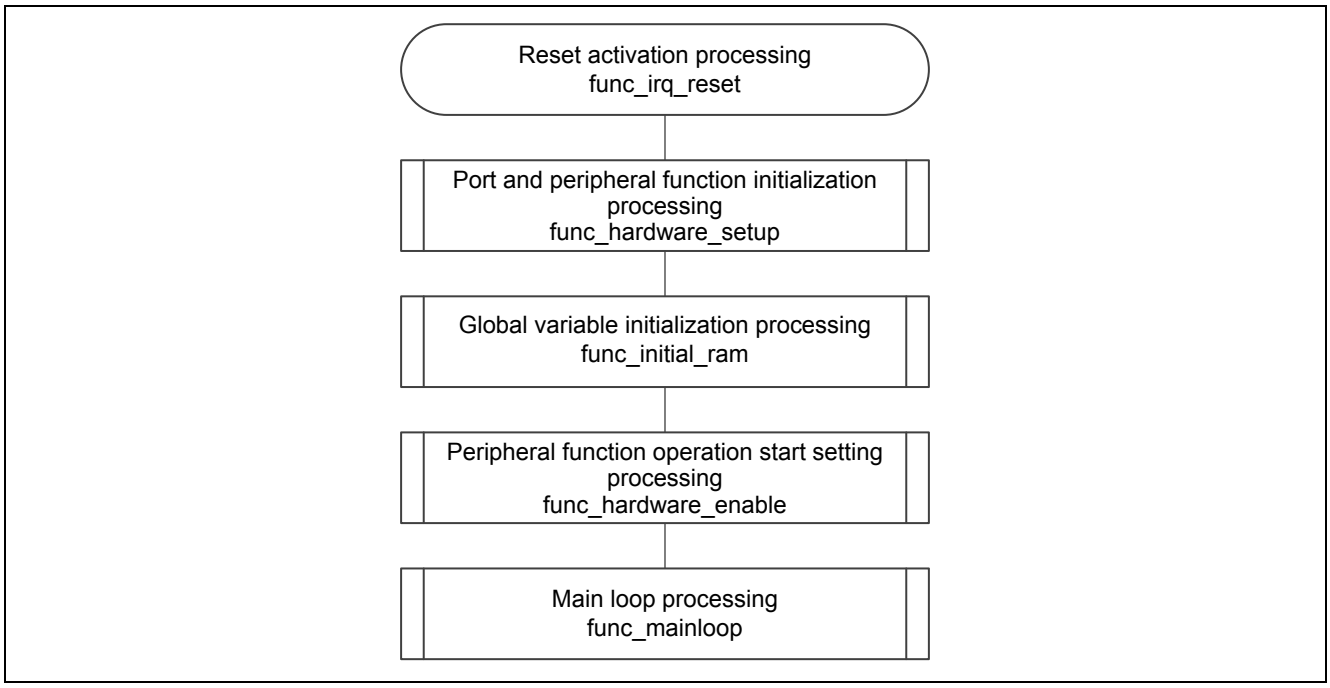
File	Function Name	Description
app.c	func_mainloop	Main loop processing
app.c	func_initial_ram	Global variable initialization processing
app.c	func_disable_pwm	MTU count stop processing
app.c	func_pwm_crest_1shunt	PWM output duty setting processing (single-shunt)
app.c	func_pwm_crest_3shunt	PWM output duty setting processing (three-shunt)
reg.c	func_hardware_setup	Port and peripheral function initialization processing
reg.c	func_hardware_enable	Peripheral function operation start setting processing
reg.c	func_irq_reset	Reset activation processing
reg.c	func_timercount_crest_isr	MTU3 TGIA3 interrupt handler (peak interrupt handler)
reg.c	func_ ipm_fault_isr	POE OEI1 interrupt handler
reg.c	func_set_ad_timing_2channel	A/D conversion timing setting processing (single-shunt only)
reg.c	func_set_pwm_to_io_port	MTU output disable processing
reg.c	func_set_io_port_to_pwm	MTU output enable processing
reg.c	func_set_pwm_duty_count_1	MTU buffer register setting processing (single-shunt/three-shunt)
reg.c	func_set_pwm_duty_count_2	MTU double buffer register setting processing (single-shunt only)
reg.c	func_reset_pwm_duty_count	MTU buffer register/double buffer register initial setting processing
reg.c	func_set_testport_on	Debug port output on processing
reg.c	func_set_testport_off	Debug port output off processing

4.7 Flowcharts

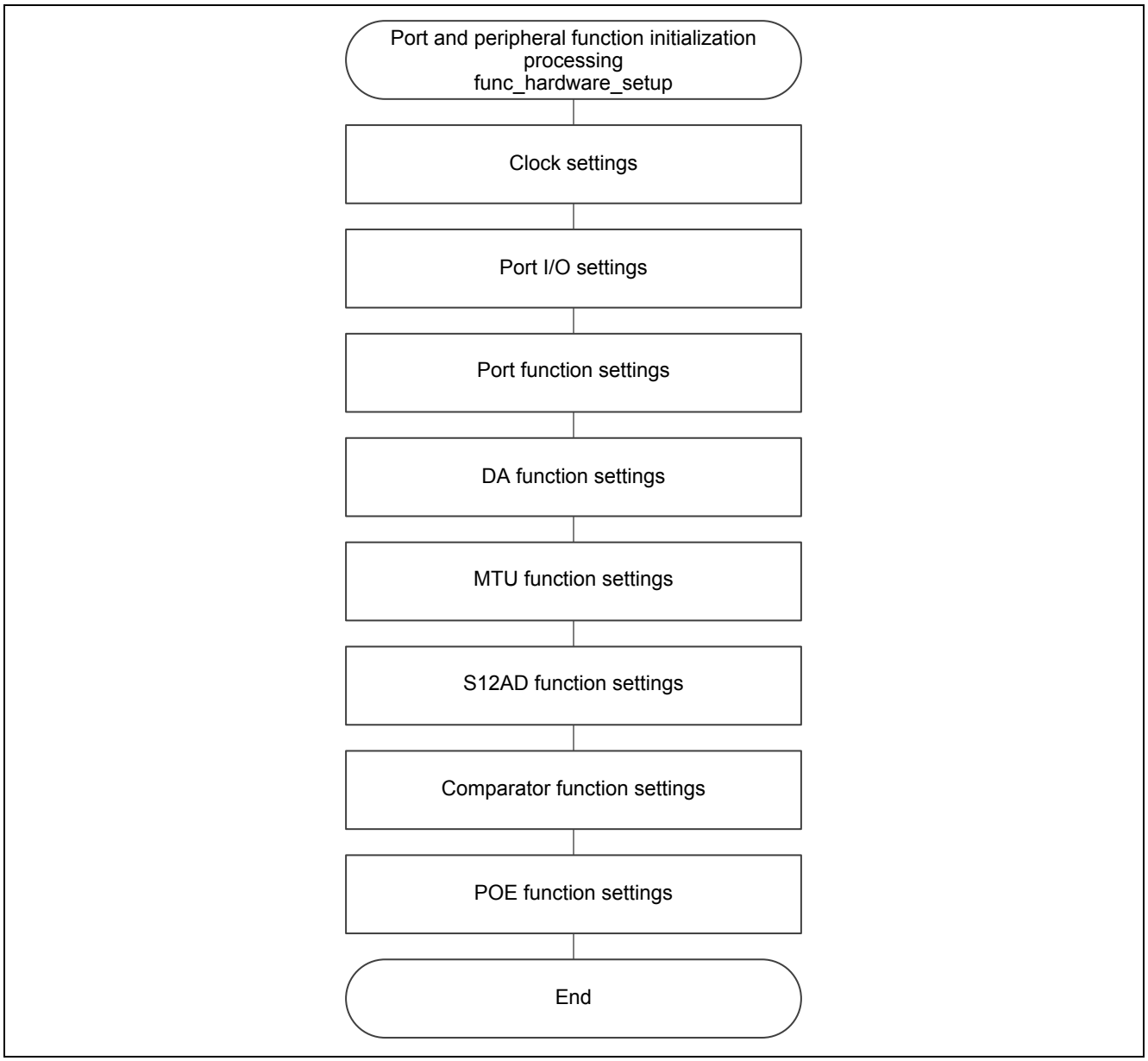
4.7.1 Activation Processing

Flowcharts of activation processing are shown below.

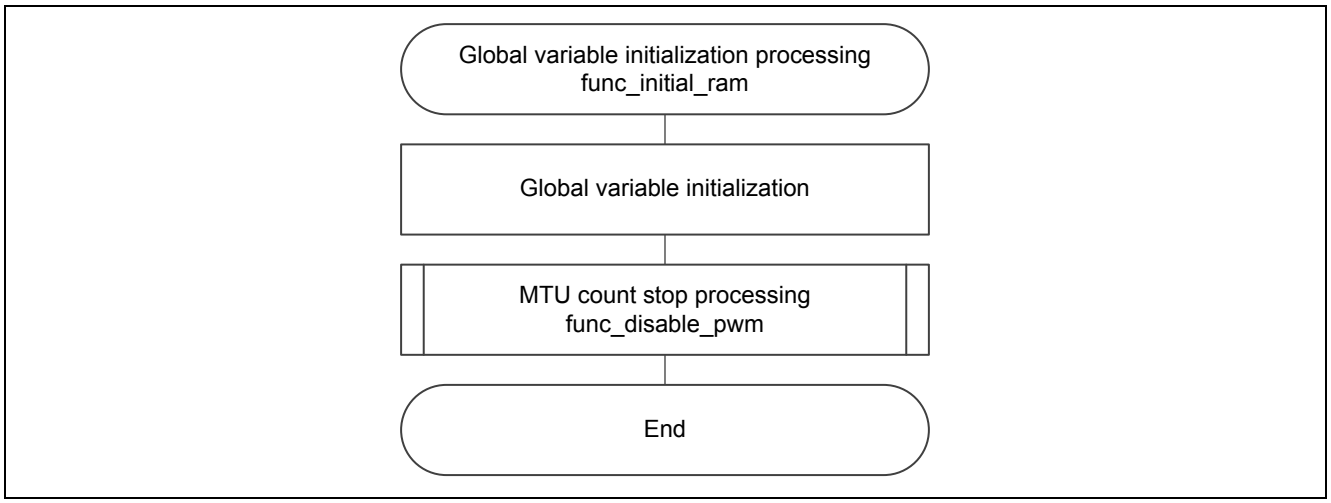
(1) Reset Activation Processing



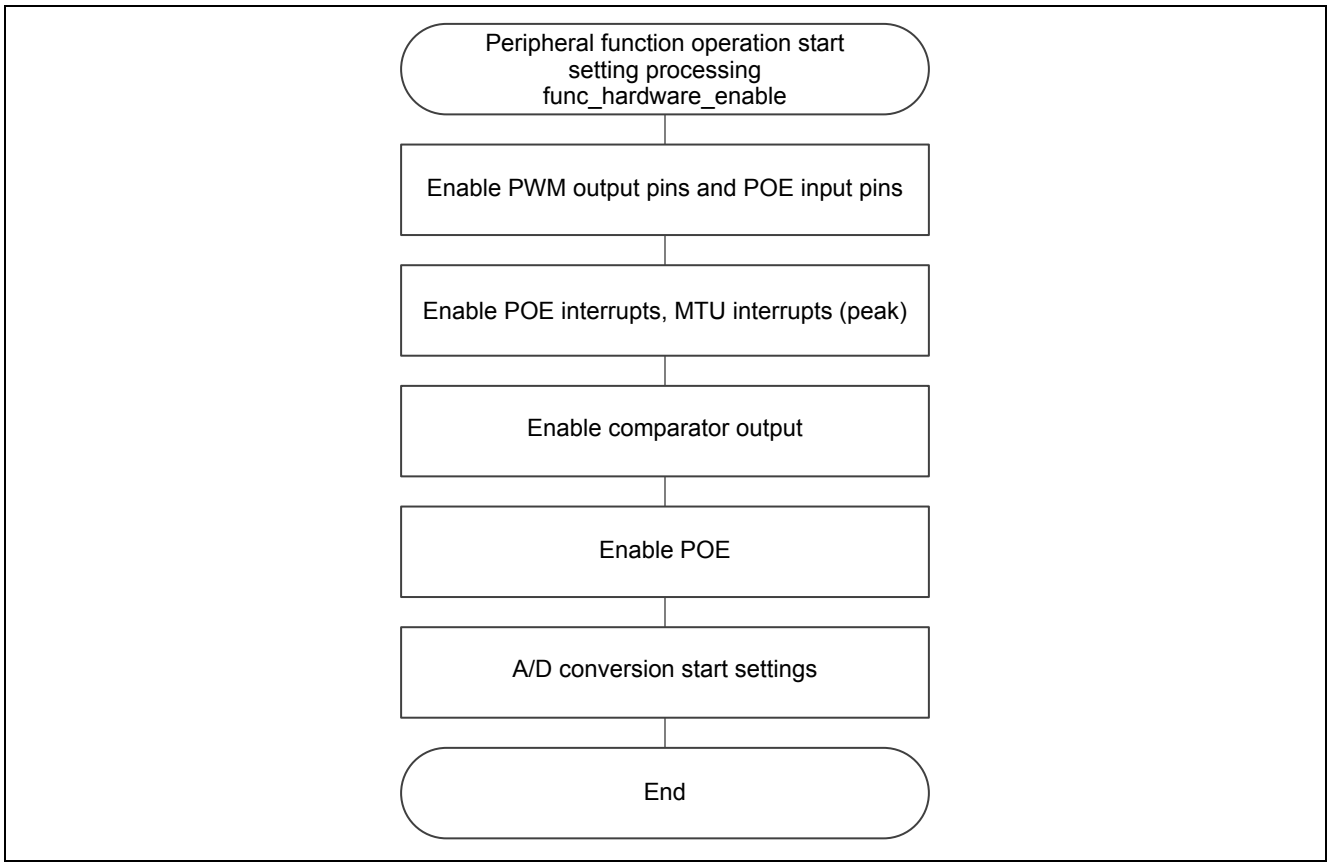
(2) Port and Peripheral Function Initialization Processing



(3) Global Variable Initialization Processing



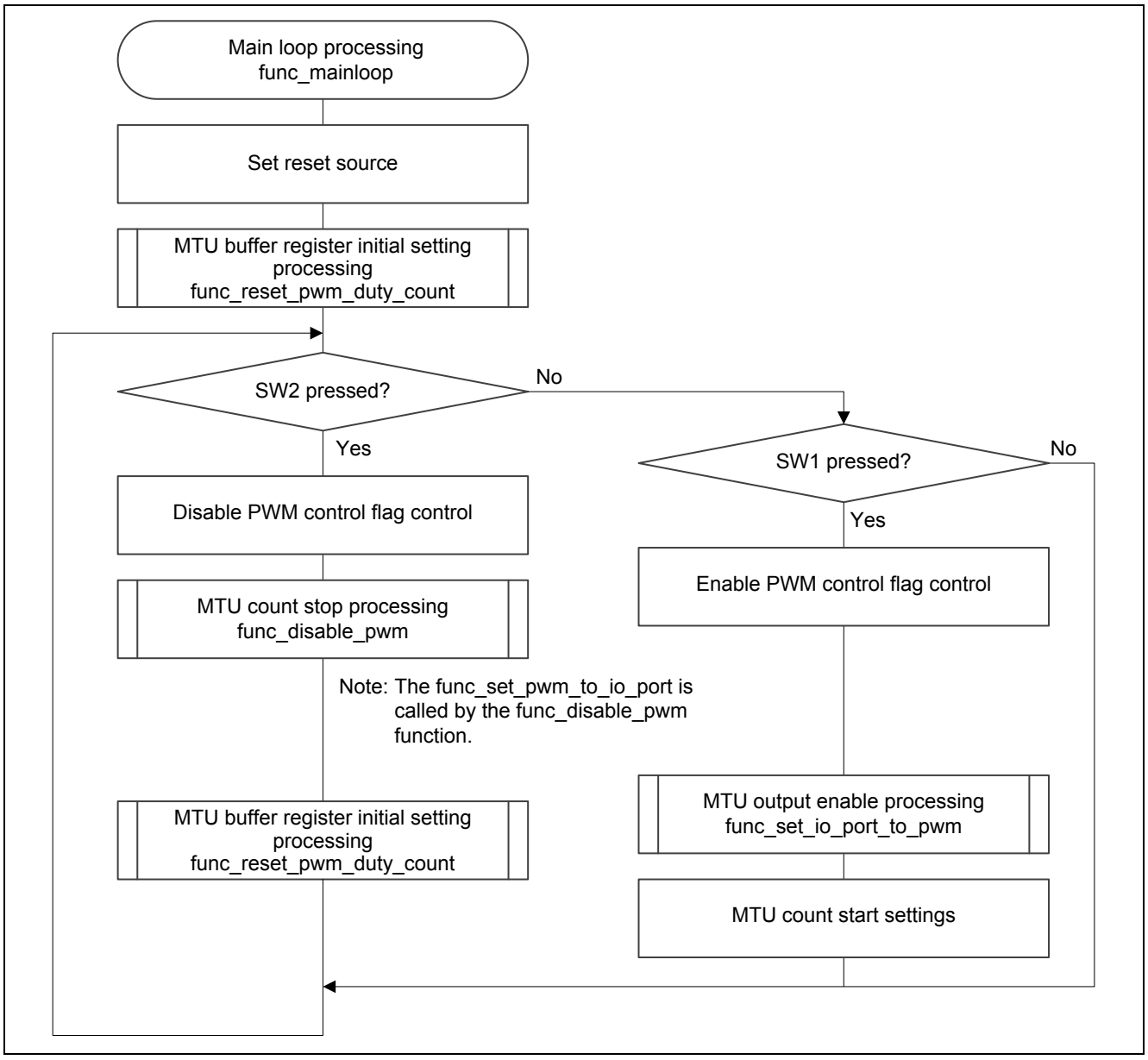
(4) Peripheral Function Operation Start Setting Processing



4.7.2 Main Processing Routine

A flowchart of the main processing routine is shown below.

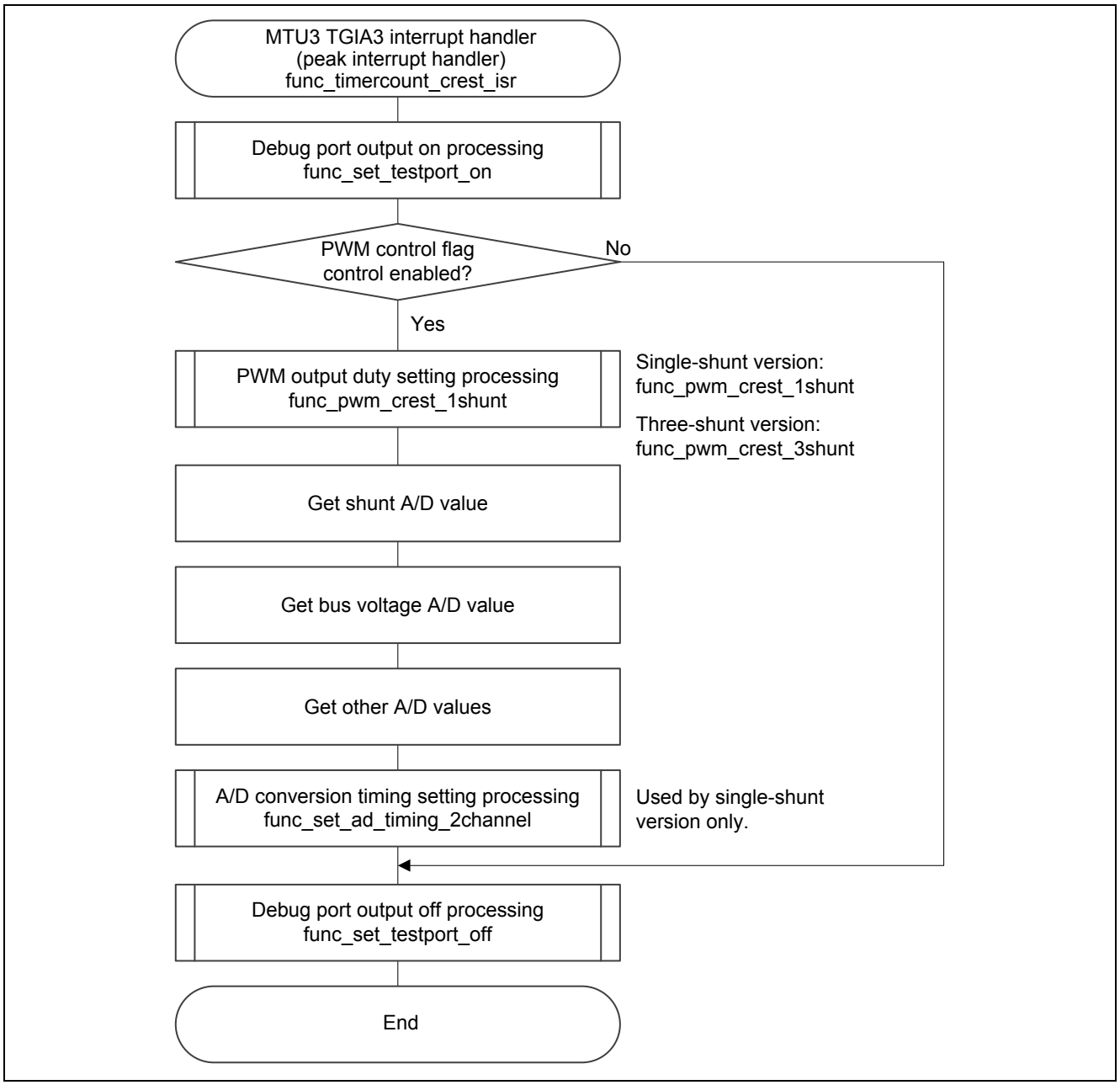
(1) Main Loop Processing



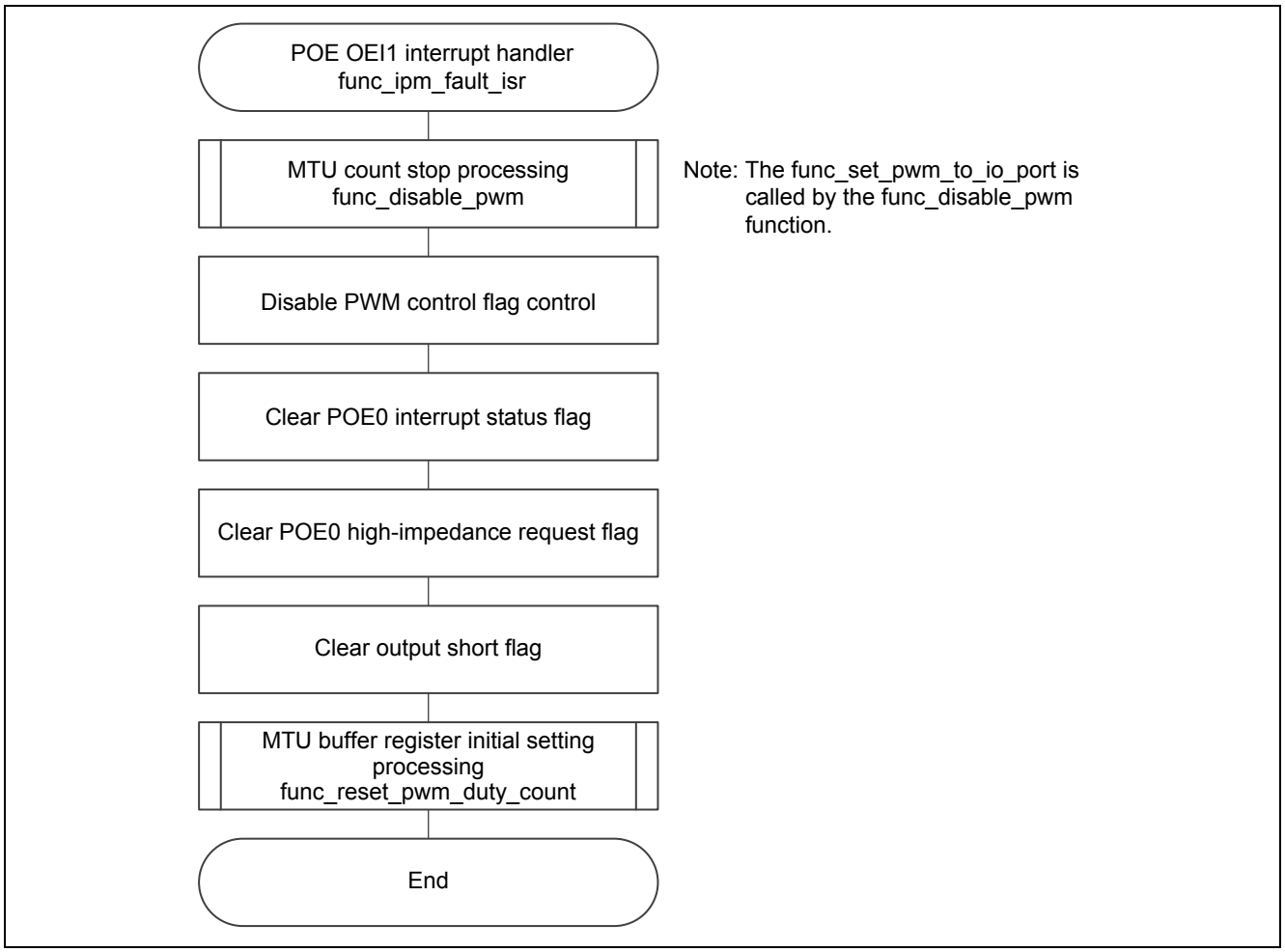
4.7.3 Interrupt Handlers

Flowcharts of the interrupt handlers are shown below.

(1) MTU3 TGIA3 Interrupt Handler (Peak Interrupt Handler)



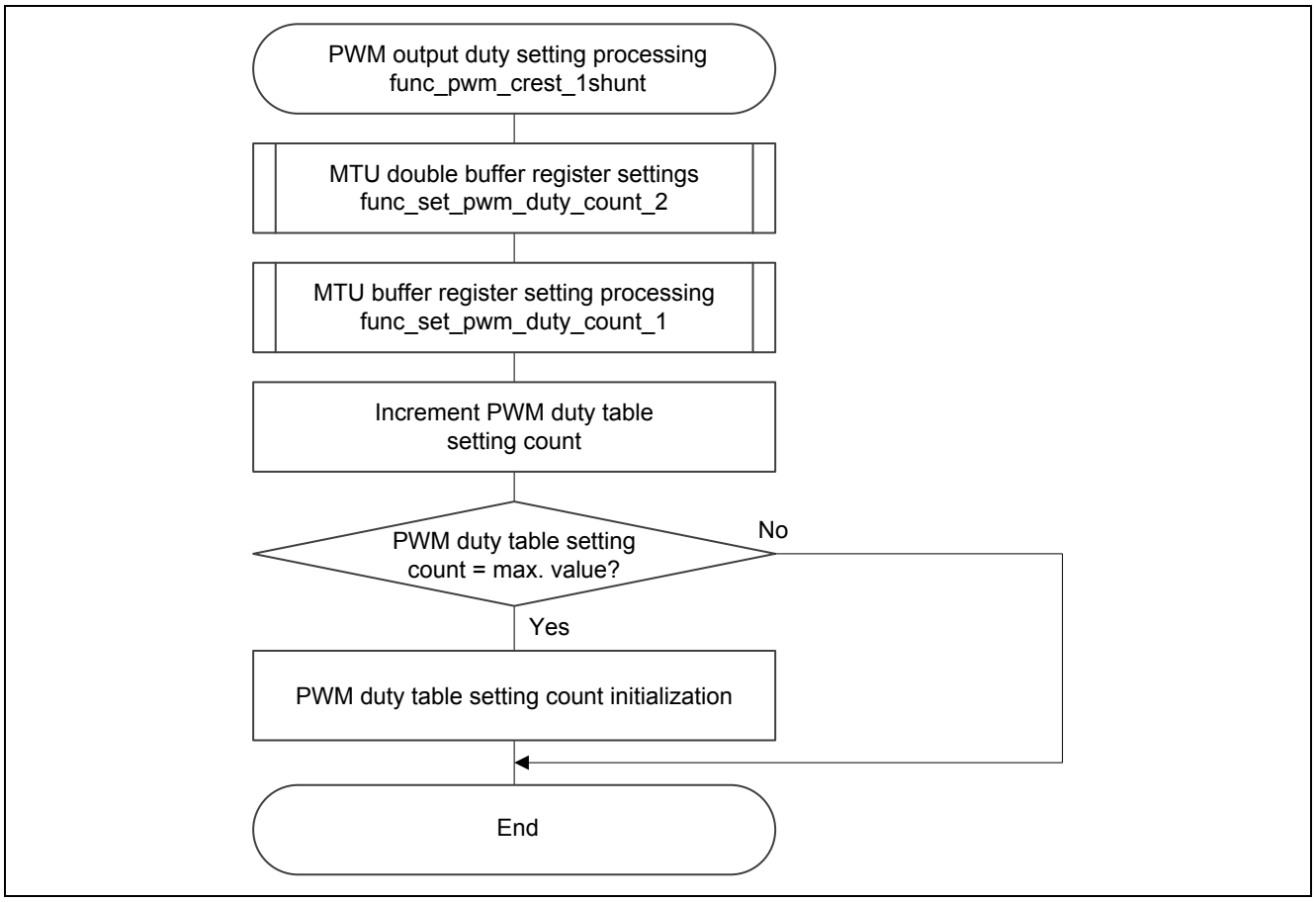
(2) POE OEI1 Interrupt Handler



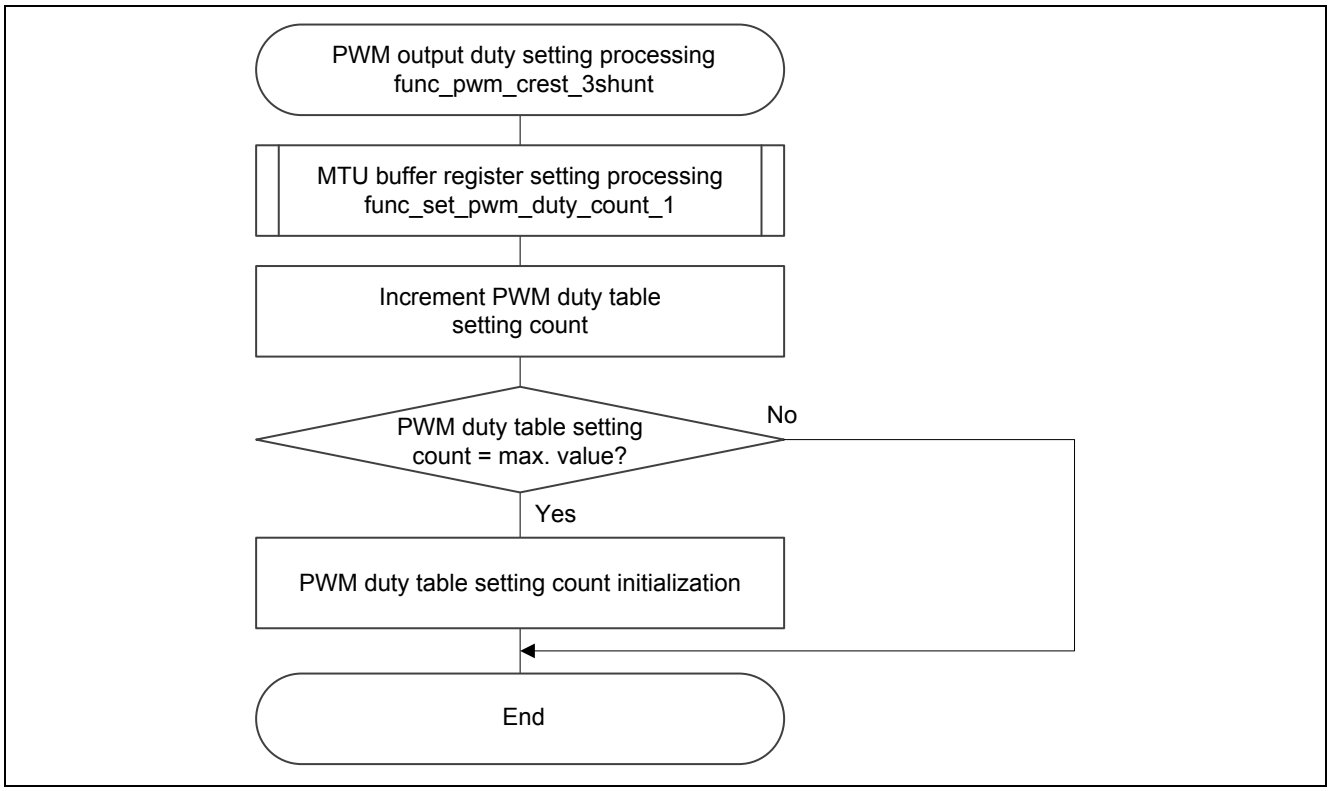
4.7.4 PWM Output Duty Setting Processing

Flowcharts of PWM output duty setting processing are shown below.

(1) PWM Output Duty Setting Processing (Single-Shunt)



(2) PWM Output Duty Setting Processing (Three-Shunt)



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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Mar. 09, 2017	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.3.0-1 November 2016)

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