RX62N Group and RX621 Group

16-Bit SDRAM Connection and Access Examples

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Introduction

This application note presents methods for connecting and accessing 16-bit SDRAM to RX62N and RX621 Group microcontrollers.

Target Devices

RX62N Group and RX621 Group

This application note also applies to RX family microcontrollers that have the same I/O registers (peripheral module control registers) as the RX62N and RX621 Group microcontrollers. However, since there have been additions to certain functions, please check the manuals carefully for differences. When applying this application note to other microcontrollers, the information presented in this application note must be modified to match the specifications of the microcontroller used and the resulting system tested thoroughly.

Contents

1. Specifications

The SDRAM interface included in the RX62N and RX621 Group microcontrollers allows the direct connection of up to 128 MB (1024 Mbits) of SDRAM. This interface supports SDRAM with a CAS latency of 1 to 3 cycles.

This application note uses a Micron Technology 128 Mbit SDRAM (the 2 Mword × 16 bit × 4 bank MT48LC8M16A2P-75), and connects to it over a 16-bit bus.

Figure 1 shows a sample DRAM connection diagram and Table 1 lists the SDRAM specifications.

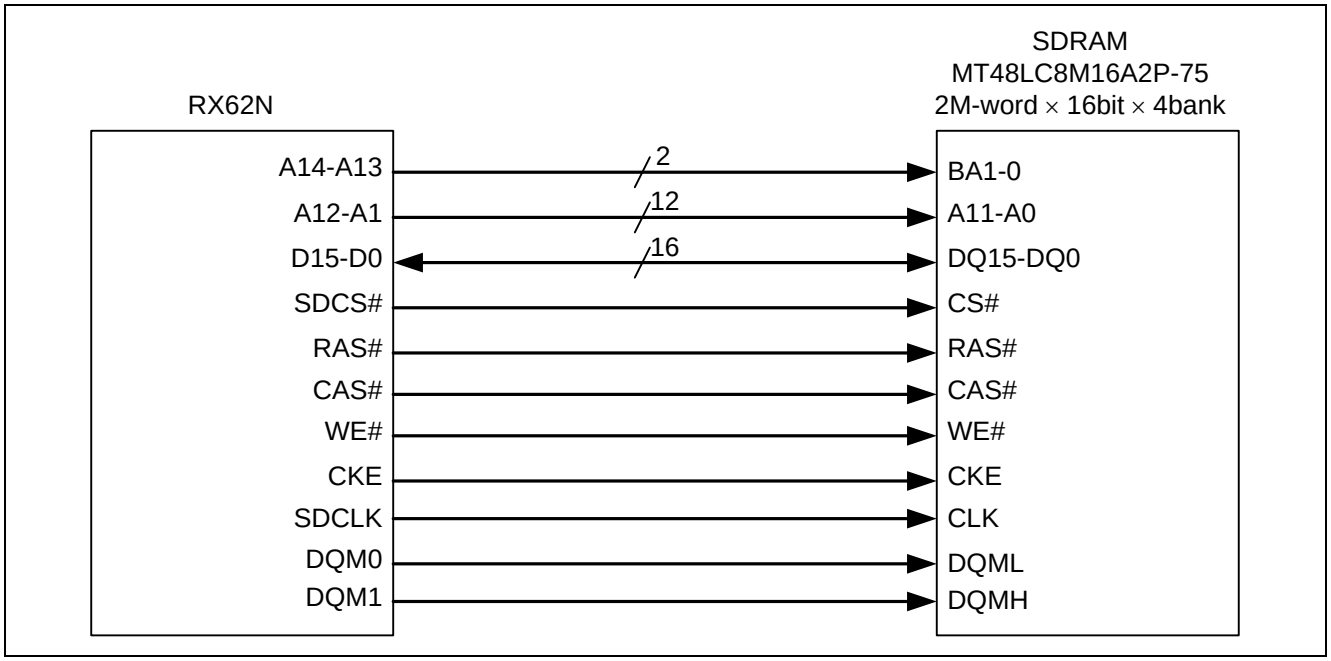


Figure 1 16-bit SDRAM Connection

Table 1 SDRAM Specifications

Item	Symbol	Description
Catalog number	—	MT48LC8M16A2P-75 (Micron Technology, Inc)
Structure	—	2 Mwords × 16 bits × 4 banks
Capacity	—	128 MB
Row address lines	—	A11-A0
Column address lines	—	A8-A0
Auto refresh interval	—	4096 refresh cycles every 64 ms
CAS latency	—	2/3
Initialization auto refresh count	—	2 times
Auto refresh period	(tRFC)	66 ns (min)
Write recovery period	(tWR)	28.33 ns (min)
Precharge command period	(tRP)	20 ns (min)
Period from active command to precharge command	(tRAS)	44 ns (min)
Delay time from active command to read/write command	(tRCD)	20 ns (min)

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2 Operation Confirmation Conditions

Item	Contents
Device	RX62N (R5F562N8BDBG)
Boad	RSK RX62N (R0K5562N0S000BE)
Power supply voltage	3.3 V (Supplied from the E1.)
Input clock	12 MHz (ICLK = 96 MHz, PCLK = 48 MHz, BCLK/SDCLK = 48 MHz)
Operating temperature	Room temperature
HEW	Version 4.09.01.007
Toolchain	RX Standard Toolchain (V.1.2.1.0)
Debugger/Emulator	E1 emulator
Debugger component	RX E1/E20 SYSTEM V.1.03.00.000

3. Usage Notes

Bus

See the User's Manual: Hardware listed in section 6, Reference Documents.

4. Operating Description

4.1 SDRAM Initialization Sequence Setup

Before accessing the SDRAM used, it is necessary to initialize that SDRAM. This initialization should be performed once after a reset. The initialization sequence must observe the initialization auto refresh interval, initialization auto refresh count, and initialization precharge cycle stipulated in the SDRAM's data sheet. The methods for determining the setting values are shown below. Table 3 lists the setting values.

(1) Initialization auto refresh interval

Since the auto refresh interval (tRFC) for the SDRAM used in this application note is 66 ns (minimum), the SDRAMC initialization auto refresh interval must meet the following condition.

66 ns (min) ≤ initialization auto refresh interval

Also, since the SDRAM clock (SDCLK) setting used in this application note is 48 MHz, the SDCLK period will be 1/48 MHz.

Therefore,

66 ns (min)/(1/48 MHz) = 3.17 cycles

Accordingly, an initialization auto refresh period of at least 4 cycles is required.
Therefore the initialization auto refresh period bits (ARFI[3:0]) are set to 0001b.

(2) Initialization auto refresh count

The SDRAM used in this application note requires that the initialization auto refresh operation be performed twice.
Therefore the initialization auto refresh count bits (ARFC[3:0]) are set to 0010b.

(3) Initialization precharge cycle

Since the precharge command period (tRP) for the SDRAM used in this application note is 20 ns (minimum), the SDRAMC initialization precharge cycle count must meet the following condition.

20 ns (min) ≤ initialization precharge cycle count

Since

20 ns/(1/48 MHz) = 0.96 cycles,

at least one SDRAM initialization precharge cycle is required. However, since fewer than 3 cycles cannot be set according to the RX62N SDRAMC specifications, the set value will be 3 cycles.
Therefore the initialization precharge cycle count setting bits (PRC[2:0]) are set to 000b.

Table 3 SDRAM Initialization Auto Refresh Control Register (SDIR)

Bit Name	Setting Value	Function
Initialization auto refresh period bits (ARFI[3:0])	0001b	4 cycles
Initialization auto refresh count bits (ARFC[3:0])	0010b	2 times
Initialization precharge cycle count setting bits (PRC[2:0])	000b	3 cycles

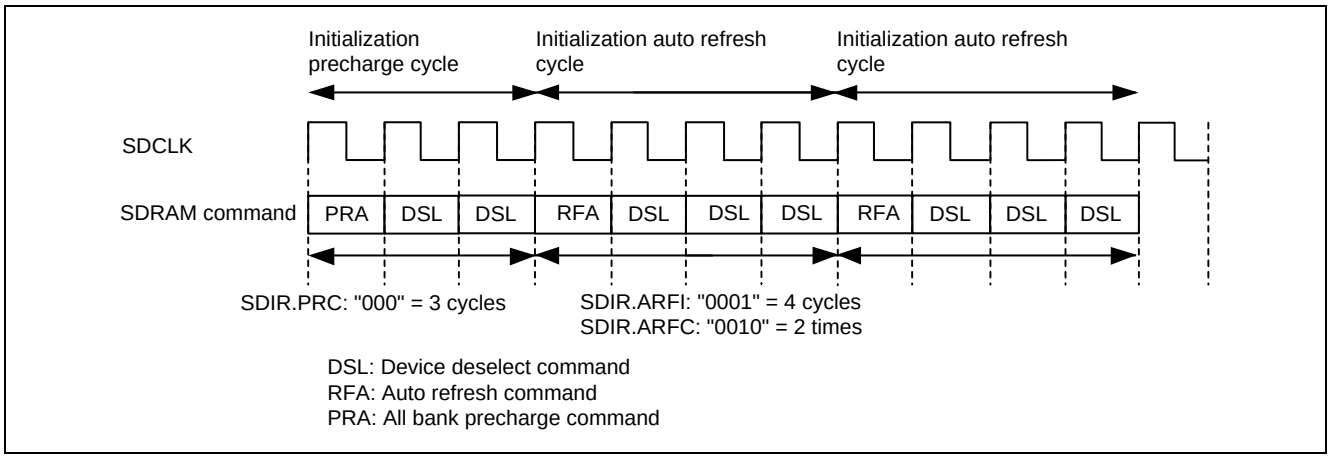


Figure 2 Initialization Sequence Timing

4.2 SDRAM Mode Register Settings

After SDRAM initialization, the SDRAM mode register must be set. The mode must be set once and only once after initialization. With the RX62N SDRAMC, the SDRAM mode register can be written automatically by setting the SDRAM mode register (SMOD). Table 4 lists the setting values.

(1) Mode register

The RX62N SDRAMC operates with a burst length of 1. Operation is not guaranteed if a burst length other then 1 is set. This application note uses a burst length of 1, a column latency of 3 cycles, and single access mode.

Table 4 SDRAM Mode Register (SDMOD)

Bit Name	Setting Value	Function
Mode register setting bits (MR[14:0])	230h	A burst length of 1, a column latency of 3 cycles, and single access mode.

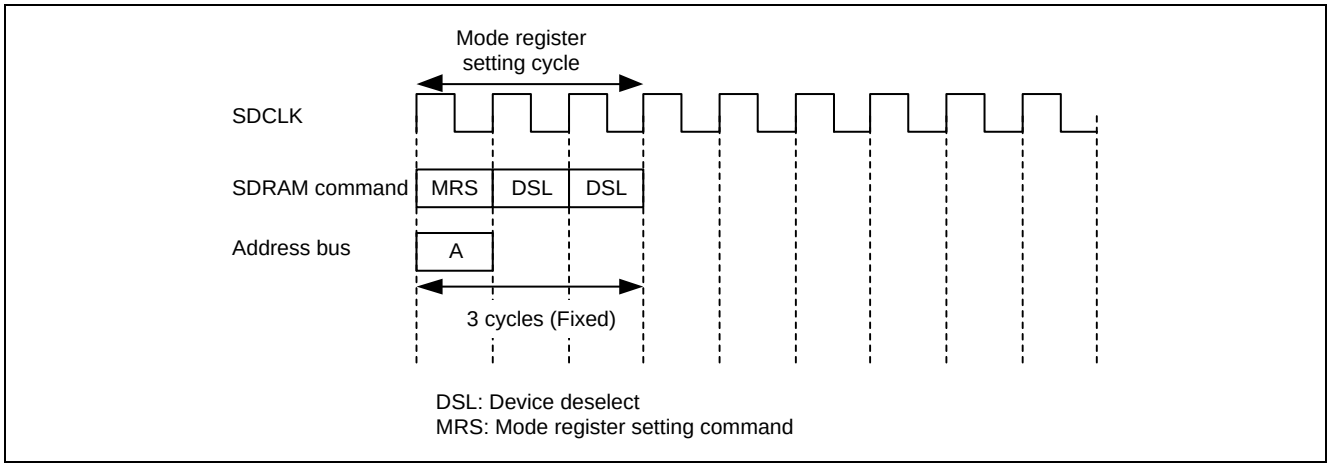


Figure 3 SDRAM Mode Register Setting Timing

4.3 Auto Refresh Settings

In this application note, auto refresh is performed for the SDRAM used. Auto refresh must be performed while observing the auto refresh required interval and auto refresh release cycles as stipulated in the SDRAM data sheet. The methods for determining the setting values are shown below. Table 5 lists the setting values used.

(1) Auto refresh required interval

The auto refresh required interval can be determined with the following formula.

RFC (auto refresh required interval setting) = (auto refresh required interval/SDCLK period) – 1

Since the SDRAM used in this application note requires that 4096 auto refresh operations be performed every 64 ms, the auto refresh interval can be determined from the following formula.

Auto refresh required interval = 64 ms/4096
= 15.62 µs

Also, since the SDRAM clock (SDCLK) frequency used in the application note is 48 MHz, the SDCLK period is 1/48 MHz.

Therefore,

RFC (auto refresh required interval setting) = (15.62 µs/(1/48 MHz)) – 1
= 749
= 2EDh

Therefore the auto refresh required interval setting bits (RFC[11:0]) are set to 2EDh.

(2) Auto refresh release cycle

Since the auto refresh period (tRFC) for the SDRAM used in this application note is 66 ns (minimum), the auto refresh release cycle must meet the following condition.

66 ns (min) ≤ auto refresh release cycle

Since this means that this cycle will be

66 ns/(1/48 MHz) = 3.17 cycles

an auto refresh release cycle count of at least 4 cycles is required.
Therefore the auto refresh release cycle setting bits (REFW[3:0]) are set to 0011b.

Table 5 SDRAM Auto Refresh Control Register (SDRFCR)

Bit Name	Setting Value	Function
Auto refresh required interval setting bits (RFC[11:0])	02EDh	749 cycles
Auto refresh cycle/auto refresh release cycle setting bits (REFW[3:0])	0011b	4 cycles

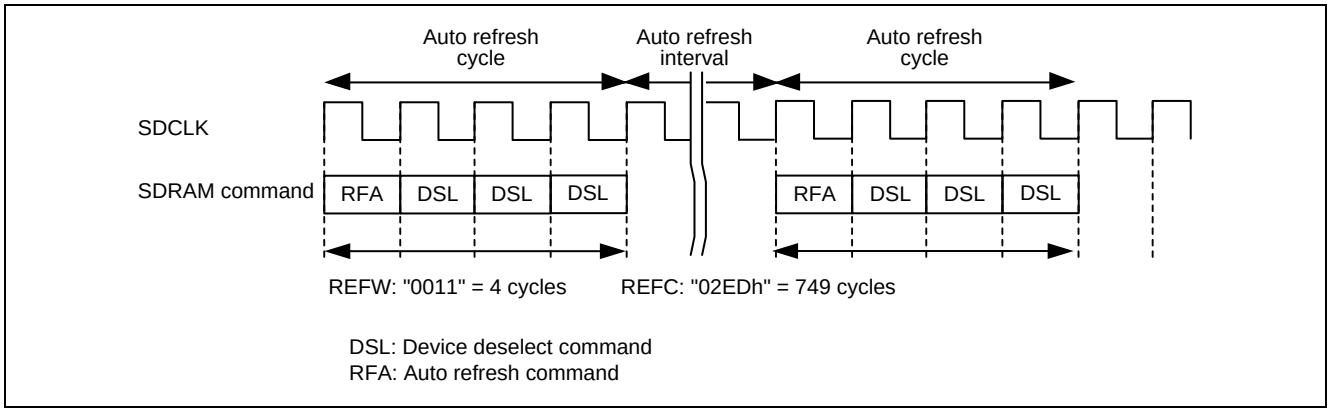


Figure 4 Auto Refresh Timing

4.4 SDRAM Timing Settings

In this application note, the access timings are set to match the specifications of the SDRAM used. It is necessary to observe the access timings stipulated in the SDRAM data sheet when accessing SDRAM. The methods for determining the setting values are shown below. Table 6 lists the setting values used.

(1) SDRAMC column latency setting

Since the SDRAM used in this application note can be operated with a CAS latency of from 1 to 3 cycles, in this application note, the CAS latency is set to 3 cycles.
Therefore the SDRAMC column latency setting bits (CL[2:0]) are set to 011b.

(2) Write recovery period setting

Since the SDRAM used in this application note has a write recovery period (tWR) of 28.3 ns (minimum), the SDRAMC write recovery period is set to meet the following condition

28.3 ns (min) ≤ write recovery period

Since

28.3 ns/(1/48 MHz) = 1.36 cycles,

A write recovery period of at least 2 cycles is required.
Therefore the write recovery period setting bit (WR) is set to 1b.

(3) Row precharge period setting

Since the SDRAM used in this application note has a row precharge period (tRP) of 20 ns (minimum), the SDRAMC row precharge period must meet the following condition.

20 ns (min) ≤ row precharge period

Since

20 ns/(1/48 MHz) = 0.96 cycles,

a row precharge period of at least 1 cycle is required.
Therefore the row precharge period setting bits (RP[2:0]) are set to 000b.

(4) Row active period setting

Since the SDRAM used in this application note has a period (tRAS) from an active command to a precharge command of 44 ns (minimum), the SDRAMC row active period will be:

44 ns (min) ≤ row active period

Since

44 ns/(1/48 MHz) = 2.11 cycles,

a row active period of at least 3 cycles is required.
Therefore the row active period setting bits (RAS[2:0]) are set to 010b.

Note that the SDRAMC row active period setting bits must be set so that the following stipulation is observed.

Row active period ≤ row column latency + SDRAC column latency

(5) Row column latency setting

Since the SDRAM used in this application note has a delay time (tRCD) of 20 ns (minimum) from the point an active command is issued until a read/write command is issued, the SDRAMC row column latency will be:

20 ns (min) ≤ row column latency

Since

20 ns/(1/48 MHz) = 0.96 cycles,

A row column latency of at least 1 cycle must be set.
To observe stipulations on the SDRAMC row active period setting bits, the following condition must be observed.

Row active period ≤ row column latency + SDRAMC column latency

In this application note, the row active period is set to 3 cycles and the SDRAMC column latency is also set to 3 cycles. Here, we determined the row column latency setting cycles using the above formula.

Row column latency setting cycle count ≥ (3 cycles) – (3 cycles)
≥ 0 cycles

However, since the row column latency setting bits (RCD[1:0]) cannot be set to 0 cycles, in this application note, this field is set to 1 cycle, or 00b.

Table 6 SDRAM Timing Register (SDTR)

Bit Name	Setting Value	Function
SDRAMC column latency setting bits (CL[2:0])	011b	3 cycles
Write recovery period setting bit (WR)	1b	2 cycles
Row precharge period setting bits (RP[2:0])	000b	1 cycle
Row active period setting bits (RAS[2:0])	010b	3 cycles
Row column latency setting bits (RCD[1:0])	00b	1 cycle

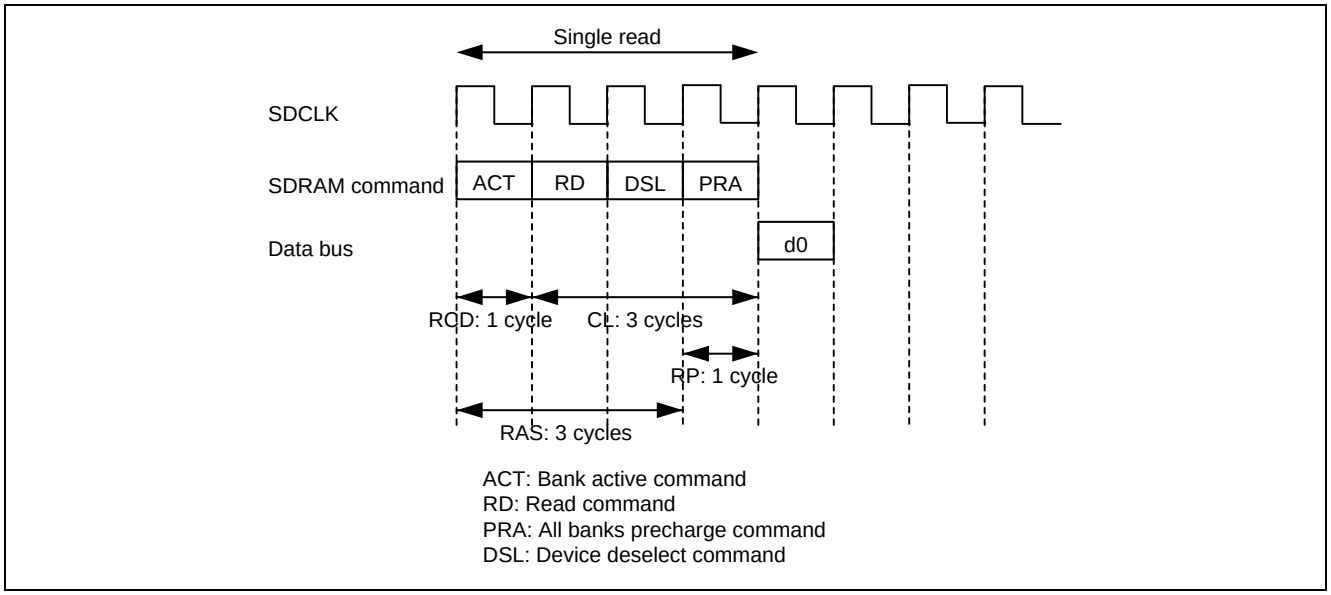


Figure 5 Read Timing

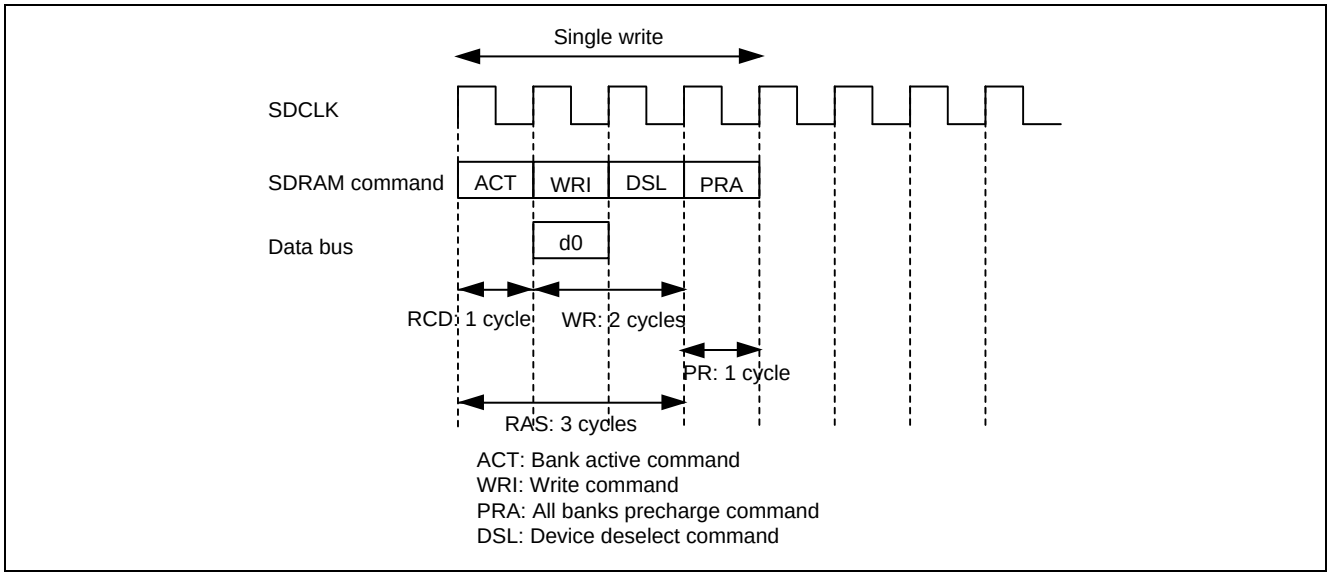


Figure 6 Write Timing

5. Software Documentation

5.1 Symbolic Constants

Table 7 Symbolic Constants

Constant Name	Setting Value	Contents	Function Used
sdram_top	0x08000000	SDRAM (32bit) SDRAM (32 bits) start address	main
sdram_end	0x09000000	SDRAM (32bit) SDRAM (32 bits) end address	main

5.2 RAM Variables

Table 8 RAM Variables

Type	Variable Name	Contents	Function Used
Unsigned long	sdram_adr	SDRAM (32 bits) address pointer	main
Unsigned long	sdram_data	SDRAM (32 bits) data variable	main
Unsigned long	sdram_cmp_data	SDRAM (32 bits) comparison data	main

5.3 Functions

Table 9 Functions

Function Name	Outline
PowerON_Reset_PC	Initialization function Sets INTB, FPSW, and PSW, changes the processor mode, and calls the function main().
Main	Main function Calls the function init(), performs program operations (reads and writes to SDRAM), and calls the function err().
Init	MCU initialization function Sets up various registers.
Err	Error function Performs SDRAM data compare check error handling.

5.4 Registers Used

The tables below lists the registers used by this application note. Note that the setting values shown are the ones used in this application note and differ from the initial values.

(1) Clock generation circuit

System clock control register (SCKCR) Bits: 32, Address: 0008 0020h

Bit	Symbol	Setting	Name	Function	R/W
b11-b8	PCK[3:0]	0001	Peripheral module clock selection bits	0001: × 4 PCLK = 48 MHz (When the EXTAL clock is 12 MHz)	R/W
b19-b16	BCK[3:0]	0001	External bus clock and SDRAM selection bits	0001: × 4 BCLK, SDCLK = 48 MHz (When the EXTAL clock is 12 MHz)	R/W
b22	PSTOP0	0	SDCLK pin output control bit	0: SDCLK output pin operates	R/W
b27-b24	ICK[3:0]	0000	System clock selection bits	0000: × 8 ICLK = 96 MHz (When the EXTAL clock is 12 MHz)	R/W

(2) Operating mode

System control register 0 (SYSCR0) Bits: 8, Address: 0008 0006h

Bit	Symbol	Setting	Name	Function	R/W
b0	ROME	1	Internal ROM enable bit	1: Internal ROM enabled	R/W
b1	EXBE	1	External bus enable bit	1: External bus enabled	R/W
b15-b8	KEY[7:0]	5Ah	SYSCR0 key code	5Ah: SYSCR0 register write enabled	R/W

(3) I/O ports

Port function register 3 (PF3BUS) Bits: 8, Address: 0008 C103h

Bit	Symbol	Setting	Name	Function	R/W
b0	A16E	0	Address A16 output enable bit	0: A16 output disabled	R/W
b1	A17E	0	Address A17 output enable bit	0: A17 output disabled	R/W
b2	A18E	0	Address A18 output enable bit	0: A18 output disabled	R/W
b3	A19E	0	Address A19 output enable bit	0: A19 output disabled	R/W
b4	A20E	0	Address A20 output enable bit	0: A20 output disabled	R/W
b5	A21E	0	Address A21 output enable bit	0: A21 output disabled	R/W
b6	A22E	0	Address A22 output enable bit	0: A22 output disabled	R/W
b7	A23E	0	Address A23 output enable bit	0: A23 output disabled	R/W

Port function register 4 (PF4BUS) Bits: 8, Address: 0008 C104h

Bit	Symbol	Setting	Name	Function	R/W
b1-0	ADRLE [1:0]	11	Address low-order A9 to A0 output enable bits	11: A9 to A0 output enabled	R/W
b2	A10E	1	Address A10 output enable bit	0: A10 output enabled	R/W
b3	A11E	1	Address A11 output enable bit	0: A11 output enabled	R/W
b4	A12E	1	Address A12 output enable bit	0: A12 output enabled	R/W
b5	A13E	1	Address A13 output enable bit	0: A13 output enabled	R/W
b6	A14E	1	Address A14 output enable bit	0: A14 output enabled	R/W
b7	A15E	0	Address A15 output enable bit	0: A15 output disabled	R/W

Port function register 5 (PF5BUS) Bits: 8, Address: 0008 C105h

Bit	Symbol	Setting	Name	Function	R/W
b4	DHE	1	Data D15 to D8 enable bit	1: PE7 to PE0 set to function as external bus D15 to D8.	R/W
b5	DHE32E	0	Data D31 to D16 enable bit	0: PG7 to PG0 and P97 to P90 set to function as I/O ports.	R/W

Port function register 6 (PF6BUS) Bits: 8, Address: 0008 C106h

Bit	Symbol	Setting	Name	Function	R/W
b4	MDSDE	1	SDRAM pin enable bit	See b6 (DQM1E bit)	R/W
b6	DQM1E	1	DQM1 output enable bit	MDSDE DQM1E 11: SDRAM enabled (all pins)	R/W
b7	SDCLKE	1	SDCLK output enable bit	1: SDCLK output enabled	R/W

Data register (P0DR) Bits: 8, Address: 0008 C020h

Bit	Symbol	Setting	Name	Function	R/W
b2	B2	0	P02 output data stored bit	0: Output data = 0	R/W
b3	B3	0	P03 output data stored bit	0: Output data = 0	R/W

Data direction register (P0DDR) Bits: 8, Address: 0008 C000h

Bit	Symbol	Setting	Name	Function	R/W
b2	B2	1	P02 I/O data specification bit	1: Output port	R/W
b3	B3	1	P03 I/O data specification bit	1: Output port	R/W

(4) External bus

Initialization sequence control register (SDICR) Bits: 8, Address: 0008 3C20h

Bit	Symbol	Setting	Name	Function	R/W
b0	INIRQ	1	Initialization sequence start bit	1: Initialization sequence start	R/W

SDRAM initialization register (SDIR) Bits: 16, Address: 0008 3C24h

Bit	Symbol	Setting	Name	Function	R/W
b3-b0	ARFI[3:0]	0001	Initialization auto refresh period bits	0001: 4 cycles	R/W
b7-b4	ARFC [3:0]	0010	Initialization auto refresh count bits	0010: 2 times	R/W
b10-b8	PRC[2:0]	000	Initialization precharge cycle count setting bits	000: 3 cycles	R/W

SDC control register (SDCCR) Bits: 8, Address: 0008 3C00h

Bit	Symbol	Setting	Name	Function	R/W
b0	EXENB	1	Operation enable bit	1: Operation enable	R/W
b5-b4	BSIZE [1:0]	00	SDRAM bus width selection bits	00: Specifies a 16-bit bus space	R/W

SDRAM mode register (SDMOD) Bits: 16, Address: 0008 3C48h

Bit	Symbol	Setting	Name	Function	R/W
b14-b0	MR[14:0]	0230h	Mode register setting bits	Executing a write: Issues a mode register set command	R/W

SDRAM refresh control register (SDRFCR) Bits: 16, Address: 0008 3C14h

Bit	Symbol	Setting	Name	Function	R/W
b11-b0	RFC[11:0]	2EDh	Auto refresh required interval setting bits	001011101101: 749 cycles	R/W
b15-b12	REFW [3:0]	0011	Auto refresh cycle/auto refresh release cycle setting bits	0011: 4 cycles	R/W

SDRAM auto refresh control register (SDRFEN) Bits: 8, Address: 0008 3C16h

Bit	Symbol	Setting	Name	Function	R/W
b0	RFEN	1	Auto refresh operation enable bit	1: Auto refresh operation enable	R/W

SDC mode register (SDCMOD) Bits: 8, Address: 0008 3C01h

Bit	Symbol	Setting	Name	Function	R/W
b0	EMODE	0	Endian specification bit	0: The SDRAM address space endian operation is set to be the same as the operating mode endian setting.	R/W

SDRAM access mode register (SDAMOD) Bits: 8, Address: 0008 3C02h

Bit	Symbol	Setting	Name	Function	R/W
b0	BE	0	Continuous access enable	0: Continuous access disabled	R/W

SDRAM address register (SDADR) Bits: 8, Address: 0008 3C40h

Bit	Symbol	Setting	Name	Function	R/W
b1-b0	MXC[1:0]	01	Address multiplexing selection bit	01: 9-bit shift	R/W

SDRAM timing register (SDTR) Bits: 32, Address: 0008 3C44h

Bit	Symbol	Setting	Name	Function	R/W
b2-b0	CL[2:0]	011	SDRAMC column latency setting bits	011: 3 cycles	R/W
b8	WR	1	Write recovery period setting bit	1: 2 cycles	R/W
b11-b9	RP[2:0]	000	Row precharge period setting bits	000: 1 cycle	R/W
b13-b12	RCD[1:0]	00	Row column latency setting bits	00: 1 cycle	R/W
b18-b16	RAS[2:0]	010	Row active period setting bits	010: 3 cycles	R/W

5.5 Function Descriptions

5.5.1 PowerON_Reset_PC

(1) Description

The PowerON_Reset_PC function initializes the stack pointer (SP), and, using embedded functions and standard library functions, sets the interrupt mask bits and sets up uninitialized and initialized data.

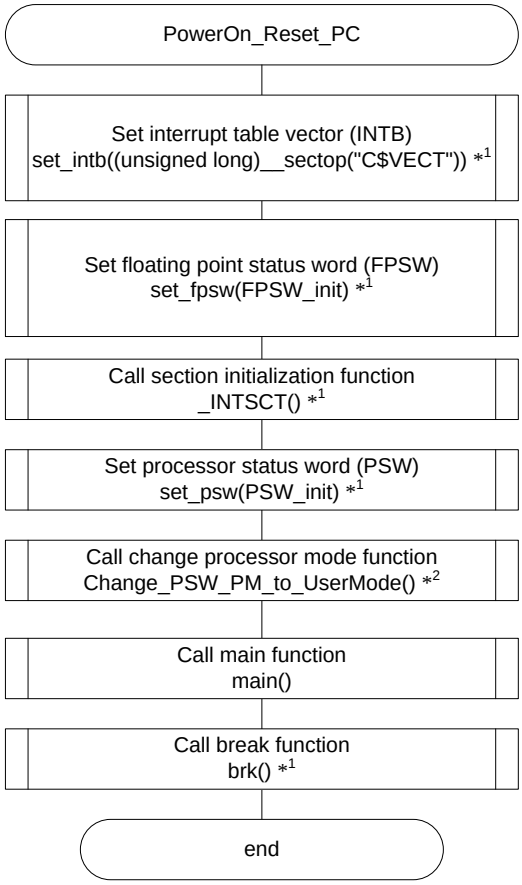
(2) Arguments

None

(3) Return value

None

(4) Flowchart



Notes: 1. set_intb, set_fpsw, set_psw functions : Embedded functions
_INTSCT function : Standard library function
brk function : Embedded function
2. Transition from supervisor mode to user mode
For details, see the development environment manual listed in section 6, Reference Documents.

Figure 7 Flow chart (PowerON_Reset_PC)

5.5.2 Main Function

(1) Description

The main() function calls the init() and err() functions and performs the program operations (reading and writing memory and comparing the data values).

(2) Arguments

None

(3) Return value

None

(4) Flowchart

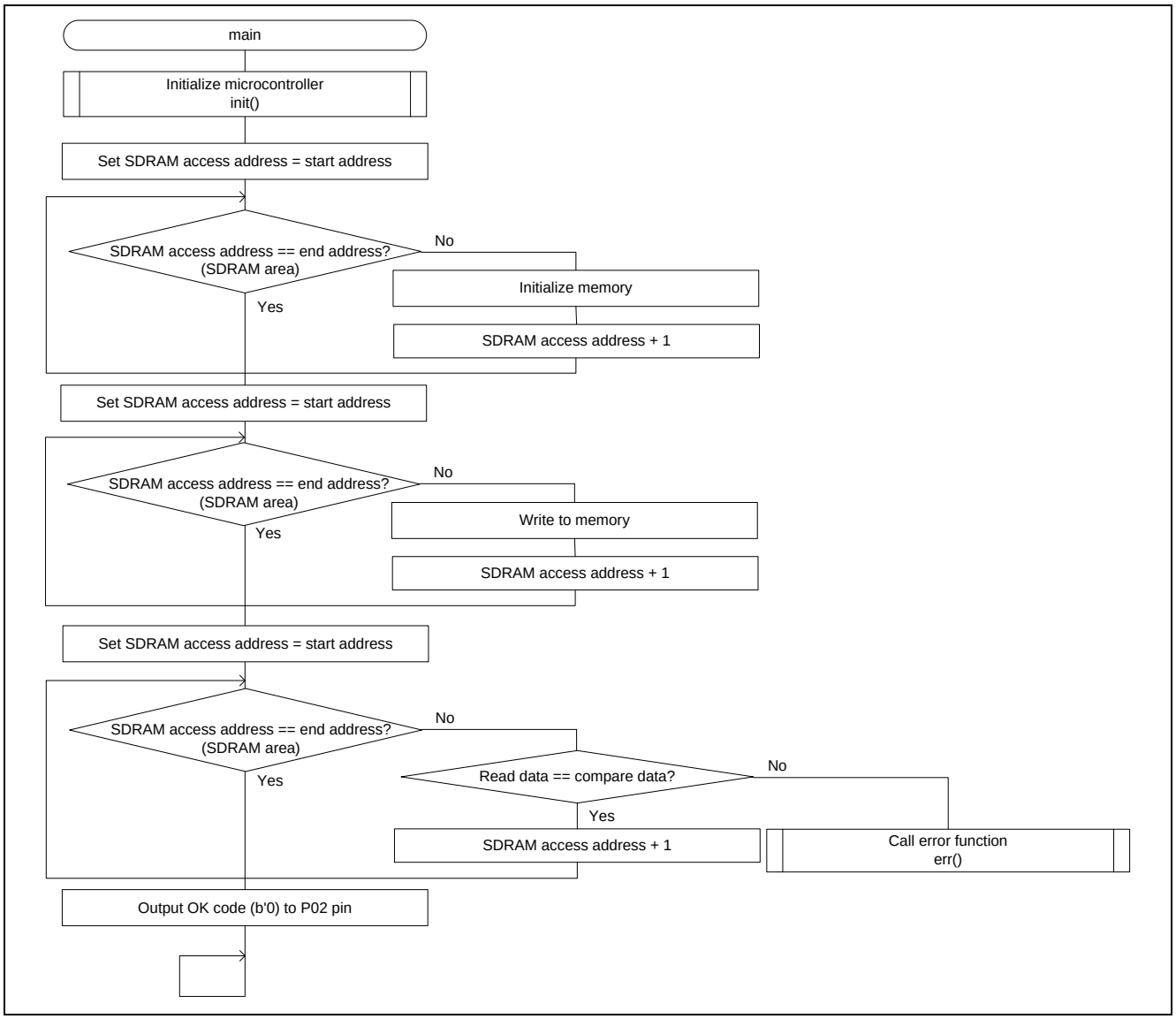


Figure 8 Flow chart (main)

5.5.3 init Function

(1) Description

The init() function initializes the functions used by the microcontroller.

(2) Arguments

None

(3) Return value

None

(4) Flowchart

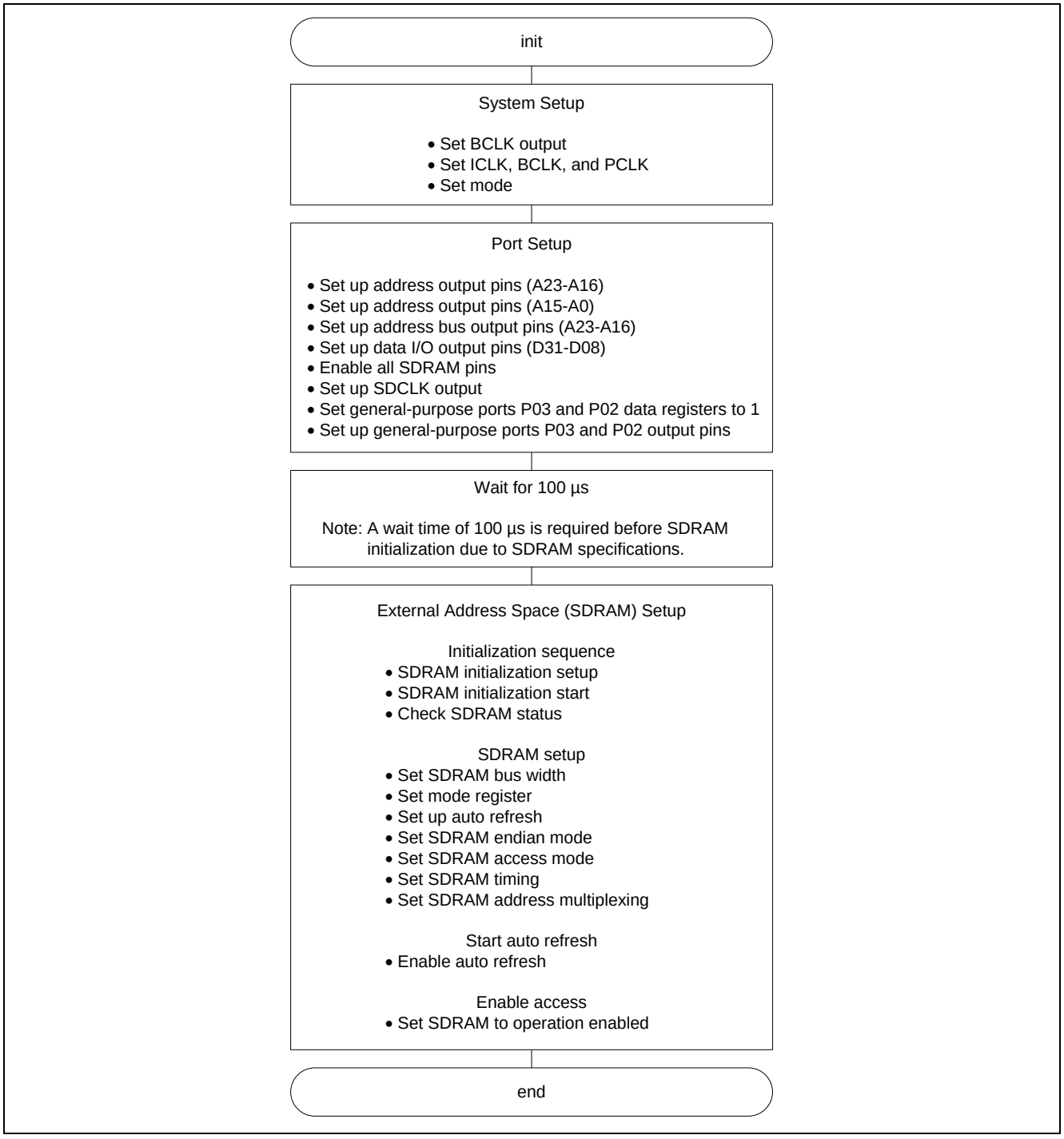


Figure 9 Flow chart (init)

5.5.4 err Function

(1) Description

The err() function outputs an error code indicating that a data compare operation found a match failure.

(2) Arguments

None

(3) Return value

None

(4) Flowchart

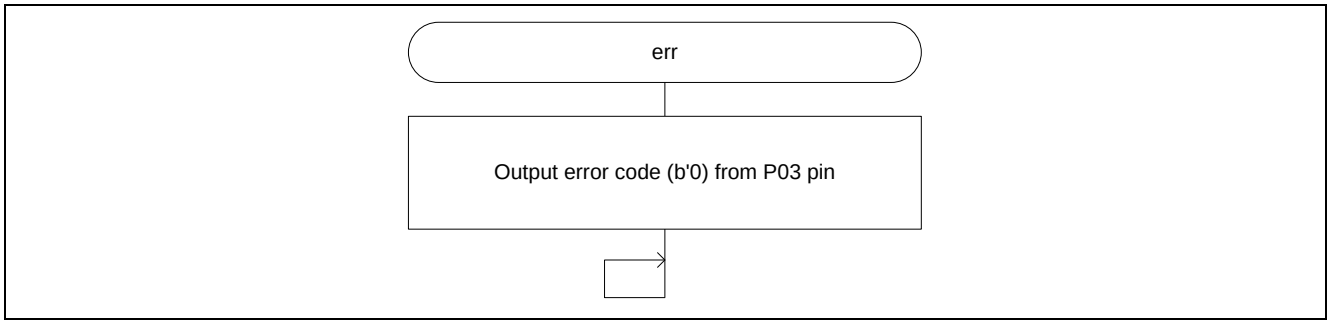


Figure 10 Flow chart (err)

6. Reference Documents

User's Manual: Hardware

RX62N and RX621 Group User's Manual: Hardware Rev.1.30

The latest version can be downloaded from the Renesas Electronics website.

User's Manual: Development Tools

RX Family C/C++ Compiler Package V.1.02

C Compiler User's Manual Rev.1.00

The latest version can be downloaded from the Renesas Electronics website.

Technical Update

The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/contact/

Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
2.02	Feb 14, 2014	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to a product with a different type number, confirm that the change will not lead to problems.
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