RX62T

3-level Inverter Control with Induction Motor

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Introduction

The objective of this application note is to implement RX62T MCU base application board and software control reference for 3-level inverter control with induction motor and to solve the natural point voltage balance problem of 3-level inverter.

Target Device

RX62T

Contents

1. Specifications

- Target Device: RX62T
- Natural Point Clamped 3-Level Inverter
- Input voltage: 400 V AC
- Output current: 2.5 A
- Rated power: 1 kW
- Switching frequency: 8 kHz
- Control Mode: V/F
- Speed Range: 140 ~ 1400 rpm
- Induction Motor
- Power: 1 HP/750 W
- Rated speed: 1400 rpm

Fig. 1 shows the block diagram for the implementation of 3-Level Inverter drives. As shown in Fig. 1, RX62T is used to realize the control software of 3-Level Inverter.

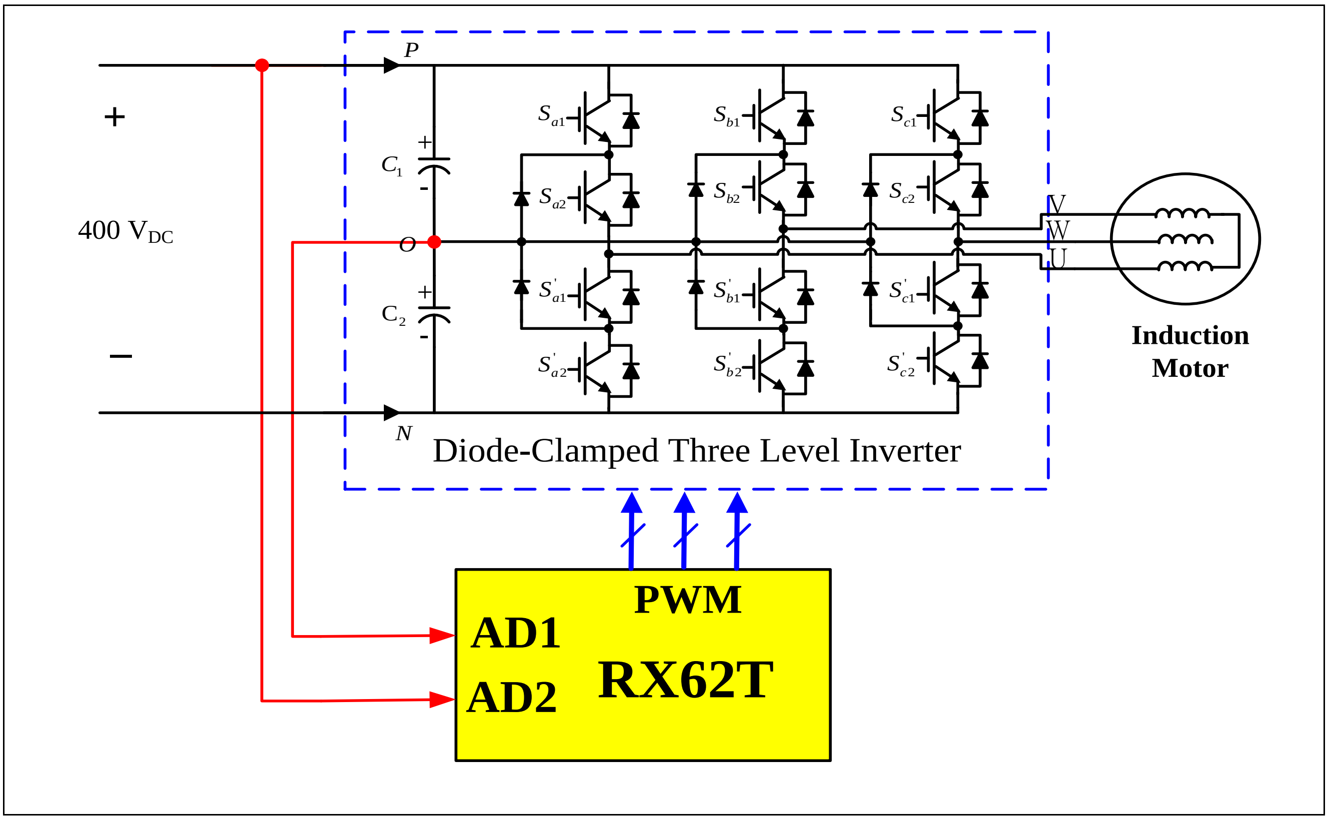


Figure 1 3-level inverter motor control

2. 3-Level Inverter and Space Vector Control

Fig. 2 shows the space vector diagram for three-level inverter control. As shown in Fig. 2, there are 27 switching states which correspond to 19 voltage vectors. Some voltage vectors are with redundant switching states. For example, voltage vector “V1” relates to switching states, “POO” and “ONN”. The inverter output voltages are represented by “P”, “N”, and “O”, respectively as shown in Fig. 3. In Fig. 3, “P” indicates that the output voltage is positive, “N” denotes negative voltage, and “O” represents null voltage. All are referred to the negative DC-link rail. Therefore, “POO” means the switching states for phase “U”, phase ‘V” and phase “W’ are “P”, “O” and “O”, respectively.

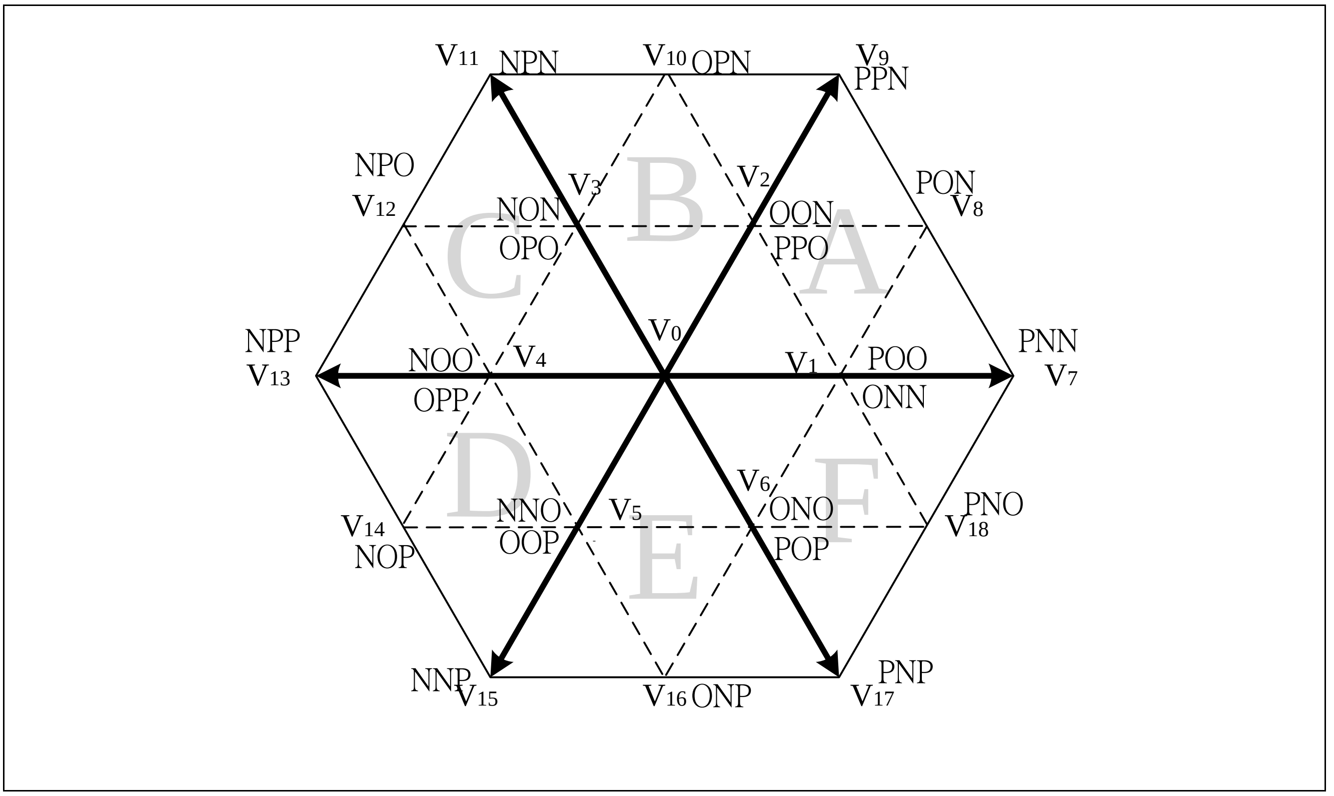


Figure 2 Diagram of voltage vectors for 3-level inverter

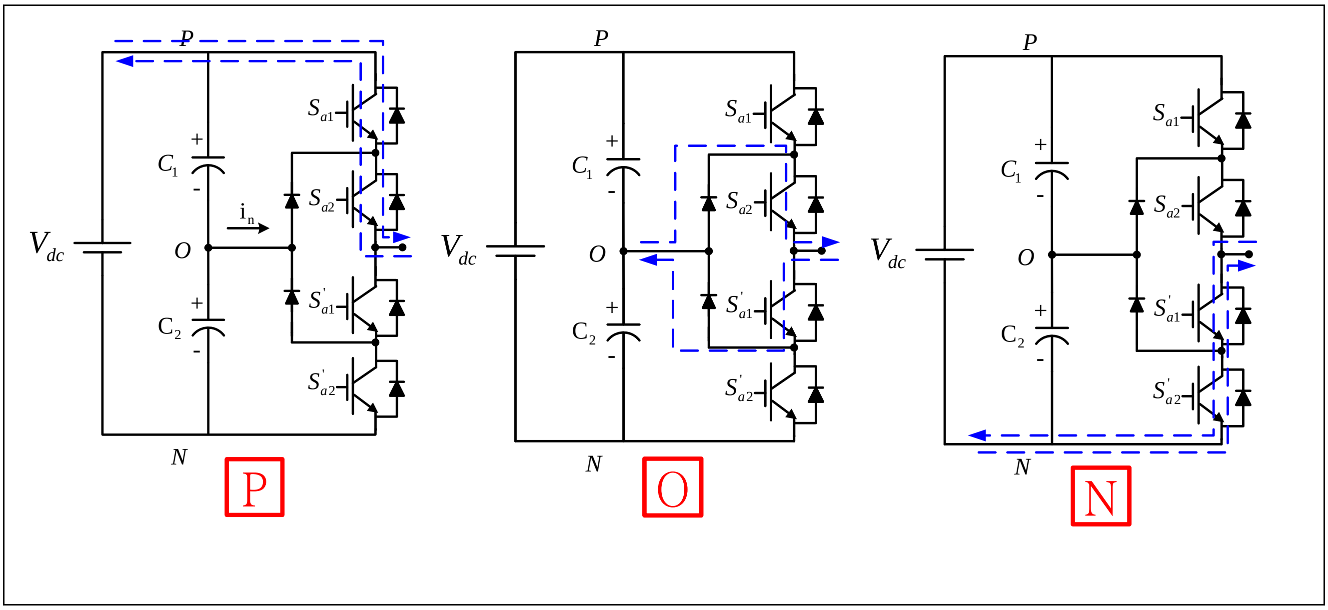


Figure 3 3-level inverter switching states

As shown in Table 1, the 19 switching states corresponding to the 27 voltage vectors can be classified into four groups according to the related output voltage. The first is zero voltage vector, which gives floating phase voltage. The zero voltage vector includes: “PPP”, “OOO”, and “NNN”. The second one is small voltage vectors, including 12 switching states. Six of them will result in the current flowing through the upper capacitor. In contrast, for the other six states, the current goes through the lower capacitor and the load. The third group is the switching states give medium voltage vectors. There are six switching states in this group. And the last group is the switching states which bring big voltage vector to the output. The current will flow through both upper-side and lower-side capacitors and has no effect on the voltage balance for these switching states.

Table 1 Effect of switching states on capacitor voltage

Voltage vector	Current path	Switching states (UVW)
Zero voltage vector	No current	PPP, OOO, NNN
Small voltage vector	Upper capacitor only	POO, PPO, OPO, OPP, OOP, POP
	Lower capacitor only	ONN, OON, NON, NOO, NNO, ONO
Medium voltage vector	—	PON, OPN, NPO, NOP, ONP, PNO
Big voltage vector	both	PNN, PPN, NPN, NPP, NNP, PNP

Fig. 4 illustrates the reference voltage vector in Sextant A as an example. The reference voltage vector, V_{ref}, can be synthesized by the voltage vectors, V_1, V_8, and V_2.

By the vector synthesis principle, the following equation can be derived.

$$\vec{V}_{ref}T_z = \vec{V}_1 T_a + \vec{V}_2 T_c + \vec{V}_8 T_b \tag{1}$$

where

T_z = sampling period

T_a, T_c, T_b = switching times of the switching states related to $\vec{V}_1$, $\vec{V}_2$, and $\vec{V}_8$, respectively

The switching times can therefore be derived by (1) and as follows.

$$T_a = T_z[1 - 2k\sin(\gamma)] \tag{2}$$

$$T_b = T_z[2k\sin(\frac{\pi}{3} + \gamma) - 1] \tag{3}$$

$$T_c = T_z[1 - 2k\sin(\frac{\pi}{3} - \gamma)] \tag{4}$$

where

$$k = \frac{2}{\sqrt{3}}V_{ref}$$

Therefore, for the illustrated reference voltage vector, the sequence of switching states in a switching period, T_s, is shown in Fig. 5. Similar results for the reference voltage vector locates at other sectors can be derived as summarized in Table 2 and the related switching sequence in a switching period are summarized in Table 3 for the reference vectors in Sextant *A* to Sextant *F*. This switching table is stored in the memory and accessed according to the position of reference vector. The related switching times are calculated as shown in Table 2. For a given reference voltage vector, once the switching pattern and switching times can be derived by the memory and calculation, respectively, the inverter devices can be controlled to give the required output voltage and frequency accordingly.

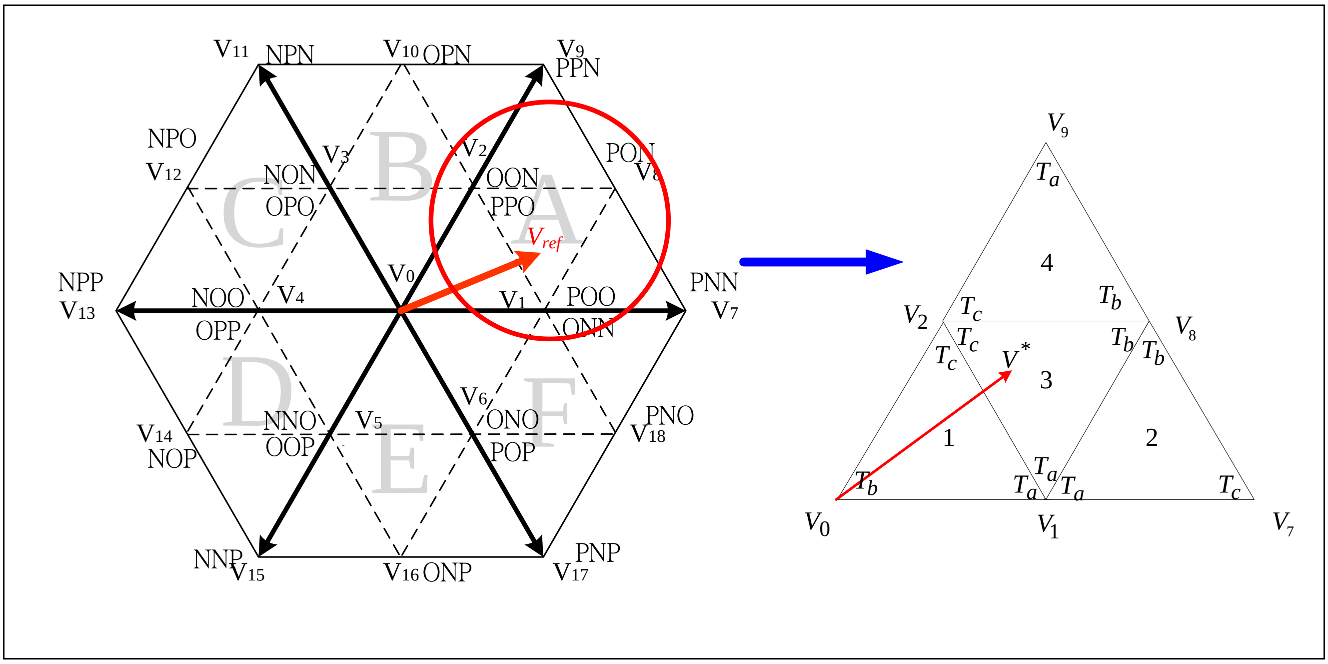


Figure 4 Voltage vector of 3-level inverter in Sextant *A*

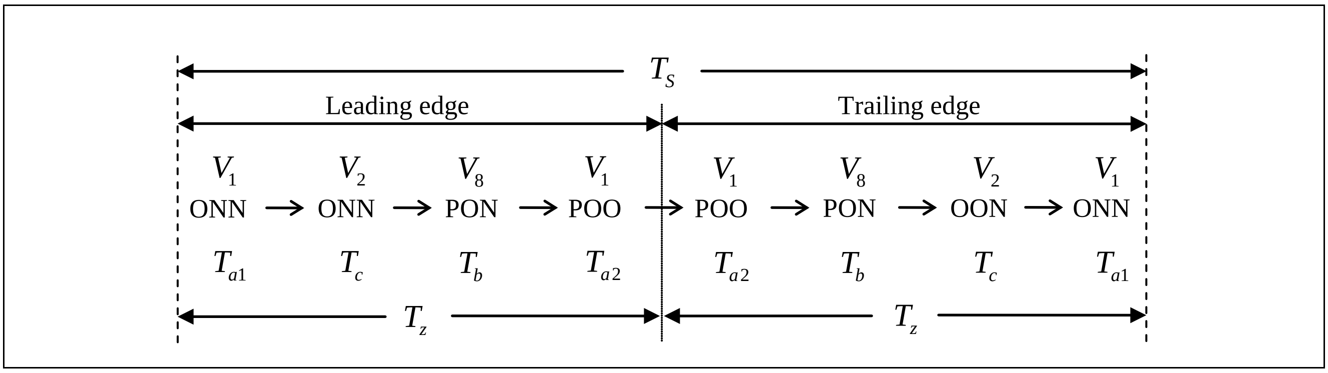


Figure 5 Illustration of sequence of switching states

Table 2 Switching times

Sector	T_a	T_b	T_c
1	$2kT_z\sin\left(\frac{\pi}{3}-\gamma\right)$	$T_z\left[1-2k\sin\left(\frac{\pi}{3}+\gamma\right)\right]$	$2kT_z\sin(\gamma)$
2	$2T_z\left[1-k\sin\left(\frac{\pi}{3}+\gamma\right)\right]$	$2kT_z\sin(\gamma)$	$T_z\left[2k\sin\left(\frac{\pi}{3}-\gamma\right)-1\right]$
3	$T_z\left[1-2k\sin(\gamma)\right]$	$T_z\left[2k\sin\left(\frac{\pi}{3}+\gamma\right)-1\right]$	$T_z\left[1-2k\sin\left(\frac{\pi}{3}-\gamma\right)\right]$
4	$T_z\left[2k\sin(\gamma)-1\right]$	$2kT_z\sin\left(\frac{\pi}{3}-\gamma\right)$	$2T_z\left[1-k\sin\left(\frac{\pi}{3}+\gamma\right)\right]$

Table 3 Sequence of switching states

Sector		A				B			
Subsector		1	2	3	4	1	2	3	4
Phase		UVW	UVW	UVW	UVW	UVW	UVW	UVW	UVW
Switching Sequence	Rising Edge	NNN	ONN	ONN	OON	OOO	NON	NON	OON
		ONN	PNN	OON	PON	OPO	NPN	OON	OPN
		OON	PON	PON	PPN	PPO	OPN	OPN	PPN
		OOO	POO	POO	PPO	PPP	OPO	OPO	PPO
	Falling Edge	OOO	POO	POO	PPO	PPP	OPO	OPO	PPO
		OON	PON	PON	PPN	PPO	OPN	OPN	PPN
		ONN	PNN	OON	PON	OPO	NPN	OON	OPN
		NNN	ONN	ONN	OON	OOO	NON	NON	OON
Sector		C				D			
Subsector		1	2	3	4	1	2	3	4
Phase		UVW	UVW	UVW	UVW	UVW	UVW	UVW	UVW
Switching Sequence	Rising Edge	NNN	NON	NON	NOO	OOO	NNO	NNO	NOO
		NON	NPN	NOO	NPO	OOP	NNP	NOO	NOP
		NOO	NPO	NPO	NPP	OPP	NOP	NOP	NPP
		OOO	OPO	OPO	OPP	PPP	OOP	OOP	OPP
	Falling Edge	OOO	OPO	OPO	OPP	PPP	OOP	OOP	OPP
		NOO	NPO	NPO	NPP	OPP	NOP	NOP	NPP
		NON	NPN	NOO	NPO	OOP	NNP	NOO	NOP
		NNN	NON	NON	NOO	OOO	NNO	NNO	NOO
Sector		E				F			
Subsector		1	2	3	4	1	2	3	4
Phase		UVW	UVW	UVW	UVW	UVW	UVW	UVW	UVW
Switching Sequence	Rising Edge	NNN	NNO	NNO	ONO	OOO	ONN	ONN	ONO
		NNO	NNP	ONO	ONP	POO	PNN	ONO	PNO
		ONO	ONP	ONP	PNP	POP	PNO	PNO	PNP
		OOO	OOP	OOP	POP	PPP	POO	POO	POP
	Falling Edge	OOO	OOP	OOP	POP	PPP	POO	POO	POP
		ONO	ONP	ONP	PNP	POP	PNO	PNO	PNP
		NNO	NNP	ONO	ONP	POO	PNN	ONO	PNO
		NNN	NNO	NNO	ONO	OOO	ONN	ONN	ONO

3 Software Implementation

The flow chart for 3-level inverter control using space vector modulation is shown in Fig. 6. As shown in Fig. 6, the space vector modulation is realized in the Interrupt Service Routine (ISR) which is initiated every sampling period. As the reference voltage vector is derived via the AD converter (ADC), the Sextant, Sector and voltage angle are calculated. Based upon these results, the switching times are calculated. And the switching states (pattern) are retrieved from the memory. The inverter PWM waveform can be generated using the switching times and switching pattern. More details of I/O assignment are summarized in Table 4.

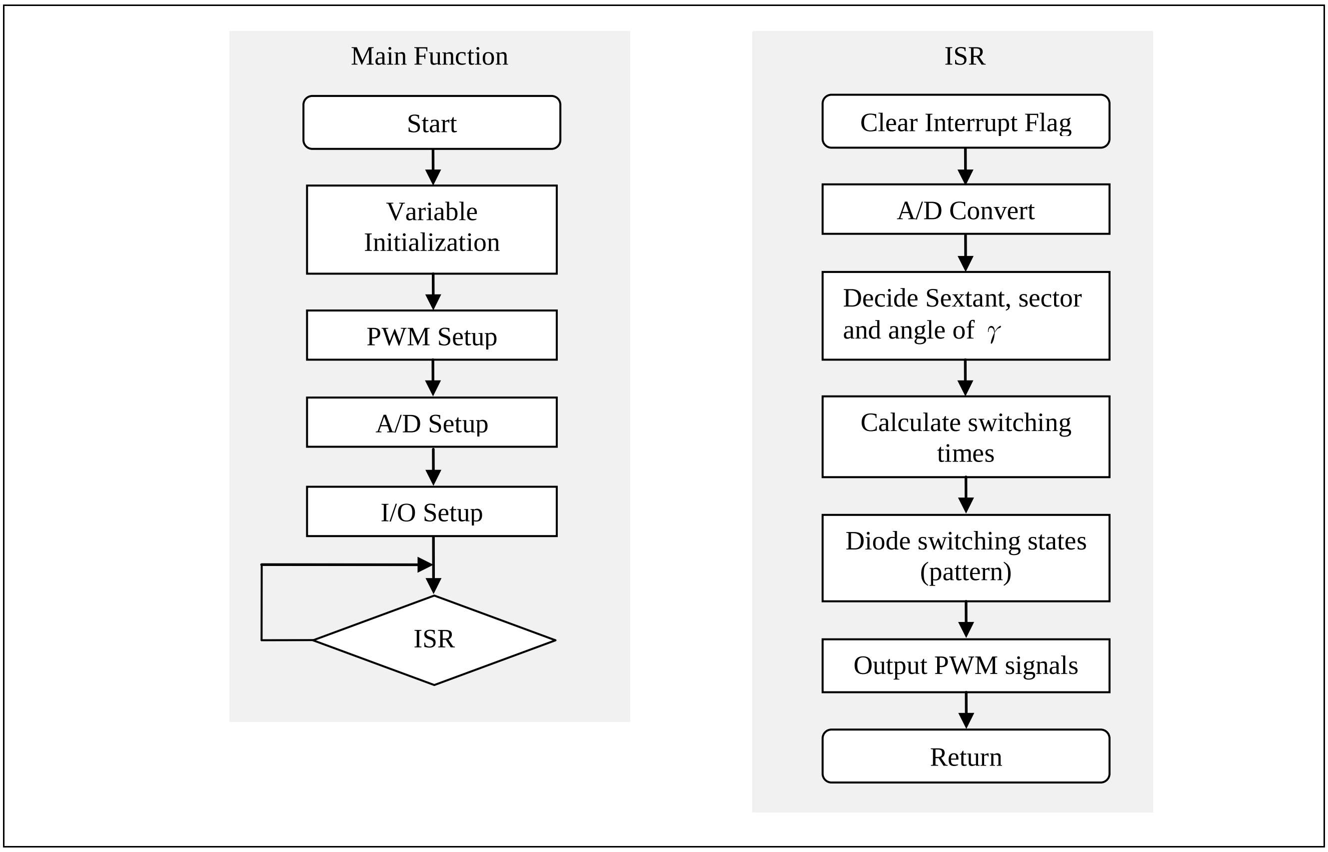


Figure 6 Flow chart of software implementation

Table 4 I/O assignment

PWM Channel	Output Pin	Description
MTU3	MTIOC3B	PWM output pin 1
	MTIOC3D	PWM output pin 1′
MTU6	MTIOC6B	PWM output pin 2
	MTIOC6D	PWM output pin 2′
MTU4	MTIOC4A	PWM output pin 3
	MTIOC4C	PWM output pin 3′
	MTIOC4B	PWM output pin 4
	MTIOC4D	PWM output pin 4′
MTU7	MTIOC7A	PWM output pin 5
	MTIOC7C	PWM output pin 5′
	MTIOC7B	PWM output pin 6
	MTIOC7D	PWM output pin 6′
A/D Channel	**Input Pin**	**Description**
	AN001	A/D Sampling
	AN002	A/D Sampling

4 Experimental Results

Fig. 7 shows the block diagram of the experimental system. An induction motor is used as the load of 3-level inverter. The induction motor is controlled via V/F control to control the speed from 140 to 1400 rpm as specified. Fig. 8 shows the photo of the implemented 3-level inverter. Both RX62 T board and the required auxiliary switching power are integrated with the 3-level inverter as shown in Fig. 8. Fig. 9 shows the measured points for the experimental results. As shown in Fig. 9, the neutral point voltage, line voltage and phase current are measured. Fig. 10 to Fig. 15 shows these measured results as motor speed varies from 10% to 100%, 140 rpm to 1400 rpm. As shown in these results, the motor can be controlled to meet the required specifications. Moreover, the DC-link voltage can be utilized to give a 5-level line voltage when voltage reference increases as shown in see Fig. 15.

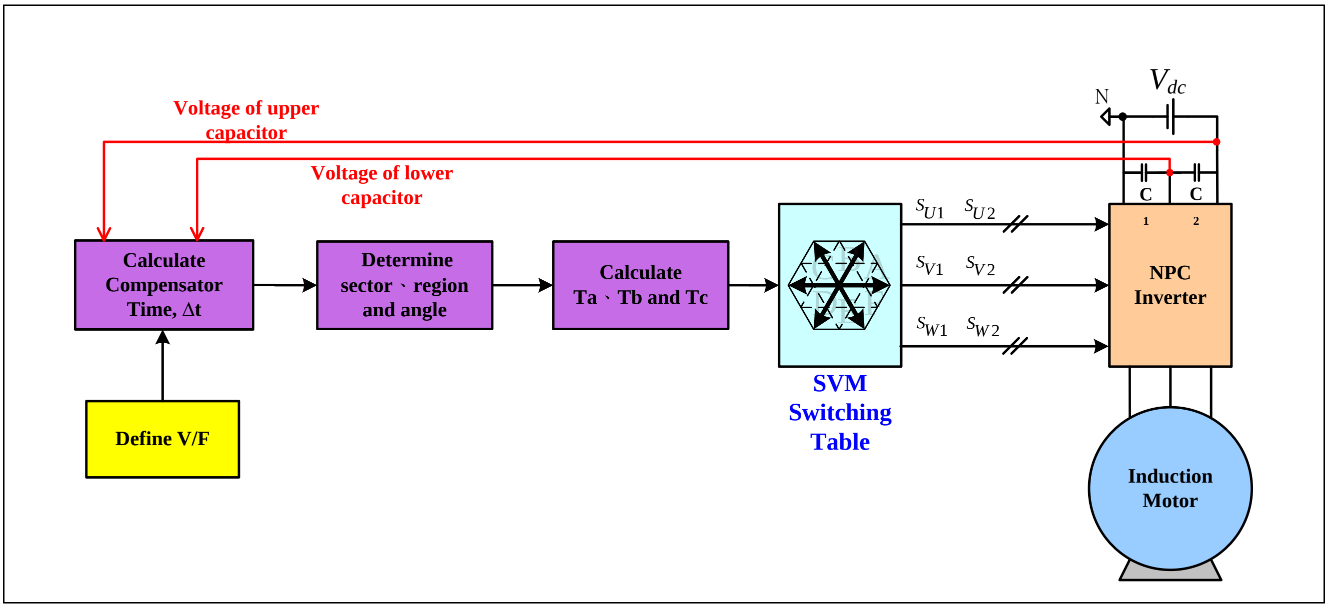


Figure 7 Block diagram of V/F control

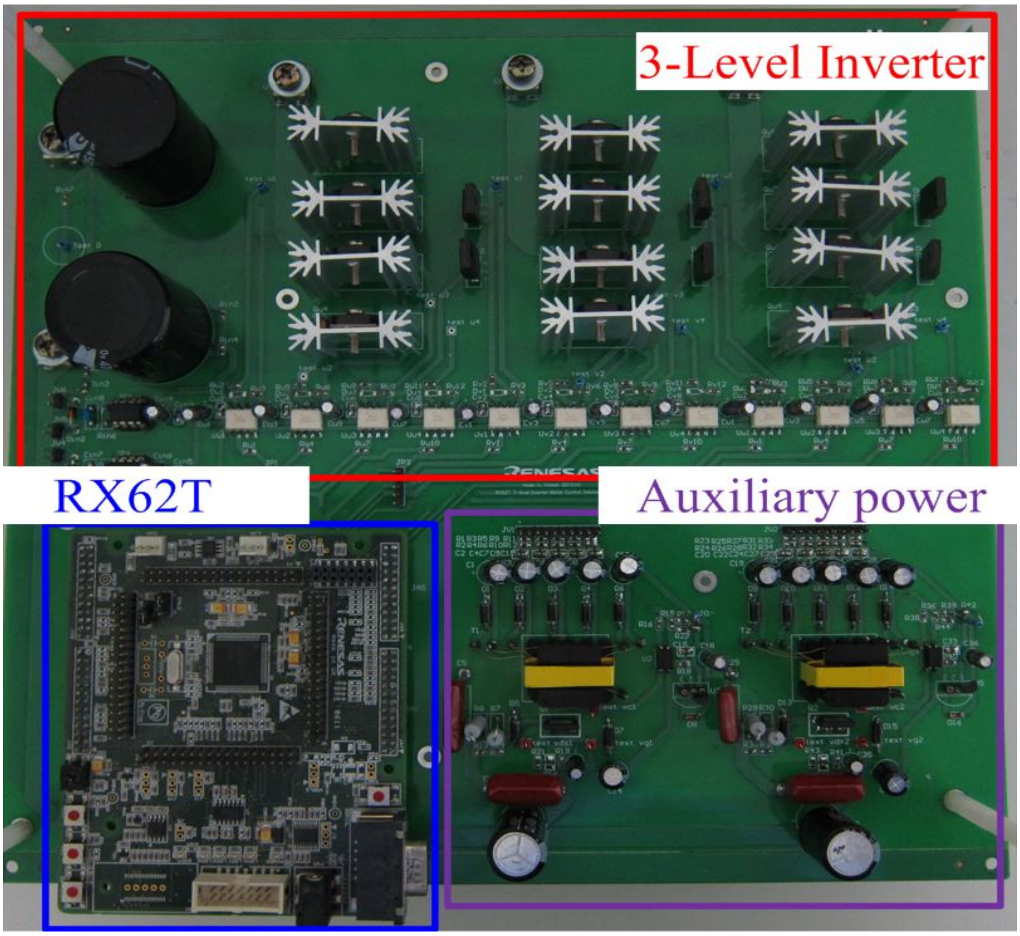


Figure 8 Implemented 3-level inverter

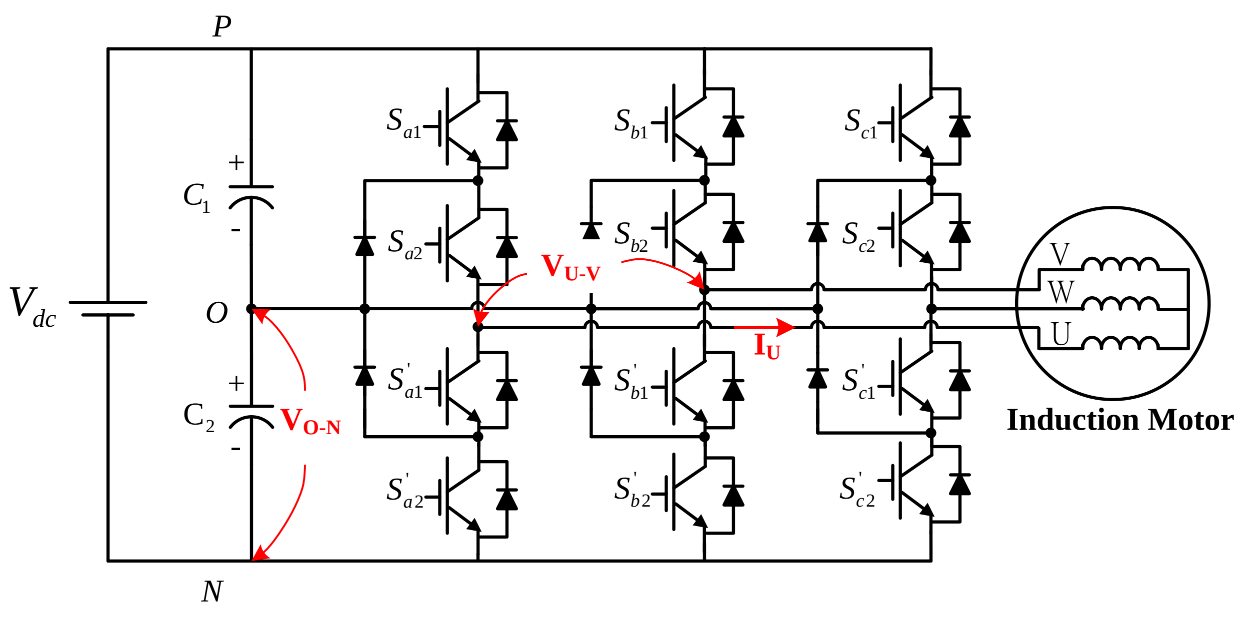
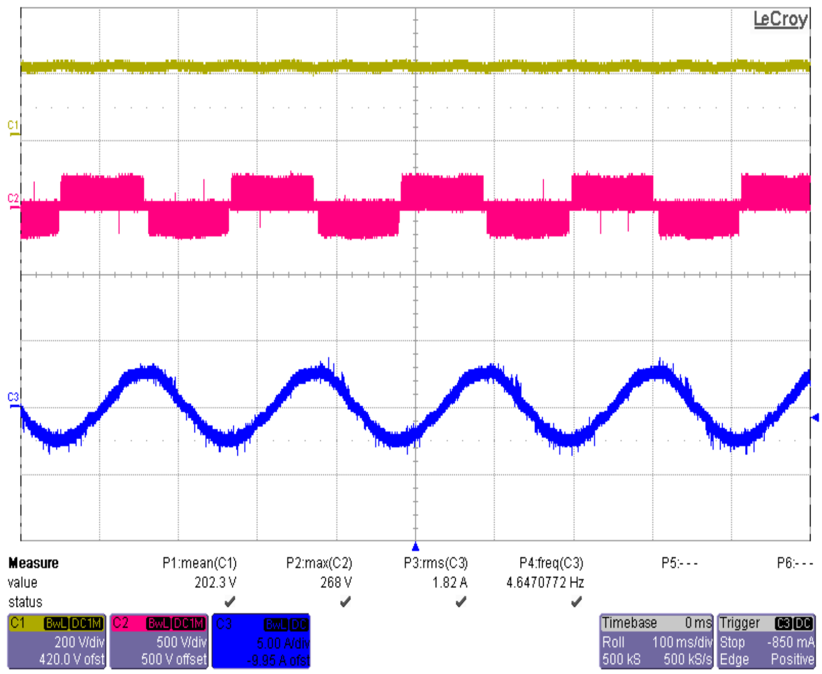
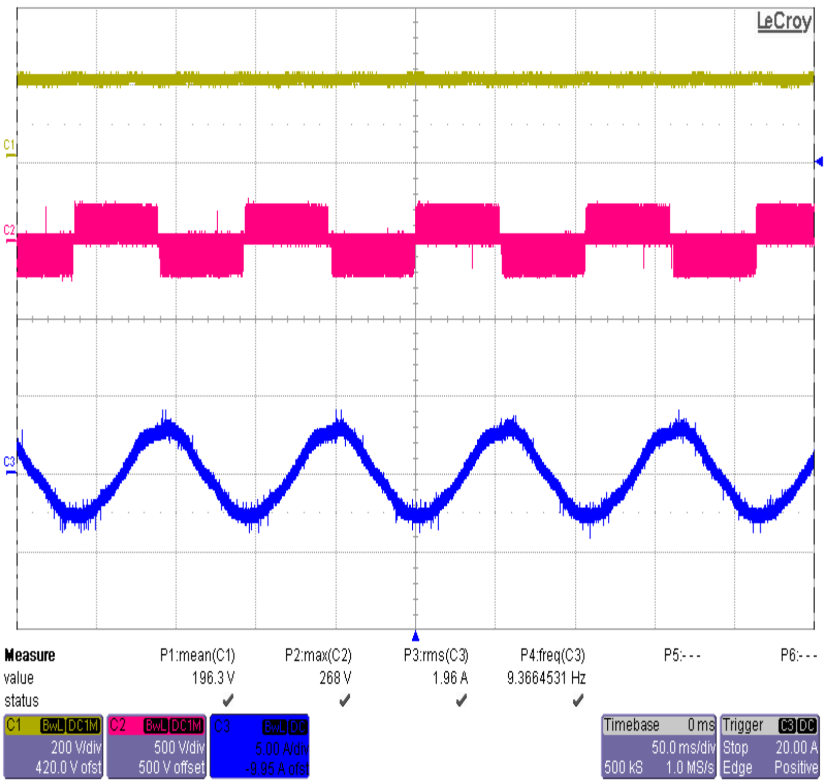


Figure 9 Measurement of 3-level inverter control experimental



- Ch1: natural point voltage
- Ch2: phase U-V voltage
- Ch3: Output voltage of phase U
- 140 rpm

Figure 10 10% of rated speed



- Ch1: natural point voltage
- Ch2: phase U-V voltage
- Ch3: Output voltage of phase U
- 280 rpm

Figure 11 20% of rated speed

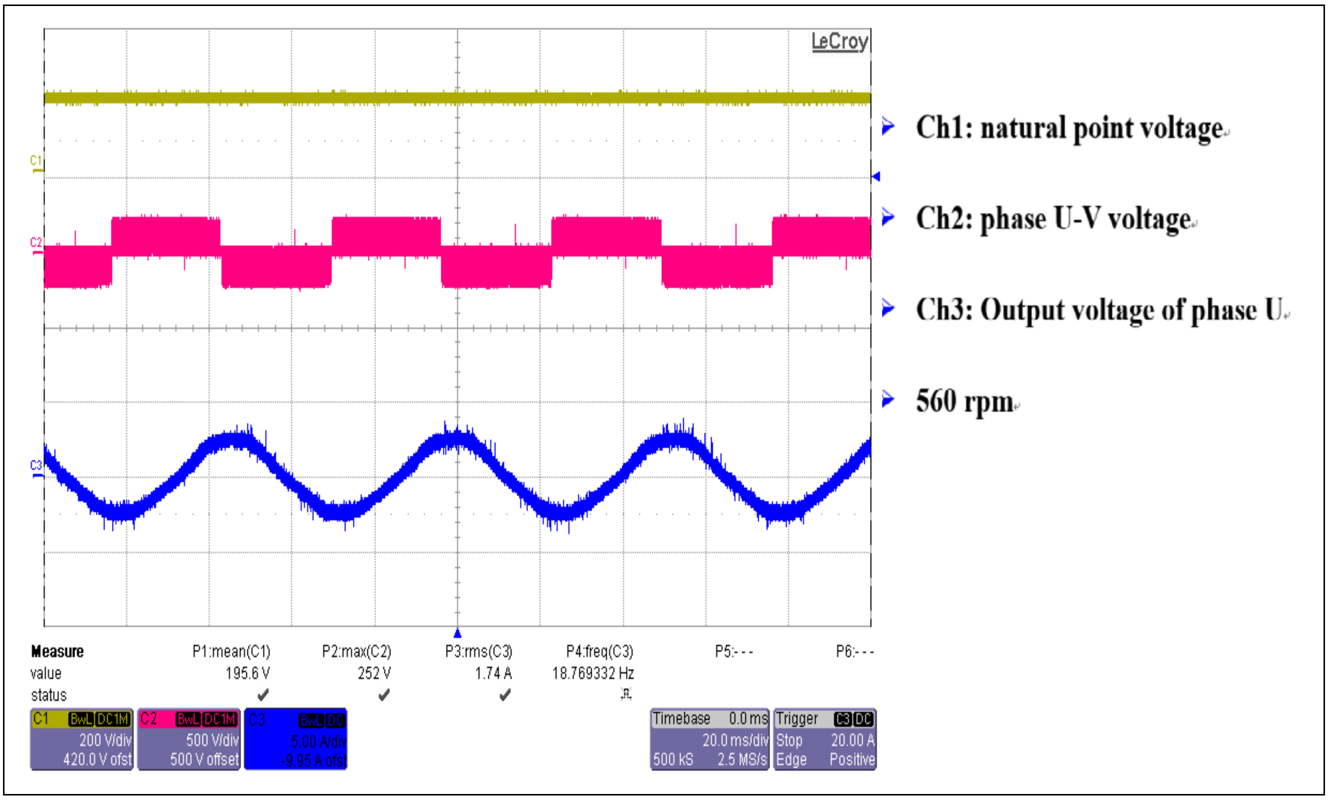


Figure 12 40% of rated speed

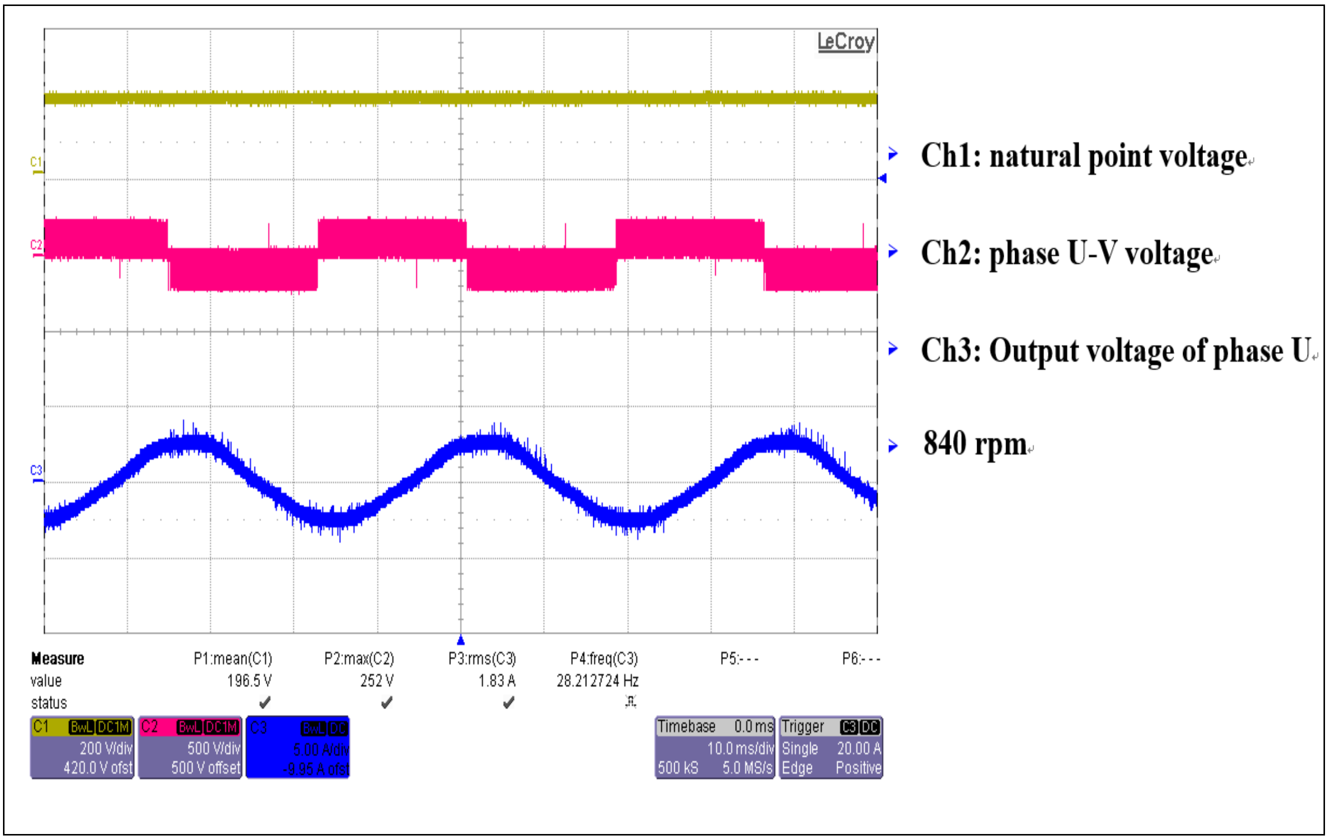


Figure 13 60% of rated speed

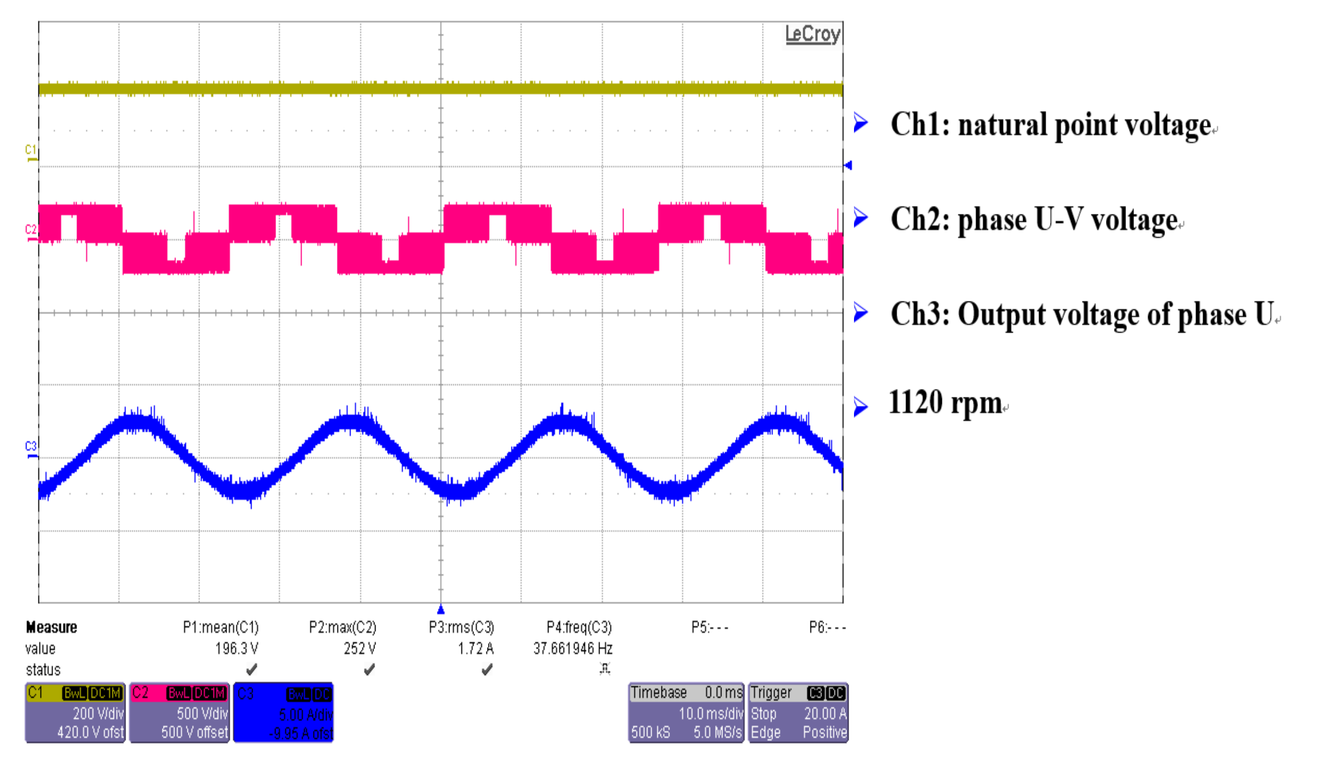


Figure 14 80% of rated speed

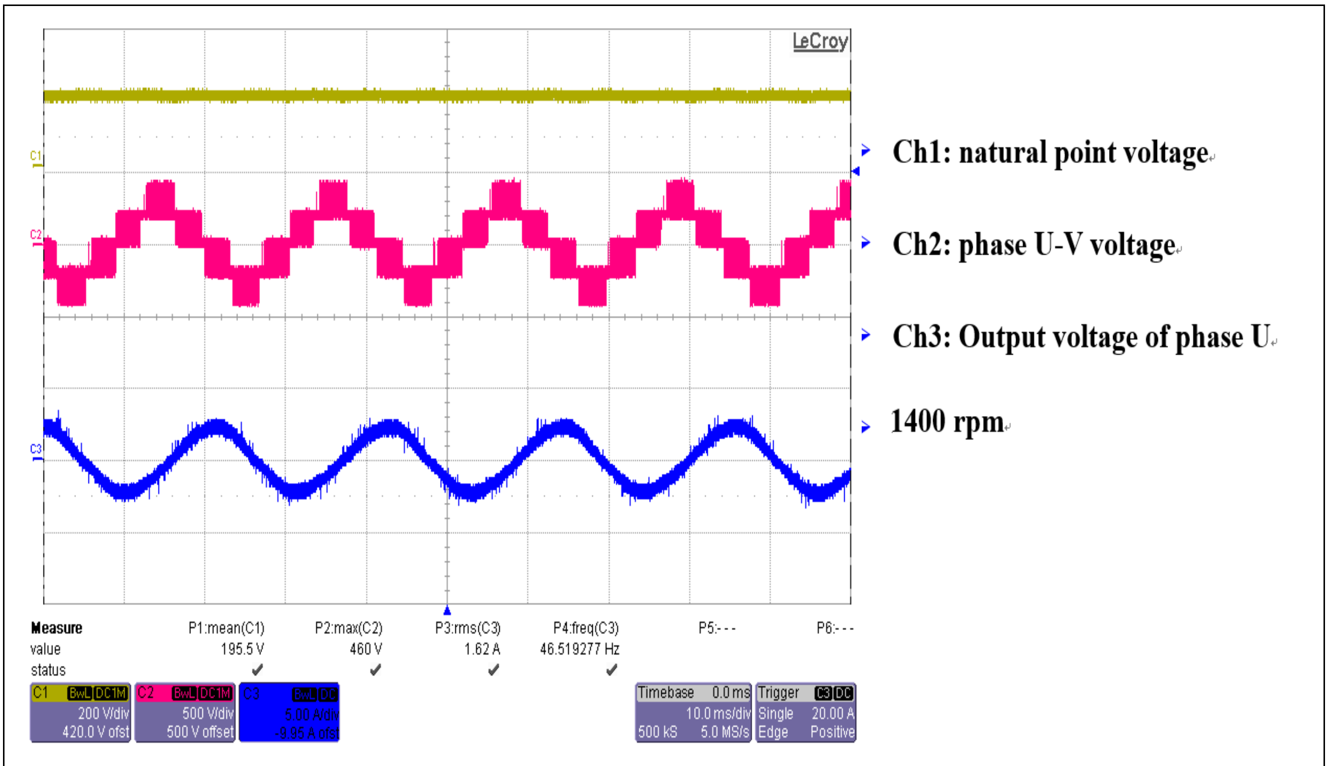


Figure 15 100% of rated speed

5 Conclusion

The purpose of this application note is to demonstrate the application of RX62T to the implementation of 3-level inverter control. The space vector modulation for 3-level inverter and its implementation based upon RX 62T are introduced. Experimental results are presented to fully support the hardware and software design and implementation. For a V/F controlled induction motor drives, smooth speed control from 140 rpm to 1400 rpm (10% to 100%) can be achieved.

6 Reference

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Revision Record

Rev.	Date	Description Page	Summary
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   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
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   The state of the product is undefined at the moment when power is supplied.
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   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
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   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
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   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
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