RX65N Group and RX651 Group

Precautions Regarding High-Temperature Operation of RX65N Group and RX651 Group

Summary

This document explains G version products for high-temperature operation guarantee, including precautions on temperature profiles and derating examples to be considered for reliability design in high-temperature applications.

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1. Relationship between Actual Usage Environment and Reliability of RX Family Products

1.1 Conceptualizing MCU Reliability

When using RX Family MCUs, the following precautions should be observed in order to ensure device reliability.

The reliability of a semiconductor device is expressed as a failure rate curve (bathtub curve). Device failures can be classified into three types: initial failures, which occur comparatively early on after the device enters use (operation); random failures, which occur over a long period of time; and wear-out (life span) failures, which become more frequent over time at the end of the intended lifetime of the device. For details on bathtub curves, refer to Semiconductor Reliability Handbook, rev. 2.50 (R51ZZ0001EJ0250).

Of the above, wear-out failures have a particularly large dependency on the temperature environment in which the semiconductor device is used. To prevent RX MCUs from undergoing wear-out failure, it is important to think about derating.

1.2 Derating

Derating is defined in JIS Z 8115 reducing a load systematically by operating a device under its rated maximum capacity to enhance reliability.

The quality and reliability of a device are greatly influenced by its usage environment. If a device is used under harsh conditions, its reliability decreases, or it increases when used under mild conditions. If a device is used in an extremely harsh usage environment equivalent to life time tests. Even if the maximum ratings are not exceeded, using a device under very harsh conditions equivalent to lifetime testing can cause wear-out failure. Thus, it is very important to think about derating.

Derating is generally applied to devices with wide usage ranges such as discrete parts and power ICs where the junction temperature should be considered even when used within the specified range (e.g. allowable voltage) in order to avoid the heat issue due to the balance between generated power, ambient temperature, and characteristics of heat-sink in use. Also, derating should be considered for devices which require adjustments to keep the balance between ambient temperature, junction temperature, voltage, current, and other mutually-related usage conditions.

For details on derating, refer to 5.2.3, Derating, in Semiconductor Reliability Handbook, rev. 2.50 (R51ZZ0001EJ0250).

This application note presents high-temperature profiles for typical high-temperature applications and derating examples for RX Family MCUs.

2. Definitions of Thermal Characteristics

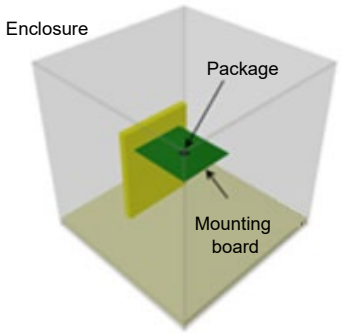
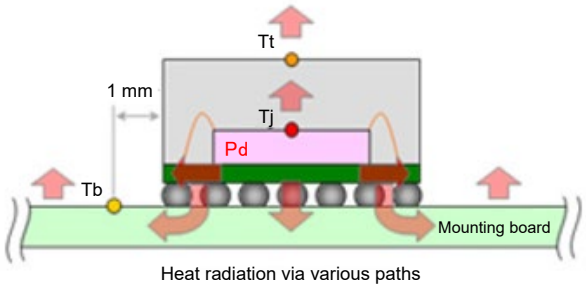
The definitions of thermal characteristics are based on the JEDEC specification referenced below. For details, refer to the following URL:

https://www.renesas.com/us/en/support/technical-resources/packaging/characteristic/heat-dissipation

Table 2.1 ICs: Definitions of Thermal Characteristics

θja	Definition	The thermal resistance between the junction temperature (Tj) and ambient temperature (Ta) when the package is mounted on the board. Two types of environment are considered: one in which only natural convection occurs, and one in which forced air cooling is assumed.
	Application	Comparison of heat radiation performance of different packages
ψjt	Definition	A thermal design parameter that expresses the temperature difference between the junction temperature (Tj) and the temperature at the center of the package top (Tt), relative to the power consumption (Pd) of the device overall.
	Application	Estimation of the junction temperature (Tj), based on ψjt calculated in an appropriate environment, Tt and Pd

Ta: Temperature in location not affected by heat generation source

Thermal Characteristic	**θja**	**ψjt**
Environment		
	• Enclosure: 304.8 × 304.8 × 304.8 mm (JESD51-2 conformant) • Mounting board: BGA 40 mm square or less → 101.6 × 114.3 × t1.6 mm, 4 layers (JESD51-9 conformant) QFP 27 mm square or more → 101.6 × 114.3 × t1.6 mm, 4 layers (JESD51-7 conformant) QFP less than 27 mm square → 76.2 × 114.3 × t1.6 mm, 4 layers (JESD51-7 conformant)	
Definition expression	$\theta ja = \frac{Tj - Ta}{Pd}$	$\psi jt = \frac{Tj - Tt}{Pd}$

3. Thermal Design

Generally speaking, the junction temperature of a semiconductor device affects the lifetime of the device and, if it rises too high, can destroy it. For this reason, system chips with high power consumption have a specified junction temperature (Tj) range, and it is necessary to ensure that the thermal design is such that the junction temperature remains within the allowable range during operation.

If the usage environment is such that the limit of the junction temperature (Tj) allowable range is likely to be approached or exceeded, estimate the junction temperature. Calculate the Tj in your own specific use case to confirm that it is below the maximum allowable junction temperature. If the result exceeds the maximum allowable value, reconsider the component layout, enclosure configuration, and power consumption.

It is not possible to measure the junction temperature (Tj) directly, so it is necessary to calculate it from the power consumption or surface temperature by using the thermal design parameters. This guide presents examples of Tj calculation using two methods.

3.1 Tj Calculation Examples

3.1.1 Precautions When Calculating Tj

θja is calculated in the environment following the JEDEC specifications, so the values may vary greatly according to the layout of the mounting board, enclosure etc. As Tj obtained from θja may deviate from Tj measured in actual usage environment of customers, please confirm Tj by [3.1.2 Calculating Tj from Temperature at Center of Package Top

3.1.2 Calculating Tj from Temperature at Center of Package Top (Tt)

Estimate the temperature at the center of the package top (Tt) and the overall power consumption (Pd) of the chip in your usage environment, and calculate the junction temperature (Tj) using the formula given below.

$Tj = Tt + Pd^{*1} \times \psi jt^{*2}$

Tj: Junction temperature [°C]

Tt: Temperature at center of package top [°C]

Pd: Overall power consumption of chip [W]

ψjt: Thermal design parameter [°C/W] from junction temperature (Tj) to center of package top

Note 1. For Pd, refer to 3.3, Calculating Power Consumption (Pd).

Note 2. For ψjt, refer to 3.2, Thermal Design Parameters.

If the junction temperature (Tj) exceeds 125°C, reconsider the component layout, enclosure configuration, and power consumption, as necessary.

3.1.3 Precautions When Calculating Tt

- Measurement Using a Thermocouple
  To ensure accurate temperature measurements, care should be taken regarding the thermocouple used and the manner in which it is attached to the measurement target.
  Some precautions and suggestions are presented below:
  — Use a thermocouple with wires that are as thin as possible. (Due to limitations on heat extraction, the recommended wire diameter is 150 µm or less.)
  — A K-type thermocouple is recommended. (T-type thermocouples tend to generate a lot of heat, and they may provide artificially low temperature measurements.)
  — Use heat-resistant plastic tape or a heat-resistant plastic material to secure the thermocouple in place.
  — Secure the thermocouple firmly to the measurement target. (Any looseness may result in measurement error.)

- Measurement Point
  Confirm that the temperature is in the saturation state and measure Tt at the center of the top surface of the package.

- Measurement Using a Thermographic Camera
  To ensure accurate temperature measurements, set the emissivity of the measurement target on the thermographic camera. The emissivity of the board surface is typically 0.8 to 0.9, but that of metal surfaces is generally lower. (Performing measurements of a metal surface with a setting of 0.8 to 0.9 will result in a lower measured value than the actual temperature.) If the emissivity is unclear, prepare the surface by applying black body spray or the like. Setting the emissivity to that of the black body spray will enable you to obtain an accurate temperature measurement.
  Note that any objects between the thermographic camera and the measurement target (even a transparent acrylic panel) will prevent you from obtaining accurate measurements. (In this example, the thermographic camera would be measuring the temperature of the transparent acrylic panel.)
  Depending on the layout of the measurement target, measurement using a thermographic camera might be more difficult than measurement using a thermocouple, but it is an effective way to determine the temperature distribution. It is therefore recommended that a thermographic camera and a thermocouple be used in combination.

3.2 Thermal Design Parameters

3.2.1 RX65N Group and RX651 Group Thermal Design Parameters

The thermal design parameters of the RX65N Group and RX651 Group are listed below.

Table 3.1 RX65N Group and RX651 Group Thermal Design Parameters

Package	Mounting Board Layers	θja [°C/W]	ψjt [°C/W]
176-pin LFQFP PLQP0176KB-A	4	48.0	1.0
144-pin LFQFP PLQP0144KA-B	4	50.9	1.5
100-pin LFQFP PLQP0100KB-B	4	52.5	1.5
64-pin LFQFP PLQP0064KB-C	4	53.7	1.5
177-pin TFLGA (PTLG0177KA-A)	4	36.3	0.3
176-pin LFBGA (PLBG0176GA-A)	4	35.4	0.3
145-pin TFLGA (PTLG0145KA-A)	4	34.6	0.4
100-pin TFLGA (PTLG0100JA-A)	4	34.1	0.4
64-pin TFBGA (PTBG0064KB-A)	4	35.3	0.5

Note: The above values were calculated using the measurement environment specified in the EIA/JEDEC standard. For details of the standard, refer to EIA/JEDEC Standard (LFQFP is based on JESD 51-2 and JESD 51-7, TFLGA/LFBGA/TFBGA are based JESD51-2 and JESD51-9).

3.3 Calculating Power Consumption (Pd)

Use the following formula to calculate the power consumption (Pd):

Power consumption = voltage × current + Σ{(VOL × IOL)} + Σ{(VCC − VOH) × | − IOH |} —— (1)

Figure 3.1 is a configuration diagram showing the current paths. Both DC and AC current are used, and they are calculated using the following formulas:

DC current = leak current + analog current —— (2)

AC current = logic current + ΣIO_AC current —— (3)

The ΣIO_AC current is calculated from the number of and capacitance of the I/O lines (input pin capacitance*1, external load capacitance), and the pin switching frequency, using the following formula:

ΣIO_AC current = Σ (input pin capacitance + external load capacitance) × switching frequency × VCC —— (4)

Note 1. For the input pin capacitance (Cin), refer to 60, Electric Characteristics, in the hardware manual of the MCU.

Calculate the leak current, analog current, and logic current from the data listed in Table 3.2, Classification of RX65N Group and RX651 Group Current Consumption. The logic current is an AC current, so multiply the unitary current (mA/MHz) by the operating frequency (MHz).

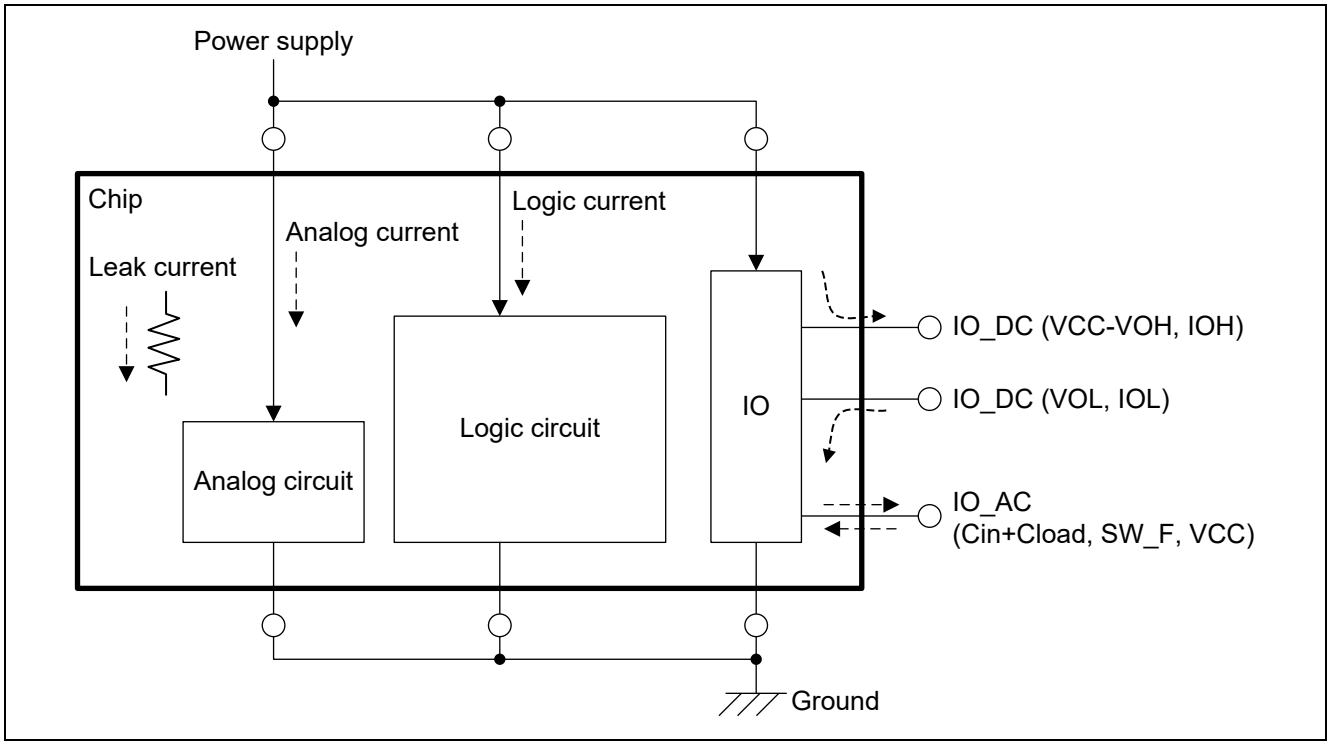


Figure 3.1 Current Path Configuration Diagram

Table 3.2 Classification of RX65N Group and RX651 Group Current Consumption

No.	Type	Category	Subcategory	Item	Frequency [MHz]	Unitary Current [mA/MHz]*2	Max. Current [mA]*1	Remarks
1	DC	Leak	Products with 1 Mbyte of code flash memory or less		—	—	9.00	
2			Products with at least 1.5 Mbytes of code flash memory		—	—	20.00	
3		Analog	USBb		—	—	10.00	
4			S12ADFa (unit0 + channel-specific S/H)		—	—	2.56	
5			S12ADFa (unit1 + temperature sensor)		—	—	1.10	
6			R12DAa		—	—	2.20	
7	AC	Logic	CPU	CoreMark operation	120	0.150	18.00	ROM 1MB or less
						0.155	18.60	ROM 1.5MB or more
8			Peripheral IP modules	DMACAa / DTCb		0.013	1.56	ROM 1MB or less
						0.018	2.16	ROM 1.5MB or more
9				MTU3a		0.018	2.16	
10				ETHERC (EDMACa included)		0.015	1.80	
11				SCIi		0.006	0.72	Value for 1ch*3
12				RSPIc		0.002	0.24	Value for 1ch*3
13				AESa		0.011	1.32	
14				GLCDC		0.065	7.80	
15				DRW2D		0.080	9.60	
16				Trusted Secure IP	60	0.200	12.00	
17				EXDMACa		0.002	0.12	
18				TPUa		0.003	0.18	
19				RTCd, WDTA, IWDTa		0.002	0.12	Value for 1unit*4
20				CMT, CMTW, TMR		0.003	0.18	Value for 1unit*4
21				POE3a, PPG		0.002	0.12	Value for 1unit*4
22				USBb		0.009	0.54	
23				SCIg		0.003	0.18	Value for 1ch*3
24				SCIh		0.003	0.18	
25				RIICa		0.002	0.12	Value for 1ch*3
26				CAN		0.004	0.24	Value for 1ch*3
27				QSPI		0.003	0.18	
28				SDHI		0.009	0.54	
29				SDSI		0.009	0.54	
30				MMCIF		0.010	0.60	
31				PDC		0.002	0.12	
32				S12ADFa, TEMPS		0.004	0.24	Value for 1unit*4
33				R12DAa		0.002	0.12	
34				DOC		0.002	0.12	
35				CRCA		0.002	0.12	
36				CAC		0.002	0.12	
37				ELC		0.002	0.12	
38				RNG		0.002	0.12	

Note 1. Worst conditions (VCC = 3.6 V, Tj = 125°C).

Note 2. The unitary current related to AC is not dependent on the VCC value.

Note 3. Accumulate the current values for the number of units or channels used.

Note 4. Accumulate the current value for the number of units for each module used.

4. Derating Examples for Typical High-Temperature Applications

Table 4.1 lists high-temperature profiles for high-temperature applications assumed to be typical for RX65N and RX651 Group MCUs as well as recommended high-temperature profiles for derating. This recommendation profiles are estimated from Renesas quality test results.

For product numbers of specific target MCUs, refer to Table 4.2, Target Product Numbers (RX65N Group and RX651 Group).

In the derating examples 10 years of operation is assumed, except for example 5.

Choose the example that best approximates your usage conditions. If none of the examples provided is applicable, please contact Renesas individually.

Table 4.1 Typical High-Temperature Applications

Example	Application	Anticipated High-Temperature Profile	Recommended High-Temperature Profile for Derating
1	Cooking devices (cooktops, IH cookers, etc.)	Operating time in high-temperature environment of 3 hours/day In standby or stopped state at other times	−40°C ≤ Tj ≤ 125°C, 3 hours/day. In standby or stopped state at −40°C ≤ Tj ≤ 90°C at other times
2	Household appliance motors, power tools, etc.	Used in high-temperature environment for 6 hours/day In standby or stopped state at other times	115°C < Tj ≤ 125°C, 3 hours/day. −40°C ≤ Tj ≤ 115°C, 3 hours/day In standby or stopped state at −40°C ≤ Tj ≤ 90°C at other times
3	EV chargers, etc.	Used in high-temperature environment for 8 hours/day In standby or stopped state at other times	115°C < Tj ≤ 125°C, 4 hours/day. −40°C ≤ Tj ≤ 115°C, 4 hours/day In standby or stopped state at −40°C ≤ Tj ≤ 85°C at other times
4	Smart meters, power controllers, etc., equipment installed out of doors, etc. (24-hour operation)	Used in high-temperature environment for 8 hours/day Also operating at other times	115°C < Tj ≤ 125°C, 4 hours/day. −40°C ≤ Tj ≤ 115°C, 4 hours/day −40°C ≤ Tj ≤ 100°C at other times
5	PC server power supplies, etc. (24-hour operation)	In continuous use for 5 years in environment that includes high temperatures	115°C < Tj ≤ 125°C, 15,000 hours −40°C ≤ Tj ≤ 115°C, 30,000 hours In continuous use for 5 years
6	Industrial motors (24-hour operation: example 1)	In continuous use in high-temperature environment	102°C < Tj ≤ 112°C, 80% −40°C ≤ Tj ≤ 102°C, 20%
7	Industrial motors (24-hour operation: example 2)	In continuous use in environment that includes very high temperatures	110°C < Tj ≤ 125°C, 5% 105°C < Tj ≤ 110°C, 75% −40°C ≤ Tj ≤ 105°C, 20%
8	Industrial motors (24-hour operation: example 3)	In continuous use in high-temperature environment	Tj ≤ 110°C, 100%

Note: The ambient temperature (Ta) should be between −40°C and 105°C.

Table 4.2 Target Product Numbers (RX65N Group and RX651 Group)

Target Product Numbers	Package	Target Product Numbers	Package
R5F5651EDGFM	LFQFP64	R5F565NEDGFB	LFQFP144
R5F5651EHGFM		R5F565NEHGFB	
R5F5651CDGFM		R5F565NCDGFB	
R5F5651CHGFM		R5F565NCHGFB	
R5F56519BGFM		R5F565N9AGFB	
R5F56519FGFM		R5F565N9BGFB	
R5F56517BGFM		R5F565N9EGFB	
R5F56517FGFM		R5F565N9FGFB	
R5F56514BGFM		R5F565N7AGFB	
R5F56514FGFM		R5F565N7BGFB	
R5F565NEDGFP	LFQFP100	R5F565N7EGFB	
R5F565NEHGFP		R5F565N7FGFB	
R5F565NCDGFP		R5F565N4AGFB	
R5F565NCHGFP		R5F565N4BGFB	
R5F565N9AGFP		R5F565N4EGFB	
R5F565N9BGFP		R5F565N4FGFB	
R5F565N9EGFP		R5F5651EDGFB	
R5F565N9FGFP		R5F5651EHGFB	
R5F565N7AGFP		R5F5651CDGFB	
R5F565N7BGFP		R5F5651CHGFB	
R5F565N7EGFP		R5F56519AGFB	
R5F565N7FGFP		R5F56519BGFB	
R5F565N4AGFP		R5F56519EGFB	
R5F565N4BGFP		R5F56519FGFB	
R5F565N4EGFP		R5F56517AGFB	
R5F565N4FGFP		R5F56517BGFB	
R5F5651EDGFP		R5F56517EGFB	
R5F5651EHGFP		R5F56517FGFB	
R5F5651CDGFP		R5F56514AGFB	
R5F5651CHGFP		R5F56514BGFB	
R5F56519AGFP		R5F56514EGFB	
R5F56519BGFP		R5F56514FGFB	
R5F56519EGFP		R5F565NEDGFC	LFQFP176
R5F56519FGFP		R5F565NEHGFC	
R5F56517AGFP		R5F565NCDGFC	
R5F56517BGFP		R5F565NCHGFC	
R5F56517EGFP		R5F5651EDGFC	
R5F56517FGFP		R5F5651EHGFC	
R5F56514AGFP		R5F5651CDGFC	
R5F56514BGFP		R5F5651CHGFC	
R5F56514EGFP			
R5F56514FGFP			

Table 4.3 Target Product Numbers (RX65N Group and RX651 Group)

Target Product Numbers	Package	Target Product Numbers	Package
R5F5651EDGBP	TFBGA64	R5F5651EDGLK	TFLGA145
R5F5651EHGBP		R5F5651EHGLK	
R5F5651CDGBP		R5F565NEDGLK	
R5F5651CHGBP		R5F565NEHGLK	
R5F56519BGBP		R5F5651CDGLK	
R5F56519FGBP		R5F5651CHGLK	
R5F56517BGBP		R5F565NCDGLK	
R5F56517FGBP		R5F565NCHGLK	
R5F56514BGBP		R5F56519AGLK	
R5F56514FGBP		R5F56519BGLK	
R5F5651EDGLJ	TFLGA100	R5F56519EGLK	
R5F5651EHGLJ		R5F56519FGLK	
R5F565NEDGLJ		R5F565N9AGLK	
R5F565NEHGLJ		R5F565N9BGLK	
R5F5651CDGLJ		R5F565N9EGLK	
R5F5651CHGLJ		R5F565N9FGLK	
R5F565NCDGLJ		R5F56517AGLK	
R5F565NCHGLJ		R5F56517BGLK	
R5F56519AGLJ		R5F56517EGLK	
R5F56519BGLJ		R5F56517FGLK	
R5F56519EGLJ		R5F565N7AGLK	
R5F56519FGLJ		R5F565N7BGLK	
R5F565N9AGLJ		R5F565N7EGLK	
R5F565N9BGLJ		R5F565N7FGLK	
R5F565N9EGLJ		R5F56514AGLK	
R5F565N9FGLJ		R5F56514BGLK	
R5F56517AGLJ		R5F56514EGLK	
R5F56517BGLJ		R5F56514FGLK	
R5F56517EGLJ		R5F565N4AGLK	
R5F56517FGLJ		R5F565N4BGLK	
R5F565N7AGLJ		R5F565N4EGLK	
R5F565N7BGLJ		R5F565N4FGLK	
R5F565N7EGLJ		R5F5651EDGBG	LFBGA176
R5F565N7FGLJ		R5F5651EHGBG	
R5F56514AGLJ		R5F565NEDGBG	
R5F56514BGLJ		R5F565NEHGBG	
R5F56514EGLJ		R5F5651CDGBG	
R5F56514FGLJ		R5F5651CHGBG	
R5F565N4AGLJ		R5F565NCDGBG	
R5F565N4BGLJ		R5F565NCHGBG	
R5F565N4EGLJ		R5F5651EDGLC	TFLGA177
R5F565N4FGLJ		R5F5651EHGLC	
		R5F565NEDGLC	
		R5F565NEHGLC	
		R5F5651CDGLC	
		R5F5651CHGLC	
		R5F565NCDGLC	
		R5F565NCHGLC	

5. Reference Document

Semiconductor Reliability Handbook Rev. 2.50 (R51ZZ0001EJ0250) January, 2017

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Oct 02, 2017	—	First edition issued.
2.00	Jun 24, 2019	P10 P11	Clerical corrections of Table 4.1 Added LFQFP64、deleted calculating Tj from θja
3.00	Oct 06, 2020	P6,P11 P9	Added TFLGA100,145,177/LFBGA176/TFBGA64 Added example 8 of high-temperature profiles
4.00	Sep 2, 2024	P3 P8	Update URL of reference site [Table 3.2 Classification of RX65N/RX651 Group Current Consumption] modified.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
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