RX74M/RX74N Group, RX72M/RX72N Group

Differences Between the RX74M/RX74N Group and the RX72M/RX72N Group

Introduction

This application note is intended as a source for reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX74M/RX74N and RX72M/RX72N Groups, as well as a guide to key points to consider when replacing MCUs.

Unless specifically otherwise noted, the information in this application note applies to the 320-pin package versions of the RX74M and RX74N Groups and the 224-pin package versions of the RX72M and RX72N Groups, which are the respective maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware for the relevant products.

Target Devices

RX74M Group, RX74N Group, RX72M Group, RX72N Group

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1. Comparison of Built-In Functions of RX72M/RX72N Group and RX74M/RX74N Group

A comparison of the built-in functions of the RX74M/RX74N Group and RX72M/RX72N Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is Comparison of Built-In Functions of RX72M, RX72N, RX74M, and RX74N.

Table 1.1 Comparison of Built-In Functions of RX72M, RX72N, RX74M, and RX74N

Function	RX72M	RX72N	RX74M	RX74N
CPU	●/▲			
Operating modes	●/▲/■			
Address space	●/■			
Resets	●/▲/■			
Option-setting memory (OFSM)	●/■			
Voltage detection circuit (LVDA): RX72M/RX72N, Programmable voltage detection circuit (PVD): RX74M/RX74N	●/▲			
Clock generation circuit	●/▲/■			
Clock frequency accuracy measurement circuit (CAC)	●/■			
Low power consumption	●/▲/■			
Battery backup function (VBATTB): RX74M/RX74N	●			
Register write protection function	●/▲/■			
Exception handling	●			
Interrupt controller (ICUD): RX72M/RX72N, (ICUM): RX74M/RX74N	●/▲/■			
Buses	●/■			
Memory-protection unit (MPU)	●/▲			
DMA controller (DMACAa)	●/▲			
EXDMA controller (EXDMACa): RX72M/RX72N, (EXDMACAa): RX74M/RX74N	●/▲			
Data transfer controller (DTCb): RX72M/RX72N, (DTCA): RX74M/RX74N	▲			
Event link controller (ELC)	●/▲/■			
I/O ports	●/▲/■			
Software configurable 32-bit programmable I/O port (PIO)	×		○	
Multi-function pin controller (MPC)	○		×	
Multi-function timer pulse unit (MTU3a)	○		×	
Port output enable 3 (POE3a)	○		×	
General PWM timer (GPTW)	●/▲			
High resolution PWM waveform generation circuit (HRPWMb)	×		○	
GPTW port output enable (POEG): RX72M/RX72N, (POEGd): RX74M/RX74N	●/▲			
16-bit timer pulse unit (TPUa)	○		×	
Programmable pulse generator (PPG)	○		×	
8-bit timer (TMRb): RX72M/RX72N, (TMRa): RX74M/RX74N	●/■			
Compare match timer (CMT)	●			
Compare match timer W (CMTW)	●			
Realtime clock (RTCd): RX72M/RX72N, (RTCBb): RX74M/RX74N	●/▲/■			
Watchdog timer (WDTA)	●			

Function	RX72M	RX72N	RX74M	RX74N
Independent watchdog timer (IWDTa)	●/▲			
Ethernet controller (ETHERC)	○		×	
PTP module for the Ethernet controller (EPTPCb)	○		×	
DMA controller for the Ethernet controller (EDMACa)	○		×	
PHY management interface (PMGI)	○		×	
Ethernet module (ESWM)	×		○	
Message forwarding engine (MFWD)	×		○	
Common agent (COMA)	×		○	
Ethernet agent (ETHA)	×		○	
Ethernet MAC (RMAC)	×		○	
Gateway CPU agent (GWCA)	×		○	
Generic PTP timer (GPTP)	×		○	
EtherCAT slave controller (ESC)	●	×	●	×
USB 2.0 full-speed host/function module (USBb): RX72M/RX72N, (USBf): RX74M/RX74N	▲/■			
USB 2.0 high-speed host/function module (USBHS)	×		○	
Serial communications interface (SCIj, SCIi, SCIh): RX72M/RX72N, (RSCI): RX74M/RX74N	●/▲/■			
I²C bus interface (RIICa): RX72M/RX72N, I3C bus interface (RI3C)/High-speed I²C-bus interface (RIICHS): RX74M/RX74N	●/▲/■			
CAN module (CAN): RX72M/RX72N, CAN FD module/CAN FD module with gateway functionality (CANFD, CANFDG): RX74M/RX74N	●/▲/■			
Serial peripheral interface (RSPIc): RX72M/RX72N, (RSPIA): RX74M/RX74N)	●/▲/■			
Quad serial peripheral interface (QSPI)	○		×	
Expanded serial peripheral interface (XSPI)	×		○	
Decryption on the fly (DOTF)	×		○	
CRC calculator (CRCA)	●			
Serial sound interface (SSIE)	●/▲			
SD host interface (SDHI): RX72M/RX72N, SD host/MMC host interface (SDHIc): RX74M/RX74N	●/▲			
MultiMediaCard interface (MMCIF)	○		×	
Parallel data capture unit (PDC)	▲			
Graphic-LCD controller (GLCDC)	○		×	
2D drawing engine (DRW2D)	○		×	
Boundary scan	▲			
Arithmetic unit for trigonometric functions (TFUv1): RX72M/RX72N, (TFUv2): RX74M/RX74N	●/▲			
Trusted secure IP (TSIP)	○		×	
Security functions	×		○	
Renesas secure IP (RSIP-E50D)	×		○	
Pulse-density modulation interface (PDMIF)	×		○	
Delta-sigma modulator interface (DSMIF): RX72M/RX72N, (DSMIFA): RX74M/RX74N	●/▲	×	●/▲	×
Phase-counting interface (PCIF)	×		○	
12-bit A/D converter (S12ADFa)	○		×	
16-bit A/D converter (ADC16H)	×		○	

Function	RX72M	RX72N	RX74M	RX74N
12-bit D/A converter (R12DAa): RX72M/RX72N, (R12DAB): RX74M/RX74N	●/▲/■			
Temperature sensor (TEMPS)	▲			
Data operation circuit (DOC): RX72M/RX72N, (DOCA): RX74M/RX74N	●/▲/■			
RAM: RX72M/RX72N SRAM and LRAM: RX74M/RX74N	●/▲/■			
Standby RAM	○		×	
Flash memory (FLASH): RX72M/RX72N, MRAM (MRAM): RX74M/RX74N	●/▲/■			
Internal voltage regulator	×		○	
Packages	●/▲/■			

○: Available, ×: Unavailable, ●: Differs due to added functionality, ▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Register specification items that have no differences between the groups are not indicated.

2.1 CPU

Table 2.1 is Comparative Overview of CPUs, and Table 2.2 is Comparison of CPU Registers.

Table 2.1 Comparative Overview of CPUs

Item	RX72M/RX72N	RX74M/RX74N
CPU	• Maximum operating frequency: 240 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • 113 instructions Standard provided instructions: 111 Basic instructions: 77 Single-precision floating-point operation instructions: 11 DSP instructions: 23 Instructions for register bank save function: 2 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Instruction cache: 8 Kbytes • Data cache: 16 bytes	• Maximum operating frequency: 600 MHz • 32-bit RX CPU (RXv3e) • Minimum instruction execution time: One clock cycle • Address space: 4 GB, linear • Protect Zone: Three “worlds” (Non-secure, Secure, and Root) • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Fifteen 32-bit registers — Accumulator: Two 72-bit registers • 117 instructions Instructions installed as standard: 111 Basic instructions: 77 Single-precision floating point instructions: 11 DSP instructions: 23 Instructions for register bank save function: 2 Protect Zone instructions: 4 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian and big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Instruction cache: 32 Kbytes • Data cache: 32 Kbytes • Branch instruction processing accelerator: 272 bytes • Local SRAM (LRAM) 128 Kbytes × 2 units

Item	RX72M/RX72N	RX74M/RX74N
FPU	• Single-precision floating-point numbers (32 bits) • Data types and floating-point exceptions in conformance with the IEEE754 standard	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard
Double-precision floating point coprocessor	• Double-precision floating-point register set Double-precision floating-point data registers: 16, each with 64-bit width Double-precision floating-point control registers: Four, each with 32-bit width • Double-precision floating-point processing instructions: 21 • Notifying the interrupt controller of double-precision floating-point exceptions	• Double-precision floating-point register set Double-precision floating-point data registers: Sixteen 64-bit registers Double-precision floating-point control registers: Four 32-bit registers • Double-precision floating-point processing instructions: 21 • Notifying the interrupt controller of double-precision floating-point exceptions
Register bank save function	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks are provided for the Root world, Secure world, and Non-secure world, respectively.

Table 2.2 Comparison of CPU Registers

Register	Bit	RX72M/RX72N	RX74M/RX74N
PSW	IPL[3:0] (RX72M/RX72N) IPL[4:0] (RX74M/RX74N)	Processor interrupt priority level b27 b24 0 0 0 0: Priority level 0 (lowest) : 1 1 1 1: Priority level 15 (highest)	Processor interrupt priority level b28 b24 0 0 0 0 0: Priority level 0 (lowest) : 0 1 1 1 1: Priority level 15 (Non-secure, highest) 1 0 0 0 0: Priority level 16 1 0 0 0 1: Priority level 17 1 0 0 1 0: Priority level 18 1 0 0 1 1: Priority level 19 1 0 1 0 0: Priority level 20 1 0 1 0 1: Priority level 21 1 0 1 1 0: Priority level 22 1 0 1 1 1: Priority level 23 1 1 0 0 0: Priority level 24 1 1 0 0 1: Priority level 25 1 1 0 1 0: Priority level 26 1 1 0 1 1: Priority level 27 1 1 1 0 0: Priority level 28 1 1 1 0 1: Priority level 29 1 1 1 1 0: Priority level 30 1 1 1 1 1: Priority level 31 (highest)
IVC	—	—	Interrupt vector control register
WID	—	—	World ID register
TRCTB	—	—	Root call vector table register
WINTB	—	—	Vector table register for interrupts that cause world transitions
WPRI	—	—	World-shared processor interrupt priority level register

2.2 Operating Modes

Table 2.3 is Comparative Overview of Operating Modes, and Table 2.4 is Comparison of Operating Mode Registers.

Table 2.3 Comparative Overview of Operating Modes

Item	RX72M/RX72N	RX74M/RX74N
Operating modes by the mode-setting pins	Single-chip mode	Single-chip mode
	—	Boot mode*1 (JTAG/SWD interface)
	Boot mode (SCI interface)	Boot mode (SCI interface)
	Boot mode (USB interface)	Boot mode (USB interface)
	Boot mode (FINE interface)	Boot mode (FINE interface)
Operating modes by register setting	Single-chip mode	Single-chip mode
	On-chip ROM disabled extended mode	—
	On-chip ROM enabled extended mode	—
Selection of endian	MDE register	MDE register

Note: 1. The MCU starts up in boot mode (JTAG/SWD interface) in response to the input of a request from the JTAG or SWD interface during the RES# pin reset.

Table 2.4 Comparison of Operating Mode Registers

Register	Bit	RX72M/RX72N	RX74M/RX74N
MDMONR	—	Mode monitor register	—
SYSCR0	ROME	On-chip ROM enable bit 0: The on-chip ROM is disabled. 1: The on-chip ROM is enabled.	On-chip code MRAM enable bit 0: The on-chip code MRAM is disabled. 1: The on-chip code MRAM is enabled.
	EXBE	External bus enable bit	—
MDSAR	—	—	Operating mode security attribution register

2.3 Address Space

Figure 2.1 is Comparative Memory Map in Single-Chip Mode.

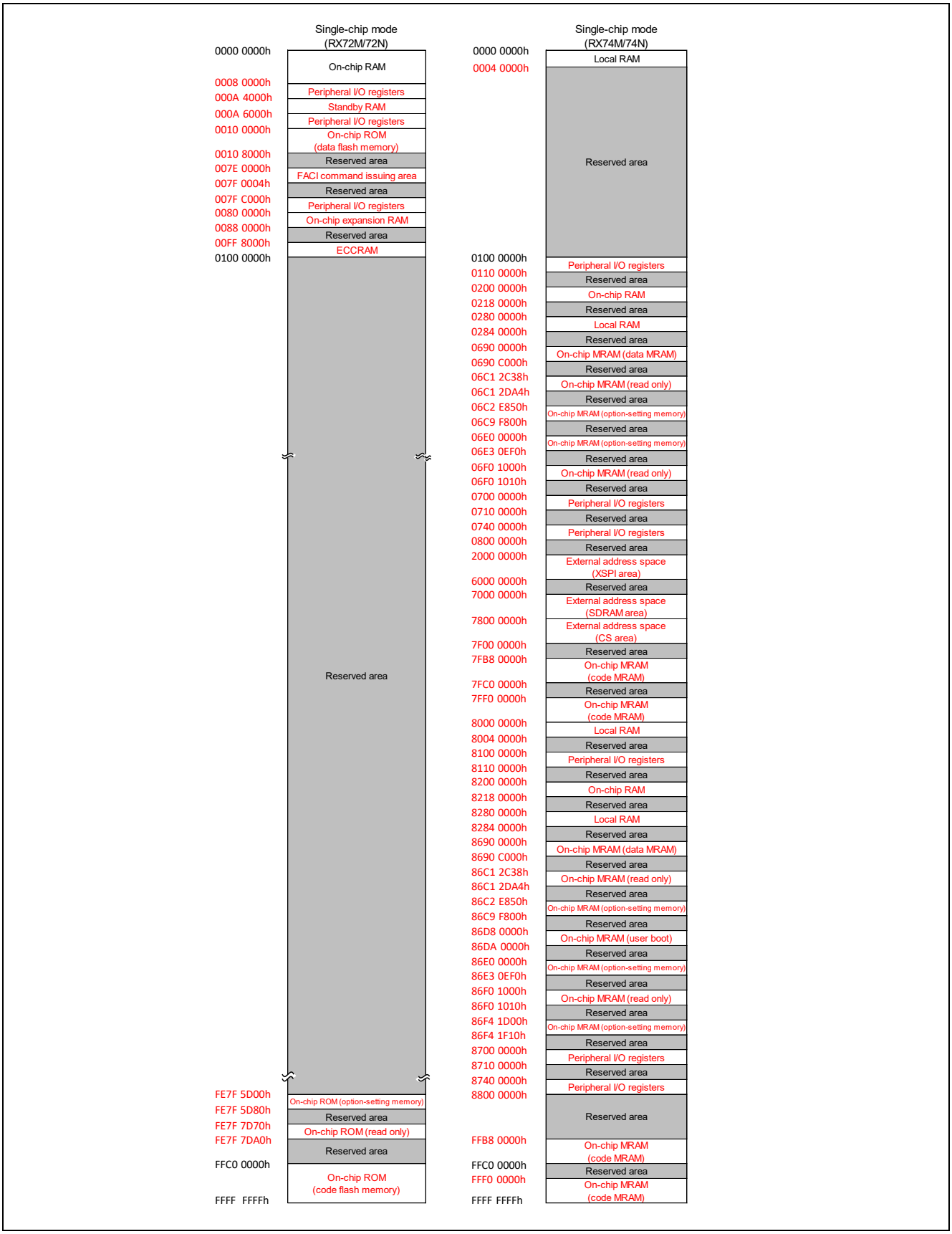


Figure 2.1 Comparative Memory Map in Single-Chip Mode

2.4 Resets

Table 2.5 is Comparative Overview of Resets, and Table 2.6 is Comparison of Reset-Related Registers.

Table 2.5 Comparative Overview of Resets

Item	RX72N/RX72M	RX74N/RX74M
RES# pin reset	Voltage input to the RES# pin is driven low.	Voltage input to the RES# pin is driven low.
Power-on reset	VCC rises (voltage detection: VPOR)	VCC rises (voltage used in monitoring: VPOR)
Voltage monitoring 0 reset	VCC falls (voltage detection: Vdet0)	VCC falls (voltage used in monitoring: Vdet0)
Voltage monitoring 1 reset	VCC falls (voltage detection: Vdet1)	VCC falls (voltage used in monitoring: Vdet1) VCC rises (voltage used in monitoring: Vdet1)
Voltage monitoring 2 reset	VCC falls (voltage detection: Vdet2)	VCC falls (voltage used in monitoring: Vdet2) VCC rises (voltage used in monitoring: Vdet2)
Voltage monitoring 4 reset	—	VCC falls (voltage used in monitoring: Vdet4) VCC rises (voltage used in monitoring: Vdet4)
Voltage monitoring 5 reset	—	VCC falls (voltage used in monitoring: Vdet5) VCC rises (voltage used in monitoring: Vdet5)
Core voltage monitoring reset	—	VDD falls (voltage used in monitoring: Vdet_VDDL) VDD rises (voltage used in monitoring: Vdet_VDDH)
Temperature monitoring reset	—	Detection of a temperature beyond the specified range
Bus error reset	—	Bus error
Common memory error reset	—	ECC error in the RAM
Local memory error reset	—	ECC error in the CPU cache or local RAM
Deep software standby reset	Deep software standby mode is canceled by an interrupt.	Release from deep software standby mode by an interrupt
Independent watchdog timer reset	Independent watchdog timer underflow or refresh error	Independent watchdog timer underflow or refresh error
Watchdog timer reset	Watchdog timer underflow or refresh error	Watchdog timer underflow or refresh error
Software reset	Register setting	Register setting

Table 2.6 Comparison of Reset-Related Registers

Register	Bit	RX72N/72M	RX74N/74M
RSTSR0	PVD4RF	—	Voltage monitoring 4 reset detect flag
	PVD5RF	—	Voltage monitoring 5 reset detect flag
	DPSRSTF	Deep software standby reset flag 0: Deep software standby mode cancelation not requested by an interrupt. 1: Deep software standby mode cancelation requested by an interrupt.	Deep software standby reset detect flag 0: Request for release from deep software standby mode by an interrupt or reset not generated 1: Request for release from deep software standby mode by an interrupt or reset generated
RSTSR1	CWSF	Cold/warm start determination flag	—
	IWDTRF	—	Independent watchdog timer reset detect flag
	WDT0RF	—	Watchdog timer reset detect flag
	SWRF	—	Software reset detect flag
	LM0RF	—	Local memory error reset detect flag
	BUSRF	—	Bus error reset detect flag
	CMRF	—	Common memory error reset detect flag
RSTSR2	IWDTRF	Independent watchdog timer reset detect flag	—
	WDTRF	Watchdog timer reset detect flag	—
	SWRF	Software reset detect flag	—
	CWSF	—	Cold/warm start determination flag
RSTSR3	—	—	Reset status register 3
SYRSTMSK0	—	—	System reset mask control register 0
SYRSTMSK2	—	—	System reset mask control register 2
TEMPRCR	—	—	Temperature monitoring reset control register
TEMPRLR	—	—	Temperature monitoring reset lock register
ROUTSR0	—	—	Reset output status register 0
ROUTSR1	—	—	Reset output status register 1
ROUTSR2	—	—	Reset output status register 2
RSTSAR	—	—	Reset security attribute register

2.5 Option-Setting Memory

Table 2.7 is Comparison of Option-Setting Memory Registers.

Table 2.7 Comparison of Option-Setting Memory Registers

Register	Bit	RX72M/RX72N	RX74M/RX74N
SPCC	—	Serial programmer command control register	—
OSIS	—	OCD/serial programmer ID setting register	—
SOTPMS_S	—	—	Secure switchable OTP memory type setting register
SOTPMS_NS	—	—	Non-secure switchable OTP memory type setting register
OFS0	IWDTTOPS[1:0]	IWDT timeout period select bits b3 b2 0 0: 1024 cycles (03FFh) 0 1: 4096 cycles (0FFFh) 1 0: 8192 cycles (1FFFh) 1 1: 16384 cycles (3FFFh)	IWDT timeout period select bits b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1024 cycles (03FFh) 1 1: 2048 cycles (07FFh)
	IWDTSLCSTP [RX72M/RX72N] IWDTSTPCTL [RX74M/RX74N]	IWDT sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, deep software standby, or all-module clock stop mode	IWDT sleep mode count stop control bit 0: Counter continues counting even in sleep mode, deep sleep mode, software standby mode, or deep software standby mode 1. 1: Counter stops when entering sleep mode, deep sleep mode, software standby mode, or deep software standby mode 1.
	WDTSTRT [RX72M/RX72N] WDT0STRT [RX74M/RX74N]	WDT start mode select bit	WDT start mode select bit
	WDTTOPS[1:0] [RX72M/RX72N] WDT0TOPS[1:0] [RX74M/RX74N]	WDT timeout period select bits	WDT timeout period select bits
	WDTCKS[3:0] [RX72M/RX72N] WDT0CKS[3:0] [RX74M/RX74N]	WDT clock frequency division ratio select bits	WDT clock division ratio select bits
	WDTRPES[1:0] [RX72M/RX72N] WDT0RPES[1:0] [RX74M/RX74N]	WDT window end position select bits	WDT window end position select bits
	WDTRPSS[1:0] [RX72M/RX72N] WDT0RPSS[1:0] [RX74M/RX74N]	WDT window start position select bits	WDT window start position select bits

Register	Bit	RX72M/RX72N	RX74M/RX74N
OFS0	WDTRSTIRQS [RX72M/RX72N] WDT0RSTIRQS [RX74M/RX74N]	WDT reset interrupt request select bit	WDT reset interrupt request select bit
OFS1	—	Option function select register 1	—
OFS2	—	—	Option function select register 2
MDE	BANKMD	Bank mode select bits	—
TMEF	—	TM enable flag register	—
TMINF	—	TM identification data register	—
BANKSEL	—	Bank select register	—
FAW	—	Flash access window setting register	—
ROMCODE	—	ROM code protection register	—
DUALSEL	—	—	Bank mode select register
BANKSEL_S	—	—	Bank select register for secure application
BANKSEL_NS	—	—	Bank select register for non-secure application
BANKSEL_SEL	—	—	BANKSEL attribute select register
BLSEL_S	—	—	Block select register for secure application
BLSEL_NS	—	—	Block select register for non-secure application
BLSEL_SEL	—	—	BLSEL attribute select register
BLKSWPn_S	—	—	Block swap setting register n for secure application
BLKSWPn_NS	—	—	Block swap setting register n for non-secure application
SAS	—	—	Start-up area setting register
SAS2	—	—	Start-up area setting register 2
OFS1_S	—	—	Option function select register 1 for secure application
OFS1_NS	—	—	Option function select register 1 for non-secure application
OFS1_SEL	—	—	OFS1 attribute select register
MRAMSABR	—	—	MRAM security attribute boundary register
BPSn_S	—	—	Block protect register n for secure application
BPSn_NS	—	—	Block protect register n for non-secure application
BPSD0_S	—	—	Data MRAM block protect register 0 for secure application
BPSD0_NS	—	—	Data MRAM block protect register 0 for non-secure application
PBPSm_S	—	—	Permanent block protect register m for secure application
PBPSm_NS	—	—	Permanent block protect register m for non-secure application
PBPSD0_S	—	—	Data MRAM permanent block protect register 0 for secure application
PBPSD0_NS	—	—	Data MRAM permanent block protect register 0 for non-secure application

Register	Bit	RX72M/RX72N	RX74M/RX74N
MOFSPSn_S	—	—	Secure MRAM option setting memory protect register n
MOFSPS0_NS	—	—	Non-secure MRAM option setting memory protect register 0
SOFSPSn_S	—	—	Secure switchable OTP option setting memory protect register n
SOFSPS0_NS	—	—	Non-secure switchable OTP option setting memory protect register 0
FSBLCTRL0	—	—	FSBL control register 0
FSBLCTRL1	—	—	FSBL control register 1
FSBLCTRL2	—	—	FSBL control register 2
SACC0n	—	—	Code certificate 0 start address register n
SACC1n	—	—	Code certificate 1 start address register n
SAMR	—	—	Measurement report start address register
REVOKE	—	—	OEM_ROOT_PK revoke register
HOEMRTPKn	—	—	OEM_ROOT_PKn hash register [i]
ZHUK	—	—	HUK zeroization register
ARCCS	—	—	Anti-rollback counter setting register
ARCS[i]	—	—	Anti-rollback counter for secure application [i]
ARCNSn[i]	—	—	Anti-rollback counter n for non-secure application [i]
ARCNS[i]	—	—	Anti-rollback counter for non-secure application [i]
ARCOEMBL[i]	—	—	Anti-rollback counter for OEM boot loader [i]
UMRECR	—	—	User extra MRAM configuration register

2.6 Voltage Detection Circuit and Programmable Voltage Detection Circuit

Table 2.8 is Comparative Overview of Voltage Detection Circuits, and Table 2.9 is Comparison of Voltage Detection Circuit Registers.

In addition, Table 2.10 is Comparison of Setting Procedures for Monitoring Vdet1, Table 2.11 is Comparison of Setting Procedures for Monitoring Vdet2, and Table 2.12 to Table 2.15 are comparative listings of the setting procedures for bits related to the voltage monitoring 1 and 2 interrupts and the voltage monitoring 1 and 2 resets.

Table 2.8 Comparative Overview of Voltage Detection Circuits and Programmable Voltage Detection Circuit

Item		RX72M/RX72N (LVDA)			RX74M/RX74N (PVD)		
		Voltage Monitoring 0	**Voltage Monitoring 1, 2**	**—**	**Programmable Voltage Monitoring 0**	**Programmable Voltage Monitoring m (m = 1, 2)**	**Programmable Voltage Monitoring n (n = 4, 5)**
VCC monitoring	Monitored voltage	Vdet0	Vdet1, Vdet2	—	Vdet0	Vdet1, Vdet2	Vdet4, Vdet5
	Detection target	When voltage drops below Vdet0	When voltage rises above or drops below Vdet1/Vdet2	—	Vdet0 > VCC	Voltage rises or falls past Vdetm	Voltage rises or falls past Vdetn
	Detection voltage	Selectable from among three different levels by using OFS1.VDSEL[1:0] bits	Selectable from among three different levels by using LVDLVLR.LVD1LVL[3:0] or LVD2LVL[3:0] bits	—	Vdet0 is selectable from among 7 different levels by using the OFS1.VDSEL[2:0] bits	Vdetm is selectable from among 12 different levels by using the PVDmCMPCR.PVDLVL[4:0] bits	Vdetn is selectable from among 12 different levels by using the PVDnCMPCR.PVDLVL[4:0] bits
	Monitoring flag	None	LVDnSR.LVDnMON flag: Monitors whether voltage is higher or lower than Vdetn	—	None	PVDmSR.MON flag: Monitors whether voltage is higher or lower than Vdetm	None
			LVDnSR.LVDnDET flag: Vdetn passage detection	—		PVDmSR.DET flag: Vdetm crossing detection	

Item		RX72M/RX72N (LVDA)			RX74M/RX74N (PVD)		
		Voltage Monitoring 0	**Voltage Monitoring 1, 2**	**—**	**Programmable Voltage Monitoring 0**	**Programmable Voltage Monitoring m (m = 1, 2)**	**Programmable Voltage Monitoring n (n = 4, 5)**
Process upon voltage detection	Reset	Voltage monitoring 0 reset	Voltage monitoring 1/2 reset	—	Voltage monitoring 0 reset	Voltage monitoring m reset	Voltage monitoring n reset
		Reset when Vdet0 > VCC: CPU restart after specified time with VCC > Vdet0	Reset when Vdet1/Vdet2 > VCC CPU restart timing selectable: after specified time with VCC > Vdet1/Vdet2 or Vdet1/Vdet2 > VCC	—	Reset when Vdet0 > VCC CPU operation restarts after the specified time with VCC > Vdet0	Reset condition selectable: Reset when Vdetm > VCC (LVD) or Vdetm < VCC (HVD) CPU restart timing selectable: after the specified time with LVD or HVD	Reset condition selectable: Reset when Vdetn > VCC (LVD) or Vdetn < VCC(HVD)
	Interrupt	No interrupt	Voltage monitoring 1/2 interrupt	—	None	Voltage monitoring m interrupt	None
			Non-maskable interrupt or maskable interrupt selectable	—		Non-maskable interrupt or maskable interrupt selectable	
			Interrupt request issued when Vdet1/Vdet2 > VCC and VCC > Vdet1/Vdet2 or either	—		Interrupt request issued in response to either or both LVD and HVD	
Digital filter	Enable/ disable switching	Digital filter function not available	Available	—	Digital filter function not available	Available	Available
	Sampling time	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	—	—	1/s LOCO frequency × 2 (s: 2, 4, 8, 16)	1/s LOCO frequency × 2 (s: 2, 4, 8, 16)
Event link function		None	Available Output of event signals on detection of Vdet crossings	—	None	Output of event signals on detection of Vdetm crossings	None
Register locking function		—	—	—	None	None	PVDLR register

Table 2.9 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX72M/RX72N (LVDA)	RX74M/RX74N (PVD)
LVD1CR1	—	Voltage monitoring 1 circuit control register 1	—
LVD1SR	—	Voltage monitoring 1 circuit status register	—
LVD2CR1	—	Voltage monitoring 2 circuit control register 1	—
LVD2SR	—	Voltage monitoring 2 circuit status register	—
LVCMPCR	—	Voltage monitoring circuit control register	—
LVDLVLR	—	Voltage detection level select register	—
LVD1CR0	—	Voltage monitoring 1 circuit control register 0	—
LVD2CR0	—	Voltage monitoring 2 circuit control register 0	—
PVDSAR	—	—	Programmable voltage detection security attribute setting register
PVDmCMPCR	—	—	Voltage monitoring m comparator control register
PVDnCMPCR	—	—	Voltage monitoring n comparator control register
PVDmCR0	—	—	Voltage monitoring m circuit control register 0
PVDnCR0	—	—	Voltage monitoring n circuit control register 0
PVDmCR1	—	—	Voltage monitoring m circuit control register 1
PVDmSR	—	—	Voltage monitoring m circuit status register
PVDmFCR	—	—	Voltage monitoring m function control register
PVDnFCR	—	—	Voltage monitoring n function control register
PVDLR	—	—	Voltage monitoring lock register

Table 2.10 Comparison of Setting Procedures for Monitoring Vdet1

Item		RX72M/RX72N (LVDA)	RX74M/RX74N (PVD)
Procedures for setting up monitoring against Vdet1	1	—	Set PVDmCMPCR.PVDE = 0 (disabling the voltage detection m circuit).
	2	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.	Select the detection voltage by setting the PVDmCMPCR.PVDLVL[4:0] bits.
	3	Set LVCMPCR.LVD1E = 1 (enabling the voltage detection 1 circuit).	Set PVDmCMPCR.PVDE = 1 (enabling the voltage detection m circuit).
	4	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).	Wait for at least td(E-A).
	5	Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits.	Select the sampling clock for the digital filter by setting the PVDmCR0.FSAMP[1:0] bits.
	6	Set LVD1CR0.LVD1DFDIS = 0 (enabling the digital filter).	Set PVDmCR0.DFDIS = 0 (enabling the digital filter).
	7	Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n).	Wait for at least 2s + 3 cycles of the LOCO (where s = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by s).
	8	Set LVD1CR0.LVD1CMPE = 1 (enabling output of the results of comparison by voltage monitoring 1).	Set PVDmCR0.CMPE = 1 (enabling output of the results of comparison by voltage monitoring m).

Table 2.11 Comparison of Setting Procedures for Monitoring Vdet2

Item		RX72M/RX72N (LVDA)	RX74M/RX74N (PVD)
Procedures for setting up monitoring against Vdet2	1	—	Set PVDmCMPCR.PVDE = 0 (disabling the voltage detection m circuit).
	2	Select the detection voltage by setting the LVDLVLR.LVD2LVL[3:0] bits.	Select the detection voltage by setting the PVDmCMPCR.PVDLVL[4:0] bits.
	3	Set LVCMPCR.LVD2E = 1 (enabling the voltage detection 2 circuit).	Set PVDmCMPCR.PVDE = 1 (enabling the voltage detection m circuit).
	4	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).	Wait for at least td(E-A).
	5	Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits.	Select the sampling clock for the digital filter by setting the PVDmCR0.FSAMP[1:0] bits.
	6	Set LVD2CR0.LVD2DFDIS = 0 (enabling the digital filter).	Set PVDmCR0.DFDIS = 0 (enabling the digital filter).
	7	Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n).	Wait for at least 2s + 3 cycles of the LOCO (where s = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by s).
	8	Set LVD2CR0.LVD2CMPE = 1 (enabling output of the results of comparison by voltage monitoring 2).	Set PVDmCR0.CMPE = 1 (enabling output of the results of comparison by voltage monitoring m).

Table 2.12 Comparison of Procedures for Setting Bits Related to Voltage Monitoring 1 Interrupt and Voltage Monitoring 1 Reset to Run Voltage Monitoring

Item		RX72M/RX72N (LVDA)	RX74M/RX74N (PVD)
Procedure for setting bits related to voltage monitoring 1 interrupt to run voltage monitoring	1	—	Set PVDmCMPCR.PVDE = 0 (disabling the voltage detection m circuit). (Disable the voltage detection m circuit before writing to the PVDmCMPCR.PVDLVL[4:0] and PVDmFCR.RHSEL bits.)
	2	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.	Select the detection voltage by setting the PVDmCMPCR.PVDLVL[4:0] bits.
	3	Set LVCMPCR.LVD1E = 1 (enabling the voltage detection 1 circuit).	Set PVDmCMPCR.PVDE = 1 (enabling the voltage detection m circuit).
	4	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).	Wait for at least td(E-A).
	5	Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits.	Select the sampling clock for the digital filter by setting the PVDmCR0.FSAMP[1:0] bits.
	6	Set LVD1CR0.LVD1DFDIS = 0 (enabling the digital filter).	Set PVDmCR0.DFDIS = 0 (enabling the digital filter).
	7	Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n).	Wait for at least 2s + 3 cycles of the LOCO (where s = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by s)*1
	8	Set LVD1CR0.LVD1RI = 0 (selecting the voltage monitoring 1 interrupt).	Set PVDmCR0.RI = 0 (voltage monitoring m interrupt).
	9	• Select the timing of interrupt requests by setting the LVD1CR1.LVD1IDTSEL[1:0] bits. • Select the type of interrupt by setting the LVD1CR1.LVD1IRQSEL bit.	• Select the timing of interrupt requests by setting the PVDmCR1.IDTSEL[1:0] bits. • Select the type of interrupt by setting the PVDmCR1.IRQSEL bit.
	10	Set LVD1SR.LVD1DET = 0.	Set PVDmSR.DET = 0.
	11	Set LVD1CR0.LVD1RIE = 1 (enabling the voltage monitoring 1 interrupt or reset).	Set PVDmCR0.RIE = 1 (enabling the voltage monitoring m interrupt or reset).
	12	Set LVD1CR0.LVD1CMPE = 1 (enabling output of the results of comparison by voltage monitoring 1).	Set PVDmCR0.CMPE = 1 (enabling output of the results of comparison by voltage monitoring m).

Note: 1. Steps 8 to 11 can be performed during the waiting time of step 7.

Item		RX72M/RX72N (LVDA)	RX74M/RX74N (PVD)
Procedure for setting bits related to voltage monitoring 1 reset to run voltage monitoring	1	—	Set PVDmCMPCR.PVDE = 0 (disabling the voltage detection m circuit). (Disable the voltage detection m circuit before writing to the PVDmCMPCR.PVDLVL[4:0] and PVDmFCR.RHSEL bits.)
	2	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.	Select the detection voltage by setting the PVDmCMPCR.PVDLVL[4:0] bits.
	3	—	Select the type of reset condition by setting the PVDmFCR.RHSEL bit.
	4	Set LVCMPCR.LVD1E = 1 (enabling the voltage detection 1 circuit).	Set PVDmCMPCR.PVDE = 1 (enabling the voltage detection m circuit).
	5	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).	Wait for at least td(E-A).
	6	Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits.	Select the sampling clock for the digital filter by setting the PVDmCR0.FSAMP[1:0] bits.
	7	Set LVD1CR0.LVD1DFDIS = 0 (enabling the digital filter).	Set PVDmCR0.DFDIS = 0 (enabling the digital filter).
	8	Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n).	Wait for at least 2s + 3 cycles of the LOCO (where s = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by s)*1
	9	• Set LVD1CR0.LVD1RI = 1 (selecting the voltage monitoring 1 reset). • Select the type of the reset negation by setting the LVD1CR0.LVD1RN bit.	• Set PVDmCR0.RI = 1 (voltage monitoring m reset). • Select the type of reset negation by setting the PVDmCR0.RN bit.
	10	Set LVD1SR.LVD1DET = 0.	—
	11	Set LVD1CR0.LVD1RIE = 1 (enabling the voltage monitoring 1 interrupt or reset).	Set PVDmCR0.RIE = 1 (enabling the voltage monitoring m interrupt or reset).
	12	Set LVD1CR0.LVD1CMPE = 1 (enabling output of the results of comparison by voltage monitoring 1).	Set PVDmCR0.CMPE = 1 (enabling output of the results of comparison by voltage monitoring m).

Note: 1. Steps 8 to 11 can be performed during the waiting time of step 7.

Table 2.13 Comparison of Procedures Setting Bits Related to Voltage Monitoring 1 Interrupt and Voltage Monitoring 1 Reset to Stop Voltage Monitoring

Item		RX72M/RX72N (LVDA)	RX74M/RX74N (PVD)
Procedure for setting bits related to voltage monitoring 1 interrupt and voltage monitoring 1 reset to stop voltage monitoring	1	Set LVD1CR0.LVD1CMPE = 0 (disabling output of the results of comparison by voltage monitoring 1).	Set PVDmCR0.CMPE = 0 (disabling output of the results of comparison by voltage monitoring m).
	2	Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n).	Wait for at least 2s + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by s).
	3	Set LVD1CR0.LVD1RIE = 0 (disabling the voltage monitoring 1 interrupt or reset).	Set PVDmCR0.RIE = 0 (disabling the voltage monitoring m interrupt or reset).
	4	Set LVD1CR0.LVD1DFDIS = 1 (disabling the digital filter).	Set PVDmCR0.DFDIS = 1 (disabling the digital filter).
	5	Set LVCMPCR.LVD1E = 0 (disabling the voltage detection 1 circuit).	Set PVDmCMPCR.PVDE = 0 (disabling the voltage detection m circuit).

Table 2.14 Comparison of Procedures for Setting Bits Related to Voltage Monitoring 2 Interrupt and Voltage Monitoring 2 Reset to Run Voltage Monitoring

Item		RX72M/RX72N (LVDA)	RX74M/RX74N (PVD)
Procedure for setting bits related to voltage monitoring 2 interrupt to run voltage monitoring	1	—	Set PVDmCMPCR.PVDE = 0 (disabling the voltage detection m circuit). (Disable the voltage detection m circuit before writing to the PVDmCMPCR.PVDLVL[4:0] and PVDmFCR.RHSEL bits.)
	2	Select the detection voltage by setting the LVDLVLR.LVD2LVL[3:0] bits.	Select the detection voltage by setting the PVDmCMPCR.PVDLVL[4:0] bits.
	3	Set LVCMPCR.LVD2E = 1 (enabling the voltage detection 2 circuit).	Set PVDmCMPCR.PVDE = 1 (enabling the voltage detection m circuit).
	4	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).	Wait for at least td(E-A).
	5	Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits.	Select the sampling clock for the digital filter by setting the PVDmCR0.FSAMP[1:0] bits.
	6	Set LVD2CR0.LVD2DFDIS = 0 (enabling the digital filter).	Set PVDmCR0.DFDIS = 0 (enabling the digital filter).
	7	Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n).	Wait for at least 2s + 3 cycles of the LOCO (where s = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by s)*1
	8	Set LVD2CR0.LVD2RI = 0 (selecting the voltage monitoring 2 interrupt).	Set PVDmCR0.RI = 0 (voltage monitoring m interrupt).
	9	• Select the timing of interrupt requests by setting the LVD2CR1.LVD2IDTSEL[1:0] bits. • Select the type of interrupt by setting the LVD2CR1.LVD2IRQSEL bit.	• Select the timing of interrupt requests by setting the PVDmCR1.IDTSEL[1:0] bits. • Select the type of interrupt by setting the PVDmCR1.IRQSEL bit.
	10	Set LVD2SR.LVD2DET = 0.	Set PVDmSR.DET = 0.
	11	Set LVD2CR0.LVD2RIE = 1 (enabling the voltage monitoring 2 interrupt or reset).	Set PVDmCR0.RIE = 1 (enabling the voltage monitoring m interrupt or reset).
	12	Set LVD2CR0.LVD2CMPE = 1 (enabling output of the results of comparison by voltage monitoring 2).	Set PVDmCR0.CMPE = 1 (enabling output of the results of comparison by voltage monitoring m).

Note: 1. Steps 8 to 11 can be performed during the waiting time of step 7.

Item		RX72M/RX72N (LVDA)	RX74M/RX74N (PVD)
Procedure for setting bits related to voltage monitoring 2 reset to run voltage monitoring	1	—	Set PVDmCMPCR.PVDE = 0 (disabling the voltage detection m circuit). (Disable the voltage detection m circuit before writing to the PVDmCMPCR.PVDLVL[4:0] and PVDmFCR.RHSEL bits.)
	2	Select the detection voltage by setting the LVDLVLR.LVD2LVL[3:0] bits.	Select the detection voltage by setting the PVDmCMPCR.PVDLVL[4:0] bits.
	3	—	Select the type of reset condition by setting the PVDmFCR.RHSEL bit.
	4	Set LVCMPCR.LVD2E = 1 (enabling the voltage detection 2 circuit).	Set PVDmCMPCR.PVDE = 1 (enabling the voltage detection m circuit).
	5	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).	Wait for at least td(E-A).
	6	Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits.	Select the sampling clock for the digital filter by setting the PVDmCR0.FSAMP[1:0] bits.
	7	Set LVD2CR0.LVD2DFDIS = 0 (enabling the digital filter).	Set PVDmCR0.DFDIS = 0 (enabling the digital filter).
	8	Wait for at least 2n + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n).	Wait for at least 2s + 3 cycles of the LOCO (where s = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by s)*1
	9	• Set LVD2CR0.LVD2RI = 1 (selecting the voltage monitoring 2 reset). • Select the type of the reset negation by setting the LVD2CR0.LVD2RN bit.	• Set PVDmCR0.RI = 1 (voltage monitoring m reset). • Select the type of reset negation by setting the PVDmCR0.RN bit.
	10	Set LVD2SR.LVD2DET = 0.	—
	11	Set LVD2CR0.LVD2RIE = 1 (enabling the voltage monitoring 2 interrupt or reset).	Set PVDmCR0.RIE = 1 (enabling the voltage monitoring m interrupt or reset).
	12	Set LVD2CR0.LVD2CMPE = 1 (enabling output of the results of comparison by voltage monitoring 2).	Set PVDmCR0.CMPE = 1 (enabling output of the results of comparison by voltage monitoring m).

Note: 1. Steps 8 to 11 can be performed during the waiting time of step 7.

Table 2.15 Comparison of Procedures for Setting Bits Related to Voltage Monitoring 2 Interrupt and Voltage Monitoring 2 Reset to Stop Voltage Monitoring

Item		RX72M/RX72N (LVDA)	RX74M/RX74N (PVD)
Procedure for setting bits related to voltage monitoring 2 interrupt and voltage monitoring 2 reset to stop voltage monitoring	1	Set LVD2CR0.LVD2CMPE = 0 (disabling output of the results of comparison by voltage monitoring 2).	Set PVDmCR0.CMPE = 0 (disabling output of the results of comparison by voltage monitoring m).
	2	Wait for at least 2n + 3 cycles of the LOCO where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n).	Wait for at least 2s + 3 cycles of the LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by s).
	3	Set LVD2CR0.LVD2RIE = 0 (disabling the voltage monitoring 2 interrupt or reset).	Set PVDmCR0.RIE = 0 (disabling the voltage monitoring m interrupt or reset).
	4	Set LVD2CR0.LVD2DFDIS = 1 (disabling the digital filter).	Set PVDmCR0.DFDIS = 1 (disabling the digital filter).
	5	Set LVCMPCR.LVD2E = 0 (disabling the voltage detection 2 circuit).	Set PVDmCMPCR.PVDE = 0 (disabling the voltage detection m circuit).

2.7 Clock Generation Circuit

Table 2.16 is Comparative Overview of Clock Generation Circuits, and Table 2.17 is Comparison of Clock Generation Circuit Registers.

Table 2.16 Comparative Overview of Clock Generation Circuits

Item	RX72M	RX72N	RX74M	RX74N
Main clock oscillator	Resonator frequency: 8 MHz to 24 MHz External clock input frequency: 30 MHz (max.) Connectable resonator or additional circuit: ceramic resonator, crystal resonator Connection pin: EXTAL, XTAL Oscillation stop detection function: This function changes the system clock source to the LOCO and places the MTU and GPTW pins in the high-impedance state when stopping of oscillation by the main clock oscillator is detected. Driving ability switching	Resonator frequency: 8 MHz to 24 MHz External clock input frequency: 30 MHz (max.) Connectable resonator or additional circuit: ceramic resonator, crystal resonator Connection pin: EXTAL, XTAL Oscillation stop detection function: This function changes the system clock source to the LOCO and places the MTU and GPTW pins in the high-impedance state when stopping of oscillation by the main clock oscillator is detected. Driving ability switching	Resonator frequency: 8 MHz to 48 MHz External clock input frequency: Up to 48 MHz Connectable resonator or additional circuit: Ceramic resonator or crystal resonator Pins for connection: EXTAL and XTAL Oscillation stop detection function Driving capacity switching	Resonator frequency: 8 MHz to 48 MHz External clock input frequency: Up to 48 MHz Connectable resonator or additional circuit: Ceramic resonator or crystal resonator Pins for connection: EXTAL and XTAL Oscillation stop detection function Driving capacity switching
Sub-clock oscillator	Resonator frequency: 32.768 kHz Connectable resonator or additional circuit: crystal resonator Connection pin: XCIN, XCOUT Driving ability switching	Resonator frequency: 32.768 kHz Connectable resonator or additional circuit: crystal resonator Connection pin: XCIN, XCOUT Driving ability switching	Resonator frequency: 32.768 kHz Connectable resonator or additional circuit: crystal resonator Pins for connection: XCIN and XCOUT External clock input Driving capacity switching Oscillation stop detection function	Resonator frequency: 32.768 kHz Connectable resonator or additional circuit: crystal resonator Pins for connection: XCIN and XCOUT External clock input Driving capacity switching Oscillation stop detection function

Item	RX72M	RX72N	RX74M	RX74N
PLL frequency synthesizer (PLL)	Input clock source: Main clock or HOCO Input pulse frequency division ratio: Selectable from 1 to 3 Input frequency: 8 MHz to 24 MHz Frequency multiplication ratio: Selectable from 10 to 30 Output clock frequency of the PLL frequency synthesizer: 120 MHz to 240 MHz	Input clock source: Main clock or HOCO Input pulse frequency division ratio: Selectable from 1 to 3 Input frequency: 8 MHz to 24 MHz Frequency multiplication ratio: Selectable from 10 to 30 Output clock frequency of the PLL frequency synthesizer: 120 MHz to 240 MHz	Input clock source: MOSC or HOCO Input clock frequency division ratio: Selectable from division by 1 to division by 3 Input clock frequency: 8 MHz to 48 MHz Input clock frequency (after input frequency division): 8 MHz to 24 MHz Frequency multiplication ratio: Selectable from 40 to 300 (Fractional part: 0, 0.33, 0.50, or 0.66) VCO frequency: 960 MHz to 2400 MHz Number of output clocks: Three different clocks are output. PLL output clock P: 60 to 600 MHz (PLL1), 60 to 500 MHz (PLL2) (Output frequency division ratio: 2, 3, 4, 6, 8, or 16) PLL output clock Q: 106.6 to 500 MHz (Output frequency division ratio: 1.5, 2, 3, 4, 5, 6, 8, or 9) PLL output clock R: 106.6 to 500 MHz (Output frequency division ratio: 1.5, 2, 3, 4, 5, 6, 8, or 9)	Input clock source: MOSC or HOCO Input clock frequency division ratio: Selectable from division by 1 to division by 3 Input clock frequency: 8 MHz to 48 MHz Input clock frequency (after input frequency division): 8 MHz to 24 MHz Frequency multiplication ratio: Selectable from 40 to 300 (Fractional part: 0, 0.33, 0.50, or 0.66) VCO frequency: 960 MHz to 2400 MHz Number of output clocks: Three different clocks are output. PLL output clock P: 60 to 600 MHz (PLL1), 60 to 500 MHz (PLL2) (Output frequency division ratio: 2, 3, 4, 6, 8, or 16) PLL output clock Q: 106.6 to 500 MHz (Output frequency division ratio: 1.5, 2, 3, 4, 5, 6, 8, or 9) PLL output clock R: 106.6 to 500 MHz (Output frequency division ratio: 1.5, 2, 3, 4, 5, 6, 8, or 9)

Item	RX72M	RX72N	RX74M	RX74N
PLL frequency synthesizer for specific purposes (PPLL)	Input clock source: Main clock or HOCO Input pulse frequency divisor: Selectable from 1 to 3 Input frequency: 8 MHz to 24 MHz Multipliers: The multiplier is selectable from 10 to 30 Output clock frequency from the PLL frequency synthesizer: 120 MHz to 240 MHz	Input clock source: Main clock or HOCO Input pulse frequency divisor: Selectable from 1 to 3 Input frequency: 8 MHz to 24 MHz Multipliers: The multiplier is selectable from 10 to 30 Output clock frequency from the PLL frequency synthesizer: 120 MHz to 240 MHz	—	—
High-speed on-chip oscillator (HOCO)	Selectable from 16 MHz, 18 MHz, and 20 MHz HOCO power supply control	Selectable from 16 MHz, 18 MHz, and 20 MHz HOCO power supply control	Oscillation frequency: 16, 18, 20, 32, or 48 MHz Frequency locked loop (FLL) function User trimming	Oscillation frequency: 16, 18, 20, 32, or 48 MHz Frequency locked loop (FLL) function User trimming
Middle-speed on-chip oscillator (MOCO)	—	—	Oscillation frequency: 8 MHz User trimming	Oscillation frequency: 8 MHz User trimming
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 240 kHz	Oscillation frequency: 240 kHz	Oscillation frequency: 32.768 kHz User trimming	Oscillation frequency: 32.768 kHz User trimming
IWDT-dedicated on-chip oscillator	Oscillation frequency: 120 kHz	Oscillation frequency: 120 kHz	—	—
External clock input for JTAG (TCK)	Input clock frequency: 10 MHz (max)	Input clock frequency: 10 MHz (max)	Input clock frequency: Up to 25 MHz	Input clock frequency: Up to 25 MHz
Control of output on the BCLK pin	BCLK clock output or high output is selectable BCLK or BCLK/2 is selectable	BCLK clock output or high output is selectable BCLK or BCLK/2 is selectable	EBCLK clock output or high output is selectable BCLK, 1/2 BCLK, or BCLKA is selectable	EBCLK clock output or high output is selectable BCLK, 1/2 BCLK, or BCLKA is selectable
Control of output on the SDCLK pin	SDCLK clock output or high output is selectable	SDCLK clock output or high output is selectable	SDCLK clock output or high output is selectable	SDCLK clock output or high output is selectable
External clock input for SWD (SWCLK)	—	—	Input clock frequency: Up to 25 MHz	Input clock frequency: Up to 25 MHz
Event linking (output)	Detection of stopping of the main clock oscillator	Detection of stopping of the main clock oscillator	Detection of stopping of the main clock oscillator	Detection of stopping of the main clock oscillator

Item	RX72M	RX72N	RX74M	RX74N
Event linking (input)	Switching of the clock source to the low-speed on-chip oscillator	Switching of the clock source to the low-speed on-chip oscillator	—	—
Operating frequency	ICLK 240 MHz PCLKA 120 MHz PCLKB 60 MHz PCLKC 60 MHz PCLKD 60 MHz FCLK 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) 60 MHz (max) (for reading from the data flash memory) BCLK 120 MHz BCLK pin output 80 MHz SDCLK pin output 80 MHz UCLK 48 MHz ESCCLK 100 MHz CLKOUT pin output 40 MHz CLKOUT25M pin output 25 MHz CACCLK Same as the clock from respective oscillators CANMCLK 24 MHz RTCSCLK 32.768 kHz RTCMCLK 1 kHz to 16 MHz IWDTCLK 120 kHz	ICLK 240 MHz PCLKA 120 MHz PCLKB 60 MHz PCLKC 60 MHz PCLKD 60 MHz FCLK 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) 60 MHz (max) (for reading from the data flash memory) BCLK 120 MHz BCLK pin output 80 MHz SDCLK pin output 80 MHz UCLK 48 MHz CLKOUT pin output 40 MHz CLKOUT25M pin output 25 MHz CACCLK Same as the clock from respective oscillators CANMCLK 24 MHz RTCSCLK 32.768 kHz RTCMCLK 1 kHz to 16 MHz IWDTCLK 120 kHz	ICLK Up to 300 MHz PCLKA Up to 150 MHz PCLKB Up to 75 MHz PCLKC Up to 75 MHz PCLKD Up to 150 MHz BCLK Up to 150 MHz EBCLK pin output UP to 100 MHz SDCLK pin output Up to 133 MHz USBCLK/ USB60CLK 48 MHz/60 MHz ESCCLK 100 MHz CLKOUT Up to 48 MHz ETHPHYCLK pin 25 or 50 MHz CANFDMCLK 8 MHz to 48 MHz RTCSCLK 32.768 kHz	ICLK Up to 300 MHz PCLKA Up to 150 MHz PCLKB Up to 75 MHz PCLKC Up to 75 MHz PCLKD Up to 150 MHz BCLK Up to 150 MHz EBCLK pin output Up to 100 MHz SDCLK pin output Up to 133 MHz USBCLK/ USB60CLK 48 MHz/60 MHz CLKOUT Up to 48 MHz ETHPHYCLK pin 25 or 50 MHz CANFDMCLK 8 MHz to 48 MHz RTCSCLK 32.768 kHz

Item	RX72M	RX72N	RX74M	RX74N
Operating frequency	JTAGTCK 10 MHz	JTAGTCK 10 MHz	JTAGTCK Up to 25 MHz CPUCLK0 Up to 600 MHz MRICLK Up to 300 MHz MRPCLK Up to 150 MHz PCLKE Up to 300 MHz BCLKA Up to 133 MHz SCICLK Up to 120 MHz SPICLK Up to 100 MHz XSPICLK Up to 266 MHz XSPIDIVCLK Up to 133 MHz CANFDCLK Up to 80 MHz ADCCLK Up to 60 MHz GPTCLK Up to 200 MHz I3CCLK Up to 100 MHz ESWCLK Up to 250 MHz DSMIFCLK Up to 200 MHz USBMCLK 12, 20, 24, or 48 MHz PDMIFCLK 8 MHz CACMCLK Up to 48 MHz CACSCLK 32.768 kHz CACHCLK 16, 18, 20, 32, or 48 MHz CACMOCLK 8 MHz CACLCLK 32.768 kHz CACPL1PCLK Up to 37.5 MHz CACPL1QCLK Up to 31.25 MHz	JTAGTCK Up to 25 MHz CPUCLK0 Up to 600 MHz MRICLK Up to 300 MHz MRPCLK Up to 150 MHz PCLKE Up to 300 MHz BCLKA Up to 133 MHz SCICLK Up to 120 MHz SPICLK Up to 100 MHz XSPICLK Up to 266 MHz XSPIDIVCLK Up to 133 MHz CANFDCLK Up to 80 MHz ADCCLK Up to 60 MHz GPTCLK Up to 200 MHz I3CCLK Up to 100 MHz ESWCLK Up to 250 MHz — USBMCLK 12, 20, 24, or 48 MHz PDMIFCLK 8 MHz CACMCLK Up to 48 MHz CACSCLK 32.768 kHz CACHCLK 16, 18, 20, 32, or 48 MHz CACMOCLK 8 MHz CACLCLK 32.768 kHz CACPL1PCLK Up to 37.5 MHz CACPL1QCLK Up to 31.25 MHz

Item	RX72M	RX72N	RX74M	RX74N
Operating frequency			CACPL1RCLK Up to 31.25 MHz CACPL2PCLK Up to 31.25 MHz CACPL2QCLK Up to 31.25 MHz CACPL2RCLK Up to 31.25 MHz SWCLK Up to 25 MHz	CACPL1RCLK Up to 31.25 MHz CACPL2PCLK Up to 31.25 MHz CACPL2QCLK Up to 31.25 MHz CACPL2RCLK Up to 31.25 MHz SWCLK Up to 25 MHz

Table 2.17 Comparison of Clock Generation Circuit Registers

Register	Bit	RX72M	RX72N	RX74M	RX74N
SCKCR	—	System clock control register	System clock control register	—	—
MEMWAIT	—	Memory wait cycle setting register	Memory wait cycle setting register	—	—
SCKCR2	—	System clock control register 2	System clock control register 2	—	—
SCKCR3	—	System clock control register 3	System clock control register 3	—	—
CGFSAR	—	—	—	Clock generation function security attribute register	Clock generation function security attribute register
SCKDIVCR	—	—	—	System clock frequency division control register	System clock frequency division control register
SCKDIVCR2	—	—	—	System clock frequency division control register 2	System clock frequency division control register 2
SYRACCR	—	—	—	System register access status register	System register access status register
SCKSCR	—	—	—	System clock source control register	System clock source control register
PLLCCR	—	—	—	PLL clock control register	PLL clock control register
PLLCCR2	—	—	—	PLL clock control register 2	PLL clock control register 2
PLLCR	PLIDIV [1:0]	PLL input frequency division ratio select bits	PLL input frequency division ratio select bits	—	—
	PLLSRCSEL	PLL clock source select bit	PLL clock source select bit	—	—
	STC[5:0]	Frequency multiplication factor select bits	Frequency multiplication factor select bits	—	—
	PLLSTP	—	—	PLL1 stop control bit	PLL1 stop control bit
PLLCR2	—	PLL control register 2	PLL control register 2	—	—
PLL2CCR	—	—	—	PLL2 clock control register	PLL2 clock control register
PLL2CCR2	—	—	—	PLL2 clock control register 2	PLL2 clock control register 2
PLL2CR	—	—	—	PLL2 control register	PLL2 control register
BCKCR	BCLKDIV	BCLK pin output select bit 0: BCLK 1: 1/2 BCLK	BCLK pin output select bit 0: BCLK 1: 1/2 BCLK	EBCLK pin output select bit 0: BCLK or BCLKA 1: BCLK/2 or BCLKA/2	EBCLK pin output select bit 0: BCLK or BCLKA 1: BCLK/2 or BCLKA/2

Register	Bit	RX72M	RX72N	RX74M	RX74N
BCKCR	EBCKASEL	—	—	External bus asynchronous source select bit	External bus asynchronous source select bit
SOSCCR	SOSTP	Sub-clock oscillator stop bit 0: Sub-clock oscillator is operating. (initial value) 1: Sub-clock oscillator is stopped.	Sub-clock oscillator stop bit 0: Sub-clock oscillator is operating. (initial value) 1: Sub-clock oscillator is stopped.	Sub-clock oscillator stop bit 0: The sub-clock oscillator is started (operating). 1: The sub-clock oscillator is stopped. (initial value)	Sub-clock oscillator stop bit 0: The sub-clock oscillator is started (operating). 1: The sub-clock oscillator is stopped. (initial value)
ILOCOCR	—	IWDT-dedicated on-chip oscillator control register	IWDT-dedicated on-chip oscillator control register	—	—
HOCOCR2	HCFRQ[1:0] (RX72M/72N) HCFRQ0[2:0] (RX74M/RX74N)	HOCO frequency setting bits b1 b0 0 0: 16 MHz 0 1: 18 MHz 1 0: 20 MHz Settings other than above are prohibited	HOCO frequency setting bits b1 b0 0 0: 16 MHz 0 1: 18 MHz 1 0: 20 MHz Settings other than above are prohibited	HOCO frequency setting 0 bits b2 b1 0 0 0: 16 MHz 0 0 1: 18 MHz 0 1 0: 20 MHz 1 0 0: 32 MHz 1 1 1: 48 MHz Settings other than above are prohibited	HOCO frequency setting 0 bits b2 b1 0 0 0: 16 MHz 0 0 1: 18 MHz 0 1 0: 20 MHz 1 0 0: 32 MHz 1 1 1: 48 MHz Settings other than above are prohibited
MOCOCR	—	—	—	Middle-speed on-chip oscillator control register	Middle-speed on-chip oscillator control register
FLLCR1	—	—	—	FLL control register 1	FLL control register 1
FLLCR2	—	—	—	FLL control register 2	FLL control register 2
OSCOVFSR		Oscillation stabilization flag register	Oscillation stabilization flag register	—	—
OSCSF	—	—	—	Oscillation stabilization flag register	Oscillation stabilization flag register
OSCMONR	—	—	—	Oscillator monitor register	Oscillator monitor register
SOSTDCR	—	—	—	Sub-clock oscillation stop detection control register	Sub-clock oscillation stop detection control register
SOSTDSR	—	—	—	Sub-clock oscillation stop detection status register	Sub-clock oscillation stop detection status register

Register	Bit	RX72M	RX72N	RX74M	RX74N
MOSCWTCR	MSTS [7:0] (RX72M/72N) MSTS [3:0] (RX74M/74N)	Main clock oscillator wait time setting bits	Main clock oscillator wait time setting bits	Main clock oscillator wait time setting bits	Main clock oscillator wait time setting bits
SOSCWTCR	—	Sub-clock oscillator wait control register	Sub-clock oscillator wait control register	—	—
MOFCR	—	Main clock oscillator forced oscillation control register	Main clock oscillator forced oscillation control register	—	—
HOCOPCR	—	High-speed on-chip oscillator power supply control register	High-speed on-chip oscillator power supply control register	—	—
MOMCR	—	—	—	Main clock oscillator mode oscillation control register	Main clock oscillator mode oscillation control register
SOMCR	—	—	—	Sub-clock oscillator mode control register	Sub-clock oscillator mode control register
CKOCR	CKOSEL [2:0] (RX72M/72N) CKOSEL [3:0] (RX74M/74N)	CLKOUT output source select bits b10 b8 0 0 0: LOCO 0 0 1: HOCO 0 1 0: Main clock oscillator 0 1 1: Sub-clock oscillator 1 0 0: PLL circuit 1 1 0: PPLL circuit Settings other than above are prohibited.	CLKOUT output source select bits b10 b8 0 0 0: LOCO 0 0 1: HOCO 0 1 0: Main clock oscillator 0 1 1: Sub-clock oscillator 1 0 0: PLL circuit 1 1 0: PPLL circuit Settings other than above are prohibited.	Clock output source select bits b3 b0 0 0 0 0: HOCO 0 0 0 1: MOCO (initial value) 0 0 1 0: LOCO 0 0 1 1: MOSC 0 1 0 0: SOSC 0 1 0 1: ICLK 1 0 0 0: PLL1P 1 1 0 1: PLL2P 1 1 1 0: PLL1Q 1 1 1 1: PLL2Q Settings other than those listed above are prohibited.	Clock output source select bits b3 b0 0 0 0 0: HOCO 0 0 0 1: MOCO (initial value) 0 0 1 0: LOCO 0 0 1 1: MOSC 0 1 0 0: SOSC 0 1 0 1: ICLK 1 0 0 0: PLL1P 1 1 0 1: PLL2P 1 1 1 0: PLL1Q 1 1 1 1: PLL2Q Settings other than those listed above are prohibited.

Register	Bit	RX72M	RX72N	RX74M	RX74N
CKOCR	CKODIV [2:0]	CLKOUT output divisor select bits b14 b12 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 Settings other than above are prohibited.	CLKOUT output divisor select bits b14 b12 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 Settings other than above are prohibited.	Clock output frequency division ratio bits b6 b4 0 0 0: Division by 1 0 0 1: Division by 2 0 1 0: Division by 4 0 1 1: Division by 8 1 0 0: Division by 16 1 0 1: Division by 32 1 1 0: Division by 64 1 1 1: Division by 28	Clock output frequency division ratio bits b6 b4 0 0 0: Division by 1 0 0 1: Division by 2 0 1 0: Division by 4 0 1 1: Division by 8 1 0 0: Division by 16 1 0 1: Division by 32 1 1 0: Division by 64 1 1 1: Division by 28
	CKOSTP	CLKOUT output stop control bit	CLKOUT output stop control bit	—	—
	CKOEN	—	—	Clock output enable bit	Clock output enable bit
PACKCR	—	Specific-use clock control register	Specific-use clock control register	—	—
PPLLCR	—	PPLL control register	PPLL control register	—	—
PPLLCR2	—	PPLL control register 2	PPLL control register 2	—	—
PPLLCR3	—	PPLL control register 3	PPLL control register 3	—	—
EBCKOCR	—	—	—	External bus clock output control register	External bus clock output control register
SDCKOCR	—	—	—	SDRAM clock output control register	SDRAM clock output control register
LOCOUTCR	—	—	—	LOCO user trimming control register	LOCO user trimming control register
MOCOUTCR	—	—	—	MOCO user trimming control register	MOCO user trimming control register
HOCOUTCR	—	—	—	HOCO user trimming control register	HOCO user trimming control register
MOSCSCR	—	—	—	Main clock oscillator standby control register	Main clock oscillator standby control register
HOCOSCR	—	—	—	High-speed on-chip oscillator standby control register	High-speed on-chip oscillator standby control register
MOCOSCR	—	—	—	Middle-speed on-chip oscillator standby control register	Middle-speed on-chip oscillator standby control register
USBCKDIVCR	—	—	—	USB clock frequency division control register	USB clock frequency division control register

Register	Bit	RX72M	RX72N	RX74M	RX74N
XSPICKDIVCR	—	—	—	XSPI clock frequency division control register	XSPI clock frequency division control register
CANFDCKDIVCR	—	—	—	CANFD core clock frequency division control register	CANFD core clock frequency division control register
USB60CKDIVCR	—	—	—	USBHS-PHY clock frequency division control register	USBHS-PHY clock frequency division control register
I3CCKDIVCR	—	—	—	I3C clock frequency division control register	I3C clock frequency division control register
USBCKCR	—	—	—	USB clock control register	USB clock control register
XSPICKCR	—	—	—	XSPI clock control register	XSPI clock control register
CANFDCKCR	—	—	—	CANFD core clock control register	CANFD core clock control register
USB60CKCR	—	—	—	USBHS-PHY clock control register	USBHS-PHY clock control register
I3CCKCR	—	—	—	I3C clock control register	I3C clock control register
SCICKDIVCR	—	—	—	SCI clock frequency division control register	SCI clock frequency division control register
SPICKDIVCR	—	—	—	SPI clock frequency division control register	SPI clock frequency division control register
ADCCKDIVCR	—	—	—	ADC clock frequency division control register	ADC clock frequency division control register
GPTCKDIVCR	—	—	—	GPT clock frequency division control register	GPT clock frequency division control register
SCICKCR	—	—	—	SCI clock control register	SCI clock control register
SPICKCR	—	—	—	SPI clock control register	SPI clock control register
ADCCKCR	—	—	—	ADC clock control register	ADC clock control register
GPTCKCR	—	—	—	GPT clock control register	GPT clock control register
BCKADIVCR	—	—	—	Asynchronous external bus clock frequency division control register	Asynchronous external bus clock frequency division control register
ESWCKDIVCR	—	—	—	ESWM clock frequency division control register	ESWM clock frequency division control register
ESWPCKDIVCR	—	—	—	ESWM-PHY clock frequency division control register	ESWM-PHY clock frequency division control register
ESCCKDIVCR	—	—	—	ESC clock frequency division control register	—

Register	Bit	RX72M	RX72N	RX74M	RX74N
ETHPCKDIVCR	—	—	—	Ethernet-PHY clock frequency division control register	Ethernet-PHY clock frequency division control register
DSMIFCKDIVCR	—	—	—	DSMIF clock frequency division control register	DSMIF clock frequency division control register
BCKACR	—	—	—	Asynchronous external bus clock control register	Asynchronous external bus clock control register
ESWCKCR	—	—	—	ESWM clock control register	ESWM clock control register
ESWPCKCR	—	—	—	ESWM-PHY clock control register	ESWM-PHY clock control register
ESCCKCR	—	—	—	ESC clock control register	—
ETHPCKCR	—	—	—	Ethernet-PHY clock control register	Ethernet-PHY clock control register
DSMIFCKCR	—	—	—	DSMIF clock control register	—

2.8 Clock Frequency Accuracy Measurement Circuit

Table 2.18 is Comparative Overview of Clock Frequency Accuracy Measurement Circuits, and Table 2.19 is Comparison of Clock Frequency Accuracy Measurement Circuit Registers.

Table 2.18 Comparative Overview of Clock Frequency Accuracy Measurement Circuits

Item	RX72M (CAC)/RX72N (CAC)	RX74M (CAC)/RX74N (CAC)
Unit	1 unit	3 units
Measurement target clocks	The frequency of the following clocks can be measured. • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB) • USB clock (UCLK) • External clock for the Ethernet-PHY (CLKOUT25M)	The frequency of the following clocks can be measured. • Main clock • Sub-clock • HOCO clock • MOCO clock • LOCO clock • Peripheral module clock B (PCLKB) • PLL1 output clock P/Q/R (divided by 16) • PLL2 output clock P/Q/R (divided by 16)
Measurement reference clocks	• External clock input to the CACREF pin • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB) • USB clock (UCLK) • External clock for the Ethernet-PHY (CLKOUT25M)	• External clock input to the CACREF pin • Main clock • Sub-clock • HOCO clock • MOCO clock • LOCO clock • Peripheral module clock B (PCLKB) • PLL1 output clock P/Q/R (divided by 16) • PLL2 output clock P/Q/R (divided by 16)
Selectable function	Digital filter function	Digital filter function
Interrupt sources	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt
Low power consumption function	Module stop state can be set.	Module stop state can be set.
ProtectZone filter	—	Security attribution can be set for each unit.

Table 2.19 Comparison of Clock Frequency Accuracy Measurement Circuit Registers

Register	Bit	RX72M (CAC)/RX72N (CAC)	RX74M (CAC)/RX74N (CAC)
CACR1	FMCS[2:0]	Measurement target clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) 1 1 0: USB clock (UCLK) 1 1 1: External clock for the Ethernet-PHY (CLKOUT25M) Settings other than above are prohibited.	Measurement target clock select bits Unit 0 b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: MOCO clock 1 0 0: LOCO clock 1 0 1: Peripheral module clock B (PCLKB) Unit 1 b3 b1 0 0 0: Main clock 0 0 1: PLL1 output clock P (divided by 16) 0 1 0: HOCO clock 0 1 1: MOCO clock 1 0 0: PLL1 output clock Q (divided by 16) 1 0 1: Peripheral module clock B (PCLKB) 1 1 0: PLL1 output clock R (divided by 16) 1 1 1: Setting prohibited. Unit 2 b3 b1 0 0 0: Main clock 0 0 1: PLL2 output clock P (divided by 16) 0 1 0: HOCO clock 0 1 1: MOCO clock 1 0 0: PLL2 output clock Q (divided by 16) 1 0 1: Peripheral module clock B (PCLKB) 1 1 0: PLL2 output clock R (divided by 16) 1 1 1: Setting prohibited. Settings other than above are prohibited.

Register	Bit	RX72M (CAC)/RX72N (CAC)	RX74M (CAC)/RX74N (CAC)
CACR2	RSCS[2:0]	Measurement reference clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) 1 1 0: USB clock (UCLK) 1 1 1: External clock for the Ethernet-PHY (CLKOUT25M) Settings other than above are prohibited.	Measurement reference clock select bits Unit 0 b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: MOCO clock 1 0 0: LOCO clock 1 0 1: Peripheral module clock B (PCLKB) Unit 1 b3 b1 0 0 0: Main clock 0 0 1: PLL1 output clock P (divided by 16) 0 1 0: HOCO clock 0 1 1: MOCO clock 1 0 0: PLL1 output clock Q (divided by 16) 1 0 1: Peripheral module clock B (PCLKB) 1 1 0: PLL1 output clock R (divided by 16) 1 1 1: Setting prohibited. Unit 2 b3 b1 0 0 0: Main clock 0 0 1: PLL2 output clock P (divided by 16) 0 1 0: HOCO clock 0 1 1: MOCO clock 1 0 0: PLL2 output clock Q (divided by 16) 1 0 1: Peripheral module clock B (PCLKB) 1 1 0: PLL2 output clock R (divided by 16) 1 1 1: Setting prohibited. Settings other than above are prohibited.

2.9 Low Power Consumption

Table 2.20 is Comparative Overview of Low Power Consumption Functions, Table 2.21 is Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, and Table 2.22 is Comparison of Low Power Consumption Registers.

Table 2.20 Comparative Overview of Low Power Consumption Functions

Item	RX72M/RX72N	RX74M/RX74N
Reducing power consumption by switching clock signals	The frequency division ratio is settable independently for the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, PCLKD), external bus clock (BCLK), and flash interface clock (FCLK).	The frequency division ratio is settable independently for the CPU clock (CPUCLK), system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKD, PCLKE), external bus clock (BCLK), and MRAM interface clock (MRICLK, MRPCLK).
BCLK output control function	BCLK output or high-level output can be selected.	BCLK output or high-level output can be selected.
SDCLK output control function	SDCLK output or high-level output can be selected.	SDCLK output or high-level output can be selected.
Module-stop function	Functions can be stopped independently for each peripheral module.	Functions can be stopped independently for each peripheral module.
Power gating control function	—	The power state can be controlled for each power domain. • Control the ON/OFF state of each power domain. • Control the retention of specific circuits during power gating.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• CPU sleep mode • CPU deep sleep mode • Software standby mode 1, 2 • Deep software standby modes 1, 2, 3
Function for lower operating power consumption	• Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage range. • Three operating power control modes — High-speed operating mode — Low-speed operating mode 1 — Low-speed operating mode 2 There is no difference in power consumption when the same conditions (frequency and voltage) are set in low-speed operating modes 1 and 2.	—

Table 2.21 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX72M/RX72N	RX74M/RX74N
Sleep mode (RX72M/RX72N) CPU sleep mode (RX74M/RX74N)	Transition condition	Control register + instruction	Control register + instruction
	Method of release other than reset	Interrupt	Interrupt
	State after release	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operating possible	Operating possible
	Sub-clock oscillator	Operating possible	Operating possible
	High-speed on-chip oscillator	Operating possible	Operating possible
	Low-speed on-chip oscillator	Operating possible	Operating possible
	IWDT-dedicated on-chip oscillator	Operating possible	Operating possible
	PLL (RX72M/RX72N) PLL1 (RX74M/RX74N)	Operating possible	Operating possible
	PPLL	Operating possible	—
	CPU	Stopped (Retained)	Stopped (Retained)
	RAM, expansion RAM, and ECCRAM (RX72M/RX72N) Local RAM (SRAM), User SRAM (RX74M/RX74N)	Operating possible (Retained)	Operating possible (Retained)
	Standby RAM (RX72M/RX72N) Backup register (RX74M/RX74N)	Operating possible (Retained)	Operating possible (Retained)
	Flash memory (RX72M/RX72N) MRAM (RX74M/RX74N)	Operating	Operating
	USBFS host/function module (USBb) (RX72M/RX72N) USB 2.0 full-speed host/function module (USB) (RX74M/RX74N)	Operating possible	Operating possible
	Watchdog timer (WDT)	Stopped (Retained)	Operating possible
	Independent watchdog timer (IWDT)	Operating possible	Operating possible
	Realtime clock (RTC)	Operating possible	Operating possible
	8-bit timer (unit 0, unit 1) (TMR)	Operating possible	Operating possible
	Port output enable (POE)	Operating possible	Operating possible
	Voltage detection circuit (LVD) (RX72M/RX72N) Programmable voltage detection circuit (PVD) (RX74M/RX74N)	Operating possible	Operating possible
	Power-on reset circuit	Operating	Operating
	Peripheral modules	Operating possible	Operating possible
	I/O ports	Operating	Operating
All-module clock stop mode	Transition condition	Control register + instruction	—
	Method of release other than reset	Interrupt	—
	State after release	Program execution state (interrupt processing)	—
	Main clock oscillator	Operating possible	—
	Sub-clock oscillator	Operating possible	—
	High-speed on-chip oscillator	Operating possible	—

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX72M/RX72N	RX74M/RX74N
All-module clock stop mode	Low-speed on-chip oscillator	Operating possible	—
	IWDT-dedicated on-chip oscillator	Operating possible	—
	PLL	Operating possible	—
	PPLL	Operating possible	—
	CPU	Stopped (Retained)	—
	RAM, expansion RAM, and ECCRAM	Stopped (Retained)	—
	Standby RAM	Stopped (Retained)	—
	Flash memory	Stopped (Retained)	—
	USBFS host/function module (USBb)	Stopped	—
	Watchdog timer (WDT)	Stopped (Retained)	—
	Independent watchdog timer (IWDT)	Operating possible	—
	Realtime clock (RTC)	Operating possible	—
	8-bit timer (unit 0, unit 1) (TMR)	Operating possible	—
	Port output enable (POE)	Operating possible	—
	Voltage detection circuit (LVD)	Operating possible	—
	Power-on reset circuit	Operating	—
	Peripheral modules	Stopped (Retained)	—
	I/O ports	Retained	—
Software standby mode	Transition condition	Control register + instruction	Control register + instruction SSTBY1 SSTBY2
	Method of release other than reset	Interrupt	Interrupt
	State after release	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operating possible	Operating possible
	Sub-clock oscillator	Operating possible	Operating possible
	High-speed on-chip oscillator	Stopped	Operating possible
	Middle-speed on-chip oscillator	—	Operating possible
	Low-speed on-chip oscillator	Stopped	Operating possible
	IWDT-dedicated on-chip oscillator	Operating possible	—
	PLL (RX72M/RX72N) PLL1 (RX74M/RX74M)	Stopped	Stopped
	PLL2	—	Stopped
	PPLL	Stopped	—
	Main clock oscillator stop detection function	—	Stopped
	Sub-clock oscillator stop detection function	—	Operating possible
	External bus	Stopped (Retained)	Stopped (Retained)
	CPU	Stopped (Retained)	Stopped (Retained)
	RAM, expansion RAM, and ECCRAM (RX72M/RX72N) Local RAM (SRAM), User SRAM (RX74M/RX74N)	Stopped (Retained)	Stopped (Retained/ Undefined)
	Standby RAM (RX72M/RX72N) Backup register (RX74M/RX74N)	Stopped (Retained)	Stopped (Retained)
	Flash memory (RX72M/RX72N) MRAM (RX74M/RX74N)	Stopped (Retained)	Stopped (Retained)

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX72M/RX72N	RX74M/RX74N
Software standby mode	Ethernet module (ESWM)	—	SSTBY1: Stopped (Retained) SSTBY2: Stopped (Undefined)
	EtherCAT slave controller (ESC)	—	SSTBY1: Stopped (Retained) SSTBY2: Stopped (Undefined)
	PDC	Stopped (Retained)	SSTBY1: Stopped (Retained) SSTBY2: Stopped (Undefined)
	USBFS host/function module (USBb) (RX72M/RX72N) USB 2.0 full-speed host/function module (USB) (RX74M/RX74N)	Stopped	Stopped (Retained)
	USB 2.0 high-speed host/function module (USBHS)	—	Stopped (Retained)
	Watchdog timer (WDT)	Stopped (Retained)	—
	Independent watchdog timer (IWDT)	Operating possible	Operating possible
	Realtime clock (RTC)	Operating possible	Operating possible
	CAN FD module with gateway functionality (CANFDG)	—	SSTBY1: Stopped (Retained) SSTBY2: Stopped (Undefined)
	CAN FD module (CANFD)	—	SSTBY1: Stopped (Retained) SSTBY2: Stopped (Undefined)
	SD host interface (SDHI) (RX72M/RX72N) SD/MMC host interface (SDHIc) (RX74M/RX74N)	Stopped (Retained)	SSTBY1: Stopped (Retained) SSTBY2: Stopped (Undefined)
	High-speed I^2C bus interface (RIICHS)	—	Operating possible
	I3C bus interface (RI3C)	—	Operating possible
	8-bit timer (unit 0, unit 1) (TMR)	Stopped (Retained)	—
	Port output enable (POE)	Stopped (Retained)	—
	Temperature sensor (TEMPS)	Stopped (Retained)	Operating possible
	Pulse-density modulation interface (PDMIF)	—	Operating possible
	IRQn (I = 0 to 31) pin interrupt	Operating possible	Operating possible
	NMI, IRQn-DS (I = 0 to 31) Pin interrupt	Operating possible	Operating possible
	Voltage detection circuit (LVD) (RX72M/RX72N) Programmable voltage detection circuit (PVD) (RX74M/RX74N)	Operating possible	Operating possible
	VCC voltage drop detection circuit dedicated to VBATT	—	Operating possible
	Power-on reset circuit	Operating	Operating
	CVM reset circuit	—	Operating possible
	Peripheral modules	Stopped (Retained)	Stopped (Retained)
	I/O ports	Retained	Retained

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX72M/RX72N	RX74M/RX74N
Deep software standby mode	Transition condition	Control register + instruction	Control register + instruction DSTBY1 DSTBY2 DSTBY3
	Method of release other than reset	Interrupt	Interrupt
	State after release	Program execution state (reset processing)	Reset state
	Main clock oscillator	Operating possible	Stopped
	Sub-clock oscillator	Operating possible	Operating possible
	High-speed on-chip oscillator	Stopped	Stopped
	Middle-speed on-chip oscillator	—	Stopped
	Low-speed on-chip oscillator	Stopped	DSTBY1: Operating possible DSTBY2: Stopped DSTBY3: Stopped
	IWDT-dedicated on-chip oscillator	Stopped (Undefined)	—
	PLL (RX72M/RX72N) PLL1 (RX74M/RX74M)	Stopped	Stopped
	PPLL	Stopped	—
	PLL2	—	Stopped
	Main clock oscillator stop detection function	—	Stopped
	Sub-clock oscillator stop detection function	—	Operating possible
	Clock/buzzer output function	—	Stopped
	External bus	Stopped (Retained)	Stopped (Retained)
	CPU	Stopped (Undefined)	Stopped (Undefined)
	RAM, expansion RAM, and ECCRAM (RX72M/RX72N) Local RAM (SRAM), User SRAM (RX74M/RX74N)	Stopped (Undefined)	Stopped (Undefined)
	Standby RAM (RX72M/RX72N) Backup register (RX74M/RX74N)	Stopped (Retained/Undefined)	Stopped (Retained)
	Flash memory (RX72M/RX72N) MRAM (RX74M/RX74N)	Stopped (Retained)	Stopped (Retained)
	USBFS host/function module (USBb) (RX72M/RX72N) USB 2.0 full-speed host/function module (USB) (RX74M/RX74N)	Stopped (Retained/Undefined)	DSTBY1: Stopped (Retained) DSTBY2: Stopped (Undefined) DSTBY3: Stopped (Undefined)
	USB 2.0 high-speed host/function module (USBHS)	—	DSTBY1: Stopped (Retained) DSTBY2: Stopped (Undefined) DSTBY3: Stopped (Undefined)
	Watchdog timer (WDT)	Stopped (Undefined)	—

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX72M/RX72N	RX74M/RX74N
Deep software standby mode	Independent watchdog timer (IWDT)	Stopped (Undefined)	DSTBY1: Operating possible DSTBY2: Stopped (Undefined) DSTBY3: Stopped (Undefined)
	Realtime clock (RTC)	Operating possible	Operating possible
	CAN FD module with gateway functionality (CANFDG)	—	Stopped (Undefined)
	CAN FD module (CANFD)	—	Stopped (Undefined)
	SD host interface (SDHI) (RX72M/RX72N) SD/MMC host interface (SDHIc) (RX74M/RX74N)	Stopped (Undefined)	Stopped (Undefined)
	High-speed I^2C bus interface (RIICHS)	—	Stopped (Undefined)
	I3C bus interface (RI3C)	—	Stopped (Undefined)
	8-bit timer (unit 0, unit 1) (TMR)	Stopped (Undefined)	—
	Port output enable (POE)	Stopped (Undefined)	—
	Temperature sensor (TEMPS)	Stopped (Undefined)	Operating possible
	Pulse-density modulation interface (PDMIF)	—	Stopped (Undefined)
	IRQn (I = 0 to 31) pin interrupt	Stopped (Undefined)	Stopped (Undefined)
	NMI, IRQn-DS (I = 0 to 31) Pin interrupt	Operating possible	Operating possible
	Voltage detection circuit (LVD) (RX72M/RX72N) Programmable voltage detection circuit (PVD) (RX74M/RX74N)	Operating possible	DSTBY1: Operating possible DSTBY2: Operating possible DSTBY3: Stopped (Undefined)
	VCC voltage drop detection circuit dedicated to VBATT	—	DSTBY1: Operating possible DSTBY2: Operating possible DSTBY3: Stopped (Undefined)
	Power-on reset circuit	Operating	Operating
	CVM reset circuit	—	Stopped
	Peripheral modules	Stopped (Undefined)	Stopped (Undefined)
	I/O ports	Retained	Retained

Note: “Operating possible” means that operating or stopped can be controlled by the control register setting.
“Stopped (Retained)” means that internal register values are retained and internal operations are suspended.
“Stopped (Undefined)” means that internal register values are undefined and power is not supplied to the internal circuit.

Table 2.22 Comparison of Low Power Consumption Registers

Register	Bit	RX72M	RX72N	RX74M	RX74N
LPMSAR	—	—	—	Low power consumption mode security attribution register	Low power consumption mode security attribution register
PGCSAR	—	—	—	Power gating security attribution register	Power gating security attribution register
DPFSAR	—	—	—	Deep software standby interrupt source security attribution register	Deep software standby interrupt source security attribution register
DPFSAR1	—	—	—	Deep software standby interrupt source security attribution register 1	Deep software standby interrupt source security attribution register 1
RSCSAR	—	—	—	RAM standby control security attribution register	RAM standby control security attribution register
SBYCR	SSBY	Software standby bit	Software standby bit	—	—
MSTPCRA	—	Module stop control register A	Module stop control register A	Module stop control register A	Module stop control register A
		The initial value after reset differs.			
	MSTPA0	Compare match timer W (unit 1) module stop bit	Compare match timer W (unit 1) module stop bit	SRAM0 module stop bit	SRAM0 module stop bit
	MSTPA1	Compare match timer W (unit 0) module stop bit	Compare match timer W (unit 0) module stop bit	SRAM1 module stop bit	SRAM1 module stop bit
	MSTPA4	8-bit timer 3/2 (unit 1) module stop	8-bit timer 3/2 (unit 1) module stop	—	—
	MSTPA5	8-bit timer 1/0 (unit 0) module stop	8-bit timer 1/0 (unit 0) module stop	—	—
	MSTPA7	General PWM timer/GPTW dedicated port output enable module stop bit	General PWM timer/GPTW dedicated port output enable module stop bit	—	—
	MSTPA9	Multifunction timer pulse unit module stop bit	Multifunction timer pulse unit module stop bit	—	—
	MSTPA10	Programmable pulse generator (unit 1) module stop bit	Programmable pulse generator (unit 1) module stop bit	—	—
	MSTPA11	Programmable pulse generator (unit 0) module stop bit	Programmable pulse generator (unit 0) module stop bit	—	—
	MSTPA13	16-bit timer pulse unit 0 (unit 0) Module Stop bit	16-bit timer pulse unit 0 (unit 0) Module Stop bit	—	—

Register	Bit	RX72M	RX72N	RX74M	RX74N
MSTPCRA	MSTPA14	Compare match timer (unit 1) module stop bit	Compare match timer (unit 1) module stop bit	—	—
	MSTPA15	Compare match timer (unit 0) module stop bit	Compare match timer (unit 0) module stop bit	—	—
	MSTPA16	12-bit A/D converter (unit 1) module stop bit	12-bit A/D converter (unit 1) module stop bit	—	—
	MSTPA17	12-bit A/D converter (unit 0) module stop bit	12-bit A/D converter (unit 0) module stop bit	—	—
	MSTPA19	12-bit D/A converter module stop bit	12-bit D/A converter module stop bit	—	—
	MSTPA22	—	—	DMA controller and data transfer controller module stop bit	DMA controller and data transfer controller module stop bit
	MSTPA24	Module stop A24 bit	Module stop A24 bit	—	—
	MSTPA27	Module stop A27 bit	Module stop A27 bit	—	—
	MSTPA28	DMA controller/data transfer controller module stop bit	DMA controller/data transfer controller module stop bit	—	—
	ACSE	All-module clock stop mode enable bit	All-module clock stop mode enable bit	—	—
MSTPCRB	MSTPB0	CAN module 0 module stop bit	CAN module 0 module stop bit	Serial communication interface 12 module stop bit	Serial communication interface 12 module stop bit
	MSTPB1	CAN module 1 module stop bit	CAN module 1 module stop bit	—	—
	MSTPB2	CAN module 2 module stop bit	CAN module 2 module stop bit	—	—
	MSTPB4	Serial communication interface SCIh module stop bit	Serial communication interface SCIh module stop bit	I3C bus interface 0 module stop bit	I3C bus interface 0 module stop bit
	MSTPB6	Data operation circuit module stop bit	Data operation circuit module stop bit	—	—
	MSTPB7	—	—	High-speed I^2C bus interface 2 module stop bit	High-speed I^2C bus interface 2 module stop bit
	MSTPB8	Temperature sensor module stop bit	Temperature sensor module stop bit	High-speed I^2C bus interface 1 module stop bit	High-speed I^2C bus interface 1 module stop bit
	MSTPB9	Event link controller module stop bit	Event link controller module stop bit	—	—

Register	Bit	RX72M	RX72N	RX74M	RX74N
MSTPCRB	MSTPB11	Δ-Σ interface module stop bit	—	USB 2.0 full-speed host/function module stop bit	USB 2.0 full-speed host/function module stop bit
	MSTPB12	—	—	USB 2.0 high-speed host/function module stop bit	USB 2.0 high-speed host/function module stop bit
	MSTPB13	Ethernet-controller PTP controller and Ethernet-controller DMA controller module stop setting bit	Ethernet-controller PTP controller and Ethernet-controller DMA controller module stop setting bit	—	—
	MSTPB14	Ethernet controller, Ethernet controller DMA controller, and PHY management interface (channel 1) modules stop bit	Ethernet controller, Ethernet controller DMA controller, and PHY management interface (channel 1) modules stop bit	—	—
	MSTPB15	Ethernet controller, Ethernet controller DMA controller, and PHY management interface (channel 0) modules stop bit	Ethernet controller, Ethernet controller DMA controller, and PHY management interface (channel 0) modules stop bit	—	—
	MSTPB16	Serial peripheral interface 1 module stop bit	Serial peripheral interface 1 module stop bit	Expanded serial peripheral interface 0 and Decryption-on-the-fly module 0 stop bit	Expanded serial peripheral interface 0 and Decryption-on-the-fly module 0 stop bit
	MSTPB17	Serial peripheral interface 0 module stop bit	Serial peripheral interface 0 module stop bit	Expanded serial peripheral interface 1 and Decryption-on-the-fly module 1 stop bit	Expanded serial peripheral interface 1 and Decryption-on-the-fly module 1 stop bit
	MSTPB18	—	—	Serial peripheral interface 1 module stop bit	Serial peripheral interface 1 module stop bit
	MSTPB19	Universal serial bus 2.0 FS interface module stop bit	Universal serial bus 2.0 FS interface module stop bit	Serial peripheral interface 0 module stop bit	Serial peripheral interface 0 module stop bit
	MSTPB20	I^2C bus interface 1 module stop bit	I^2C bus interface 1 module stop bit	Serial communication interface 11 module stop bit	Serial communication interface 11 module stop bit
	MSTPB21	I^2C bus interface 0 module stop bit	I^2C bus interface 0 module stop bit	Serial communication interface 10 module stop bit	Serial communication interface 10 module stop bit
	MSTPB22	Parallel data capture unit module stop bit	Parallel data capture unit module stop bit	Serial communication interface 9 module stop bit	Serial communication interface 9 module stop bit

Register	Bit	RX72M	RX72N	RX74M	RX74N
MSTPCRB	MSTPB23	CRC calculator module stop bit	CRC calculator module stop bit	Serial communication interface 8 module stop bit	Serial communication interface 8 module stop bit
MSTPCRC	—	Module stop control register C	Module stop control register C	Module stop control register C	Module stop control register C
		The initial value after reset differs.			
	MSTPC0	RAM module stop bit	RAM module stop bit	Clock frequency accuracy measurement circuit module stop bit	Clock frequency accuracy measurement circuit module stop bit
	MSTPC1	—	—	CRC calculator module stop bit	CRC calculator module stop bit
	MSTPC2	Expansion RAM module stop bit	Expansion RAM module stop bit	Parallel data capture unit module stop bit	Parallel data capture unit module stop bit
	MSTPC6	ECCRAM module stop bit	ECCRAM module stop bit	—	—
	MSTPC7	Standby RAM module stop bit	Standby RAM module stop bit	Serial sound interface 1 module stop bit	Serial sound interface 1 module stop bit
	MSTPC8	—	—	Serial sound interface 0 module stop bit	Serial sound interface 0 module stop bit
	MSTPC12	—	—	SD/MMC host interface module stop bit	SD/MMC host interface module stop bit
	MSTPC13	—	—	Data operation circuit module stop bit	Data operation circuit module stop bit
	MSTPC14	—	—	Event link controller module stop bit	Event link controller module stop bit
	MSTPC17	I^2C bus interface 2 module stop bit	I^2C bus interface 2 module stop bit	—	—
	MSTPC19	CAC module stop bit	CAC module stop bit	—	—
	MSTPC22	Serial peripheral interface 2 module stop bit	Serial peripheral interface 2 module stop bit	—	—
	MSTPC23	Quad serial peripheral interface module stop bit	Quad serial peripheral interface module stop bit	Serial peripheral interface 2 module stop bit	Serial peripheral interface 2 module stop bit
	MSTPC24	Serial communications interface 11 module stop bit	Serial communications interface 11 module stop bit	Pulse-density modulation interface module stop bit	Pulse-density modulation interface module stop bit
	MSTPC25	Serial communications interface 10 module stop bit	Serial communications interface 10 module stop bit	CAN FD module with gateway functionality module stop bit	CAN FD module with gateway functionality module stop bit
	MSTPC26	Serial communications interface 9 module stop bit	Serial communications interface 9 module stop bit	—	—

Register	Bit	RX72M	RX72N	RX74M	RX74N
MSTPCRC	MSTPC27	Serial communications interface 8 module stop bit	Serial communications interface 8 module stop bit	CAN FD module stop bit	CAN FD module stop bit
	MSTPC28	2D drawing engine module stop bit	2D drawing engine module stop bit	Ethernet-PHY clock module stop bit	Ethernet-PHY clock module stop bit
	MSTPC29	Graphic-LCD controller module stop bit	Graphic-LCD controller module stop bit	EtherCAT slave controller module stop bit	—
	MSTPC30	—	—	Ethernet module stop bit	Ethernet module stop bit
	MSTPC31	—	—	Renesas secure IP module stop bit	Renesas secure IP module stop bit
MSTPCRD	—	Module stop control register D	Module stop control register D	Module stop control register D	Module stop control register D
		The initial value after reset differs.			
	MSTPD0	Module stop D0 bit	Module stop D0 bit	—	—
	MSTPD1	Module stop D1 bit	Module stop D1 bit	—	—
	MSTPD2	Module stop D2 bit	Module stop D2 bit	—	—
	MSTPD3	Module stop D3 bit	Module stop D3 bit	—	—
	MSTPD4	Module stop D4 bit	Module stop D4 bit	—	—
	MSTPD5	Module stop D5 bit	Module stop D5 bit	—	—
	MSTPD6	Module stop D6 bit	Module stop D6 bit	High resolution PWM waveform generation circuit module stop bit	High resolution PWM waveform generation circuit module stop bit
	MSTPD7	Module stop D7 bit	Module stop D7 bit	—	—
	MSTPD8	—	—	Delta-sigma modulator interface 1 module stop bit	—
	MSTPD9	—	—	Delta-sigma modulator interface 0 module stop bit	—
	MSTPD11	EtherCAT slave controller module stop bit	—	Port output enable for GPTW group D module stop bit	Port output enable for GPTW group D module stop bit
	MSTPD12	—	—	Port output enable for GPTW group C module stop bit	Port output enable for GPTW group C module stop bit
	MSTPD13	—	—	Port output enable for GPTW group B module stop bit	Port output enable for GPTW group B module stop bit
	MSTPD14	Extended serial sound interface 1 module stop bit	Extended serial sound interface 1 module stop bit	Port output enable for GPTW group A module stop bit	Port output enable for GPTW group A module stop bit
	MSTPD15	Extended serial sound interface 0 module stop bit	Extended serial sound interface 0 module stop bit	—	—
	MSTPD19	SD host interface module stop bit	SD host interface module stop bit	12-bit D/A converter 1 module stop bit	12-bit D/A converter 1 module stop bit
	MSTPD20	—	—	12-bit D/A converter 0 module stop bit	12-bit D/A converter 0 module stop bit

Register	Bit	RX72M	RX72N	RX74M	RX74N
MSTPCRD	MSTPD21	MMC host interface module stop bit	MMC host interface module stop bit	16-bit A/D converter module stop bit	16-bit A/D converter module stop bit
	MSTPD22	—	—	Temperature sensor module stop bit	Temperature sensor module stop bit
	MSTPD27	Trusted secure IP module stop bit	Trusted secure IP module stop bit	—	—
MSTPCRE	—	—	—	Module stop control register E	Module stop control register E
MSTPCRF	—	—	—	Module stop control register F	Module stop control register F
OPCCR	—	Operating power control register	Operating power control register	—	—
RSTCKCR	—	Sleep mode return clock source switching register	Sleep mode return clock source switching register	—	—
PGSCR	—	—	—	Power gating shift control register	Power gating shift control register
PSSTCRn	—	—	—	Power switch control start time control register n	Power switch control start time control register n
PDCTRESWM	—	—	—	ESWM power domain control register	ESWM power domain control register
PDRAMSCR0	—	—	—	SRAM power domain standby control register 0	SRAM power domain standby control register 0
PDRAMSCR2	—	—	—	SRAM power domain standby control register 2	SRAM power domain standby control register 2
SBYCR	—	—	—	Standby control register	Standby control register
SSCR1	—	—	—	Software standby control register 1	Software standby control register 1
LPSCR	—	—	—	Low power consumption state control register	Low power consumption state control register
DPSBYCR	DEEPCUT[1:0]	Deep cut bit	Deep cut bit	—	—
	LDOSSMODE[1:0]	—	—	LDO soft start mode bit	LDO soft start mode bit
	DCSSMODE[1:0]	—	—	DCDC soft start mode bit	DCDC soft start mode bit
	DPSBY	Deep software standby bit	Deep software standby bit	—	—
DPSIER2	DLVD1IE	LVD1 deep standby release signal enable bit	LVD1 deep standby release signal enable bit	—	—
	DLVD2IE	LVD2 deep standby release signal enable bit	LVD2 deep standby release signal enable bit	—	—

Register	Bit	RX72M	RX72N	RX74M	RX74N
DPSIER2	DPVD1IE	—	—	PVD1 deep software standby release signal enable bit	PVD1 deep software standby release signal enable bit
DPSIER2	DPVD2IE	—	—	PVD2 deep software standby release signal enable bit	PVD2 deep software standby release signal enable bit
	DRIICDIE	SDA2-DS deep standby release signal enable bit	SDA2-DS deep standby release signal enable bit	—	—
	DRIICCIE	SCL2-DS deep standby release signal enable bit	SCL2-DS deep standby release signal enable bit	—	—
	DUSBIE	USB suspend/resume deep standby release signal enable bit	USB suspend/resume deep standby release signal enable bit	—	—
DPSIER3	DCANIE	CRX1-DS deep standby release signal enable bit	CRX1-DS deep standby release signal enable bit	—	—
	DUSBFSIE	—	—	USBFS suspend/resume deep software standby release signal enable bit	USBFS suspend/resume deep software standby release signal enable bit
	DUSBHSIE	—	—	USBHS suspend/resume deep software standby release signal enable bit	USBHS suspend/resume deep software standby release signal enable bit
	DIWDTIE	—	—	IWDT underflow deep software standby release signal enable bit	IWDT underflow deep software standby release signal enable bit
	DSOSTDIE	—	—	Sub-clock oscillation stop detection deep software standby release signal enable bit	Sub-clock oscillation stop detection deep software standby release signal enable bit
	DVBATTADIE	—	—	VBATT tamper detection deep software standby release signal enable bit	VBATT tamper detection deep software standby release signal enable bit
DPSIER4	—	—	—	Deep software standby interrupt enable register 4	Deep software standby interrupt enable register 4
DPSIER5	—	—	—	Deep software standby interrupt enable register 5	Deep software standby interrupt enable register 5
DPSIFR2	DLVD1IF	LVD1 deep standby release flag bit	LVD1 deep standby release flag bit	—	—

Register	Bit	RX72M	RX72N	RX74M	RX74N
DPSIFR2	DLVD2IF	LVD2 deep standby release flag bit	LVD2 deep standby release flag bit	—	—
	DPVD1IF	—	—	PVD1 deep software standby release flag bit	PVD1 deep software standby release flag bit
DPSIFR2	DPVD2IF	—	—	PVD2 deep software standby release flag bit	PVD2 deep software standby release flag bit
	DRIICDIF	SDA2-DS deep standby release flag bit	SDA2-DS deep standby release flag bit	—	—
	DRIICCIF	SCL2-DS deep standby release flag bit	SCL2-DS deep standby release flag bit	—	—
	DUSBIF	USB suspend/resume deep standby release flag bit	USB suspend/resume deep standby release flag bit	—	—
DPSIFR3	DCANIF	CRX1-DS deep standby release flag bit	CRX1-DS deep standby release flag bit	—	—
	DUSBFSIF	—	—	USBFS suspend/resume deep software standby release flag bit	USBFS suspend/resume deep software standby release flag bit
	DUSBHSIF	—	—	USBHS suspend/resume deep software standby release flag bit	USBHS suspend/resume deep software standby release flag bit
	DIWDTIF	—	—	IWDT underflow deep software standby release flag bit	IWDT underflow deep software standby release flag bit
	DSOSTDIF	—	—	Sub-clock oscillation stop detection deep software standby release flag bit	Sub-clock oscillation stop detection deep software standby release flag bit
	DVBATTADIF	—	—	VBATT tamper detection deep software standby release flag bit	VBATT tamper detection deep software standby release flag bit
DPSIFR4	—	—	—	Deep software standby interrupt flag register 4	Deep software standby interrupt flag register 4
DPSIFR5	—	—	—	Deep software standby interrupt flag register 5	Deep software standby interrupt flag register 5
DPSIEGR2	DLVD1EG	LVD1 edge select bit	LVD1 edge select bit	—	—
	DLVD2EG	LVD2 edge select bit	LVD2 edge select bit	—	—
	DPVD1EG	—	—	PVD1 edge select bit	PVD1 edge select bit

Register	Bit	RX72M	RX72N	RX74M	RX74N
DPSIEGR2	DPVD2EG	—	—	PVD2 edge select bit	PVD2 edge select bit
	DRIICDEG	SDA2-DS edge select bit	SDA2-DS edge select bit	—	—
DPSIEGR2	DRIICCEG	SCL2-DS edge select bit	SCL2-DS edge select bit	—	—
DPSIEGR3	DCANIEG	CRX1-DS edge select bit	CRX1-DS edge select bit	—	—
	DIRQ16EG	—	—	IRQ16-DS pin edge select bit	IRQ16-DS pin edge select bit
	DIRQ17EG	—	—	IRQ17-DS pin edge select bit	IRQ17-DS pin edge select bit
	DIRQ18EG	—	—	IRQ18-DS pin edge select bit	IRQ18-DS pin edge select bit
	DIRQ19EG	—	—	IRQ19-DS pin edge select bit	IRQ19-DS pin edge select bit
	DIRQ20EG	—	—	IRQ20-DS pin edge select bit	IRQ20-DS pin edge select bit
	DIRQ21EG	—	—	IRQ21-DS pin edge select bit	IRQ21-DS pin edge select bit
	DIRQ22EG	—	—	IRQ22-DS pin edge select bit	IRQ22-DS pin edge select bit
	DIRQ23EG	—	—	IRQ23-DS pin edge select bit	IRQ23-DS pin edge select bit
DPSIEGR4	—	—	—	Deep software standby interrupt edge register 4	Deep software standby interrupt edge register 4
DPSBKRy	—	Deep standby backup register	Deep standby backup register	—	—
PLL1LDOCR	—	—	—	PLL1-LDO control register	PLL1-LDO control register
PLL2LDOCR	—	—	—	PLL2-LDO control register	PLL2-LDO control register
HOCOLDOCR	—	—	—	HOCO/LDO control register	HOCO/LDO control register
VSCR	—	—	—	Voltage scaling control register	Voltage scaling control register
SVSCR	—	—	—	SSTBY voltage scaling control register	SSTBY voltage scaling control register
LDOECR	—	—	—	LDO efficiency control register	LDO efficiency control register
DCCR	—	—	—	DSTBY condition control register	DSTBY condition control register
CLPCR	—	—	—	CPU low power control register	CPU low power control register

2.10 Battery Backup Function

Table 2.23 is Comparative Overview of Battery Backup Functions, and Table 2.24 is Comparison of Battery Backup Function Registers.

Table 2.23 Comparative Overview of Battery Backup Functions

Item	RX72M/RX72N	RX74M/RX74N
Scope of backup	• Sub-clock oscillator • Realtime clock (RTC)	All modules in the backup domain • Backup registers • Sub-clock oscillator • Power-down detector • Tamper detector • Realtime clock (RTC)
Backup registers	—	128 bytes The backup registers can immediately be erased in response to the detection of physical tampering.
Backup domain power-down detection	—	A backup domain reset signal is generated when the supply voltage for the backup domain has fallen below V_{PDR}.
Tamper event detection	—	When the tamper detector has detected an intrusion to the system, it indicates this by setting a flag and, if this is selected, generating an interrupt.
Protect Zone filter	—	Security attribute can be set for each register.

Table 2.24 Comparison of Battery Backup Function Registers

Register	Bit	RX72M/RX72N	RX74M/RX74N
VBSAR	—	—	VBATT security attribution register
BKRSABR	—	—	Backup register security attribute boundary register
VBATTMCR	—	—	Battery voltage measurement function control register
VBATTCR1	—	—	Battery backup function control register 1
VBATTCR2	—	—	Battery backup function control register 2
BKPSR	—	—	Backup domain power status register
TAMPSR	—	—	Tamper status register
TAMPCR	—	—	Tamper control register
TAMPCR2	—	—	Tamper control register 2
TCECR	—	—	Time capture event control register
TAMPICR1	—	—	Tamper/RTCIC input control register 1
TAMPICR2	—	—	Tamper/RTCIC input control register 2
TAMPICR3	—	—	Tamper/RTCIC input control register 3
TAMPIMR	—	—	Tamper/RTCIC input monitoring register
BKRCR	—	—	Backup register control register
BKRN	—	—	Backup register n

2.11 Register Write Protection Function

Table 2.25 is Comparative Overview of Register Write Protection Functions, and Table 2.26 is Comparison of Operating Mode Registers.

Table 2.25 Comparative Overview of Register Write Protection Functions

Item	RX72M/RX72N	RX74M/RX74N
PRC0 bit	• Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PACKCR, PLLCR, PLLCR2, PPLLCR, PPLLCR2, PPLLCR3, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR, CKOCR	• Registers related to the clock generation circuit: SCKDIVCR, SCKDIVCR2, SCKSCR, PLLCCR, PLLCR, BCKCR, MOSCCR, HOCOCR, HOCOCR2, MOCOCR, FLLCR1, FLLCR2, CKOCR, OSTDCR, OSTDSR, SOSTDCR, SOSTDSR, PLL2CCR, PLL2CR, PLLCCR2, PLL2CCR2, EBCKOCR, SDCKOCR, SCICKDIVCR, SCICKCR, SPICKDIVCR, SPICKCR, ADCCKDIVCR, ADCCKCR, GPTCKDIVCR, GPTCKCR, BCKADIVCR, ESWCKDIVCR, ESWPCKDIVCR, ESCCKDIVCR, ETHPCKDIVCR, DSMIFCKDIVCR, BCKACR, ESWCKCR, ESWPCKCR, ESCCKCR, ETHPCKCR, DSMIFCKCR, MOCOUTCR, HOCOUTCR, USBCKDIVCR, XSPICKDIVCR, CANFDCKDIVCR, USB60CKDIVCR, I3CCKDIVCR, USBCKCR, XSPICKCR, CANFDCKCR, USB60CKCR, I3CCKCR, MOSCSCR, HOCOSCR, MOCOSCR, MOSCWTCR, LOCOCR, LOCOUTCR, MOMCR, SOSCCR, SOMCR
PRC1 bit	• Registers related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, DPSBYCR, DPSIER0 to 3, DPSIFR0 to 3, DPSIEGR0 to 3 • Registers related to clock generation circuit: MOSCWTCR, SOSCWTCR, MOFCR, HOCOPCR	• Register related to the operating modes: SYSCR0 • Registers related to the low power consumption functions: PGSCR, PSSTCR2, PSSTCR4, PSSTCR5, PDCTRESWM, PDRAMSCR0, PDRAMSCR2, SBYCR, SSCR1, LPSCR, DPSBYCR, DPSIERn (n = 0-5), DPSIFRn (n = 0-5), DPSIEGRn (n = 0-4), PLL1LDOCR, PLL2LDOCR, HOCOLDOCR, LVOCR, VSCR, SVSCR, MWMCR, LDOECR, DCCR

Item	RX72M/RX72N	RX74M/RX74N
PRC1 bit	• Software reset register: SWRR	• Registers related to battery backup: BKRCR, TAMPICR1, BKRn (n = 0 to 127), VBATTCR1, VBATTCR2, BKPSR, TAMPSR, TAMPCR, TCECR, TAMPICR2, TAMPCR2, TAMPICR3 • Software reset register: SWRR
PRC3 bit	• Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	• Registers related to the PVD: PVD1CMPCR, PVD2CMPCR, PVD4CMPCR, PVD5CMPCR, PVD1CR0, PVD2CR0, PVD4CR0, PVD5CR0, PVD1CR1, PVD1SR, PVD2CR1, PVD2SR, PVD1FCR, PVD2FCR, PVD4FCR, PVD5FCR, PVDLR, VBATTMCR
PRC4 bit	—	• Registers related to the security function: ELCSARx (x = A to D), PSARx (x = B to F), MSSAR, PmSAR (m = 0 to 9, A to G), CACHESAR, IFUSR, LRMSAR, LRMSABARx (x = 0, 1), ICUSARx (x = A to D), ICU0SARx (x = 0 to 7), TEVTRCR, ICUNSACR, PRTZCR, BUSSARx (x = A to C), MMPUSARB, DMACCHSAR, DMACSAR, EXDMACCHSAR, EXDMACSAR, DTCSAR, SRAMSABARx (x = 0, 1), SRAMSAR, MSAR, CGFSAR, RSTSAR, LPMSAR, PVDSAR, VBSAR, DPFSAR, DPFSAR1, RSCSAR, PGCSAR, BKRSABR
PRC5 bit	—	• Registers related to the resets: SYRSTMSK0, SYRSTMSK2, TEMPRCR, TEMPRLR

Table 2.26 Comparison of Register Write Protection Function Registers

Register	Bit	RX72M/RX72N	RX74M/RX74N
PRCR (RX72M/ RX72N) PRCR_S (RX74M/ RX74N)	PRC1	Protect bit 1 Enables writing to the registers related to operating modes, clock generation circuit, low power consumption, and software reset. 0: Write disabled 1: Write enabled	Protect bit 1 Enables writing to the registers related to operating modes, low power consumption, battery backup, and software reset. 0: Write disabled 1: Write enabled
	PRC4	—	Protect bit 4
	PRC5	—	Protect bit 5
PRCR_NS	—	—	Protect register

2.12 Exception Handling

Table 2.27 is Comparative Overview of Exception Handling, Table 2.28 is Comparison of Vectors, and Table 2.29 is Comparison of Instructions for Returning from Exception Handling Routine.

Table 2.27 Comparative Overview of Exception Handling

Item	RX72M/RX72N	RX74M/RX74N
Exception events	• Undefined instruction exception • Privileged instruction exception • Access exceptions • Address exceptions • Single-precision floating-point exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap	• Undefined instruction exception • Privileged instruction exception • Access exceptions • Address exceptions • Single-precision floating-point exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap • Secure exception

Table 2.28 Comparison of Vectors

Item	RX72M/RX72N	RX74M/RX74N
Exception without world transitions		
Undefined instruction exception	Exception vector table (EXTB)	Exception vector table in the current world
Privileged instruction exception	Exception vector table (EXTB)	Exception vector table in the current world
Access exception	Exception vector table (EXTB)	Exception vector table in the current world
Access exception	Exception vector table (EXTB)	Exception vector table in the current world
Single-precision floating-point exception	Exception vector table (EXTB)	Exception vector table in the current world
Reset	Exception vector table (EXTB)	FFFF FFFCh
Non-maskable interrupts	Exception vector table (EXTB)	Exception vector table in the current world
Interrupt: Fast interrupt	FINTV	FINTV
Interrupt: Other than above	Interrupt vector table (INTB)	Interrupt vector table in the current world
Unconditional trap	Interrupt vector table (INTB)	Interrupt vector table in the current world

Table 2.29 Comparison of Instructions for Returning from Exception Handling Routine

Item		RX72M/RX72N	RX74M/RX74N
Undefined instruction exception		RTE	RTE
Privileged instruction exception		RTE	RTE
Access exception		RTE	RTE
Address exception		RTE	RTE
Single-precision floating-point exception		RTE	RTE
Reset		Return is impossible	Return is impossible
Non-maskable interrupt (Normal acceptance)		Prohibited	RTE*2
Non-maskable interrupt (World-transition acceptance)		—	TRRTE*2
Interrupt (Normal acceptance)	Fast interrupt	RTFI	RTFI
	Other than above	RTE	RTE
Interrupt (world transition)	Other than above	—	TRRTE
Unconditional trap (Normal acceptance)		RTE	RTE
Unconditional trap (World-transition acceptance)		—	TRRTE
Secure exceptions		—	TRRTE*1

Notes: 1. Returning to the original program is not possible.
2. Returning to the original program is not recommended. If the destination world of the non-maskable interrupt is secure or non-secure, returning to the original program is in any case not possible.

2.13 Interrupt Controller

Table 2.30 is Comparative Overview of Interrupt Controllers, and Table 2.31 is Comparison of Interrupt Controller Registers.

Table 2.30 Comparative Overview of Interrupt Controllers

Item		RX72M (ICUD)/RX72N (ICUD)	RX74M (ICUM)/RX74N (ICUM)
Interrupts	Peripheral interrupts	Interrupts from peripheral modules • Interrupt detection method: Edge detection/level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as an interrupt source. — Group IE0 interrupt: Interrupt sources of coprocessors that use ICLK as the operating clock (edge detection) — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207. • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.	Interrupts from peripheral modules • Interrupt detection method: Edge detection/level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as an interrupt source. — Group IL0 interrupt: Interrupt sources of coprocessors that use ICLK as the operating clock — Group BL0 and Group BL1 interrupts: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0 to Group AL6 interrupts: Interrupt sources of peripheral modules that use PCLKA as the operating clock • Software configurable interrupt: Any of the interrupt sources for peripheral modules can be assigned to interrupt vector numbers 128 to 255.
	External pin interrupt	Interrupt by the input signal to the IRQi pin (i = 0 to 15) • Interrupt detection method: Detection of low level, falling edge, rising edge, rising and falling edges One of these detection methods can be set for each source. • Digital filter can be used to remove noise.	Interrupt by the input signal to the IRQi pin (i = 0 to 31) • Interrupt detection method: Detection of low level, falling edge, rising edge, rising and falling edges One of these detection methods can be set for each source. • Digital filter can be used to remove noise.

Item		RX72M (ICUD)/RX72N (ICUD)	RX74M (ICUM)/RX74N (ICUM)
Interrupts	Software interrupt	• Interrupt request can be generated by writing to a register. • Two interrupt sources	• Interrupt request can be generated by writing to a register. • Two interrupt sources
	Interrupt priority	Priority level can be set with interrupt source priority register r (IPRr) (r = 000 to 255).	Priority level can be set with interrupt source priority register r (IPRr) (r = 000 to 255).
	Fast interrupt function	CPU interrupt response time can be reduced. This function can be used for only one interrupt source.	Fast interrupt response due to the use of internal CPU resources instead of a stack. This function can be used for only one interrupt source.
	DTC/DMAC control	Interrupt sources can be used to start the DTC and DMAC.	Interrupt sources can be used to start the DTC and DMAC.
	EXDMAC control	• Interrupt selected by software configurable interrupt B source select register 144 or software configurable interrupt A source select register 208 can be used to start EXDMAC0. • Interrupt selected by software configurable interrupt B source select register 145 or software configurable interrupt A source select register 209 can be used to start EXDMAC1.	Any two of the interrupt sources assigned to software configurable interrupts can be used to start EXDMAC0 and EXDMAC1, respectively.
Non-maskable interrupts	NMI pin interrupt	Interrupt by the input signal to the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter can be used to remove noise.	Interrupt by the input signal to the NMI pin • Interrupt detection: Falling edge/rising edge • Digital noise filter can be used to remove noise.
	Oscillation stop detection interrupt (RX72M/72N) Main clock oscillation stop detection interrupt (RX74M/74N)	This interrupt occurs when the main clock oscillator stop is detected.	This interrupt occurs when the main clock oscillator stop is detected.
	Sub clock oscillation stop detection interrupt	—	This interrupt occurs when the sub clock oscillator stop is detected.
	WDT underflow/refresh error interrupt	This interrupt occurs when the watchdog timer (WDT) underflows or a refresh error occurs.	This interrupt occurs when the watchdog timer (WDT) underflows or a refresh error occurs.
	IWDT underflow/refresh error interrupt	This interrupt occurs when the independent watchdog timer (IWDT) underflows or a refresh error occurs.	This interrupt occurs when the independent watchdog timer (IWDT) underflows or a refresh error occurs.
	Voltage monitoring 1 interrupt	Interrupt from voltage detection circuit 1 (LVD1)	Interrupt from voltage detection circuit 1 (PVD1)
	Voltage monitoring 2 interrupt	Interrupt from voltage detection circuit 2 (LVD2)	Interrupt from voltage detection circuit 2 (PVD2)

Item		RX72M (ICUD)/RX72N (ICUD)	RX74M (ICUM)/RX74N (ICUM)
Non-maskable interrupts	RAM error interrupt	This interrupt occurs when a parity check error is detected in the RAM (including the expanded RAM) or an ECC error is detected in the ECCRAM.	—
	Double-precision floating-point exceptions	Exceptions from double-precision floating-point coprocessor	Exceptions from double-precision floating-point coprocessor
	Bus error interrupt	—	This interrupt occurs when a bus error occurs.
	Common memory error interrupt	—	This interrupt occurs when an ECC error occurs in SRAM0 or SRAM1.
	Local memory error interrupt	—	This interrupt occurs when an ECC error occurs in the cache memory or LRAM in the CPU.
	Code MRAM read access error interrupt	—	This interrupt occurs when a read access error occurs in the code area of MRAM.
	Extra MRAM read access error interrupt	—	This interrupt occurs when a read access error occurs in the extra area of MRAM.

Table 2.31 Comparison of Interrupt Controller Registers

Register	Bit	RX72M (ICUD)/RX72N (ICUD)	RX74M (ICUM)/RX74N (ICUM)
IPRr	IPR[3:0] (RX72M/72N) IPR[4:0] (RX74M/74N)	Interrupt priority level select bits b3 b0 0 0 0 0: Level 0 (interrupt disabled) 0 0 0 0: Level 1 0 0 0 1: Level 2 0 0 1 0: Level 3 : : 1 1 1 1: Level 15	Interrupt priority level select bits b4 b0 0 0 0 0 0: Level 0 (interrupt disabled) 0 0 0 0 0: Level 1 0 0 0 0 1: Level 2 0 0 1 0 0: Level 3 : : 0 1 1 1 1: Level 15 (highest in Non-secure) 1 0 0 0 0: Level 16 1 0 0 0 1: Level 17 1 0 0 1 0: Level 18 : : 1 1 1 1 1: Level 31
IRQCRi	IRQMD[1:0]	IRQ detection select bits b3 b2 0 0: Low level 0 1: Falling edge 1 0: Rising edge 1 1: Rising and falling edges	IRQ detection select bits b1 b0 0 0: Falling edge 0 1: Rising edge 1 0: Rising and falling edges 1 1: Low level
	FLTMD	—	IRQ digital noise filter operation mode select bit
	FCLKSEL [2:0]	—	IRQ digital noise filter sampling clock select bits
	FLTEN	—	IRQ digital noise filter enable bit
IRQFLTE0	—	IRQ pin digital filter enable register 0	—

Register	Bit	RX72M (ICUD)/RX72N (ICUD)	RX74M (ICUM)/RX74N (ICUM)
IRQFLTE1	—	IRQ pin digital filter enable register 1	—
IRQFLTC0	—	IRQ pin digital filter setting register 0	—
IRQFLTC1	—	IRQ pin digital filter setting register 1	—
NMISR	—	Non-maskable interrupt status register (b0 to b7)	Non-maskable interrupt status register (b0 to b31)
	NMIST	NMI status flag (b0)	NMI pin interrupt status flag (b7)
	OSTST	Oscillation stop detection interrupt status flag (b1)	Main clock oscillation stop detection interrupt status flag (b6)
	WDTST	WDT underflow/refresh error status flag (b2)	WDT underflow/refresh error status flag (b1)
	IWDTST	IWDT underflow/refresh error status flag (b3)	IWDT underflow/refresh error status flag (b0)
	LVD1ST (RX72M/72N) PVD1ST (RX74M/74N)	Voltage monitoring 1 interrupt status flag (b4)	Voltage monitoring 1 interrupt status flag (b2)
	LVD2ST (RX72M/72N) PVD2ST (RX74M/74N)	Voltage monitoring 2 interrupt status flag (b5)	Voltage monitoring 2 interrupt status flag (b3)
	EXNMIST	Expanded non-maskable interrupt status flag	—
	SOSTST	—	Sub clock oscillation stop detection interrupt status flag
	BUSST	—	Bus error interrupt status flag
	CMST	—	Common memory error interrupt status flag
	LMST	—	Local memory error interrupt status flag
	DPFPUST	—	Double-precision floating-point exception status flag
	MRCRDST	—	Code MRAM read access error interrupt status flag
	MRERDST	—	Extra MRAM read access error interrupt status flag
NMIER	—	Non-maskable interrupt enable register (b0 to b7)	Non-maskable interrupt enable register (b0 to b31)
	NMIEN	NMI pin interrupt enable bit (b0)	NMI pin interrupt enable bit (b7)
	OSTEN	Oscillation stop detection interrupt enable bit (b1)	Main clock oscillation stop detection interrupt enable bit (b6)
	WDTEN	WDT underflow/refresh error enable bit (b2)	WDT underflow/refresh error enable bit (b1)
	IWDTEN	IWDT underflow/refresh error enable bit (b3)	IWDT underflow/refresh error enable bit (b0)
	LVD1EN (RX72M/72N) PVD1EN (RX74M/74N)	Voltage monitoring 1 interrupt enable bit (b4)	Voltage monitoring 1 interrupt enable bit (b2)
	LVD2EN (RX72M/72N) PVD2EN (RX74M/74N)	Voltage monitoring 2 interrupt enable bit (b5)	Voltage monitoring 2 interrupt enable bit (b3)

Register	Bit	RX72M (ICUD)/RX72N (ICUD)	RX74M (ICUM)/RX74N (ICUM)
NMIER	EXNMIEN	Expanded non-maskable interrupt enable bit	—
	SOSTEN	—	Sub clock oscillation stop detection interrupt enable bit
	BUSEN	—	Bus error interrupt enable bit
	CMEN	—	Common memory error interrupt enable bit
	LMEN	—	Local memory error interrupt enable bit
	DPFPUEN	—	Double-precision floating-point exception enable bit
	MRCRDEN	—	Code MRAM read access error interrupt enable bit
	MRERDEN	—	Extra MRAM read access error interrupt enable bit
NMICLR	—	Non-maskable interrupt status clear register (b0 to b7)	Non-maskable interrupt status clear register (b0 to b31)
	NMICLR	NMI clear bit (b0)	NMI clear bit (b7)
	OSTCLR	OST clear bit (b1)	OST clear bit (b6)
	WDTCLR	WDT clear bit (b2)	WDT clear bit (b1)
	IWDTCLR	IWDT clear bit (b3)	IWDT clear bit (b0)
	LVD1CLR (RX72M/72N) PVD1CLR (RX74M/74N)	LVD1 clear bit (b4)	PVD1 clear bit (b2)
	LVD2CLR (RX72M/72N) PVD2CLR (RX74M/74N)	LVD2 clear bit (b5)	PVD2 clear bit (b3)
	SOSTCLR	—	SOST clear bit (b5)
NMICR	NMIMD	NMI detection set bit (b3)	NMI detection select bit (b0)
	NFLTMD	—	NMI digital noise filter operation mode select bit
	NFCLKSEL [2:0]	—	NMI digital noise filter sampling clock bits
	NFLTEN	—	NMI digital noise filter enable bit
EXNMISR	—	Expanded non-maskable interrupt status register	—
EXNMIER	—	Expanded non-maskable interrupt enable register	—
EXNMICLR	—	Expanded non-maskable interrupt status clear register	—
NMIFLTE	—	NMI pin digital filter enable register	—
NMIFLTC	—	NMI pin digital filter setting register	—
GRPIE0	—	Group IE0 interrupt request register	—
GRPBE0	—	Group BE0 interrupt request enable register	—
GRPILi_NS	—	—	Group ILi non-secure interrupt request register

Register	Bit	RX72M (ICUD)/RX72N (ICUD)	RX74M (ICUM)/RX74N (ICUM)
GRPBL0/ GRPBL1/ GRPBL2 (RX72M/RX72N) GRPBLi_NS (RX74M/RX74N)	—	Group BL0/BL1/BL2 interrupt request enable register	Group BLi non-secure interrupt request register (i = 0, 1)
GRPAL0/ GRPAL1 (RX72M/RX72N) GRPALi_NS (RX74M/RX74N)	—	Group AL0/AL1 interrupt request enable register	Group ALi non-secure interrupt request register (i = 0 to 6)
GRPILi_S	—	—	Group ILi secure interrupt request register
GRPBLi_S	—	—	Group BLi secure interrupt request register
GRPALi_S	—	—	Group ALi secure interrupt request register
GENIE0	—	Group IE0 interrupt request enable register	—
GENBE0	—	Group BE0 interrupt request enable register	—
GENILi_NS	—	—	Group ILi non-secure interrupt request enable register
GENBL0/ GENBL1/ GENBL2 (RX72M/RX72N) GENBLi_NS (RX74M/RX74N)	—	Group BL0/BL1/BL2 interrupt request enable register	Group BLi non-secure interrupt request enable register (i = 0, 1)
GENAL0/ GENAL1 (RX72M/RX72N) GENALi_NS (RX74M/RX74N)	—	Group AL0/AL1 interrupt request enable register	Group ALi non-secure interrupt request enable register (i = 0 to 6)
GENILi_S	—	—	Group ILi secure interrupt request enable register
GENBLi_S	—	—	Group BLi secure interrupt request enable register
GENALi_S	—	—	Group ALi secure interrupt request enable register
GCRIE0	—	Group IE0 interrupt clear register	—
GCRBE0	—	Group BE0 interrupt clear register	—
PIBRk	—	Software configurable interrupt B request register k	—
PIARk	—	Software configurable interrupt A request register k	—

Register	Bit	RX72M (ICUD)/RX72N (ICUD)	RX74M (ICUM)/RX74N (ICUM)
PIXRk	—	—	Software configurable interrupt request register Xk (k = 0, 1)
PIRk	—	—	Software configurable interrupt request register k (k = 0 to 127)
SLIBXRn	—	Software configurable interrupt B source select register Xn	—
SLIBRn	—	Software configurable interrupt B source select register n	—
SLIARn	—	Software configurable interrupt A source select register n	—
SLIXRn	—	—	Software configurable interrupt source select register Xn (n = 128 to 143)
SLIRn	—	—	Software configurable interrupt source select register n (n = 144 to 255)
SELEXDR	—	EXDMAC trigger select register	—
SELEXDRn	—	—	EXDMAC trigger select register n
SLIPRCR	—	Software configurable interrupt source select register write protect register	—
SLIPRCR_NS	—	—	Non-secure software configurable interrupt source select register write protect register
SLIPRCR_S	—	—	Secure software configurable interrupt source select register write protect register
ICUSARA	—	—	ICU security attribution register A
ICUSARB	—	—	ICU security attribution register B
ICUSARC	—	—	ICU security attribution register C
ICUSARD	—	—	ICU security attribution register D
ICU0SAR0	—	—	ICU security attribution register 0
ICU0SAR1	—	—	ICU security attribution register 1
ICU0SAR2	—	—	ICU security attribution register 2
ICU0SAR3	—	—	ICU security attribution register 3
ICU0SAR4	—	—	ICU security attribution register 4
ICU0SAR5	—	—	ICU security attribution register 5
ICU0SAR6	—	—	ICU security attribution register 6
ICU0SAR7	—	—	ICU security attribution register 7
TEVTRCR	—	—	Trusted event route control register
ICUNSACR	—	—	ICU non-secure access control register
PRTZCR	—	—	Protect zone interrupt control register

2.14 Buses

Table 2.32 is Comparative Overview of Buses, and Table 2.33 is Comparison of Bus Registers.

Table 2.32 Comparative Overview of Buses

	RX72N/RX72M		RX74N/RX74M	
Bus Type	**Bus Name**	**Synchronization Clock**	**Bus Name**	**Synchronization Clock**
CPU bus	Instruction bus	ICLK	CPU0IFBI	CPUCLK0
	Operand bus		CPU0OABI	
Memory bus	Memory bus 1 Memory bus 2 Memory bus 3	ICLK	S0BI S1BI MRC0BI MRC1BI MRE0BI LRAM0BI LRAM1BI	ICLK MRICLK MRPCLK CPUCLK0
Internal main bus	Internal main bus 1 Internal main bus 2	ICLK	CPU0IFAXI CPU0IFAHB CPU0OAAXI CPU0OAAHB DMAC/DTC0BI EXDMACBI EDMACBI	ICLK
Internal peripheral bus	Internal peripheral bus 1 Internal peripheral bus 2 Internal peripheral bus 3 Internal peripheral bus 4 Internal peripheral bus 5 Internal peripheral bus 6	ICLK PCLKB PCLKA FCLK	PBBI PABI PIBI PS0BI PC0BI SPI0MBI XSPI0BI XSPI1BI PSBI	ICLK PCLKB PCLKA CPUCLK0 MRPCLK
External bus	CS area SDRAM area	BCLK SDCLK	ECBI	BCLK

Table 2.33 Comparison of Bus Registers

Register	Bit	RX72M/RX72N	RX74M/RX74N
BUSSARA	—	—	Bus security attribution register A
BUSSARB	—	—	Bus security attribution register B
BUSSARC	—	—	Bus security attribution register C
BERCLR	—	Bus error status clear register	—
BEREN	—	Bus error monitoring enable register	—
BERSR1	—	Bus error status register 1	—
BERSR2	—	Bus error status register 2	—
BUSPRI	—	Bus priority control register	—
EBMAPCR	—	Extended bus master priority control register	—
EXBERR	—	—	EXBUS error status register
EXBEREN	—	—	EXBUS error enable register
EXBECLR	—	—	EXBUS error status clear register
EXBEAD	—	—	EXBUS error address register

Register	Bit	RX72M/RX72N	RX74M/RX74N
EXHLDEN	—	—	EXBUS hold enable register
BUSSABT0 MRE0BI/ BUSSABT0 S0BI/ BUSSABT0 S1BI/ BUSSABT0 ECBI/ BUSSABT0 XSPI0BI/ BUSSABT0 XSPI1BI/ BUSSABT0 PBBI/ BUSSABT0 PABI/ BUSSABT0 PIBI/ BUSSABT0 PSBI/ BUSSABT0 PS0BI	—	—	Bus slave arbitration control register 0
BUSSABT1 MRC0BI/ BUSSABT1 MRC1BI	—	—	Bus slave arbitration control register 1
BUSERRST ATCPU0IF/ BUSERRST ATCPU0OA/ BUSERRST ATDMAC0/ BUSERRST ATEXDMAC/ BUSERRST ATEDMAC/ BUSERRST ATXSPI0/ BUSERRST ATXSPI1	—	—	Bus error status register

Register	Bit	RX72M/RX72N	RX74M/RX74N
BUSERRCLR CPU0IF/ BUSERRCLR CPU0OA/ BUSERRCLR DMAC0/ BUSERRCLR EXDMAC/ BUSERRCLR EDMAC/ BUSERRCLR XSPI0/ BUSERRCLR XSPI1	—	—	Bus error clear register
BUSOAD	—	—	Bus operation after detection register
BUSOADPT	—	—	Bus operation after detection protect register
MBWERRSTAT	—	—	Master bufferable write error status register
MBWERRCLR	—	—	Master bufferable write error clear register
BUSINTEN CPU0IF/ BUSINTEN CPU0OA/ BUSINTEN DMAC0/ BUSINTEN EXDMAC/ BUSINTEN EDMAC/ BUSINTEN XSPI0/ BUSINTEN XSPI1	—	—	Bus error interrupt enable register

2.15 Memory-Protection Unit

Table 2.34 is Comparative Overview of Memory-Protection Units, and Table 2.35 is Comparison of Memory-Protection Unit Registers.

Table 2.34 Comparative Overview of Memory-Protection Units

Item		RX72M (MPU)/RX72N (MPU)	RX74M (MPU)/RX74N (MPU)
Number of units		1 unit	3 units CPU MPU Secure access Non-secure access Bus master MPU
CPU MPU	Region to be covered by memory protection and processor mode	0000 0000h to FFFF FFFFh (in user mode) No memory protection in supervisor mode	0000 0000h to FFFF FFFFh (in user mode) No memory protection applies in supervisor mode and only the cache attribute settings are effective.
	Number of regions	8	8
	Page size (smallest unit of protection)	16 bytes	32 bytes
	Specifying addresses of individual regions	Setting the page numbers where regions start and end	Setting the page numbers where regions start and end
	Setting to make memory protection effective or ineffective in individual regions	A V (valid) bit in each region-n end page number register (REPAGEn) makes the settings effective or ineffective for the corresponding region (n = 0 to 7).	A V (valid) bit in each region-n end page number register (REPAGEn) makes the settings effective or ineffective for the corresponding region (n = 0 to 7).
	Access-control information settings for individual regions	Instruction execution: Permission to execute Operand access: Permission to read, permission to write	Instruction execution: Permission to execute Operand access: Permission to read, permission to write
	Cache attribute information settings for individual regions	—	Set cache attributes for individual regions. Instruction access: Not cached Instruction cached Data access: Not cached Cached (write-through) Cached (write-back)
	Start of memory-protection operations	After the memory-protection unit has been enabled, access monitoring starting up with the transition to user mode.	After the memory-protection unit has been enabled, access monitoring starting up with the transition to user mode.
	Memory-protection error processing	Generation of access exceptions	Generation of access exceptions

Item		RX72M (MPU)/RX72N (MPU)	RX74M (MPU)/RX74N (MPU)
CPU MPU	Addresses where memory-protection errors are generated	Address in instruction execution: The PC value is preserved on the stack. Address in operand access: The address is stored in the data memory-protection error address register (MPDEA).	Address in instruction execution: The PC value is preserved on the stack. Address in operand access: The address is stored in the data memory-protection error address register (MPDEA).
	Determining the reasons for memory-protection errors	The memory-protection error status register (MPESTS) holds indicators of the reason.	The memory-protection error status register (MPESTS) holds indicators of the reason.
	Background region access control setting	Access-control information can be set for the background region (the whole address space).	Access-control information can be set for the background region (the whole address space).
	Background region cache settings	—	Caches can be set for the background region (the whole address space).
	Processing where regions overlap	The access-control information for access to an overlap between regions is the logical OR of the attributes for the given regions, and permission is given priority.	If region settings overlap for an address and the access control information for these regions is different, the information is handled as the logical OR of each bit setting. As a result, permission is given priority in access control. The information for the cache attribute is also handled in the same way, as the logical OR of the settings.
Bus master MPU	Memory protection (except for the CPU)	—	Memory protection function for the bus master
	Number of regions	—	xSPI0: 4 regions; xSPI1: 4 regions The parameter settings determine the numbers in the respective sets of regions.
	Protected region	—	0000 0000h to FFFF FFFFh
	Specifying addresses of individual regions	—	The start/end addresses of individual regions can be set.
	Memory protection permission/ prohibition setting for individual regions	—	Setting for permission or prohibition for the relevant region
	Access control settings for individual regions	—	Permitting writing or reading, permitting non-privileged access
	Error detection operation	—	Reset or error response
	Register protection	—	Protection against illegal writing

Table 2.35 Comparison of Memory-Protection Unit Registers

Register	Bit	RX72M (MPU)/RX72N (MPU)	RX74M (MPU)/RX74N (MPU)
RSPAGEn	DCA[1:0]	—	Data cache attribute setting bits
	ICA	—	Instruction cache attribute setting bit
	RSPN[27:0] (RX72M/72N) RSPN[26:0] (RX74M/74N)	Region-start page number bits	Region start page number bits
REPAGEn	REPN[27:0] (RX72M/72N) REPN[26:0] (RX74M/74N)	Region-end page number bits	Region-end page number bits
MPBAC	DCA[1:0]	—	Data cache attribute setting bits
	ICA	—	Instruction cache attribute setting bit
MMPUSARB	—	—	Master memory-protection unit security attribute register B
MMPUSXSPImn	—	—	MMPU start address register for xSPI
MMPUEXSPImn	—	—	MMPU end address register for xSPI
MMPUACXSPImn	—	—	MMPU access control register for xSPI
MMPUENXSPIm	—	—	MMPU enable register for xSPI
MMPUENPTXSPIm	—	—	MMPU enable protect register for xSPI
MMPURPTXSPIm	—	—	MMPU region protect register for xSPI
MMPUOAD	—	—	MMPU post-detection operation register
MMPUOADPT	—	—	MMPU post-detection operation protect register

2.16 DMA Controller

Table 2.36 is Comparative Overview of DMA Controllers, and Table 2.37 is Comparison of DMA Controller Registers.

Table 2.36 Comparative Overview of DMA Controllers

Item		RX72M (DMACAa)/RX72N (DMACAa)	RX74M (DMACAa)/RX74N (DMACAa)
Number of channels		8 (DMACm (m = 0 to 7))	8 (DMAC0m (m = 0 to 7))
Transfer space		512 Mbytes (0000 0000h to 0FFF FFFFh and F000 0000h to FFFF FFFFh excluding reserved areas)	4 Gbytes (0000 0000h to FFFF FFFFh excluding reserved areas)
Maximum transfer volume		64M data (Maximum number of transfers in block transfer mode: 1024 data × 65536 blocks)	64M data (Maximum number of transfers in block transfer mode: 1024 data × 65536 blocks)
DMA activation source		Request source selectable for each channel — Software trigger — Interrupt requests from peripheral modules or trigger input to external interrupt input pins	Activation source selectable for each channel — Software trigger — Interrupt requests from peripheral modules or trigger input to external interrupt input pins
Channel priority		Channel 0 > Channel 1 > Channel 2 > Channel 3... > Channel 7 (Channel 0: Highest)	Selectable from fixed priority or round-robin Fixed priority: Channel 0 > channel 1 > channel 2 > channel 3... > channel 7 > DTC (channel 0: Highest) Round-robin
Transfer data	Single data	Bit length: 8, 16, 32 bits	Bit length: 8, 16, 32, 64 bits
	Block size	Number of data: 1 to 1024	Number of data: 1 to 1024
Transfer mode	Normal transfer mode	One data transfer by one DMA transfer request Free running mode (setting in which total number of data transfers is not specified) settable	One data transfer by one DMA transfer request Free running mode (setting in which total number of data transfers is not specified) settable
	Repeat transfer mode	One data transfer by one DMA transfer request Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. Maximum settable repeat size: 1024	One data transfer by one DMA transfer request Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. Maximum settable repeat size: 1024 Selectable free running function
	Block transfer mode	One block data transfer by one DMA transfer request Maximum settable block size: 1024 data	One block data transfer by one DMA transfer request Maximum settable block size: 1024 data Selectable free running function
	Repeat-block transfer mode	—	One block data transfer by one DMA transfer request Maximum settable block size: 1024 data Block transfer can be repeated Maximum settable repeat size: 64K Selectable free running function

Item		RX72M (DMACAa)/RX72N (DMACAa)	RX74M (DMACAa)/RX74N (DMACAa)
Selective functions	Extended repeat area function	Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed Area of 2 bytes to 128 Mbytes separately settable as extended repeat area for transfer source and destination	Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed Area of 2 bytes to 128 Mbytes separately settable as extended repeat area for transfer source and destination
Processing on DMA transfer error		—	When DMA transfer error occurs, the transfer that caused the error is stopped For clearing requests to the registers for activation request in the ICU, clearing targets are selectable for each channel or all channels.
Interrupt request	Transfer end interrupt	Generated when the specified number of transfers is completed in normal transfer mode Generated when the specified repeat count of transfers is completed in repeat transfer mode Generated when the specified block count of transfers is completed in block transfer mode	Generated on completion of transferring data volume specified by the transfer counter
	Transfer escape end interrupt	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.	Generated when the repeat size of data transfer is completed. Generated when the source address extended repeat area overflows. Generated when the destination address extended repeat area overflows.
Event link function		An event link request is generated after each data transfer (for block transfer, after each block is transferred).	An event link request is generated after each data transfer (for block transfer, after each block is transferred).
Power consumption reduction function		Module-stop state can be set.	Module-stop state can be set.
Protect Zone Filter		—	Security attribute can be set for each channel.

Table 2.37 Comparison of DMA Controller Registers

Register	Bit	RX72M (DMACAa)/RX72N (DMACAa)	RX74M (DMACAa)/RX74N (DMACAa)
DMACCHSAR	—	—	DMAC channel security attribution register
DMACSAR	—	—	DMA controller security attribution register
DMSAR	—	DMA source address register Specifies the transfer source start address. 0000 0000h to 0FFF FFFFh (256 Mbytes) F000 0000h to FFFF FFFFh (256 Mbytes)	DMA source address register Specifies the transfer source start address. 0000 0000h to FFFF FFFFh (4 Gbytes)
DMSRR	—	—	DMA source reload address register
DMDAR	—	DMA destination address register Specifies the transfer destination start address. 0000 0000h to 0FFF FFFFh (256 Mbytes) F000 0000h to FFFF FFFFh (256 Mbytes)	DMA destination address register Specifies the transfer destination start address. 0000 0000h to FFFF FFFFh (4 Gbytes)
DMDRR	—	—	DMA destination reload address register
DMCRB	—	DMA block transfer count register The corresponding register has a length of 16 bits.	DMA block transfer count register The corresponding register has a length of 32 bits.
DMTMD	SZ[1:0]	Transfer data size select bits b9 b8 0 0: 8 bits 0 1: 16 bits 1 0: 32 bits 1 1: Setting prohibited	Data transfer size bits b9 b8 0 0: 8 bits 0 1: 16 bits 1 0: 32 bits 1 1: 64 bits
	TKP	—	Transfer keeping bit
DMAMD	DADR	—	Destination address update setting after reload bit
	SADR	—	Source address update setting after reload bit
DMSBS	—	—	DMA source buffer size register
DMDBS	—	—	DMA destination buffer size register
DMBWR	—	—	DMA bufferable write enable register
DMECHR	—	—	DMAC error channel register
DMCTL	—	—	DMAC control register

2.17 EXDMA Controller

Table 2.38 is Comparative Overview of EXDMA Controllers, and Table 2.39 is Comparison of EXDMA Controller Registers.

Table 2.38 Comparative Overview of EXDMA Controllers

Item		RX72M (EXDMACa)/ RX72N (EXDMACa)	RX74M (EXDMACAa)/ RX74N (EXDMACAa)
Number of channels		2 (EXDMAC0 and EXDMAC1)	2 (EXDMAC0n (n = 0, 1))
Transfer space		512 Mbytes (External areas at addresses 0000 0000h to 0FFF FFFFh and F000 0000h to FFFF FFFFh excluding reserved areas)	SRAM0/SRAM1 (Secure: 8200 0000h to 8217 FFFFh, Non-secure: 0200 0000h to 0217 FFFFh) CS0 to CS7/SDRAM (7000 0000h to 7FFF FFFFh) xSPI0/xSPI1 (2000 0000h to 5FFF FFFFh)
Maximum transfer volume		1 M data (Maximum number of transfer operations in block transfer mode: 1,024 data × 1,024 blocks)	64M data (Maximum number of transfers in block transfer mode: 1024 data × 65536 blocks)
DMA activation source		Request source selectable from the following three sources for each channel Software trigger External DMA transfer request input DMA transfer request from peripheral modules (TPU1.TRGA or MTU1.TRGA) (Channel 0: a software configurable interrupt B request from TPU1.TRGA selected in ICU.SLIBR144 or a software configurable interrupt A request from MTU1.TRGA selected in ICU.SLIAR208; Channel 1: a software configurable interrupt B request from TPU1.TRGA selected in ICU.SLIBR145 or a software configurable interrupt A request from MTU1.TRGA selected in ICU.SLIAR209)	Activation source selectable for each channel Software trigger Interrupt requests from peripheral modules or trigger input to external interrupt input pins
Channel priority		Channel 0 > Channel 1 (Channel 0: Highest)	Selectable from fixed priority or round-robin Fixed priority: Channel 0 > channel 1 (channel 0: Highest) Round-robin
Transfer data	Single data	Bit length: 8, 16, 32 bits	Bit length: 8, 16, 32, 64 bits
	Block size	Number of data: 1 to 1,024 data	Number of data: 1 to 1024
Transfer mode	Normal transfer mode	One data transfer by one DMA transfer request Free running mode (setting in which total number of data transfer operations is not specified) settable	One data transfer by one DMA transfer request Free running mode (setting in which total number of data transfers is not specified) settable
	Repeat transfer mode	One data transfer by one DMA transfer request Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. Maximum settable repeat size: 1,024 data	One data transfer by one DMA transfer request Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. Maximum settable repeat size: 1024 Selectable free running function

Item		RX72M (EXDMACa)/ RX72N (EXDMACa)	RX74M (EXDMACAa)/ RX74N (EXDMACAa)
Transfer mode	Block transfer mode	One block data transfer by one DMA transfer request Maximum settable block size: 1,024 data	One block data transfer by one DMA transfer request Maximum settable block size: 1024 data Selectable free running function
	Cluster transfer mode	One cluster data transfer by one DMA transfer request Maximum settable cluster size: 8 data (32 bytes)	—
	Repeat-block transfer mode	—	One block data transfer by one DMA transfer request Maximum settable block size: 1024 data Block transfer can be repeated Maximum settable repeat size: 64K Selectable free running function
Selective functions	Extended repeat area function	Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed Area of 2 bytes to 128 Mbytes separately settable as extended repeat area for transfer source and destination	Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed Area of 2 bytes to 128 Mbytes separately settable as extended repeat area for transfer source and destination
Processing on DMA transfer error		—	When DMA transfer error occurs, the transfer that caused the error is stopped For clearing requests to the registers for activation request in the ICU, clearing targets are selectable for each channel or all channels.
Interrupt request	Transfer end interrupt	Generated when the specified number of transfers is completed in normal transfer mode Generated when the specified repeat count of transfers is completed in repeat transfer mode Generated when the specified block count of transfers is completed in block transfer mode Generated when the specified cluster count of transfers is completed in cluster transfer mode	Generated on completion of transferring data volume specified by the transfer counter.
	Transfer escape end interrupt	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.	Generated when the repeat size of data transfer is completed. Generated when the source address extended repeat area overflows. Generated when the destination address extended repeat area overflows
Low-power consumption function		The module-stop state can be set.	The module-stop state can be set.
Protect Zone Filter		—	Security attribute can be set for each channel.

Table 2.39 Comparison of EXDMA Controller Registers

Register	Bit	RX72M (EXDMACa)/ RX72N (EXDMACa)	RX74M (EXDMACAa)/ RX74N (EXDMACAa)
EXDMACCHSAR	—	—	EXDMAC channel security attribution register
EXDMACSAR	—	—	EXDMAC controller security attribution register
EDMSAR	—	EXDMA source address register Specifies the transfer source start address. 0000 0000h to 0FFF FFFFh (256 Mbytes) F000 0000h to FFFF FFFFh (256 Mbytes)	EXDMA source address register Specifies the transfer source start address. 0000 0000h to FFFF FFFFh (4 Gbytes)
EDMSRR	—	—	EXDMA source reload address register
EDMDAR	—	EXDMA destination address register Specifies the transfer destination start address. 0000 0000h to 0FFF FFFFh (256 Mbytes) F000 0000h to FFFF FFFFh (256 Mbytes)	EXDMA destination address register Specifies the transfer destination start address. 0000 0000h to FFFF FFFFh (4 Gbytes)
EDMDRR	—	—	EXDMA source reload address register
EDMCRB	—	EXDMA block transfer count register (b0 to b15)	EXDMA block transfer count register (b0 to b31)
EDMTMD	DCTG[1:0]	Transfer request source select bits b1 b0 0 0: Software 0 1: Setting prohibited 1 0: External DMA transfer request pin (EDREQn) 1 1: DMA transfer request from peripheral modules (TPU1.TRGA or MTU1.TRGA)	Transfer request source select bits b1 b0 0 0: Software 0 1: Interrupts from peripheral modules or external interrupt input pins 1 0: Setting prohibited 1 1: Setting prohibited
	SZ[1:0]	Transfer data size select bits b9 b8 0 0: 8 bits 0 1: 16 bits 1 0: 32 bits 1 1: Setting prohibited	Data transfer size bits b9 b8 0 0: 8 bits 0 1: 16 bits 1 0: 32 bits 1 1: 64 bits
	TKP	—	Transfer keeping bit
	MD[1:0]	Transfer mode select bits b15 b14 0 0: Normal transfer 0 1: Repeat transfer 1 0: Block transfer 1 1: Cluster transfer	Transfer mode select bits b15 b14 0 0: Normal transfer 0 1: Repeat transfer 1 0: Block transfer 1 1: Repeat-block transfer
EDMOMD	—	EXDMA output setting register	—
EDMAMD	DADR	—	Destination address update setting after reload bit
	SADR	—	Source address update setting after reload bit
	DIR	Single address direction select bit	—
	AMS	Address mode select bit	—
EDMSBS	—	—	EXDMA source buffer size register

Register	Bit	RX72M (EXDMACa)/ RX72N (EXDMACa)	RX74M (EXDMACAa)/ RX74N (EXDMACAa)
EDMDBS	—	—	EXDMA destination buffer size register
EDMBWR	—	—	EXDMA bufferable write enable register
EDMECHR	—	—	EXDMAC error channel register
EDMCTL	—	—	EXDMAC control register
EDMRMD	—	EXDMA external request sense mode register	—
EDMERF	—	EXDMA external request flag register	—
CLSBRy	—	Cluster buffer register y	—

2.18 Data Transfer Controller

Table 2.40 is Comparative Overview of Data Transfer Controllers, and Table 2.41 is Comparison of Data Transfer Controller Registers.

Table 2.40 Comparative Overview of Data Transfer Controllers

Item	RX72M (DTCb)/RX72N (DTCb)	RX74M (DTCA)/RX74N (DTCA)
Number of transfer channels	The same number as all interrupt sources that can start the DTC transfer.	The same number as all interrupt sources that can start the DTC transfer.
Transfer modes	• Normal transfer mode — A single transfer request leads to a single data transfer. • Repeat transfer mode — A single transfer request leads to a single data transfer. — The transfer address is returned to the transfer start address after the number of data transfers corresponding to “repeat size”. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, 1024 bytes. • Block transfer mode — A single transfer request leads to a single data transfer. — The maximum block size is 256 × 32 bits = 1024 bytes.	• Normal transfer mode — A single transfer request leads to a single data transfer. • Repeat transfer mode — A single transfer request leads to a single data transfer. — The transfer address is returned to the transfer start address after the number of data transfers corresponding to “repeat size”. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 64 bits, 2048 bytes. • Block transfer mode — A single transfer request leads to the transfer of a single block. — The maximum block size is 256 × 64 bits = 2048 bytes.
Chain transfer	• Multiple types of data transfers can sequentially be executed in response to a single request. • Either “performed only when the transfer counter becomes 0” or “every time” can be selected.	• Multiple types of data transfers can sequentially be executed in response to a single request. • Either “performed only when the transfer counter becomes 0” or “every time” can be selected.
Sequence transfer	A series of complicated transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed. • Only one trigger source can be set at a time. • Up to 256 sequences for a single trigger source • The data that is initially transferred in response to a transfer request determines a sequence • The whole sequence can be executed on a single request, or be suspended in the middle of the sequence and resumed on the next transfer request (division of sequence).	A series of complicated transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed. • Only one trigger source can be set at a time. • Up to 256 sequences for a single trigger source • The data that is initially transferred in response to a transfer request determines a sequence • The whole sequence can be executed on a single request, or be suspended in the middle of the sequence and resumed on the next transfer request (division of sequence).
Transfer space	• In short-address mode: 16 Mbytes (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh except reserved areas) • In full-address mode: 4 Gbytes (Area from 0000 0000h to FFFF FFFFh except reserved areas)	• 4 Gbytes (Area from 0000 0000h to FFFF FFFFh except reserved areas)

Item	RX72M (DTCb)/RX72N (DTCb)	RX74M (DTCA)/RX74N (DTCA)
Data transfer units	• Single data: 1 byte (8 bits), 1 word (16 bits), 1 longword (32 bits) • Single block size: 1 to 256 data	• Single data: 1 byte (8 bits), 1 word (16 bits), 1 longword (32 bits), 1 double longword (64 bits) • Single block size: 1 to 256 data
CPU interrupt source	• An interrupt request can be generated to the CPU on a request source for a data transfer. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of specified volume.	• An interrupt request can be generated to the CPU on a request source for a data transfer. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of specified volume.
Transfer error handling	—	If a transfer error (bus error) occurs, the transfer is aborted and the IR flag of the transfer request source is cleared.
Event link function	An event link request is generated after one data transfer (for block, after one block transfer).	An event link request is generated after one data transfer (for block, after one block transfer).
Read skip	Reading of the transfer information can be skipped when the same transfer is repeated.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	Write-back of the transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.	Write-back of the transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Write-back disable	Allows disabling the write-back of transfer information.	Allows disabling the write-back of transfer information.
Displacement addition	The displacement value can be added to the transfer source address (for each transfer information)	The displacement value can be added to the transfer source address (for each transfer information)
Low power consumption function	Module stop state can be set.	Module stop state can be set.
Protect Zone filter	—	Security attributes can be set.

Table 2.41 Comparison of Data Transfer Controller Registers

Register	Bit	RX72M (DTCb)/RX72N (DTCb)	RX74M (DTCA)/RX74N (DTCA)
MRA	SM[1:0]	Transfer source address addressing mode bits b3 b2 0 0: The address in the SAR register is fixed. (write-back to SAR is skipped.) 0 1: The address in the SAR register is fixed. (write-back to SAR is skipped.) 1 0: The SAR value is incremented after a data transfer. (+1 when the SZ[1:0] bits are 00b, +2 when 01b, +4 when 10b) 1 1: The SAR value is decremented after a data transfer. (–1 when the SZ[1:0] bits are 00b, –2 when 01b, –4 when 10b)	Transfer source address addressing mode bits b3 b2 0 0: The address in the SAR register is fixed. (write-back to SAR is skipped.) 0 1: The address in the SAR register is fixed. (write-back to SAR is skipped.) 1 0: The SAR value is incremented after a data transfer. (+1 when the SZ[1:0] bits are 00b, +2 when 01b, +4 when 10b, +8 when 11b) 1 1: The SAR value is decremented after a data transfer. (–1 when the SZ[1:0] bits are 00b, –2 when 01b, –4 when 10b, –8 when 11b)
	SZ[1:0]	DTC data transfer size bits b5 b4 0 0: Byte (8-bit) transfer 0 1: Word (16-bit) transfer 1 0: Longword (32-bit) transfer 1 1: Setting prohibited	DTC data transfer size bits b5 b4 0 0: Byte (8-bit) transfer 0 1: Word (16-bit) transfer 1 0: Longword (32-bit) transfer 1 1: Double longword (64-bit) transfer
MRB	DM[1:0]	Transfer destination address addressing mode bits b3 b2 0 0: The address in the DAR register is fixed. (Write-back to DAR is skipped.) 0 1: The address in the DAR register is fixed. (Write-back to DAR is skipped.) 1 0: The DAR value is incremented after data transfer. (+1 when the MRA.SZ[1:0] bits are 00b, +2 when 01b, +4 when 10b) 1 1: The DAR value is decremented after data transfer. (–1 when the MRA.SZ[1:0] bits are 00b, –2 when 01b, –4 when 10b)	Transfer destination address addressing mode bits b3 b2 0 0: The address in the DAR register is fixed. (Write-back to DAR is skipped.) 0 1: The address in the DAR register is fixed. (Write-back to DAR is skipped.) 1 0: The DAR value is incremented after data transfer. (+1 when the MRA.SZ[1:0] bits are 00b, +2 when 01b, +4 when 10b, +8 when 11b) 1 1: The DAR value is decremented after data transfer. (–1 when the MRA.SZ[1:0] bits are 00b, –2 when 01b, –4 when 10b, –8 when 11b)
DTCCR	—	DTC control register	—
DTCCR_S	—	—	DTC control register for secure application
DTCCR_NS	—	—	DTC control register for non-secure application
DTCVBR	—	DTC vector base register	—

Register	Bit	RX72M (DTCb)/RX72N (DTCb)	RX74M (DTCA)/RX74N (DTCA)
DTCVBR_S	—	—	DTC vector base register for secure application
DTCVBR_NS	—	—	DTC vector base register for non-secure application
DTCADMOD	—	DTC address mode register	—
DTCEVR	—	—	DTC error vector register
DTCSAR	—	—	DTC security attribution register

2.19 Event Link Controller

Table 2.42 is Comparative Overview of Event Link Controllers, Table 2.43 is Comparison of Event Link Controller Registers, Table 2.44 is Correspondence between Values Set in ELSRn Registers and Peripheral Modules, and Table 2.45 is Correspondence between Event Signal Names Set in ELSRn.ELS and Signal Numbers.

Table 2.42 Comparative Overview of Event Link Controllers

Item	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
Event link function	• 137 types of event signals can be directly interconnected to modules. • Operation for timer modules when inputting an event signal can be selected. • Event linkage operation is possible for port B and port E. — Single port: Event linkage operation can be set in a single specified port. — Port group: Event linkage operation can be set by grouping multiple specified ports among total of eight ports	• 135 types of event signals can be directly interconnected to modules. • Operation for timer modules when inputting an event signal can be selected. • Event linkage operation is possible for port B and port E. — Single port: Event linkage operation can be set in a single specified port. — Port group: Event linkage operation can be set by grouping multiple specified ports among total of eight ports	• 381 types of event signals can be directly interconnected to modules. • Operation for timer modules when inputting an event signal can be selected.	• 377 types of event signals can be directly interconnected to modules. • Operation for timer modules when inputting an event signal can be selected.
Low power consumption function	Module stop state can be set.	Module stop state can be set.	Module stop state can be set.	Module stop state can be set.
Protect Zone filter	—	—	Security attribute can be set for each register.	Security attribute can be set for each register.

Table 2.43 Comparison of Event Link Controller Registers

Register	Bit	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
ELCSARA	—	—	—	ELC security attribution register A	ELC security attribution register A
ELCSARB	—	—	—	ELC security attribution register B	ELC security attribution register B
ELCSARC	—	—	—	ELC security attribution register C	ELC security attribution register C
ELCSARD	—	—	—	ELC security attribution register D	ELC security attribution register D
ELSEGRm	—	—	—	Software event generation register m	Software event generation register m
ELCR	—	Event link control register	Event link control register	Event link control register	Event link control register
		The initial value after reset differs.			
	b6 to b0	These bits are read as 1. The write value should be 1.	These bits are read as 1. The write value should be 1.	These bits are read as 0. The write value should be 0.	These bits are read as 0. The write value should be 0.
ELSRn	—	Event link setting register n (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 33, 35 to 38, 41 to 45, 48 to 57) The register length is 8 bits.	Event link setting register n (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 33, 35 to 38, 45, 48 to 57) The register length is 8 bits.	Event link setting register n (n = 0 to 26, 46, 47, 50 to 78, 88 to 91) The register length is 16 bits.	Event link setting register n (n = 0 to 26,46, 47, 50 to 52, 73 to 78, 88 to 91) The register length is 16 bits.
	ELS[7:0] (RX72M/72N) ELS[9:0] (RX74M/74N)	Event link select bits 00h: Event signal output to the corresponding peripheral module is disabled. 01h to CFh: Set the number for the event signal to be linked. Settings other than above are prohibited.	Event link select bits 00h: Event signal output to the corresponding peripheral module is disabled. 01h to CDh: Set the number for the event signal to be linked. Settings other than above are prohibited.	Event link select bits 000h: Event signal output to the corresponding peripheral module is disabled. 021h to 33Bh: Set the number for the event signal to be linked. Settings other than above are prohibited.	Event link select bits 000h: Event signal output to the corresponding peripheral module is disabled. 021h to 33Bh: Set the number for the event signal to be linked. Settings other than above are prohibited.
ELOPA	MTU0MD[1:0]	MTU0 operation select bits	MTU0 operation select bits	—	—
	MTU3MD[1:0]	MTU3 operation select bits	MTU3 operation select bits	—	—
	CMT1MD[1:0]	—	—	CMT1 operation select bits	CMT1 operation select bits
ELOPB	MTU4MD[1:0]	MTU4 operation select bits	MTU4 operation select bits	—	—
	CMTW0MD[1:0]	—	—	CMTW0 operation select bits	CMTW0 operation select bits
ELOPC	CMT1MD[1:0]	CMT1 operation select bits	CMT1 operation select bits	—	—

Register	Bit	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
ELOPC	TMR0MD[1:0]	—	—	TMR0 operation select bits	TMR0 operation select bits
	TMR1MD[1:0]	—	—	TMR1 operation select bits	TMR1 operation select bits
ELOPD	TMR0MD[1:0]	TMR0 operation select bits	TMR0 operation select bits	—	—
	TMR1MD[1:0]	TMR1 operation select bits	TMR1 operation select bits	—	—
	TMR2MD[1:0]	TMR2 operation select bits (b5, b4)	TMR2 operation select bits (b5, b4)	TMR2 operation select bits (b1, b0)	TMR2 operation select bits (b1, b0)
ELOPD	TMR3MD[1:0]	TMR3 operation select bits (b7, b6)	TMR3 operation select bits (b7, b6)	TMR3 operation select bits (b3, b2)	TMR3 operation select bits (b3, b2)
ELOPF	—	Event link option setting register F	Event link option setting register F	—	—
ELOPH	—	Event link option setting register H	Event link option setting register H	—	—
PGRn	—	Port group setting register n	Port group setting register n	—	—
PGCn	—	Port group control register n	Port group control register n	—	—
PDBFn	—	Port buffer register n	Port buffer register n	—	—
PELm	—	Event link port setting register m	Event link port setting register m	—	—
ELSEGR	—	Event link software event generation register	Event link software event generation register	—	—

Table 2.44 Correspondence between Values Set in ELSRn Registers and Peripheral Modules

Register	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
ELSR0	MTU0	MTU0	CMT1	CMT1
ELSR1	—	—	CMTW0	CMTW0
ELSR2	—	—	TMR0	TMR0
ELSR3	MTU3	MTU3	TMR1	TMR1
ELSR4	MTU4	MTU4	TMR2	TMR2
ELSR5	—	—	TMR3	TMR3
ELSR6	—	—	GPTW event source A (common to all channels)	GPTW event source A (common to all channels)
ELSR7	CMT1	CMT1	GPTW event source B (common to all channels)	GPTW event source B (common to all channels)
ELSR8	—	—	GPTW event source C (common to all channels)	GPTW event source C (common to all channels)
ELSR9	—	—	GPTW event source D (common to all channels)	GPTW event source D (common to all channels)
ELSR10	TMR0	TMR0	GPTW event source E (common to all channels)	GPTW event source E (common to all channels)
ELSR11	TMR1	TMR1	GPTW event source F (common to all channels)	GPTW event source F (common to all channels)

Register	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
ELSR12	TMR2	TMR2	GPTW event source G (common to all channels)	GPTW event source G (common to all channels)
ELSR13	TMR3	TMR3	GPTW event source H (common to all channels)	GPTW event source H (common to all channels)
ELSR14	—	—	Port B	Port B
ELSR15	S12AD (ELCTRG00N)	S12AD (ELCTRG00N)	Port C	Port C
ELSR16	DA0	DA0	Port D	Port D
ELSR17	—	—	Port E	Port E
ELSR18	ICU (Interrupt 1)	ICU (Interrupt 1)	ADC trigger 0 (common to all units)	ADC trigger 0 (common to all units)
ELSR19	ICU (Interrupt 2)	ICU (Interrupt 2)	ADC trigger 1 (common to all units)	ADC trigger 1 (common to all units)
ELSR20	Output port group 1	Output port group 1	ADC trigger 2 (common to all units)	ADC trigger 2 (common to all units)
ELSR21	Output port group 2	Output port group 2	ADC trigger 3 (common to all units)	ADC trigger 3 (common to all units)
ELSR22	Input port group 1	Input port group 1	ADC trigger 4 (common to all units)	ADC trigger 4 (common to all units)
ELSR23	Input port group 2	Input port group 2	ADC trigger 5 (common to all units)	ADC trigger 5 (common to all units)
ELSR24	Single port 0	Single port 0	ADC trigger 6 (common to all units)	ADC trigger 6 (common to all units)
ELSR25	Single port 1	Single port 1	ADC trigger 7 (common to all units)	ADC trigger 7 (common to all units)
ELSR26	Single port 2	Single port 2	ADC trigger 8 (common to all units)	ADC trigger 8 (common to all units)
ELSR27	Single port 3	Single port 3	—	—
ELSR28	Clock source switching to LOCO	Clock source switching to LOCO	—	—
ELSR33	CMTW0	CMTW0	—	—
ELSR35	TPU0	TPU0	—	—
ELSR36	TPU1	TPU1	—	—
ELSR37	TPU2	TPU2	—	—
ELSR38	TPU3	TPU3	—	—
ELSR41	DSMIF0 trigger 0	—	—	—
ELSR42	DSMIF0 trigger 1	—	—	—
ELSR43	DSMIF1 trigger 0	—	—	—
ELSR44	DSMIF1 trigger 1	—	—	—
ELSR45	S12AD1 (ELCTRG10N)	S12AD1 (ELCTRG10N)	—	—
ELSR46	—	—	DAC0	DAC0
ELSR47	—	—	DAC1	DAC1
ELSR48	GPTW event source A (common to all channels)	GPTW event source A (common to all channels)	—	—
ELSR49	GPTW event source B (common to all channels)	GPTW event source B (common to all channels)	—	—
ELSR50	GPTW event source C (common to all channels)	GPTW event source C (common to all channels)	RI3C0	RI3C0

Register	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
ELSR51	GPTW event source D (common to all channels)	GPTW event source D (common to all channels)	GPTP (CAPTURE0)	GPTP (CAPTURE0)
ELSR52	GPTW event source E (common to all channels)	GPTW event source E (common to all channels)	GPTP (CAPTURE1)	GPTP (CAPTURE1)
ELSR53	GPTW event source F (common to all channels)	GPTW event source F (common to all channels)	ESC (ESC_LATCH0)	—
ELSR54	GPTW event source G (common to all channels)	GPTW event source G (common to all channels)	ESC (ESC_LATCH1)	—
ELSR55	GPTW event source H (common to all channels)	GPTW event source H (common to all channels)	DSMIF0 (CAP_TRG0)	—
ELSR56	S12AD (ELCTRG01N)	S12AD (ELCTRG01N)	DSMIF0 (CAP_TRG1)	—
ELSR57	S12AD1 (ELCTRG11N)	S12AD1 (ELCTRG11N)	DSMIF0 (CAP_TRG2)	—
ELSR58	—	—	DSMIF0 (CAP_TRG3)	—
ELSR59	—	—	DSMIF0 (CAP_TRG4)	—
ELSR60	—	—	DSMIF0 (CAP_TRG5)	—
ELSR61	—	—	DSMIF0 (CDCNT_INT_TRG0)	—
ELSR62	—	—	DSMIF0 (CDCNT_INT_TRG1)	—
ELSR63	—	—	DSMIF0 (CDCNT_INT_TRG2)	—
ELSR64	—	—	DSMIF1 (CAP_TRG0)	—
ELSR65	—	—	DSMIF1 (CAP_TRG1)	—
ELSR66	—	—	DSMIF1 (CAP_TRG2)	—
ELSR67	—	—	DSMIF1 (CAP_TRG3)	—
ELSR68	—	—	DSMIF1 (CAP_TRG4)	—
ELSR69	—	—	DSMIF1 (CAP_TRG5)	—
ELSR70	—	—	DSMIF1 (CDCNT_INT_TRG0	—
ELSR71	—	—	DSMIF1 (CDCNT_INT_TRG1	—
ELSR72	—	—	DSMIF1 (CDCNT_INT_TRG2	—
ELSR73	—	—	PCIF0 (ELC_IN)	PCIF0 (ELC_IN)
ELSR74	—	—	PCIF0 (PEK_IN)	PCIF0 (PEK_IN)
ELSR75	—	—	PCIF0 (VLY_IN)	PCIF0 (VLY_IN)
ELSR76	—	—	PCIF1 (ELC_IN)	PCIF1 (ELC_IN)
ELSR77	—	—	PCIF1 (PEK_IN)	PCIF1 (PEK_IN)
ELSR78	—	—	PCIF1 (VLY_IN)	PCIF1 (VLY_IN)
ELSR88	—	—	ICU (Interrupt 1)*1	ICU (Interrupt 1)*1
ELSR89	—	—	ICU (Interrupt 2)*1	ICU (Interrupt 2)*1
ELSR90	—	—	ICU (Interrupt 3)*1	ICU (Interrupt 3)*1
ELSR91	—	—	ICU (Interrupt 4)*1	ICU (Interrupt 4)*1

Note: 1. Specify an event number from among 050h to 053h and 313h. Do not set other values.

Table 2.45 Correspondence between Event Signal Names Set in ELSRn.ELS and Signal Numbers

Value of ELS Bits	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
01h	MTU0 compare match 0A	MTU0 compare match 0A	—	—
02h	MTU0 compare match 0B	MTU0 compare match 0B	—	—
03h	MTU0 compare match 0C	MTU0 compare match 0C	—	—
04h	MTU0 compare match 0D	MTU0 compare match 0D	—	—
05h	MTU0 compare match 0E	MTU0 compare match 0E	—	—
06h	MTU0 compare match 0F	MTU0 compare match 0F	—	—
07h	MTU0 overflow	MTU0 overflow	—	—
10h	MTU3 compare match 3A	MTU3 compare match 3A	—	—
11h	MTU3 compare match 3B	MTU3 compare match 3B	—	—
12h	MTU3 compare match 3C	MTU3 compare match 3C	—	—
13h	MTU3 compare match 3D	MTU3 compare match 3D	—	—
14h	MTU3 overflow	MTU3 overflow	—	—
15h	MTU4 compare match 4A	MTU4 compare match 4A	—	—
16h	MTU4 compare match 4B	MTU4 compare match 4B	—	—
17h	MTU4 compare match 4C	MTU4 compare match 4C	—	—
18h	MTU4 compare match 4D	MTU4 compare match 4D	—	—
19h	MTU4 overflow	MTU4 overflow	—	—
1Ah	MTU4 underflow	MTU4 underflow	—	—
1Fh	CMT1 compare match 1	CMT1 compare match 1	—	—
21h	—	—	DMAC0 transfer end	DMAC0 transfer end
22h	TMR0 compare match A0	TMR0 compare match A0	DMAC1 transfer end	DMAC1 transfer end
23h	TMR0 compare match B0	TMR0 compare match B0	DMAC2 transfer end	DMAC2 transfer end
24h	TMR0 overflow	TMR0 overflow	DMAC3 transfer end	DMAC3 transfer end
25h	TMR1 compare match A1	TMR1 compare match A1	DMAC4 transfer end	DMAC4 transfer end
26h	TMR1 compare match B1	TMR1 compare match B1	DMAC5 transfer end	DMAC5 transfer end
27h	TMR1 overflow	TMR1 overflow	DMAC6 transfer end	DMAC6 transfer end
28h	TMR2 compare match A2	TMR2 compare match A2	DMAC7 transfer end	DMAC7 transfer end
29h	TMR2 compare match B2	TMR2 compare match B2	—	—
2Ah	TMR2 overflow	TMR2 overflow	—	—
2Bh	TMR3 compare match A3	TMR3 compare match A3	—	—

Value of ELS Bits	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
2Ch	TMR3 compare match B3	TMR3 compare match B3	—	—
2Dh	TMR3 overflow	TMR3 overflow	—	—
2Eh	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)	—	—
31h	IWDT underflow or refresh error	IWDT underflow or refresh error	DTC transfer end	DTC transfer end
33h	—	—	PVD1 voltage detection	PVD1 voltage detection
34h	—	—	PVD2 voltage detection	PVD2 voltage detection
38h	—	—	Oscillation stop detection with the main clock	Oscillation stop detection with the main clock
3Ah	SCI5 error (receive error or error signal detection)	SCI5 error (receive error or error signal detection)	—	—
3Bh	SCI5 receive data full	SCI5 receive data full	—	—
3Ch	SCI5 transmit data empty	SCI5 transmit data empty	—	—
3Dh	SCI5 transmit end	SCI5 transmit end	—	—
4Ch	—	—	IWDT underflow or refresh error	IWDT underflow or refresh error
4Dh	—	—	WDT underflow or refresh error	WDT underflow or refresh error
4Eh	RIIC0 communication error or event generation	RIIC0 communication error or event generation	—	—
4Fh	RIIC0 receive data full	RIIC0 receive data full	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)
50h	RIIC0 transmit data empty	RIIC0 transmit data empty	Software event 0	Software event 0
51h	RIIC0 transmit end	RIIC0 transmit end	Software event 1	Software event 1
52h	RSPI0 error (mode fault, overrun, underrun, or parity error)	RSPI0 error (mode fault, overrun, underrun, or parity error)	Software event 2	Software event 2
53h	RSPI0 idle	RSPI0 idle	Software event 3	Software event 3
54h	RSPI0 receive buffer full	RSPI0 receive buffer full	Port B event	Port B event
55h	RSPI0 transmit buffer empty	RSPI0 transmit buffer empty	Port C event	Port C event
56h	RSPI0 transmit end	RSPI0 transmit end	Port D event	Port D event
57h	—	—	Port E event	Port E event
58h	S12AD A/D conversion end	S12AD A/D conversion end	CMT1 compare match	CMT1 compare match
59h	—	—	CMTW0 compare match	CMTW0 compare match
5Ah	—	—	TMR0 compare match A	TMR0 compare match A

Value of ELS Bits	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
5Bh	LVD1 voltage detection	LVD1 voltage detection	TMR0 compare match B	TMR0 compare match B
5Ch	LVD2 voltage detection	LVD2 voltage detection	TMR0 overflow	TMR0 overflow
5Dh	DMAC0 transfer end	DMAC0 transfer end	TMR1 compare match A	TMR1 compare match A
5Eh	DMAC1 transfer end	DMAC1 transfer end	TMR1 compare match B	TMR1 compare match B
5Fh	DMAC2 transfer end	DMAC2 transfer end	TMR1 overflow	TMR1 overflow
60h	DMAC3 transfer end	DMAC3 transfer end	TMR2 compare match A	TMR2 compare match A
61h	DTC transfer end	DTC transfer end	TMR2 compare match B	TMR2 compare match B
62h	Oscillation stop detection of clock generation circuit	Oscillation stop detection of clock generation circuit	TMR2 overflow	TMR2 overflow
63h	Input edge detection of input port group 1	Input edge detection of input port group 1	TMR3 compare match A	TMR3 compare match A
64h	Input edge detection of input port group 2	Input edge detection of input port group 2	TMR3 compare match B	TMR3 compare match B
65h	Input edge detection of single input port 0	Input edge detection of single input port 0	TMR3 overflow	TMR3 overflow
66h	Input edge detection of single input port 1	Input edge detection of single input port 1	—	—
67h	Input edge detection of single input port 2	Input edge detection of single input port 2	—	—
68h	Input edge detection of single input port 3	Input edge detection of single input port 3	—	—
69h	Software event	Software event	—	—
6Ah	DOC data operation condition met	DOC data operation condition met	—	—
6Ch	S12AD1 A/D conversion end	S12AD1 A/D conversion end	—	—
7Eh	CMTW0 compare match	CMTW0 compare match	—	—
80h	GPTW0 compare match A	GPTW0 compare match A	—	—
81h	GPTW0 compare match B	GPTW0 compare match B	—	—
82h	GPTW0 compare match C	GPTW0 compare match C	—	—
83h	GPTW0 compare match D	GPTW0 compare match D	—	—
84h	GPTW0 compare match E	GPTW0 compare match E	—	—
85h	GPTW0 compare match F	GPTW0 compare match F	—	—
86h	GPTW0 overflow	GPTW0 overflow	—	—
87h	GPTW0 underflow	GPTW0 underflow	—	—
88h	GPTW1 compare match A	GPTW1 compare match A	—	—
89h	GPTW1 compare match B	GPTW1 compare match B	—	—

Value of ELS Bits	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
8Ah	GPTW1 compare match C	GPTW1 compare match C	—	—
8Bh	GPTW1 compare match D	GPTW1 compare match D	—	—
8Ah	GPTW1 compare match E	GPTW1 compare match E	—	—
8Bh	GPTW1 compare match F	GPTW1 compare match F	—	—
8Eh	GPTW1 overflow	GPTW1 overflow	—	—
8Fh	GPTW1 underflow	GPTW1 underflow	—	—
90h	GPTW2 compare match A	GPTW2 compare match A	—	—
91h	GPTW2 compare match B	GPTW2 compare match B	—	—
92h	GPTW2 compare match C	GPTW2 compare match C	—	—
93h	GPTW2 compare match D	GPTW2 compare match D	—	—
94h	GPTW2 compare match E	GPTW2 compare match E	—	—
95h	GPTW2 compare match F	GPTW2 compare match F	—	—
96h	GPTW2 overflow	GPTW2 overflow	—	—
97h	GPTW2 underflow	GPTW2 underflow	—	—
98h	GPTW3 compare match A	GPTW3 compare match A	—	—
99h	GPTW3 compare match B	GPTW3 compare match B	—	—
9Ah	GPTW3 compare match C	GPTW3 compare match C	—	—
9Bh	GPTW3 compare match D	GPTW3 compare match D	—	—
9Ah	GPTW3 compare match E	GPTW3 compare match E	—	—
9Bh	GPTW3 compare match F	GPTW3 compare match F	—	—
9Eh	GPTW3 overflow	GPTW3 overflow	—	—
9Fh	GPTW3 underflow	GPTW3 underflow	—	—
A0h	EPTPC STCA timer 0 rising edge detection	EPTPC STCA timer 0 rising edge detection	—	—
A1h	EPTPC STCA timer 1 rising edge detection	EPTPC STCA timer 1 rising edge detection	—	—
A2h	EPTPC STCA timer 2 rising edge detection	EPTPC STCA timer 2 rising edge detection	—	—
A3h	EPTPC STCA timer 3 rising edge detection	EPTPC STCA timer 3 rising edge detection	—	—
A4h	EPTPC STCA timer 4 rising edge detection	EPTPC STCA timer 4 rising edge detection	—	—
A5h	EPTPC STCA timer 5 rising edge detection	EPTPC STCA timer 5 rising edge detection	—	—
A6h	EPTPC STCA timer 0 falling edge detection	EPTPC STCA timer 0 falling edge detection	—	—

Value of ELS Bits	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
A7h	EPTPC STCA timer 1 falling edge detection	EPTPC STCA timer 1 falling edge detection	—	—
A8h	EPTPC STCA timer 2 falling edge detection	EPTPC STCA timer 2 falling edge detection	—	—
A9h	EPTPC STCA timer 3 falling edge detection	EPTPC STCA timer 3 falling edge detection	—	—
AAh	EPTPC STCA timer 4 falling edge detection	EPTPC STCA timer 4 falling edge detection	—	—
ABh	EPTPC STCA timer 5 falling edge detection	EPTPC STCA timer 5 falling edge detection	—	—
ACh	TPU0 compare match A	TPU0 compare match A	—	—
ADh	TPU0 compare match B	TPU0 compare match B	—	—
AEh	TPU0 compare match C	TPU0 compare match C	—	—
AFh	TPU0 compare match D	TPU0 compare match D	—	—
B0h	TPU0 overflow	TPU0 overflow	—	—
B1h	TPU1 compare match A	TPU1 compare match A	—	—
B2h	TPU1 compare match B	TPU1 compare match B	—	—
B3h	TPU1 overflow	TPU1 overflow	—	—
B4h	TPU1 underflow	TPU1 underflow	—	—
B5h	TPU2 compare match A	TPU2 compare match A	—	—
B6h	TPU2 compare match B	TPU2 compare match B	—	—
B7h	TPU2 overflow	TPU2 overflow	—	—
B8h	TPU2 underflow	TPU2 underflow	—	—
B9h	TPU3 compare match A	TPU3 compare match A	—	—
BAh	TPU3 compare match B	TPU3 compare match B	—	—
BBh	TPU3 compare match C	TPU3 compare match C	—	—
BCh	TPU3 compare match D	TPU3 compare match D	—	—
BDh	TPU3 overflow	TPU3 overflow	—	—
C6h	GPTW0 A/D converter start request A	GPTW0 A/D converter start request A	—	—
C7h	GPTW0 A/D converter start request B	GPTW0 A/D converter start request B	—	—
C8h	GPTW1 A/D converter start request A	GPTW1 A/D converter start request A	—	—
C9h	GPTW1 A/D converter start request B	GPTW1 A/D converter start request B	GPTW (OPS) U-/V-/W-phase input edge detected	GPTW (OPS) U-/V-/W-phase input edge detected
CAh	GPTW2 A/D converter start request A	GPTW2 A/D converter start request A	GPTW0 compare match A	GPTW0 compare match A
CBh	GPTW2 A/D converter start request B	GPTW2 A/D converter start request B	GPTW0 compare match B	GPTW0 compare match B
CCh	GPTW3 A/D converter start request A	GPTW3 A/D converter start request A	GPTW0 compare match C	GPTW0 compare match C
CDh	GPTW3 A/D converter start request B	GPTW3 A/D converter start request B	GPTW0 compare match D	GPTW0 compare match D
CEh	ESC SYNC0	—	GPTW0 compare match E	GPTW0 compare match E
CFh	ESC SYNC1	—	GPTW0 compare match F	GPTW0 compare match F
0D0h	—	—	GPTW0 overflow	GPTW0 overflow
0D1h	—	—	GPTW0 underflow	GPTW0 underflow

Value of ELS Bits	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
0D2h	—	—	GPTW0 cycle count end	GPTW0 cycle count end
0D4h	—	—	GPTW0 A/D converter start request A	GPTW0 A/D converter start request A
0D5h	—	—	GPTW0 A/D converter start request B	GPTW0 A/D converter start request B
0D6h	—	—	GPTW1 compare match A	GPTW1 compare match A
0D7h	—	—	GPTW1 compare match B	GPTW1 compare match B
0D8h	—	—	GPTW1 compare match C	GPTW1 compare match C
0D9h	—	—	GPTW1 compare match D	GPTW1 compare match D
0DAh	—	—	GPTW1 compare match E	GPTW1 compare match E
0DBh	—	—	GPTW1 compare match F	GPTW1 compare match F
0DCh	—	—	GPTW1 overflow	GPTW1 overflow
0DDh	—	—	GPTW1 underflow	GPTW1 underflow
0DEh	—	—	GPTW1 cycle count end	GPTW1 cycle count end
0E0h	—	—	GPTW1 A/D converter start request A	GPTW1 A/D converter start request A
0E1h	—	—	GPTW1 A/D converter start request B	GPTW1 A/D converter start request B
0E2h	—	—	GPTW2 compare match A	GPTW2 compare match A
0E3h	—	—	GPTW2 compare match B	GPTW2 compare match B
0E4h	—	—	GPTW2 compare match C	GPTW2 compare match C
0E5h	—	—	GPTW2 compare match D	GPTW2 compare match D
0E6h	—	—	GPTW2 compare match E	GPTW2 compare match E
0E7h	—	—	GPTW2 compare match F	GPTW2 compare match F
0E8h	—	—	GPTW2 overflow	GPTW2 overflow
0E9h	—	—	GPTW2 underflow	GPTW2 underflow
0EAh	—	—	GPTW2 cycle count end	GPTW2 cycle count end
0ECh	—	—	GPTW2 A/D converter start request A	GPTW2 A/D converter start request A
0EDh	—	—	GPTW2 A/D converter start request B	GPTW2 A/D converter start request B
0EEh	—	—	GPTW3 compare match A	GPTW3 compare match A
0EFh	—	—	GPTW3 compare match B	GPTW3 compare match B
0F0h	—	—	GPTW3 compare match C	GPTW3 compare match C

Value of ELS Bits	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
0F1h	—	—	GPTW3 compare match D	GPTW3 compare match D
0F2h	—	—	GPTW3 compare match E	GPTW3 compare match E
0F3h	—	—	GPTW3 compare match F	GPTW3 compare match F
0F4h	—	—	GPTW3 overflow	GPTW3 overflow
0F5h	—	—	GPTW3 underflow	GPTW3 underflow
0F6h	—	—	GPTW3 cycle count end	GPTW3 cycle count end
0F8h	—	—	GPTW3 A/D converter start request A	GPTW3 A/D converter start request A
0F9h	—	—	GPTW3 A/D converter start request B	GPTW3 A/D converter start request B
0FAh	—	—	GPTW4 compare match A	GPTW4 compare match A
0FBh	—	—	GPTW4 compare match B	GPTW4 compare match B
0FCh	—	—	GPTW4 compare match C	GPTW4 compare match C
0FDh	—	—	GPTW4 compare match D	GPTW4 compare match D
0FEh	—	—	GPTW4 compare match E	GPTW4 compare match E
0FFh	—	—	GPTW4 compare match F	GPTW4 compare match F
100h	—	—	GPTW4 overflow	GPTW4 overflow
101h	—	—	GPTW4 underflow	GPTW4 underflow
102h	—	—	GPTW4 cycle count end	GPTW4 cycle count end
104h	—	—	GPTW4 A/D converter start request A	GPTW4 A/D converter start request A
105h	—	—	GPTW4 A/D converter start request B	GPTW4 A/D converter start request B
106h	—	—	GPTW5 compare match A	GPTW5 compare match A
107h	—	—	GPTW5 compare match B	GPTW5 compare match B
108h	—	—	GPTW5 compare match C	GPTW5 compare match C
109h	—	—	GPTW5 compare match D	GPTW5 compare match D
10Ah	—	—	GPTW5 compare match E	GPTW5 compare match E
10Bh	—	—	GPTW5 compare match F	GPTW5 compare match F
10Ch	—	—	GPTW5 overflow	GPTW5 overflow
10Dh	—	—	GPTW5 underflow	GPTW5 underflow
10Eh	—	—	GPTW5 cycle count end	GPTW5 cycle count end
110h	—	—	GPTW5 A/D converter start request A	GPTW5 A/D converter start request A

Value of ELS Bits	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
111h	—	—	GPTW5 A/D converter start request B	GPTW5 A/D converter start request B
112h	—	—	GPTW6 compare match A	GPTW6 compare match A
113h	—	—	GPTW6 compare match B	GPTW6 compare match B
114h	—	—	GPTW6 compare match C	GPTW6 compare match C
115h	—	—	GPTW6 compare match D	GPTW6 compare match D
116h	—	—	GPTW6 compare match E	GPTW6 compare match E
117h	—	—	GPTW6 compare match F	GPTW6 compare match F
118h	—	—	GPTW6 overflow	GPTW6 overflow
119h	—	—	GPTW6 underflow	GPTW6 underflow
11Ah	—	—	GPTW6 cycle count end	GPTW6 cycle count end
11Ch	—	—	GPTW6 A/D converter start request A	GPTW6 A/D converter start request A
11Dh	—	—	GPTW6 A/D converter start request B	GPTW6 A/D converter start request B
11Eh	—	—	GPTW7 compare match A	GPTW7 compare match A
11Fh	—	—	GPTW7 compare match B	GPTW7 compare match B
120h	—	—	GPTW7 compare match C	GPTW7 compare match C
121h	—	—	GPTW7 compare match D	GPTW7 compare match D
122h	—	—	GPTW7 compare match E	GPTW7 compare match E
123h	—	—	GPTW7 compare match F	GPTW7 compare match F
124h	—	—	GPTW7 overflow	GPTW7 overflow
125h	—	—	GPTW7 underflow	GPTW7 underflow
126h	—	—	GPTW7 cycle count end	GPTW7 cycle count end
128h	—	—	GPTW7 A/D converter start request A	GPTW7 A/D converter start request A
129h	—	—	GPTW7 A/D converter start request B	GPTW7 A/D converter start request B
12Ah	—	—	GPTW8 compare match A	GPTW8 compare match A
12Bh	—	—	GPTW8 compare match B	GPTW8 compare match B
12Ch	—	—	GPTW8 compare match C	GPTW8 compare match C
12Dh	—	—	GPTW8 compare match D	GPTW8 compare match D
12Eh	—	—	GPTW8 compare match E	GPTW8 compare match E

Value of ELS Bits	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
12Fh	—	—	GPTW8 compare match F	GPTW8 compare match F
130h	—	—	GPTW8 overflow	GPTW8 overflow
131h	—	—	GPTW8 underflow	GPTW8 underflow
132h	—	—	GPTW8 cycle count end	GPTW8 cycle count end
134h	—	—	GPTW8 A/D converter start request A	GPTW8 A/D converter start request A
135h	—	—	GPTW8 A/D converter start request B	GPTW8 A/D converter start request B
136h	—	—	GPTW9 compare match A	GPTW9 compare match A
137h	—	—	GPTW9 compare match B	GPTW9 compare match B
138h	—	—	GPTW9 compare match C	GPTW9 compare match C
139h	—	—	GPTW9 compare match D	GPTW9 compare match D
13Ah	—	—	GPTW9 compare match E	GPTW9 compare match E
13Bh	—	—	GPTW9 compare match F	GPTW9 compare match F
13Ch	—	—	GPTW9 overflow	GPTW9 overflow
13Dh	—	—	GPTW9 underflow	GPTW9 underflow
13Eh	—	—	GPTW9 cycle count end	GPTW9 cycle count end
140h	—	—	GPTW9 A/D converter start request A	GPTW9 A/D converter start request A
141h	—	—	GPTW9 A/D converter start request B	GPTW9 A/D converter start request B
142h	—	—	GPTW10 compare match A	GPTW10 compare match A
143h	—	—	GPTW10 compare match B	GPTW10 compare match B
144h	—	—	GPTW10 compare match C	GPTW10 compare match C
145h	—	—	GPTW10 compare match D	GPTW10 compare match D
146h	—	—	GPTW10 compare match E	GPTW10 compare match E
147h	—	—	GPTW10 compare match F	GPTW10 compare match F
148h	—	—	GPTW10 overflow	GPTW10 overflow
149h	—	—	GPTW10 underflow	GPTW10 underflow
14Ah	—	—	GPTW10 cycle count end	GPTW10 cycle count end
14Ch	—	—	GPTW10 A/D converter start request A	GPTW10 A/D converter start request A
14Dh	—	—	GPTW10 A/D converter start request B	GPTW10 A/D converter start request B
14Eh	—	—	GPTW11 compare match A	GPTW11 compare match A

Value of ELS Bits	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
14Fh	—	—	GPTW11 compare match B	GPTW11 compare match B
150h	—	—	GPTW11 compare match C	GPTW11 compare match C
151h	—	—	GPTW11 compare match D	GPTW11 compare match D
152h	—	—	GPTW11 compare match E	GPTW11 compare match E
153h	—	—	GPTW11 compare match F	GPTW11 compare match F
154h	—	—	GPTW11 overflow	GPTW11 overflow
155h	—	—	GPTW11 underflow	GPTW11 underflow
156h	—	—	GPTW11 cycle count end	GPTW11 cycle count end
158h	—	—	GPTW11 A/D converter start request A	GPTW11 A/D converter start request A
159h	—	—	GPTW11 A/D converter start request B	GPTW11 A/D converter start request B
15Ah	—	—	GPTW12 compare match A	GPTW12 compare match A
15Bh	—	—	GPTW12 compare match B	GPTW12 compare match B
15Ch	—	—	GPTW12 compare match C	GPTW12 compare match C
15Dh	—	—	GPTW12 compare match D	GPTW12 compare match D
15Eh	—	—	GPTW12 compare match E	GPTW12 compare match E
15Fh	—	—	GPTW12 compare match F	GPTW12 compare match F
160h	—	—	GPTW12 overflow	GPTW12 overflow
161h	—	—	GPTW12 underflow	GPTW12 underflow
162h	—	—	GPTW12 cycle count end	GPTW12 cycle count end
164h	—	—	GPTW12 A/D converter start request A	GPTW12 A/D converter start request A
165h	—	—	GPTW12 A/D converter start request B	GPTW12 A/D converter start request B
166h	—	—	GPTW13 compare match A	GPTW13 compare match A
167h	—	—	GPTW13 compare match B	GPTW13 compare match B
168h	—	—	GPTW13 compare match C	GPTW13 compare match C
169h	—	—	GPTW13 compare match D	GPTW13 compare match D
16Ah	—	—	GPTW13 compare match E	GPTW13 compare match E
16Bh	—	—	GPTW13 compare match F	GPTW13 compare match F
16Ch	—	—	GPTW13 overflow	GPTW13 overflow
16Dh	—	—	GPTW13 underflow	GPTW13 underflow

Value of ELS Bits	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
16Eh	—	—	GPTW13 cycle count end	GPTW13 cycle count end
170h	—	—	GPTW13 A/D converter start request A	GPTW13 A/D converter start request A
171h	—	—	GPTW13 A/D converter start request B	GPTW13 A/D converter start request B
172h	—	—	GPTW14 compare match A	GPTW14 compare match A
173h	—	—	GPTW14 compare match B	GPTW14 compare match B
174h	—	—	GPTW14 compare match C	GPTW14 compare match C
175h	—	—	GPTW14 compare match D	GPTW14 compare match D
176h	—	—	GPTW14 compare match E	GPTW14 compare match E
177h	—	—	GPTW14 compare match F	GPTW14 compare match F
178h	—	—	GPTW14 overflow	GPTW14 overflow
179h	—	—	GPTW14 underflow	GPTW14 underflow
17Ah	—	—	GPTW14 cycle count end	GPTW14 cycle count end
17Ch	—	—	GPTW14 A/D converter start request A	GPTW14 A/D converter start request A
17Dh	—	—	GPTW14 A/D converter start request B	GPTW14 A/D converter start request B
17Eh	—	—	GPTW15 compare match A	GPTW15 compare match A
17Fh	—	—	GPTW15 compare match B	GPTW15 compare match B
180h	—	—	GPTW15 compare match C	GPTW15 compare match C
181h	—	—	GPTW15 compare match D	GPTW15 compare match D
182h	—	—	GPTW15 compare match E	GPTW15 compare match E
183h	—	—	GPTW15 compare match F	GPTW15 compare match F
184h	—	—	GPTW15 overflow	GPTW15 overflow
185h	—	—	GPTW15 underflow	GPTW15 underflow
186h	—	—	GPTW15 cycle count end	GPTW15 cycle count end
188h	—	—	GPTW15 A/D converter start request A	GPTW15 A/D converter start request A
189h	—	—	GPTW15 A/D converter start request B	GPTW15 A/D converter start request B
259h	—	—	PTP pulse output 0	PTP pulse output 0
25Ah	—	—	PTP pulse output 1	PTP pulse output 1
25Bh	—	—	PTP pulse output 2	—
25Ch	—	—	PTP pulse output 3	—
25Dh	—	—	gPTP0 media clock recovery (GPTP0_MATCH)	gPTP0 media clock recovery (GPTP0_MATCH)

Value of ELS Bits	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
25Eh	—	—	gPTP1 media clock recovery (GPTP1_MATCH)	gPTP1 media clock recovery (GPTP1_MATCH)
26Dh	—	—	RSCI0 receive data full	RSCI0 receive data full
26Eh	—	—	RSCI0 transmit data empty	RSCI0 transmit data empty
26Fh	—	—	RSCI0 transmit end	RSCI0 transmit end
270h	—	—	RSCI0 error (receive error or error signal detection)	RSCI0 error (receive error or error signal detection)
271h	—	—	RSCI0 effective edge detected	RSCI0 effective edge detected
272h	—	—	RSCI0 receive data matched	RSCI0 receive data matched
273h	—	—	RSCI0 receive data unmatched	RSCI0 receive data unmatched
274h	—	—	RSCI1 receive data full	RSCI1 receive data full
275h	—	—	RSCI1 transmit data empty	RSCI1 transmit data empty
276h	—	—	RSCI1 transmit end	RSCI1 transmit end
277h	—	—	RSCI1 error (receive error or error signal detection)	RSCI1 error (receive error or error signal detection)
278h	—	—	RSCI1 effective edge detected	RSCI1 effective edge detected
279h	—	—	RSCI1 receive data matched	RSCI1 receive data matched
27Ah	—	—	RSCI1 receive data unmatched	RSCI1 receive data unmatched
27Bh	—	—	RSCI2 receive data full	RSCI2 receive data full
27Ch	—	—	RSCI2 transmit data empty	RSCI2 transmit data empty
27Dh	—	—	RSCI2 transmit end	RSCI2 transmit end
27Eh	—	—	RSCI2 error (receive error or error signal detection)	RSCI2 error (receive error or error signal detection)
27Fh	—	—	RSCI2 effective edge detected	RSCI2 effective edge detected
280h	—	—	RSCI2 receive data matched	RSCI2 receive data matched
281h	—	—	RSCI2 receive data unmatched	RSCI2 receive data unmatched
282h	—	—	RSCI3 receive data full	RSCI3 receive data full
283h	—	—	RSCI3 transmit data empty	RSCI3 transmit data empty
284h	—	—	RSCI3 transmit end	RSCI3 transmit end
285h	—	—	RSCI3 error (receive error or error signal detection)	RSCI3 error (receive error or error signal detection)
286h	—	—	RSCI3 effective edge detected	RSCI3 effective edge detected
287h	—	—	RSCI3 receive data matched	RSCI3 receive data matched

Value of ELS Bits	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
288h	—	—	RSCI3 receive data unmatched	RSCI3 receive data unmatched
289h	—	—	RSCI4 receive data full	RSCI4 receive data full
28Ah	—	—	RSCI4 transmit data empty	RSCI4 transmit data empty
28Bh	—	—	RSCI4 transmit end	RSCI4 transmit end
28Ch	—	—	RSCI4 error (receive error or error signal detection)	RSCI4 error (receive error or error signal detection)
28Dh	—	—	RSCI4 effective edge detected	RSCI4 effective edge detected
28Eh	—	—	RSCI4 receive data matched	RSCI4 receive data matched
28Fh	—	—	RSCI4 receive data unmatched	RSCI4 receive data unmatched
290h	—	—	RSCI5 receive data full	RSCI5 receive data full
291h	—	—	RSCI5 transmit data empty	RSCI5 transmit data empty
292h	—	—	RSCI5 transmit end	RSCI5 transmit end
293h	—	—	RSCI5 error (receive error or error signal detection)	RSCI5 error (receive error or error signal detection)
294h	—	—	RSCI5 effective edge detected	RSCI5 effective edge detected
295h	—	—	RSCI5 receive data matched	RSCI5 receive data matched
296h	—	—	RSCI5 receive data unmatched	RSCI5 receive data unmatched
297h	—	—	RSCI6 receive data full	RSCI6 receive data full
298h	—	—	RSCI6 transmit data empty	RSCI6 transmit data empty
299h	—	—	RSCI6 transmit end	RSCI6 transmit end
29Ah	—	—	RSCI6 error (receive error or error signal detection)	RSCI6 error (receive error or error signal detection)
29Bh	—	—	RSCI6 effective edge detected	RSCI6 effective edge detected
29Ch	—	—	RSCI6 receive data matched	RSCI6 receive data matched
29Dh	—	—	RSCI6 receive data unmatched	RSCI6 receive data unmatched
29Eh	—	—	RSCI7 receive data full	RSCI7 receive data full
29Fh	—	—	RSCI7 transmit data empty	RSCI7 transmit data empty
2A0h	—	—	RSCI7 transmit end	RSCI7 transmit end
2A1h	—	—	RSCI7 error (receive error or error signal detection)	RSCI7 error (receive error or error signal detection)
2A2h	—	—	RSCI7 effective edge detected	RSCI7 effective edge detected
2A3h	—	—	RSCI7 receive data matched	RSCI7 receive data matched

Value of ELS Bits	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
2A4h	—	—	RSCI7 receive data unmatched	RSCI7 receive data unmatched
2A5h	—	—	RSCI8 receive data full	RSCI8 receive data full
2A6h	—	—	RSCI8 transmit data empty	RSCI8 transmit data empty
2A7h	—	—	RSCI8 transmit end	RSCI8 transmit end
2A8h	—	—	RSCI8 error (receive error or error signal detection)	RSCI8 error (receive error or error signal detection)
2A9h	—	—	RSCI8 effective edge detected	RSCI8 effective edge detected
2AAh	—	—	RSCI8 receive data matched	RSCI8 receive data matched
2ABh	—	—	RSCI8 receive data unmatched	RSCI8 receive data unmatched
2ACh	—	—	RSCI9 receive data full	RSCI9 receive data full
2ADh	—	—	RSCI9 transmit data empty	RSCI9 transmit data empty
2AEh	—	—	RSCI9 transmit end	RSCI9 transmit end
2AFh	—	—	RSCI9 error (receive error or error signal detection)	RSCI9 error (receive error or error signal detection)
2B0h	—	—	RSCI9 effective edge detected	RSCI9 effective edge detected
2B1h	—	—	RSCI9 receive data matched	RSCI9 receive data matched
2B2h	—	—	RSCI9 receive data unmatched	RSCI9 receive data unmatched
2B3h	—	—	RSCI10 receive data full	RSCI10 receive data full
2B4h	—	—	RSCI10 transmit data empty	RSCI10 transmit data empty
2B5h	—	—	RSCI10 transmit end	RSCI10 transmit end
2B6h	—	—	RSCI10 error (receive error or error signal detection)	RSCI10 error (receive error or error signal detection)
2B7h	—	—	RSCI10 effective edge detected	RSCI10 effective edge detected
2B8h	—	—	RSCI10 receive data matched	RSCI10 receive data matched
2B9h	—	—	RSCI10 receive data unmatched	RSCI10 receive data unmatched
2BAh	—	—	RSCI11 receive data full	RSCI11 receive data full
2BBh	—	—	RSCI11 transmit data empty	RSCI11 transmit data empty
2BCh	—	—	RSCI11 transmit end	RSCI11 transmit end
2BDh	—	—	RSCI11 error (receive error or error signal detection)	RSCI11 error (receive error or error signal detection)
2BEh	—	—	RSCI11 effective edge detected	RSCI11 effective edge detected

Value of ELS Bits	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
2BFh	—	—	RSCI11 receive data matched	RSCI11 receive data matched
2C0h	—	—	RSCI11 receive data unmatched	RSCI11 receive data unmatched
2C1h	—	—	RSCI12 receive data full	RSCI12 receive data full
2C2h	—	—	RSCI12 transmit data empty	RSCI12 transmit data empty
2C3h	—	—	RSCI12 transmit end	RSCI12 transmit end
2C4h	—	—	RSCI12 error (receive error or error signal detection)	RSCI12 error (receive error or error signal detection)
2C5h	—	—	RSCI12 effective edge detected	RSCI12 effective edge detected
2C6h	—	—	RSCI12 receive data matched	RSCI12 receive data matched
2C7h	—	—	RSCI12 receive data unmatched	RSCI12 receive data unmatched
2C8h	—	—	RSPI0 receive buffer full	RSPI0 receive buffer full
2C9h	—	—	RSPI0 transmit buffer empty	RSPI0 transmit buffer empty
2CAh	—	—	RSPI0 idle	RSPI0 idle
2CBh	—	—	RSPI0 error (mode fault, overrun, underrun, or parity error)	RSPI0 error (mode fault, overrun, underrun, or parity error)
2CCh	—	—	RSPI0 communication end	RSPI0 communication end
2CDh	—	—	RSPI1 receive buffer full	RSPI1 receive buffer full
2CEh	—	—	RSPI1 transmit buffer empty	RSPI1 transmit buffer empty
2CFh	—	—	RSPI1 idle	RSPI1 idle
2D0h	—	—	RSPI1 error (mode fault, overrun, underrun, or parity error)	RSPI1 error (mode fault, overrun, underrun, or parity error)
2D1h	—	—	RSPI1 communication end	RSPI1 communication end
2D2h	—	—	RSPI2 receive buffer full	RSPI2 receive buffer full
2D3h	—	—	RSPI2 transmit buffer empty	RSPI2 transmit buffer empty
2D4h	—	—	RSPI2 idle	RSPI2 idle
2D5h	—	—	RSPI2 error (mode fault, overrun, underrun, or parity error)	RSPI2 error (mode fault, overrun, underrun, or parity error)
2D6h	—	—	RSPI2 communication end	RSPI2 communication end
2DBh	—	—	RIICHS1 receive data full	RIICHS1 receive data full
2DCh	—	—	RIICHS1 transmit data empty	RIICHS1 transmit data empty
2DDh	—	—	RIICHS1 transmit end	RIICHS1 transmit end

Value of ELS Bits	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
2DEh	—	—	RIICHS1 communication error or communication event	RIICHS1 communication error or communication event
2DFh	—	—	RIICHS2 receive data full	RIICHS2 receive data full
2E0h	—	—	RIICHS2 transmit data empty	RIICHS2 transmit data empty
2E1h	—	—	RIICHS2 transmit end	RIICHS2 transmit end
2E2h	—	—	RIICHS2 communication error or communication event	RIICHS2 communication error or communication event
2E3h	—	—	RI3C0 response queue full	RI3C0 response queue full
2E4h	—	—	RI3C0 command queue empty	RI3C0 command queue empty
2E5h	—	—	RI3C0 IBI queue empty	RI3C0 IBI queue empty
2E6h	—	—	RI3C0 receive data full	RI3C0 receive data full
2E7h	—	—	RI3C0 transmit data empty	RI3C0 transmit data empty
2E8h	—	—	RI3C0 receive status queue full	RI3C0 receive status queue full
2E9h	—	—	RI3C0 high priority response queue full	RI3C0 high priority response queue full
2EAh	—	—	RI3C0 high priority command queue empty	RI3C0 high priority command queue empty
2EBh	—	—	RI3C0 high priority receive data full	RI3C0 high priority receive data full
2ECh	—	—	RI3C0 high priority transmit data empty	RI3C0 high priority transmit data empty
2EDh	—	—	RI3C0 transmit end (in I^2C mode)	RI3C0 transmit end (in I^2C mode)
2EEh	—	—	RI3C0 communication error or communication event	RI3C0 communication error or communication event
2EFh	—	—	RI3C0 synchronous timing	RI3C0 synchronous timing
2F0h	—	—	RI3C0 MREF counter overflow	RI3C0 MREF counter overflow
2F1h	—	—	RI3C0 MREF capture	RI3C0 MREF capture
2F2h	—	—	RI3C0 additional master-initiated bus event	RI3C0 additional master-initiated bus event
313h	—	—	DOC data operation condition met	DOC data operation condition met
314h	—	—	Group 0 A/D conversion end	Group 0 A/D conversion end
315h	—	—	Group 1 A/D conversion end	Group 1 A/D conversion end
316h	—	—	Group 2 A/D conversion end	Group 2 A/D conversion end
317h	—	—	Group 3 A/D conversion end	Group 3 A/D conversion end

Value of ELS Bits	RX72M (ELC)	RX72N (ELC)	RX74M (ELC)	RX74N (ELC)
318h	—	—	Group 4 A/D conversion end	Group 4 A/D conversion end
319h	—	—	Group 5 A/D conversion end	Group 5 A/D conversion end
31Ah	—	—	Group 6 A/D conversion end	Group 6 A/D conversion end
31Bh	—	—	Group 7 A/D conversion end	Group 7 A/D conversion end
31Ch	—	—	Group 8 A/D conversion end	Group 8 A/D conversion end
31Dh	—	—	Group 9 A/D conversion end	Group 9 A/D conversion end
31Eh	—	—	Group 10 A/D conversion end	Group 10 A/D conversion end
31Fh	—	—	Group 11 A/D conversion end	Group 11 A/D conversion end
324h	—	—	Multiplex compare match 0	Multiplex compare match 0
325h	—	—	Multiplex compare match 1	Multiplex compare match 1
326h	—	—	Multiplex compare match 2	Multiplex compare match 2
327h	—	—	Multiplex compare match 3	Multiplex compare match 3
328h	—	—	Multiplex compare match 4	Multiplex compare match 4
329h	—	—	Multiplex compare match 5	Multiplex compare match 5
32Ah	—	—	Multiplex compare match 6	Multiplex compare match 6
32Bh	—	—	Multiplex compare match 7	Multiplex compare match 7
334h	—	—	Multiplex compare mismatch 0	Multiplex compare mismatch 0
335h	—	—	Multiplex compare mismatch 1	Multiplex compare mismatch 1
336h	—	—	Multiplex compare mismatch 2	Multiplex compare mismatch 2
337h	—	—	Multiplex compare mismatch 3	Multiplex compare mismatch 3
338h	—	—	Multiplex compare mismatch 4	Multiplex compare mismatch 4
339h	—	—	Multiplex compare mismatch 5	Multiplex compare mismatch 5
33Ah	—	—	Multiplex compare mismatch 6	Multiplex compare mismatch 6
33Bh	—	—	Multiplex compare mismatch 7	Multiplex compare mismatch 7

2.20 I/O Ports

Table 2.46 is Comparative Overview of I/O Ports on 224-Pin Products, Table 2.47 is Comparative Overview of I/O Ports on 176-Pin Products, Table 2.48 is Comparative Overview of I/O Ports on 145-Pin and 144-Pin Products, Table 2.49 is Comparative Overview of I/O Ports on 100-Pin Products, Table 2.50 is Comparison of I/O Port Functions, and Table 2.51 is Comparison of I/O Port Registers.

Table 2.46 Comparative Overview of I/O Ports on 224-Pin Products

Item	RX72M (224 Pins)/RX72N (224 Pins)	RX74M (224 Pins)/RX74N (224 Pins)
PORT0	P00 to P03, P05, P07	P000 to P007
PORT1	P10 to P17	P100 to P115
PORT2	P20 to P27	P200 to P215
PORT3	P30 to P37	P300 to P312, P315
PORT4	P40 to P47	P400 to P407, P414, P415
PORT5	P50 to P57	P500 to P507
PORT6	P60 to P67	P600 to P607
PORT7	P70 to P77	P700 to P707
PORT8	P80 to P87	P800 to P807
PORT9	P90 to P97	P900 to P907
PORTA	PA0 to PA7	PA00 to PA07
PORTB	PB0 to PB7	PB00 to PB07
PORTC	PC0 to PC7	PC00 to PC07
PORTD	PD0 to PD7	PD00 to PD07
PORTE	PE0 to PE7	PE00 to PE07
PORTF	PF0 to PF5	PF00 to PF09
PORTG	PG0 to PG7	PG00 to PG07
PORTH	PH0 to PH7	—
PORTJ	PJ0 to PJ3, PJ5	—
PORTK	PK0 to PK7	—
PORTL	PL0 to PL7	—
PORTM	PM0 to PM7	—
PORTN	PN0 to PN5	—
PORTQ	PQ0 to PQ7	—

Table 2.47 Comparative Overview of I/O Ports on 176-Pin Products

Item	RX72M (176 Pins)/RX72N (176 Pins)	RX74M (176 Pins)/RX74N (176 Pins)
PORT0	P00 to P03, P05, P07	P000 to P007
PORT1	P10 to P17	P100 to P107
PORT2	P20 to P27	P200 to P207
PORT3	P30 to P37	P300 to P312, P315
PORT4	P40 to P47	P400 to P407, P414, P415
PORT5	P50 to P57	P500 to P503
PORT6	P60 to P67	P600 to P607
PORT7	P70 to P77	P700 to P707
PORT8	P80 to P87	P800 to P805
PORT9	P90 to P97	P900 to P903
PORTA	PA0 to PA7	PA00 to PA07
PORTB	PB0 to PB7	PB00 to PB07
PORTC	PC0 to PC7	PC00 to PC07
PORTD	PD0 to PD7	PD00 to PD07
PORTE	PE0 to PE7	PE00 to PE07
PORTF	PF0 to PF5	PF00, PF01
PORTG	PG0 to PG7	PG00 to PG02
PORTJ	PJ0 to PJ3, PJ5	—

Table 2.48 Comparative Overview of I/O Ports on 145-Pin and 144-Pin Products

Item	RX72M (144 Pins)	RX72N (145 Pins, 144 Pins)	RX74M (144 Pins)/ RX74N (144 Pins)
PORT0	P00 to P03, P05	P00 to P03, P05, P07	P000 to P007
PORT1	P12 to P17	P12 to P17	P100 to P107
PORT2	P20 to P27	P20 to P27	P200 to P207
PORT3	P30 to P37	P30 to P37	P300 to P312, P315
PORT4	P40 to P44	P40 to P47	P400 to P405, P414, P415
PORT5	P50 to P56	P50 to P56	—
PORT6	P60 to P67	P60 to P67	P600 to P605
PORT7	P73 to P77	P70 to P77	P700 to P702
PORT8	P80 to P83, P86, P87	P80 to P83, P86, P87	P800 to P803
PORT9	P90 to P93, P96, P97	P90 to P93	P900, P901
PORTA	PA0 to PA7	PA0 to PA7	PA00 to PA07
PORTB	PB0 to PB7	PB0 to PB7	PB00 to PB07
PORTC	PC0 to PC7	PC0 to PC7	PC00 to PC07
PORTD	PD0 to PD7	PD0 to PD7	PD00 to PD07
PORTE	PE0 to PE7	PE0 to PE7	PE00 to PE07
PORTF	—	PF5	PF00, PF01
PORTG	PG0 to PG2, PG5 to PG7	—	—
PORTJ	PJ2, PJ3	PJ3, PJ5	—

Table 2.49 Comparative Overview of I/O Ports on 100-Pin Products

Item	RX72M (100 Pins)	RX72N (100 Pins)	RX74M (100 Pins)/ RX74N (100 Pins)
PORT0	P00	P05, P07	P001 to P007
PORT1	P14 to P17	P12 to P17	P101 to P107
PORT2	P20, P21, P23 to P27	P20 to P27	P200, P201
PORT3	P30 to P37	P30 to P37	P300 to P312, P315
PORT4	P40 to P42	P40 to P47	P400, P402, P404, P414
PORT5	P50 to P52, P56	P50 to P55	—
PORT6	P60 to P64, P66, P67	—	P600, P601
PORT8	P80 to P82, P86, P87	—	—
PORT9	P90 to P93, P96, P97	—	—
PORTA	PA0 to PA4, PA6	PA0 to PA7	PA00 to PA07
PORTB	PB0, PB1, PB3 to PB7	PB0 to PB7	PB00 to PB06
PORTC	PC2, PC4 to PC7	PC0 to PC7	PC00 to PC06
PORTD	PD1, PD2, PD6, PD7	PD0 to PD7	PD00 to PD07
PORTE	PE3 to PE5	PE0 to PE7	PE00 to PE06
PORTF	—	—	PF00, PF01
PORTG	PG2, PG5, PG6	—	—
PORTJ	—	PJ3	—

Table 2.50 Comparison of I/O Port Functions

Item	Port Symbol	RX72M/RX72N	RX74M/RX74N
Input pull-up	PORT0	P00 to P03, P05, P07	P000 to P015
	PORT1	P10 to P17	P100 to P115
	PORT2	P20 to P27	P200 to P215
	PORT3	P30 to P34, P36, P37	P300 to P307, P310 to P312, P315
	PORT4	P40 to P47	P400 to P415
	PORT5	P50 to P57	P500 to P515
	PORT6	P60 to P67	P600 to P607
	PORT7	P70 to P77	P700 to P715
	PORT8	P80 to P87	P800 to P807
	PORT9	P90 to P97	P900 to P907
	PORTA	PA0 to PA7	PA00 to PA07
	PORTB	PB0 to PB7	PB00 to PB07
	PORTC	PC0 to PC7	PC00 to PC07
	PORTD	PD0 to PD7	PD00 to PD07
	PORTE	PE0 to PE7	PE00 to PE07
	PORTF	PF0 to PF5	PF00 to PF09
	PORTG	PG0 to PG7	PG00 to PG15
	PORTH	PH0 to PH7	—
	PORTJ	PJ0 to PJ3, PJ5	—
	PORTK	PK0 to PK7	—
	PORTL	PL0 to PL7	—
	PORTM	PM0 to PM7	—
	PORTN	PN0 to PN5	—
	PORTQ	PQ0 to PQ7	—
Open-drain output	PORT0	P00 to P03, P05, P07	P000 to P015
	PORT1	P10 to P17	P100 to P115
	PORT2	P20 to P27	P200 to P215
	PORT3	P30 to P34, P36, P37	P300 to P304, P306, P307, P310 to P312, P315
	PORT4	P40 to P47	P400 to P415
	PORT5	P50 to P57	P500 to P515
	PORT6	P60 to P67	P600 to P607
	PORT7	P70 to P77	P700 to P715
	PORT8	P80 to P87	P800 to P807
	PORT9	P90 to P97	P900 to P907
	PORTA	PA0 to PA7	PA00 to PA07
	PORTB	PB0 to PB7	PB00 to PB07
	PORTC	PC0 to PC7	PC00 to PC07
	PORTD	PD0 to PD7	PD00 to PD07
	PORTE	PE0 to PE7	PE00 to PE07
	PORTF	PF0 to PF5	PF00 to PF09
	PORTG	PG0 to PG7	PG00 to PG15
	PORTH	PH0 to PH7	—
	PORTJ	PJ0 to PJ3, PJ5	—
	PORTK	PK0 to PK7	—
	PORTL	PL0 to PL7	—
	PORTM	PM0 to PM7	—
	PORTN	PN0 to PN5	—
	PORTQ	PQ0 to PQ7	—

Item	Port Symbol	RX72M/RX72N	RX74M/RX74N
Driving ability switching *1	PORT0	P00 to P03, P05, P07	P000 to P015
	PORT1	P10 to P17	P100 to P115
	PORT2	P20 to P27	P200 to P215
	PORT3	P30 to P34, P36, P37	P300 to P304, P306, P307, P310 to P312, P315
	PORT4	P40 to P47	P400 to P415
	PORT5	P50 to P57	P500 to P515
	PORT6	P60 to P67	P600 to P607
	PORT7	P70 to P77	P700 to P715
	PORT8	P80 to P87	P800 to P807
	PORT9	P90 to P97	P900 to P907
	PORTA	PA0 to PA7	PA00 to PA07
	PORTB	PB0 to PB7	PB00 to PB07
	PORTC	PC0 to PC7	PC00 to PC07
	PORTD	PD0 to PD7	PD00 to PD07
	PORTE	PE0 to PE7	PE00 to PE07
	PORTF	PF0 to PF5	PF00 to PF09
	PORTG	PG0 to PG7	PG00 to PG15
	PORTH	PH0 to PH7	—
	PORTJ	PJ0 to PJ3, PJ5	—
	PORTK	PK0 to PK7	—
	PORTL	PL0 to PL7	—
	PORTM	PM0 to PM7	—
	PORTN	PN0 to PN5	—
	PORTQ	PQ0 to PQ7	—
5-V tolerant	PORT0	P07	—
	PORT1	P11 to P17	P100 to P107
	PORT2	P20, P21	P200 to P207
	PORT3	P30 to P33	—
	PORT6	P67	—
	PORTC	PC0 to PC3	—
3-V tolerant	PORT3	—	P310 to P312

Note:1. Note that the configurable items for the driving ability switching of the RX74M/RX74N Group have changed significantly from those of the RX72M/RX72N Group.

Table 2.51 Comparison of I/O Port Registers

Register	Bit	RX72M/RX72N	RX74M/RX74N
PDR	—	Port direction register PDR is an 8-bit register.	Port direction register PDR is a 16-bit register.
	B0 to B7 (RX72M/RX72N) PDR00 to PDR07 (RX74M/RX74N)	Pm0 to 7 I/O select bits (m = 0 to 9, A to H, J to N, Q)	Pm00 to 07 I/O direction select bits (m = 0 to 9, A to G)
	PDR08 to PDR15	—	Pm08 to 15 I/O direction select bits (m = 0 to 9, A to G)
PODR	—	Port output data register PODR is an 8-bit register.	Port output data register PODR is a 16-bit register.
	B0 to B7 (RX72M/RX72N) PODR00 to PODR07 (RX74M/RX74N)	Pm0 to 7 output data store bits (m = 0 to 9, A to H, J to N, Q)	Pm00 to 07 output data bits (m = 0 to 9, A to G)
	PODR08 to PODR15	—	Pm08 to 15 output data bits (m = 0 to 9, A to G)
PIDR	—	Port input register PIDR is an 8-bit register.	Port input data register PIDR is a 16-bit register.
	B0 to B7 (RX72M/RX72N) PIDR00 to PIDR07 (RX74M/RX74N)	Pm0 to 7 bits (m = 0 to 9, A to H, J to N, Q)	Pm00 to 07 input data bits (m = 0 to 9, A to G)
	PIDR08 to PIDR15	—	Pm08 to 15 input data bits (m = 0 to 9, A to G)
PMR	—	Port mode register	—
ODR0	—	Open-drain control register 0	—
ODR1	—	Open-drain control register 1	—
PCR	—	Pull-up resistor control register	—
DSCR	—	Drive capacity control register	—
DSCR2	—	Drive capacity control register 2	—
PCNTR1	—	—	Port control register 1
PCNTR2	—	—	Port control register 2
EIDR	—	—	Port event input data register
PCNTR3	—	—	Port control register 3
POSR	—	—	Port output set register
PORR	—	—	Port output reset register
PCNTR4	—	—	Port control register 4
EOSR	—	—	Event output set register
EORR	—	—	Event output reset register

Register	Bit	RX72M/RX72N	RX74M/RX74N
PmnPFS	—	—	Pmn pin function selection register (m = 0 to 9, A to G, n = 00 to 15)
PWPR_NS	—	—	Non-secure world write protection register
PWPR_S	—	—	Secure world write protection register
PmSAR	—	—	Port security attribute setting register (m = 0 to 9, A to G)
LVOCR	—	—	Low-voltage operating characteristics control register

2.21 General PWM Timer

Table 2.52 is Comparative Overview of General PWM Timers, Table 2.53 is Comparison of General PWM Timer Registers, and Table 2.54 is Comparison of Settings of GTIOA/B Bits.

Table 2.52 Comparative Overview of General PWM Timers

Item	RX72M (GPTW)/RX72N (GPTW)	RX74M (GPTW)/RX74N (GPTW)
Functions	• 32 bits × 4 channels • Up-counting or down-counting (sawtooth waves) or up/down-counting (triangle waves) for each counter. • Clock sources independently selectable for each channel • Two I/O pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms. • Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow) • Generation of dead times in PWM operation • Simultaneous start/stop/clearing of desired channel counters Operation of count start/count stop/counter clearing/up-counting/down-counting/input capture by maximum of eight ELC events based on the ELC setting • Operation of count start/count stop/counter clearing/up-counting/down-counting/input capture by detecting two input signal conditions • Operation of count start/count stop/counter clearing/up-counting/down-counting/input capture by maximum of four external triggers	• 32 bits ×16 channels • Up-counting or down-counting (sawtooth waves) or up/down-counting (triangle waves) for each counter • Clock sources independently selectable for each channel • Two I/O pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can take place at crests or troughs, enabling the generation of laterally asymmetrical PWM waveforms. • Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow) • Generation of dead times in PWM operation • The direction of counting can be switched in triangle-wave PWM mode. • Generation of high accuracy duty in the vicinity of duty 0% and 100% PWM waveform • In output compare operation, setting compare register is immediately used to generate PWM waveform with dead times • Simultaneous start/stop/clearing/switch of desired channel counters • Operation of count start/count stop/counter clearing/count switch/up-counting/down-counting/input capture by maximum of eight ELC events based on the ELC setting • Operation of count start/count stop/counter clearing/up-counting/down-counting/input capture by detecting two input signal conditions • Operation of count start/count stop/counter clearing/count switch/up-counting/down-counting/input capture by maximum of four external triggers

Item	RX72M (GPTW)/RX72N (GPTW)	RX74M (GPTW)/RX74N (GPTW)
Functions	• Function to control output negation by requests for disabling of output from the POEG • A/D conversion start trigger generation function • Event signals for compare match A to F and for overflow/underflow can be output to the ELC • Input capture input can select noise filter function • Bus clock: PCLKA, GPTW count reference clock: PCLKA	• Function to control output negation by dead time error and requests for disabling of output from the POEG • A/D conversion start trigger generation function • Event signals for compare match A to F and for overflow/underflow can be output to the ELC • Input capture input can select noise filter function • Cycle count function • External pulse width measuring function • Logical operation between the channel output • Synchronous counter clearing/counter setting/input capture among channels • The timer-linked synchronization signal output function enables synchronous operation between channels synchronized with the timer period, and synchronous operation with other IPs synchronized with the timer period. • GTIOCnA/GTIOCnB pin input/output polarity inversion • Bus clock: PCLKA, GPTW count reference clock: GTCLK*1 Frequency ratio between PCLKA:PCLKD = 1:N (N = 1/2/4/8/16/32/64) when the synchronous clock is in use; PCLKA ≤ GPTCLK when the asynchronous clock is in use

Note: 1. Selection of the synchronous clock leads to the selection of PCLKD and selection of the asynchronous clock leads to the selection of GPTCLK as the GPTW count reference clock (GTCLK).

Table 2.53 Comparison of General PWM Timer Registers

Register	Bit	RX72M (GPTW)/ RX72N (GPTW)	RX74M (GPTW)/ RX74N (GPTW)
GTSTR	CSTRT4	—	Channel 4 count start bit
	CSTRT5	—	Channel 5 count start bit
	CSTRT6	—	Channel 6 count start bit
	CSTRT7	—	Channel 7 count start bit
	CSTRT8	—	Channel 8 count start bit
	CSTRT9	—	Channel 9 count start bit
	CSTRT10	—	Channel 10 count start bit
	CSTRT11	—	Channel 11 count start bit
	CSTRT12	—	Channel 12 count start bit
	CSTRT13	—	Channel 13 count start bit
	CSTRT14	—	Channel 14 count start bit
	CSTRT15	—	Channel 15 count start bit
GTSTP	CSTOP4	—	Channel 4 count stop bit
	CSTOP5	—	Channel 5 count stop bit
	CSTOP6	—	Channel 6 count stop bit
	CSTOP7	—	Channel 7 count stop bit
	CSTOP8	—	Channel 8 count stop bit
	CSTOP9	—	Channel 9 count stop bit
	CSTOP10	—	Channel 10 count stop bit
	CSTOP11	—	Channel 11 count stop bit
	CSTOP12	—	Channel 12 count stop bit
	CSTOP13	—	Channel 13 count stop bit
	CSTOP14	—	Channel 14 count stop bit
	CSTOP15	—	Channel 15 count stop bit
GTCLR	CCLR4	—	Channel 4 counter clear bit
	CCLR5	—	Channel 5 counter clear bit
	CCLR6	—	Channel 6 counter clear bit
	CCLR7	—	Channel 7 counter clear bit
	CCLR8	—	Channel 8 counter clear bit
	CCLR9	—	Channel 9 counter clear bit
	CCLR10	—	Channel 10 counter clear bit
	CCLR11	—	Channel 11 counter clear bit
	CCLR12	—	Channel 12 counter clear bit
	CCLR13	—	Channel 13 counter clear bit
	CCLR14	—	Channel 14 counter clear bit
	CCLR15	—	Channel 15 counter clear bit
GTCSR	CSCMSC[2:0]	—	Compare match/input capture/synchronous counter clearing source counter clear enable bits
	CP1CCE	—	Complementary PWM mode 1 crest source counter clear enable bit
GTUPSR	USILVL[3:0]	—	External input level source count-up enable bits
GTDNSR	DSILVL[3:0]	—	External input level source count-down enable bits
GTICASR	ASOC	—	Other channel source GTCCRA input capture enable bit
GTICBSR	BSOC	—	Other channel source GTCCRB input capture enable bit

Register	Bit	RX72M (GPTW)/ RX72N (GPTW)	RX74M (GPTW)/ RX74N (GPTW)
GTSWSR	—	—	General PWM timer switch source select register
GTSWOS	—	—	General PWM timer switch offset setting register
GPTWm.GTCR (m = 0 to 3)	AINV	—	GTIOCnA input/output pin polarity reversal control bit
	BINV	—	GTIOCnB input/output pin polarity reversal control bit
	SCGTIOC	—	GTIOC input source synchronous clear enable bit
	SSCGRP[1:0]	—	Synchronous set/clear group select bits
	SSCEN	—	Synchronous set/clear enable bit
	TPCS[3:0]	Timer prescaler select bits b26 b23 0 0 0 0: PCLKA 0 0 0 1: PCLKA/2 0 0 1 0: PCLKA/4 0 0 1 1: PCLKA/8 0 1 0 0: PCLKA/16 0 1 0 1: PCLKA/32 0 1 1 0: PCLKA/64 0 1 1 1: Setting prohibited 1 0 0 0: PCLKA/256 1 0 0 1: Setting prohibited 1 0 1 0: PCLKA/1024 1 0 1 1: Setting prohibited 1 1 0 0: GTETRGA (via the POEG) 1 1 0 1: GTETRGB (via the POEG) 1 1 1 0: GTETRGC (via the POEG) 1 1 1 1: GTETRGD (via the POEG)	Timer prescaler select bits b26 b23 0 0 0 0: GTCLK 0 0 0 1: GTCLK/2 0 0 1 0: GTCLK/4 0 0 1 1: GTCLK/8 0 1 0 0: GTCLK/16 0 1 0 1: GTCLK/32 0 1 1 0: GTCLK/64 0 1 1 1: GTCLK/128 1 0 0 0: GTCLK/256 1 0 0 1: GTCLK/512 1 0 1 0: GTCLK/1024 1 0 1 1: Setting prohibited 1 1 0 0: GTETRGA (via the POEG) 1 1 0 1: GTETRGB (via the POEG) 1 1 1 0: GTETRGC (via the POEG) 1 1 1 1: GTETRGD (via the POEG)
	CKEG[1:0]	—	Clock edge select bits
	SWMD[2:0]	—	Switch mode select bits
GPTWm.GTCR (m = 4 to 15)	—	—	General PWM timer control register
GTIOR	GTIOA[4:0]	GTIOCnA pin function select bits See Table 2.54.	GTIOCnA pin function select bits See Table 2.54.
	CPSCIR	—	Complementary PWM mode initial output at synchronous clear disable bit
	OAEOCD	—	GTCCRA register compare match cycle end output invalidate bit
	PSYE	—	PWM synchronous output enable bit

Register	Bit	RX72M (GPTW)/ RX72N (GPTW)	RX74M (GPTW)/ RX74N (GPTW)
GTIOR	NFCSA[1:0]	GTIOCnA pin input noise filter sampling clock select bits b15 b14 0 0: PCLKA 0 1: PCLKA/4 1 0: PCLKA/16 1 1: PCLKA/64	GTIOCnA pin input noise filter sampling clock select bits b15 b14 0 0: GTCLK 0 1: GTCLK/4 1 0: GTCLK/16 1 1: GTCLK/64
	GTIOB[4:0]	GTIOCnB pin function select bits See Table 2.54.	GTIOCnB pin function select bits See Table 2.54.
	OBEOCD	—	GTCCRB register compare match cycle end output invalidate bit
	NFCSB[1:0]	GTIOCnB pin input noise filter sampling clock select bits b31 b30 0 0: PCLKA 0 1: PCLKA/4 1 0: PCLKA/16 1 1: PCLKA/64	GTIOCnB pin input noise filter sampling clock select bits b31 b30 0 0: GTCLK 0 1: GTCLK/4 1 0: GTCLK/16 1 1: GTCLK/64
GTINTAD	SCFA	—	GTCCRA register compare match/input capture source synchronous clear enable bit
	SCFB	—	GTCCRB register compare match/input capture source synchronous clear enable bit
	SCFC	—	GTCCRC register compare match/input capture source synchronous clear enable bit
	SCFD	—	GTCCRD register compare match/input capture source synchronous clear enable bit
	SCFE	—	GTCCRE register compare match source synchronous clear enable bit
	SCFF	—	GTCCRF register compare match source synchronous clear enable bit
	SCFPO	—	Overflow source synchronous clear enable bit
	SCFPU	—	Underflow source synchronous clear enable bit
	GTINTPC	—	Cycle count end interrupt enable bit
GTST	TCFA	—	Input capture/compare match flag A
	TCFB	—	Input capture/compare match flag B
	TCFC	—	Compare match flag C
	TCFD	—	Compare match flag D
	TCFE	—	Compare match flag E
	TCFF	—	Compare match flag F
	TCFPO	—	Overflow flag
	TCFPU	—	Underflow flag
	PCF	—	Cycle count end flag
GTBER	DBRTSCA	—	GTCCRA register double buffer repeat operation period select bit

Register	Bit	RX72M (GPTW)/ RX72N (GPTW)	RX74M (GPTW)/ RX74N (GPTW)
GTBER	DBRTSCB	—	GTCCRB register double buffer repeat operation period select bit
	DBRTEADA	—	GTADTRA register double buffer repeat operation enable bit
	DBRTSADA	—	GTADTRA register double buffer repeat operation period select bit
	DBRTEADB	—	GTADTRB register double buffer repeat operation enable bit
	DBRTSADB	—	GTADTRB register double buffer repeat operation period select bit
	ADTTA[1:0]	GTADTRA register buffer transfer timing select bits • Triangle waves b25 b24 0 0: No transfer 0 1: Transfer at crest 1 0: Transfer at trough 1 1: Transfer at both crest and trough • Sawtooth waves b25 b24 0 0: No transfer Values other than 0 0: Transfer at underflow (during down-counting), overflow (during up-counting), or counter clearing	GTADTRA register buffer transfer timing select bits • Triangle waves or in complementary PWM mode b25 b24 0 0: No transfer 0 1: Transfer at crest 1 0: Transfer at trough 1 1: Transfer at both crest and trough • Sawtooth waves b25 b24 0 0: No transfer Values other than 0 0: Transfer at underflow (during down-counting), overflow (during up-counting), or counter clearing
	ADTTB[1:0]	GTADTRB register buffer transfer timing select bits • Triangle waves b29 b28 0 0: No transfer 0 1: Transfer at crest 1 0: Transfer at trough 1 1: Transfer at both crest and trough • Sawtooth waves b29 b28 0 0: No transfer Values other than 0 0: Transfer at underflow (during down-counting), overflow (during up-counting), or counter clearing	GTADTRB register buffer transfer timing select bits • Triangle waves or in complementary PWM mode b29 b28 0 0: No transfer 0 1: Transfer at crest 1 0: Transfer at trough 1 1: Transfer at both crest and trough • Sawtooth waves b29 b28 0 0: No transfer Values other than 0 0: Transfer at underflow (during down-counting), overflow (during up-counting), or counter clearing
GTBER2	—	—	General PWM timer buffer enable register 2

Register	Bit	RX72M (GPTW)/ RX72N (GPTW)	RX74M (GPTW)/ RX74N (GPTW)
GTEITC	EIVTC1[1:0]	Extended interrupt skipping counter 1 count source select bits b1 b0 0 0: Not counted (not skipped) 0 1: Counting both at overflow or underflow in sawtooth-wave mode, and counting crests in triangle-wave mode 1 0: Counting both at overflow or underflow in sawtooth-wave mode, and counting troughs in triangle-wave mode 1 1: Counting both at overflow or underflow in sawtooth-wave mode, and counting both crests and troughs in triangle-wave mode	Extended interrupt skipping counter 1 count source select bits b1 b0 0 0: Not counted (not skipped) 0 1: Counting both at overflow or underflow in sawtooth-wave mode, and counting crests in triangle-wave mode or complementary PWM mode 1 0: Counting both at overflow or underflow in sawtooth-wave mode, and counting troughs in triangle-wave mode or complementary PWM mode 1 1: Counting both at overflow or underflow in sawtooth-wave mode, and counting both crests and troughs in triangle-wave mode or complementary PWM mode
	EIVTC2[1:0]	Extended interrupt skipping counter 2 count source select bits b17 b16 0 0: Not counted (not skipped) 0 1: Counting both at overflow or underflow in sawtooth-wave mode, and counting crests in triangle-wave mode 1 0: Counting both at overflow or underflow in sawtooth-wave mode, and counting troughs in triangle-wave mode 1 1: Counting both at overflow or underflow in sawtooth-wave mode, and counting both crests and troughs in triangle-wave mode	Extended interrupt skipping counter 2 count source select bits b17 b16 0 0: Not counted (not skipped) 0 1: Counting both at overflow or underflow in sawtooth-wave mode, and counting crests in triangle-wave mode or complementary PWM mode 1 0: Counting both at overflow or underflow in sawtooth-wave mode, and counting troughs in triangle-wave mode or complementary PWM mode 1 1: Counting both at overflow or underflow in sawtooth-wave mode, and counting both crests and troughs in triangle-wave mode or complementary PWM mode
GTICLF	—	—	General PWM timer inter channel logical operation function setting register
GTPC	—	—	General PWM timer cycle count register
GTADCMSC	—	—	General PWM timer A/D conversion start request compare match skipping control register
GTADCMSS	—	—	General PWM timer A/D conversion start request compare match skipping setting register

Register	Bit	RX72M (GPTW)/ RX72N (GPTW)	RX74M (GPTW)/ RX74N (GPTW)
GTSECSR	SECSEL4	—	Channel 4 operation enable bit simultaneous control channel select bit
	SECSEL5	—	Channel 5 operation enable bit simultaneous control channel select bit
	SECSEL6	—	Channel 6 operation enable bit simultaneous control channel select bit
	SECSEL7	—	Channel 7 operation enable bit simultaneous control channel select bit
	SECSEL8	—	Channel 8 operation enable bit simultaneous control channel select bit
	SECSEL9	—	Channel 9 operation enable bit simultaneous control channel select bit
	SECSEL10	—	Channel 10 operation enable bit simultaneous control channel select bit
	SECSEL11	—	Channel 11 operation enable bit simultaneous control channel select bit
	SECSEL12	—	Channel 12 operation enable bit simultaneous control channel select bit
	SECSEL13	—	Channel 13 operation enable bit simultaneous control channel select bit
	SECSEL14	—	Channel 14 operation enable bit simultaneous control channel select bit
	SECSEL15	—	Channel 15 operation enable bit simultaneous control channel select bit
GTSECR	SPCE	—	Cycle count function simultaneous enable bit
	SSCE	—	Synchronous set/clear simultaneous enable bit
	SPCD	—	Cycle count function simultaneous disable bit
	SSCD	—	Synchronous set/clear simultaneous disable bit
GTOLBR	—	—	General PWM timer output level buffer register
GTICCR	—	—	General PWM timer inter channel cooperation input capture control register
GTSYNCFCR	—	—	General PWM timer-linked synchronization control register
GTSYNCSCR	—	—	General PWM timer-linked synchronization signal output control register

Register	Bit	RX72M (GPTW)/ RX72N (GPTW)	RX74M (GPTW)/ RX74N (GPTW)
OPSCR	—	—	Output phase switching control register
GTCLKCR	—	—	General PWM timer clock control register

Table 2.54 Comparison of Settings of GTIOA/B Bits (in Complementary PWM Mode)

Bit	RX72M (GPTW)/RX72N (GPTW) GTIOA/B[4:0] Bits	RX74M (GPTW)/RX74N (GPTW) GTIOA/B[4:0] Bits
b4	—	0: Initial output is Low. Active level is High. 1: Initial output is High. Active level is Low.
b3, b2	—	0 1: Low output 1 0: High output
b1, b0	—	0 1: Low output 1 0: High output

2.22 GPTW Port Output Enable

Table 2.55 is Comparative Overview of GPTW Port Output Enable, and Table 2.56 is Comparison of GPTW Port Output Enable Registers.

Table 2.55 Comparative Overview of GPTW Port Output Enable

Item	RX72M (POEG)/RX72N (POEG)	RX74M (POEGd)/RX74N (POEGd)
Request of output stopping in response to input level detection (RX72M/RX72N) Output disabling request by input level detection on the GTETRGx pin (RX74M/RX74N)	• The request to stop output is issued to the GPTW when a POEGGn.PIDF flag is set in response to the detection of input of the selected level on the corresponding GTETRGn pin (n = A to D).	• The output disabling request is issued to the GPTW when a POEGGx.PIDF flag is set to 1 by the detection of input of the selected level on the GTETRGx pin.
Output disabling request by detection of input level or edge on the POEGx pin	—	• The output disabling request is issued to the GPTW when an OEGPICRx.PIDF flag is set to 1 by the detection of either input of the selected level or the selected edge on the POEGx pin.
Requests to stop output in the form of an output stopping signal from the GPTW	• The request to stop output is issued to the GPTW when the GPTW detects the active level (high or low) on the GTIOCA and GTIOCB pins at the same time while the corresponding POEGGn.IOCF flag is set. • The request to stop output is issued to the GPTW when the GPTW detects a deadtime error while the corresponding POEGGn.IOCF flag is set.	• The output disabling request is issued to the GPTW when the GPTW detects a simultaneous active level (high or low) on the GTIOCA and GTIOCB pins and the POEGGx.IOCF flag is set to 1. • The output disabling request is issued to the GPTW when the GPTW detects a deadtime error and the POEGGx.IOCF flag is set to 1.
Output disabling request in response to detecting the overcurrent of DSMIF	—	• The output disabling request is issued to the GPTW when the POEGGx.DERRmST flag is set to 1 by notifications from the DSMIFm overcurrent detection window (m = 0, 1).
Requests to stop output in response to detecting the stopping of oscillation	• A request to stop output is issued to the GPTW when the oscillation stop detection circuit for the main clock detects the stopping of oscillation while the corresponding POEGGn.OSTPF flag is set.	• The output disabling request is issued to the GPTW when the oscillation stop detection circuit for the main clock detects the oscillation stop and the POEGGx.OSTPF flag is set to 1.
Requests by software to stop output	• The request to stop output is issued to the GPTW when the software sets the POEGGn.SSF flag.	• The output disabling request is issued to the GPTW when the software sets the POEGGx.SSF bit to 1.

Item	RX72M (POEG)/RX72N (POEG)	RX74M (POEGd)/RX74N (POEGd)
Interrupt	• An interrupt is generated in response to the request to stop output in the form of the POEGGn.PIDF flag. • An interrupt is generated in response to the request to stop output in the form of the POEGGn.IOCF flag.	• An interrupt is generated by an output disabling request via the POEGGx.PIDF flag. • An interrupt is generated by an output disabling request via the POEGGx.IOCF flag. • An interrupt is generated by an output disabling request via the POEGGx.DERRmST flag. • An interrupt is generated by an output disabling request via the POEGPICRx.PIDF flag.
External trigger output to the GPTW	• The GTETRGn pin is used for output as external triggers.	• The input signal from the GTETRGx pin is output to the GPTW as an external trigger.
Noise removal	• Each GTETRGn pin has a digital noise filter. — Four types of sampling clock are selectable for the filter.	• Each GTETRGx pin has a digital noise filter. — Four types of sampling clock are selectable for the filter. • Each POEGx pin has a digital noise filter. — Six types of sampling clock are selectable for the filter. — Match detection conditions can be selected from two to 64 consecutive samples with the same level.
Protect Zone filter	—	• Security attribution can be set for each group of the POEG.

Table 2.56 Comparison of GPTW Port Output Enable Registers

Register	Bit	RX72M (POEG)/RX72N (POEG)	RX74M (POEGd)/RX74N (POEGd)
POEGGn (n = A to D)	DERR0ST	—	DSMIF0 error detection flag
	DERR1ST	—	DSMIF1 error detection flag
	DERR0E	—	DSMIF0 notification signal enable bit
	DERR1E	—	DSMIF1 notification signal enable bit
	NFCS[1:0]	Noise filter clock select bits b31 b30 0 0: Samples the input level of GTETRGn pin three times per PCLKB/1 clock 0 1: Samples the input level of GTETRGn pin three times per PCLKB/8 clock 1 0: Samples the input level of GTETRGn pin three times per PCLKB/32 clock 1 1: Samples the input level of GTETRGn pin three times per PCLKB/128 clock	Noise filter clock select bits b31 b30 0 0: The input signal from the GTETRGx pin is sampled every PCLKA/1 clock 0 1: The input signal from the GTETRGx pin is sampled every PCLKA/8 clock 1 0: The input signal from the GTETRGx pin is sampled every PCLKA/32 clock 1 1: The input signal from the GTETRGx pin is sampled every PCLKA/128 clock
POEGPICRx (x = A to D)	—	—	POEGx pin input control register

2.23 8-Bit Timer

Table 2.57 is Comparative Overview of 8-Bit Timers, and Table 2.58 is Comparison of 8-Bit Timer Registers.

Table 2.57 Comparative Overview of 8-Bit Timers

Item	RX72M (TMRb)/RX72N (TMRb)	RX74M (TMRa)/RX74N (TMRa)
Count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192 • External clock: external count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192 • External clock: external count clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 2 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selected by compare match A or B, or an external counter reset signal.	Selected by compare match A or B, or an external counter reset signal.
Timer output	Output pulses with a desired duty cycle or PWM output	Output pulses with a desired duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (Output)	Compare match A, compare match B, and overflow (TMR0 to TMR3)	Compare match A, compare match B, and overflow (TMR0 to TMR3)
Event link function (Input)	One of the following three operations proceeds in response to an event reception: (1) Counting start operation (TMR0 to TMR3) (2) Event counting operation (TMR0 to TMR3) (3) Counting restart operation (TMR0 to TMR3)	One of the following three operations proceeds in response to an event reception: (1) Counting start operation (TMR0 to TMR3) (2) Event counting operation (TMR0 to TMR3) (3) Counting restart operation (TMR0 to TMR3)
DTC activation	DTC can be activated by compare match A interrupts or compare match B interrupts.	DTC can be activated by compare match A interrupts or compare match B interrupts.
Capable of generating base clock for RSCI	—	Generates base clock for RSCI.
A/D conversion start trigger of the A/D converter	Compare match A of TMR0 and TMR2	—
Capable of generating base clock for SCI	Generates base clock for SCI.	—
Low power consumption function	Each unit can be placed in a module stop state	Each unit can be placed in a module stop state
Protect Zone filter	—	Security attribute can be set for each channel.

Table 2.58 Comparison of 8-Bit Timer Registers

Register	Bit	RX72M (TMRb)/RX72N (TMRb)	RX74M (TMRa)/RX74N (TMRa)
TMR0.TCSR, TMR2.TCSR	ADTE	A/D trigger enable bit	—

2.24 Compare Match Timer

Table 2.59 is Comparative Overview of Compare Match Timers.

Table 2.59 Comparative Overview of Compare Match Timers

Item	RX72M(CMT)/RX72N(CMT)	RX74M(CMT)/RX74N(CMT)
Count clocks	• Four frequency dividing clocks One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.	• Four frequency dividing clocks One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.
Interrupt	A compare match interrupt can be requested for each channel.	A compare match interrupt can be requested for each channel.
Event link function (output)	An event signal is output upon a CMT1 compare match.	An event signal is output upon a CMT1 compare match.
Event link function (input)	• Linking to the specified module is possible. • CMT1 count start, event counter, or count restart operation is possible.	• Linking to the specified module is possible. • CMT1 count start, event counter, or count restart operation is possible.
Low power consumption function	Each unit can be placed in a module stop state.	Each unit can be placed in a module stop state.
Protect Zone filter	—	Security attributes can be set for each unit.

2.25 Compare Match Timer W

Table 2.60 is Comparative Overview of Compare Match Timers W.

Table 2.60 Comparative Overview of Compare Match Timers W

Item	RX72M (CMTW)/RX72N (CMTW)	RX74M (CMTW)/RX74N (CMTW)
Number of channels	Two channels (unit 0, unit 1)	Two channels (unit 0, unit 1)
Timer counter	• 16-bit/32-bit selectable up-counter • The counter returns to 0000 0000h after a compare match.	• 16-bit/32-bit selectable up-counter • The counter returns to 0000 0000h after a compare match.
Prescaler	Four dividing clocks are output. — Selectable from any of PCLK/8, PCLK/32, PCLK/128, and PCLK/512	Four dividing clocks are output. — Selectable from any of PCLK/8, PCLK/32, PCLK/128, and PCLK/512
Input capture	Up to two input capture input signals available.	Up to two input capture input signals available.
Output compare	Up to two output compare output signals available.	Up to two output compare output signals available.
Compare match	One compare match available (no output compare output pin used).	One compare match available (no output compare output pin used).
Interrupts	• Compare match interrupt • Input capture 0 and 1 interrupts • Output compare 0 and 1 interrupts	• Compare match interrupt • Input capture 0 and 1 interrupts • Output compare 0 and 1 interrupts
Event link function (output) (Unit 0)	Compare match	Compare match
Event link function (input) (Unit 0)	One of the following operations is enabled after an event is accepted: • Count start operation • Event count operation • Count restart operation	One of the following operations is enabled after an event is accepted: • Count start operation • Event count operation • Count restart operation
Low power consumption function	Each unit can be placed in the module stop state.	Each unit can be placed in the module stop state.
Protect Zone filter	—	Security attributes can be set for each unit.

2.26 Realtime Clock

Table 2.61 is Comparative Overview of Realtime Clocks, and Table 2.62 is Comparison of Realtime Clock Registers.

Table 2.61 Comparative Overview of Realtime Clocks

Item	RX72M (RTCd)/RX72N (RTCd)	RX74M (RTCBb)/RX74N (RTCBb)
Count mode	Calendar count mode/binary count mode	Calendar count mode/binary count mode
Count source	Sub-clock (XCIN) or main clock (EXTAL)	Sub-clock (XCIN or EXCIN) or LOCO clock
Clock and calendar functions	Calendar count mode — Year, month, date, day-of-week, hour, minute, second are counted, BCD display — 12 hours/24 hours mode switching function — 30 seconds adjustment function (a number less than 30 is rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute) — Automatic adjustment function for leap years Binary count mode — Count seconds in 32 bits, binary display Common to both modes — Start/stop function — The sub-second digit is displayed in binary units (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz). 4Hz, 8Hz, 16Hz, 32Hz, 64Hz) — Clock error correction function — Clock (1 Hz/64 Hz) output	Calendar count mode — Year, month, date, day-of-week, hour, minute, second are counted, BCD display — 12 hours/24 hours mode switching function — 30 seconds adjustment function (a number less than 30 is rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute) — Automatic adjustment function for leap years Binary count mode — Count seconds in 32 bits, binary display Common to both modes — Start/stop function — The sub-second digit is displayed in binary units (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz). 4Hz, 8Hz, 16Hz, 32Hz, 64Hz) — Clock error correction function — Clock (1 Hz/64 Hz) output

Item	RX72M (RTCd)/RX72N (RTCd)	RX74M (RTCBb)/RX74N (RTCBb)
Interrupts	Alarm interrupt (ALM) As an alarm interrupt condition, selectable which of the below is compared with: — Calendar count mode: Year, month, date, day-of-week, hour, minute, or second can be selected — Binary count mode: Each bit of the 32-bit binary counter Periodic interrupt (PRD) — 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as an interrupt period. Carry interrupt (CUP) An interrupt is generated at either of the following timings: — When a carry from the 64-Hz counter to the second counter is generated. — When the 64-Hz counter is changed and the R64CNT register is read at the same time. • Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt	Alarm interrupt (ALM) As an alarm interrupt condition, selectable which of the below is compared with: — Calendar count mode: Year, month, date, day-of-week, hour, minute, or second can be selected — Binary count mode: Each bit of the 32-bit binary counter Periodic interrupt (PRD) — 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as an interrupt period. Carry interrupt (CUP) An interrupt is generated at either of the following timings: — When a carry from the 64-Hz counter to the second counter is generated. — When the 64-Hz counter is changed and the R64CNT register is read at the same time. • Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt
Time capture function	• Times can be captured when the edge of the time capture event input pin is detected. • For every event input, month, date, hour, minute, and second are captured or 32-bit binary counter value is captured.	• Times can be captured when the edge of the time capture event input pin is detected. • For every event input, month, date, hour, minute, and second are captured or 32-bit binary counter value is captured.
Event link function	Periodic event output	Periodic event output
Protect Zone filter	—	Security attribute can be set.

Table 2.62 Comparison of Realtime Clock Registers

Register	Bit	RX72M (RTCd)/RX72N (RTCd)	RX74M (RTCBb)/RX74N (RTCBb)
RCR3	—	RTC control register 3	—
RCR4	RCKSEL	Count source select bit 0: Sub-clock oscillator is selected. 1: Main clock oscillator is selected.	Clock source select bit 0: Sub-clock is selected. 1: LOCO clock is selected.
RFRH	RFC	Frequency divide ratio setting bit Set the divide ratio of the main clock to generate the reference clock of 128 Hz. If the setting value in the RFC[16:0] bits is n, the prescaler divides the main clock by n + 1.	Frequency divide ratio setting bit Set the divide ratio of the LOCO clock to generate the reference clock of 128 Hz. If the setting value in the RFC[16:0] bits is n, the prescaler divides the LOCO clock by n + 1.

Register	Bit	RX72M (RTCd)/RX72N (RTCd)	RX74M (RTCBb)/RX74N (RTCBb)
RFRL	RFC[15:0]	Frequency divide ratio setting bits Set the divide ratio of the main clock to generate the reference clock of 128 Hz. If the setting value in the RFC[16:0] bits is n, the prescaler divides the main clock by n + 1.	Frequency divide ratio setting bits Set the divide ratio of the LOCO clock to generate the reference clock of 128 Hz. If the setting value in the RFC[16:0] bits is n, the prescaler divides the LOCO clock by n + 1.

2.27 Watchdog Timer

Table 2.63 is Comparative Overview of Watchdog Timers, and Table 2.64 is Comparison of Watchdog Timer Registers.

Table 2.63 Comparative Overview of Watchdog Timers

Item	RX72M (WDTA)/RX72N (WDTA)	RX74M (WDTA)/RX74N (WDTA)
Count source	Peripheral module clock (PCLK)	Peripheral module clock (PCLKB)
Clock division ratio	Divide by 4, 64, 128, 512, 2048, or 8192	Divide by 4, 64, 128, 512, 2048, or 8192
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit counter
Conditions for starting the counter	Auto-start mode: Counting automatically starts after a reset is released Register start mode: Counting is started by refresh operation (writing 00h and then FFh to the WDTRR register)	Auto-start mode: Counting automatically starts after a reset is released Register start mode: Counting is started by refresh operation (writing 00h and then FFh to the WDTRR register)
Conditions for stopping the counter	• Reset • In low power consumption states • A counter underflows or a refresh error occurs (only in register start mode)	• Reset • In low power consumption modes (depends on the register setting) • A counter underflows or a refresh error occurs (only in register start mode)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Watchdog timer reset sources (RX72M/RX72N) Reset output sources (RX74M/RX74N)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/interrupt sources (RX72M/RX72N) Non-maskable interrupt/ maskable interrupt sources (RX74M/RX74N)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by the WDTSR register.	The counter value can be read by the WDTSR register.
Event link function (output)	—	• Counter underflow event output • Refresh error event output
Protect Zone filter	—	Security attribute can be set.

Table 2.64 Comparison of Watchdog Timer Registers

Register	Bit	RX72M (WDTA)/RX72N (WDTA)	RX74M (WDTA)/RX74N (WDTA)
WDTCSTPR	—	—	WDT count stop control register

2.28 Independent Watchdog Timer

Table 2.65 is Comparative Overview of Independent Watchdog Timers, and Table 2.66 is Comparison of Independent Watchdog Timer Registers.

Table 2.65 Comparative Overview of Independent Watchdog Timers

Item	RX72M (IWDTa)/RX72N (IWDTa)	RX74M (IWDTa)/RX74N (IWDTa)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT clock (IWDTCLK)
Clock divide ratio	Divide by 1, 16, 32, 64, 128, or 256	Divide by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit counter
Conditions for starting the counter	Auto-start mode: Counting automatically starts after a reset is released Register start mode: Counting is started by refresh operation (writing 00h and then FFh to the IWDTRR register).	Auto-start mode: Counting automatically starts after a reset is released Register start mode: Counting is started by refresh operation (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Reset • In low power consumption states (depends on the register setting) • A counter underflows or a refresh error occurs (only in register start mode)	• Reset • In low power consumption states (depends on the register setting) • A counter underflows or a refresh error occurs (only in register start mode)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/interrupt sources (RX72M/RX72N) Non-maskable interrupt/ maskable interrupt sources (RX74M/RX74N)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by the IWDTSR register.	The counter value can be read by the IWDTSR register.
Event link function (output)	• Down-counter underflow event output • Refresh error event output	• Counter underflow event output • Refresh error event output
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep mode count stop control output	—

Item	RX72M (IWDTa)/RX72N (IWDTa)	RX74M (IWDTa)/RX74N (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock frequency divide ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)	• Selecting the clock frequency divide ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the counter operation/stop in low power consumption mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency divide ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)	• Selecting the clock frequency divide ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bits) • Selecting the counter operation/stop in low power consumption mode (IWDTCSTPR.SLCSTP bit)
Protect Zone filter	—	Security attribute can be set.

Table 2.66 Comparison of Independent Watchdog Timer Registers

Register	Bit	RX72M (IWDTa)/RX72N (IWDTa)	RX74M (IWDTa)/RX74N (IWDTa)
IWDTCR	TOPS[1:0]	Timeout period select bits b1 b0 0 0: 1024 cycles (03FFh) 0 1: 4096 cycles (0FFFh) 1 0: 8192 cycles (1FFFh) 1 1: 16384 cycles (3FFFh)	Timeout period select bits b1 b0 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1024 cycles (03FFh) 1 1: 2048 cycles (07FFh)
IWDTCSTPR	SLCSTP	Sleep mode count stop control bit 0: Count stop is disabled. 1: Count is stopped at a transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode.	Sleep mode count stop control bit 0: Counter continues counting in low power consumption mode 1: Counter stops in low power consumption mode

2.29 EtherCAT Slave Controller

Table 2.67 is Comparative Overview of EtherCAT Slave Controllers, and Table 2.68 is Comparison of EtherCAT Slave Controller Registers.

Table 2.67 Comparative Overview of EtherCAT Slave Controllers

Item		RX72M (ESC)	RX74M (ESC)
Number of ports		2	2
Fieldbus memory management unit (FMMU) entities		8	8
SyncManager entities		8	8
Process data RAM		8 Kbytes	8 Kbytes
Distributed clocks		Yes (64 bits)	Yes (64 bits)
EBus		No	No
Process data interfaces (PDI)	Digital I/O	No	No
	SPI slave	No	No
	Host MPU interface	On-chip bus	On-chip bus
Data alignment		Little endian	Little endian
Protect Zone filter		—	Security attribute can be set.

Table 2.68 Comparison of EtherCAT Slave Controller Registers

Register	Bit	RX72M (ESC)	RX74M (ESC)
ESCICR	LAT0S	—	LATCH0 signal input select bit
	LAT1S	—	LATCH1 signal input select bit

2.30 USB 2.0 Full-Speed Host/Function Module

Table 2.69 is Comparative Overview of USB 2.0 Full-Speed Host/Function Modules, and Table 2.70 is Comparison of USB 2.0 Full-Speed Host/Function Module Registers.

Table 2.69 Comparative Overview of USB 2.0 Full-Speed Host/Function Modules

Item	RX72M/RX72N (USBb)	RX74M/RX74N (USBf)
Features	• USB Device Controller (UDC) and transceiver for USB 2.0 are incorporated. — Host controller, function controller, and On-The-Go (OTG) are supported (one channel) • The host controller and the function controller can be switched by software. • Self-power mode or bus power mode can be selected.	• USB Device Controller (UDC) and transceiver for USB 2.0 are incorporated. — Host controller, function controller, and On-The-Go (OTG) are supported (one channel) • The host controller and the function controller can be switched by software. • Self-power mode or bus power mode can be selected.
	When the host controller is selected: • Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) are supported • Automatic scheduling for SOF and packet transmissions • Programmable intervals for isochronous and interrupt transfers • Multiple peripheral devices can be connected for communication via a one-stage hub.	When the host controller is selected: • Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) are supported • Automatic scheduling for SOF and packet transmissions • Programmable intervals for isochronous and interrupt transfers • Multiple peripheral devices can be connected for communication via a one-stage hub.
	When the function controller is selected: • Full-speed transfer (12 Mbps) is supported • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS request • SOF interpolation function	When the function controller is selected: • Full-speed transfer (12 Mbps) is supported • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS request • SOF interpolation function
Communication data transfer type	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer
Pipe configuration	• Buffer memory for USB communication is provided. • Up to 10 pipes can be selected (including the default control pipe). • Pipes 1 to 9 can be assigned any endpoint number.	• Buffer memory for USB communication is provided. • Up to 10 pipes can be selected (including the default control pipe). • Pipes 1 to 9 can be assigned any endpoint number.
	Transfer conditions that can be set for each pipe: • Pipe 0: Control transfer, 64-byte single buffer • Pipes 1 and 2: 64-byte double buffer can be specified for bulk transfer and 256-byte double buffer for isochronous transfer • Pipes 3 to 5: Bulk transfer, 64-byte double buffer • Pipes 6 to 9: Interrupt transfer, 64-byte single buffer	Transfer conditions that can be set for each pipe: • Pipe 0: Control transfer, 64-byte single buffer • Pipes 1 and 2: 64-byte double buffer can be specified for bulk transfer and 256-byte double buffer for isochronous transfer • Pipes 3 to 5: Bulk transfer, 64-byte double buffer • Pipes 6 to 9: Interrupt transfer, 64-byte single buffer

Item	RX72M/RX72N (USBb)	RX74M/RX74N (USBf)
Others	• Reception ending function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0, 1) port has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK) • On-chip pull-up and pull-down resistors of D+/D–	• Reception ending function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0, 1) port has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK) • On-chip pull-up and pull-down resistors of D+/D–
Low power consumption function	Module-stop state can be set.	Module-stop state can be set.
Protect Zone filter	—	Security attribute can be set.

Table 2.70 Comparison of USB 2.0 Full-Speed Host/Function Module Registers

Register	Bit	RX72M (USBb)/RX72N (USBb)	RX74M (USBf)/RX74N (USBf)
PHYSLEW	—	PHY cross point adjustment register	—
DPUSR0R	FIXPHY0	USB0 transceiver output fix bit 0: The outputs are fixed in normal mode and on return from deep software standby mode. 1: The outputs are fixed on transitions to deep software standby mode.	USB0 transceiver output fix bit 0: The outputs are fixed in normal mode and on return from deep software standby mode 1. 1: The outputs are fixed on transitions to deep software standby mode 1.
DPUSR1R	DPINTE0	USB0 D+ interrupt enable/clear bit 0: Recovery from deep software standby mode is disabled. 1: Recovery from deep software standby mode is enabled.	USB0 D+ interrupt enable/clear bit 0: Recovery from deep software standby mode 1 is disabled. 1: Recovery from deep software standby mode 1 is enabled.
	DMINTE0	USB0 D– interrupt enable/clear bit 0: Recovery from deep software standby mode is disabled. 1: Recovery from deep software standby mode is enabled.	USB0 D– interrupt enable/clear bit 0: Recovery from deep software standby mode 1 is disabled. 1: Recovery from deep software standby mode 1 is enabled.
	DOVRCRAE0	USB0 OVRCURA interrupt enable/clear bit 0: Recovery from deep software standby mode is disabled. 1: Recovery from deep software standby mode is enabled.	USB0 OVRCURA interrupt enable/clear bit 0: Recovery from deep software standby mode 1 is disabled. 1: Recovery from deep software standby mode 1 is enabled.
	DOVRCRBE0	USB0 OVRCURB interrupt enable/clear bit 0: Recovery from deep software standby mode is disabled. 1: Recovery from deep software standby mode is enabled.	USB0 OVRCURB interrupt enable/clear bit 0: Recovery from deep software standby mode 1 is disabled. 1: Recovery from deep software standby mode 1 is enabled.
	DVBSE0	USB0 VBUS interrupt enable/clear bit 0: Recovery from deep software standby mode is disabled. 1: Recovery from deep software standby mode is enabled.	USB0 VBUS interrupt enable/clear bit 0: Recovery from deep software standby mode 1 is disabled. 1: Recovery from deep software standby mode 1 is enabled.
	DPINT0	USB0 D+ interrupt source recovery flag 0: The system has not returned from deep software standby mode. 1: The system has returned from deep software standby mode.	USB0 D+ interrupt source recovery flag 0: The system has not returned from deep software standby mode 1. 1: The system has returned from deep software standby mode 1.

Register	Bit	RX72M (USBb)/RX72N (USBb)	RX74M (USBf)/RX74N (USBf)
DPUSR1R	DMINT0	USB0 D– interrupt source recovery flag 0: The system has not returned from deep software standby mode. 1: The system has returned from deep software standby mode.	USB0 D– interrupt source recovery flag 0: The system has not returned from deep software standby mode 1. 1: The system has returned from deep software standby mode 1.
	DOVRCRA0	USB0 OVRCURA interrupt source recovery flag 0: The system has not returned from deep software standby mode. 1: The system has returned from deep software standby mode.	USB0 OVRCURA interrupt source recovery flag 0: The system has not returned from deep software standby mode 1. 1: The system has returned from deep software standby mode 1.
	DOVRCRB0	USB0 OVRCURB interrupt source recovery flag 0: The system has not returned from deep software standby mode. 1: The system has returned from deep software standby mode.	USB0 OVRCURB interrupt source recovery flag 0: The system has not returned from deep software standby mode 1. 1: The system has returned from deep software standby mode 1.
	DVBINT0	USB0 VBUS interrupt source recovery flag 0: The system has not returned from deep software standby mode. 1: The system has returned from deep software standby mode.	USB0 VBUS interrupt source recovery flag 0: The system has not returned from deep software standby mode 1. 1: The system has returned from deep software standby mode 1.

2.31 Serial Communications Interface

Table 2.71 is Comparative Overview of Serial Communications Interfaces, Table 2.72 is Comparison of Serial Communications Interface Channels, and Table 2.73 is Comparison of Serial Communications Interface Registers.

Table 2.71 Comparative Overview of Serial Communications Interfaces

Item	RX72M (SCIj, SCIi, SCIh)/ RX72N (SCIj, SCIi, SCIh)	RX74M (RSCI)/RX74N (RSCI)
Number of channels	• SCIj: 7 channels • SCIi: 5 channels • SCIh: 1 channel	• RSCI: 13 channels
Serial communication modes	• Asynchronous • Clock synchronous • Smart card interface • Simple I^2C bus • Simple SPI bus • Extended serial	• Asynchronous • Manchester • Clock synchronous • Smart card interface • Simple I^2C • Simple SPI (4-wire serial bus) • Extended serial
Operating clock	• SCI0 to SCI6, SCI12: PCLKB • SCI7 to SCI11: PCLKA	• Selectable from peripheral module clock (PCLKA) or SCI clock (SCICLK)
Transfer speed	Bit rate specifiable with the on-chip baud rate generator.	Bit rate specifiable with the on-chip baud rate generator.
Full-duplex communications	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Half-duplex communications	Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin	Half-duplex communication is possible by using only TXDn pins
Data transfer	Selectable as LSB first or MSB first transfer*1	Selectable as LSB first or MSB first transfer*1
I/O signal level inverting function	—	Input signal and output signal can be inverted independently.
RXD input path selection	—	Encoded serial data can be input to RXD2 and RXD3 after having been decoded through GPTW10 and GPTW12, respectively.
TXD output path selection	—	Serial data output from TXD2 and TXD3 can be encoded through GPTW11 and GPTW13, respectively.

Item		RX72M (SCIj, SCIi, SCIh)/ RX72N (SCIj, SCIi, SCIh)	RX74M (RSCI)/RX74N (RSCI)
Interrupt sources		• Transmit end, transmit data empty, receive data full, receive error, receive data ready (SCI7 to 11), and data match (SCI7 to 11) • Completion of generation of a start condition, restart condition, or stop condition (for simple I^2C mode)	• Transmit end, transmit data empty, receive data full, receive error, receive data ready, and receive data match • Break Field detection/transmission, Bus collision detection, Active edge detection • Completion of generation of a start condition, restart condition, or stop condition
RS-485 driver control function		—	Output DE signal to enable external transceiver transmit mode
Loopback function		—	Self-diagnosis of communication function is possible by connecting TXD and RXD inside the RSCI
Synchronizer bypass function		—	Synchronizer is bypassed when the peripheral module clock (PCLKA) is selected for the operating clock (TCLK).
Low power consumption function		Module stop state can be set for each channel.	Module stop state can be set for each channel.
Protect Zone filter		—	Security attribute can be set for each channel.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bit	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Transmit/receive FIFO	16-stage FIFOs for transmit and receive buffers (SCI7 to 11)	Selectable either 1 stage register or 16-stage FIFO
	Data match detection	Compares receive data and comparison data, and generates interrupt when they are matched (SCI0 to 11)	The interrupt request can issue by detecting the match between receive data and comparison data.
	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.
	Receive data sampling timing adjustment	—	Sampling point of receive data can be changed to front or rear of center of bit.
	Transmit signal transition timing adjustment	—	Falling or rising edge of the transmit data can be delayed.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or reading the SPTR.RXDMON flag (SCI0 to SCI11).	When a framing error occurs, a break can be detected by reading the SSR register.

Item		RX72M (SCIj, SCIi, SCIh)/ RX72N (SCIj, SCIi, SCIh)	RX74M (RSCI)/RX74N (RSCI)
Asynchronous mode	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used. (SCI5, SCI6, SCI12)	• An internal, external, or TMR clock can be selected.
	Double-speed mode	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
	HBS support mode	—	Transmission/reception using inverted RZI (Return to Zero, Inverted) code is possible.
Manchester mode	Data length	—	7, 8, or 9 bits
	Transmission stop bit	—	1 or 2 bits
	Receive error detection	—	Parity, overrun, framing, Manchester code errors, preface, start bit, and receive Sync
	Hardware flow control	—	CTSn# and RTSn# pins can be used in controlling transmission.
	Clock source	—	Only internal clock can be used. (The setting of external clock is prohibited because it is not the object of operation guarantee.)
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	—	Serial communication among multiple processors
	Noise cancellation	—	The signal paths from input on the RXDn pins incorporate digital noise filters.
	Manchester encoding/ decoding function	—	Function to perform Manchester encoding/decoding of transmission/reception data and communicate using Manchester code
	Preface setting/detection function	—	Function to detect the beginning of a frame from the preface pattern. Preface pattern can be selected from 4 types. The length can also be changed from 0 to 15 bits.
	Start Bit setting/detection function	—	The Start Bit length can be set to 1 bit or 3 bits. In the case of 3-bit length, it is possible to judge the type of subsequent data with two types of patterns.
	Reception retiming function	—	Function to perform timing correction for each bit center edge by using Manchester code having edge at bit center

Item		RX72M (SCIj, SCIi, SCIh)/ RX72N (SCIj, SCIi, SCIh)	RX74M (RSCI)/RX74N (RSCI)
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Clock source	—	An internal clock (master mode) or external clock (slave mode) can be selected.
	Double-speed mode	—	Baud rate generator double-speed mode is selectable
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Transmit/receive FIFO	16-stage FIFOs for transmit and receive buffers (SCI7 to 11)	Selectable either 1 stage register or 16-stage FIFO
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Transfer format	I^2C-bus format	I^2C-bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Fast mode is supported (refer to the bit rate register (BRR) to set the transfer rate).	Fast mode is supported (refer to control register 2 (SCR2) to set the transfer rate).
	Noise cancellation	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.	• The signal paths from input on the SCL and SDA pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.
Simple SPI bus	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	Clock source	—	An internal clock (master mode) or external clock (slave mode) can be selected.
	Double-speed mode	—	Baud rate generator double-speed mode is selectable
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	When the SSn# pin is high level, the output pin can be set to high impedance.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
	Transmission/Reception	—	Selectable either 1 stage register or 16-stage FIFO

Item		RX72M (SCIj, SCIi, SCIh)/ RX72N (SCIj, SCIi, SCIh)	RX74M (RSCI)/RX74N (RSCI)
Event linking (RX72M/RX72N: SCI5) (RX74M/RX74N: All channels)		• Error (receive error, error signal detected) event output • Receive data full event output • Transmit data empty event output • Transmit end event output	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output • Receive data match event output • Receive data unmatch event output • Active edge detection event output
Extended serial mode (only supported by SCI12)	Start Frame transmission	• Output of a low level as the Break Field over a specified width and generation of interrupts on completion • Detection of bus collisions and the generation of interrupts on detection	• Break Field transmission possible, Break Field transmission complete interrupt output possible • Bus collision detection possible, bus collision detection interrupt output possible
	Start Frame reception	• Detection of the Break Field low width and generation of an interrupt on detection • Comparison of Control Fields 0 and 1 and generation of an interrupt when the two match • Two kinds of data for comparison (primary and secondary) can be set in Control Field 1. • A priority interrupt bit can be set in Control Field 1. • Function for measuring bit rates • Handling of Start Frames that do not include a Break Field • Handling of Start Frames that do not include a Control Field 0	• Break Field detectable, Break Field detected interrupt output possible • Control Field 0/1 data comparison function • Control Field 1 can set two types of comparison data of primary and secondary • Priority interrupt bit can be set in Control Field 1 • Bit rate measurement function
	I/O control function	• Selectable polarity for TXDX12 and RXDX12 signals • Selection of a digital filter for the RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDX12	—
	Timer function	Usable as a reload timer	—
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.

Note: 1. On the RX72M/RX72N Group, data can be transferred with MSB first only in simple I^2C mode.
On the RX74M/RX74N Group, data can be transferred with MSB first only in simple I^2C mode and with LSB first only in extended serial mode.

Table 2.72 Comparison of Serial Communications Interface Channels

Item	RX72M (SCIj, SCIi, SCIh)/ RX72N (SCIj, SCIi, SCIh)	RX74M (RSCI)/RX74N (RSCI)
Asynchronous mode	SCI0 to SCI12	SCI0 to SCI12
Clock synchronous mode	SCI0 to SCI12	SCI0 to SCI12
Smart card interface mode	SCI0 to SCI12	SCI0 to SCI12
Simple I^2C mode	SCI0 to SCI12	SCI0 to SCI12
Simple SPI mode	SCI0 to SCI12	SCI0 to SCI12
FIFO mode	SCI7 to SCI11	SCI7 to SCI11
Data match detection	SCI0 to SCI11	SCI0 to SCI11
Extended serial mode	SCI12	SCI0 to SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI0 to SCI12
Event link function	SCI5	SCI0 to SCI12

Table 2.73 Comparison of Serial Communications Interface Registers

Register	Bit	RX72M (SCIj, SCIi, SCIh)/ RX72N (SCIj, SCIi, SCIh)	RX74M (RSCI)/RX74N (RSCI)
RDR	—	Receive data register RDR is an 8-bit register.	Receive data register RDR is a 32-bit register.
	RDAT[8:0]	—	Receive data bits
	MPB	—	Multi-processor bit monitor flag
	DR	—	Receive data ready flag
	PER	—	Parity error flag
	FER	—	Framing error flag
	ORER	—	Overrun error flag
	APER	—	Aggregate parity error flag
	AFER	—	Aggregate framing error flag
RDRH	—	Receive data register H	—
RDRL	—	Receive data register L	—
RDRHL	—	Receive data register HL	—
FRDR	—	Receive FIFO data register	—
TDR	—	Transmit data register TDR is an 8-bit register.	Transmit data register TDR is a 32-bit register.
	TDAT[8:0]	—	Transmit data bits
	MPBT	—	Transmit multi-processor bit
	SYNC	—	Sync pulse select bit
TDRH	—	Transmit data register H	—
TDRL	—	Transmit data register L	—
TDRHL	—	Transmit data register HL	—
FTDR	—	Transmit FIFO data register	—
FCR	—	FIFO control register FCR is a 16-bit register.	FIFO control register FCR is a 32-bit register.
	FM	FIFO mode select bit	—

Register	Bit	RX72M (SCIj, SCIi, SCIh)/ RX72N (SCIj, SCIi, SCIh)	RX74M (RSCI)/RX74N (RSCI)
FCR	RFRST	Receive FIFO reset bit (b1)*1 Writing 1 clears the number of data stored in the receive FIFO to 0	Receive FIFO reset bit (b23) This bit enables only when SCR3.FM bit is 1.) 0: It is invalid. It does not affect the operation. 1: The number of data stored in receive FIFO (RDR register) are made 0 The read value is always 0.
	TFRST	Transmit FIFO reset bit (b2)*1 Writing 1 clears the number of data stored in the transmit FIFO to 0	Transmit FIFO reset bit (b15) (This bit enables only when SCR3.FM bit is 1.) 0: It is invalid. It does not affect the operation. 1: The number of data stored in transmit FIFO (TDR register) are made 0 The read value is always 0.
	DRES	Receive data ready interrupt select bit (b3)	Receive data ready interrupt select bit (b0)
	TTRG[3:0] (RX72M/RX72N) TTRG[4:0] (RX74M/RX74N)	Transmit FIFO threshold setting bits (b7 to b4) Specifies the threshold value for the SSRFIFO.TDFE flag to become 1 b7 b4 0 0 0 0: Transmit FIFO threshold value is 0 0 0 0 1: Transmit FIFO threshold value is 1 : 1 1 1 1: Transmit FIFO threshold value is 15	Transmit FIFO threshold setting bits (b12 to b8) (Valid in asynchronous mode (including multi-processor mode), clock synchronous mode, simple SPI mode) b12 b8 0 0 0 0 0: Trigger number 0 : : : : 0 1 1 1 1: Trigger number 15 Settings other than above are prohibited.

Register	Bit	RX72M (SCIj, SCIi, SCIh)/ RX72N (SCIj, SCIi, SCIh)	RX74M (RSCI)/RX74N (RSCI)
FCR	RTRG[3:0] (RX72M/RX72N) RTRG[4:0] (RX74M/RX72N)	Receive FIFO threshold setting bits Specifies the threshold value for the SSRFIFO.RDF flag to become 1 b11 b8 0 0 0 0: Setting prohibited 0 0 0 1: Receive FIFO threshold value is 1 : 1 1 1 1: Receive FIFO threshold value is 15	Receive FIFO threshold setting bits (Valid in asynchronous mode (including multi-processor mode), clock synchronous mode, simple SPI mode) b20 b16 0 0 0 0 0: Trigger number 0 : : : : : : 0 1 1 1 1: Trigger number 15 Settings other than above are prohibited.
	RSTRG[3:0] (RX72M/RX72N) RSTRG[4:0] (RX74M/RX74N)	RTS# output threshold setting bits*2 Specifies the threshold value for the RTSn# pin to be driven high b15 b12 0 0 0 0: Setting prohibited 0 0 0 1: Receive FIFO threshold value is 1 : 1 1 1 1: Receive FIFO threshold value is 15	RTS# output threshold setting bits (Valid in asynchronous mode (including multi-processor mode), clock synchronous mode) This bit enables only when SCR3.FM bit = 1, SCR1.CTSE bit = 0, and SCR0.SSE bit = 0. b28 b24 0 0 0 0 0: Trigger number 0 : : : : : : 0 1 1 1 1: Trigger number 15 Settings other than above are prohibited.
SSR	—	Serial status register (non-FIFO mode) SSR is an 8-bit register.	Status register (non-FIFO mode) SSR is a 32-bit register.
	MPBT	Multi-processor bit transfer bit	—
	MPB	Multi-processor bit	—
	TEND	Transmit end flag (b2) 0: A character is being transmitted. 1: Character transfer has been completed.	Transmit end flag (b30) 0: A character is being transmitted or standing by for transmission. 1: Character transfer has been completed, or sending Break Field.
	PER	Parity error flag	—
	FER	Framing error flag	—
	ORER	Overrun error flag (b5)	Overrun error flag (b24)
	RDRF	Receive data full flag (b6)	Receive data full flag (b31)
	TDRE	Transmit data empty flag (b7)	Transmit data empty flag (b29)
	RXDMON	—	RXD line monitoring flag
	DCMF	—	Data match flag
	DPER	—	Matched data parity error flag

Register	Bit	RX72M (SCIj, SCIi, SCIh)/ RX72N (SCIj, SCIi, SCIh)	RX74M (RSCI)/RX74N (RSCI)
SSR	DFER	—	Matched data framing error flag
	MFF	—	Mode fault flag
	APER	—	Aggregate parity error flag
	AFER	—	Aggregate framing error flag
SSRFIFO (RX72M/RX72N) SSR (RX74M/RX74N)	—	Serial status register (FIFO mode) SSR is an 8-bit register.	Status register (FIFO mode) SSR is a 32-bit register.
	DR	Receive data ready flag	—
	TEND	Transmit end flag (b2) 0: A character is being transmitted 1: Character transfer has been completed	Transmit end flag (b30) 0: A character is being transmitted or standing by for transmission. 1: Character transfer has been completed, or sending Break Field.
	PER	Parity error flag	—
	FER	Framing error flag	—
	ORER	Overrun error flag (b5)	Overrun error flag (b24)
	RDF	Receive FIFO full flag	—
	TDFE	Transmit FIFO empty flag	—
	ERS	—	Error signal status flag
	RXDMON	—	RXD line monitoring flag
	DCMF	—	Data match flag
	DPER	—	Matched data parity error flag
	DFER	—	Matched data framing error flag
	MFF	—	Mode fault flag
	APER	—	Aggregate parity error flag
	AFER	—	Aggregate framing error flag
	TDRE	—	Transmit data empty flag
	RDRF	—	Receive data full flag
SISR	—	I^2C status register SISR is an 8-bit register.	I^2C status register SISR is a 32-bit register.
	IICSTIF	—	Condition Generation completed flag
SCR0	—	—	Control register 0
SCR1	—	—	Control register 1
SCR2	—	—	Control register 2
SCR3	—	—	Control register 3
SCR4	—	—	Control register 4
SIMR	—	—	I^2C mode register
MMCR	—	—	Manchester mode control register
DECR	—	—	DE signal control register
XCR0	—	—	Extended serial mode control register 0
XCR1	—	—	Extended serial mode control register 1
XCR2	—	—	Extended serial mode control register 2
RFSR	—	—	Receive FIFO status register
TFSR	—	—	Transmit FIFO status register
MMSR	—	—	Manchester mode status register

Register	Bit	RX72M (SCIj, SCIi, SCIh)/ RX72N (SCIj, SCIi, SCIh)	RX74M (RSCI)/RX74N (RSCI)
XSR0	—	—	Extended serial mode status register 0
XSR1	—	—	Extended serial mode status register 1
SSCR	—	—	Status clear register
SISCR	—	—	I^2C status clear register
RFSCR	—	—	Receive FIFO status clear register
MMSCR	—	—	Manchester mode status clear register
XSCR	—	—	Extended serial mode status clear register
SISSR	—	—	Internal signal status register
HBSCR	—	—	HBS support mode control register
RXDSEL	—	—	RXD Input path select register
GTIOCSEL	—	—	GTIOC input path select register
SMR	—	Serial mode register	—
SCR	—	Serial control register	—
SCMR	—	Smart card mode register	—
BRR	—	Bit rate register	—
MDDR	—	Modulation duty register	—
SEMR	—	Serial extended mode register	—
SNFR	—	Noise filter setting register	—
SIMR1	—	I^2C mode register 1	—
SIMR2	—	I^2C mode register 2	—
SIMR3	—	I^2C mode register 3	—
SPMR	—	SPI mode register	—
FDR	—	FIFO data count register	—
LSR	—	Line status register	—
CDR	—	Comparison data register	—
DCCR	—	Data comparison control register	—
SPTR	—	Serial port register	—
ESMER	—	Extended serial module enable register	—
CR0	—	Control register 0	—
CR1	—	Control register 1	—
CR2	—	Control register 2	—
CR3	—	Control register 3	—
PCR	—	Port control register	—
ICR	—	Interrupt control register	—
STR	—	Status register	—
STCR	—	Status clear register	—
CF0DR	—	Control field 0 data register	—
CF0CR	—	Control field 0 compare enable register	—
CF0RR	—	Control field 0 receive data register	—
PCF1DR	—	Primary control field 1 data register	—
SCF1DR	—	Secondary control field 1 data register	—

Register	Bit	RX72M (SCIj, SCIi, SCIh)/ RX72N (SCIj, SCIi, SCIh)	RX74M (RSCI)/RX74N (RSCI)
CF1CR	—	Control field 1 compare enable register	—
CF1RR	—	Control field 1 receive data register	—
TCR	—	Timer control register	—
TMR	—	Timer mode register	—
TPRE	—	Timer prescaler register	—
TCNT	—	Timer count register	—

Notes: 1. These bits are only valid when the FM bit is 1.
2. These bits are valid when the FM bit is 1 and the SPMR.CTSE and SPMR.SSE bits are both 0 (RTS# output is enabled).

2.32 I²C-Bus Interface and I3C Bus Interface/High-Speed I²C-Bus Interface

Table 2.74 is Comparative Overview of I2C-Bus Interface and I3C Bus Interface/High-Speed I2C-Bus Interface.

Table 2.74 Comparative Overview of I²C-Bus Interface and I3C Bus Interface/High-Speed I²C-Bus Interface

Item	RX72M (RIICa)/RX72N (RIICa)	RX74M (RI3C/RIICHS)/ RX74N (RI3C/RIICHS)
Number of channels	3	3 (RI3C0, RIICHS1, RIICHS2)
Communications format Transfer rate	• I²C-bus format or SMBus format — Standard-mode (Sm): up to 100 kbps — Fast-mode (Fm): up to 400 kbps — Fast-mode Plus (Fm+): up to 1 Mbps • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate	• I²C-bus format — Standard-mode (Sm): 0 to 100 kbps — Fast-mode (Fm): 0 to 400 kbps — Fast-mode Plus (Fm+): 0 to 1 Mbps — High-speed mode (Hs-mode) 0 to 3.4 Mbps • SMBus format: 10 to 100 kbps • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
SCL clock	For master operation, the duty cycle of the SCL is selectable in the range from 4 to 96%.	For master operation, the duty cycle of the SCL is selectable in the range from 4 to 96%.
Generating and detecting conditions	Start, restart, and stop conditions are automatically generated. Start conditions (including restart conditions) and stop conditions are detectable.	START, repeated START, and STOP conditions are automatically generated. START conditions (including repeated START conditions) and STOP conditions are detectable.
Slave address	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.	• Slave address (static address) (max 3 addresses) • 7-bit and 10-bit address formats are supported. • General call address • Hs mode master code • Device ID • Host address
Acknowledgment	• For transmission, the acknowledgment bit is automatically loaded. — Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge signal. • For reception, the acknowledgment bit is automatically transmitted. — If a wait between the eighth and ninth clock pulses has been selected, software control of the acknowledgment in response to the received data is possible.	• For transmission, the acknowledgment bit is automatically loaded. — Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge signal. • For reception, the acknowledgment bit is automatically transmitted. — If a wait between the eighth and ninth clock pulses has been selected, software control of the acknowledgment in response to the received data is possible.

Item	RX72M (RIICa)/RX72N (RIICa)	RX74M (RI3C/RIICHS)/ RX74N (RI3C/RIICHS)
Wait function	• During reception, cycles of waiting by holding the SCL line low can be inserted at the following two types of timing: — Waiting between the eighth and ninth clock pulses — Waiting between the ninth clock pulse and the first clock pulse of the next byte	• During reception, cycles of waiting by holding the SCL line low can be inserted at the following two types of timing: — Waiting between the eighth and ninth clock pulses — Waiting between the ninth clock pulse and the first clock pulse of the next byte
SDA output delay function	Changes in the timing of the output of data bits for transmission, and of the acknowledgment bit, can be delayed relative to the falling edge of SCL.	It is possible to delay the change timing of the output of the transmission data bits and the acknowledgment bit relative to the falling edge of SCL.
Arbitration	• For multi-master operation — Clock synchronization for the SCL line in cases of conflict with the SCL signal from another master is possible. — When generating the start condition would create conflict on the bus, loss in arbitration is detected by testing for non-matching between the internal data level and the actual level on the SDA line. — During master operation, loss in arbitration is detected by testing for non-matching between the actual level on the SDA line and the internal data level. • Loss in arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the generating of double start conditions). • Loss in arbitration in transfer of a not-acknowledge signal due to the internal signal (NACK) and the actual level on the SDA line not matching is detectable. • Loss in arbitration due to non-matching of internal data level and the actual level on the SDA line is detectable in slave transmission.	• For multi-master operation — Clock synchronization for the SCL line in cases of conflict with the SCL signal from another master is possible. — When generating the START condition would create conflict on the bus, loss in arbitration is detected by testing for non-matching between the internal data level and the actual level on the SDA line. — During master operation, loss in arbitration is detected by testing for non-matching between the actual level on the SDA line and the internal data level. • Loss in arbitration due to detection of the START condition while the bus is busy is detectable (to prevent the generating of double START conditions). • Loss in arbitration in transfer of a not-acknowledge signal due to the internal signal (NACK) and the actual level on the SDA line not matching is detectable. • Loss in arbitration due to non-matching of internal data level and the actual level on the SDA line is detectable in slave transmission.
Timeout function	The internal timeout function is capable of detecting long-interval stop of the SCL.	The internal timeout function is capable of detecting long-interval stop of the SCL.
Noise cancellation	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.	• Analog noise filter • Digital noise filter

Item	RX72M (RIICa)/RX72N (RIICa)	RX74M (RI3C/RIICHS)/ RX74N (RI3C/RIICHS)
Interrupt sources	Four sources: • Communication error/communication event — Detection of arbitration-lost, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmission end	Five sources: • Communication error or communication event (EEI) — Arbitration lost — NACK detection — Timeout detection — START condition detection (including repeated START condition) — STOP condition detection • Receive data full (RXI) • Transmit data empty (TXI) • Wake-up (WUI) — Slave address match detection • Transmission end (TEI)
Low power consumption function	Module stop state can be set.	Module stop state can be set.
RIIC operating modes	• Four — Master transmit mode — Master receive mode — Slave transmit mode — Slave receive mode	• Four — Master transmit mode — Master receive mode — Slave transmit mode — Slave receive mode
Event link function (output)	Four sources (RIIC0): • Communication error/communication event — Detection of arbitration-lost, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmission end	• Communication error/communication event • Receive data full • Transmit data empty • Transmission end

Table 2.75 Comparison of I²C-Bus Interface and I3C Bus Interface/High-Speed I²C-Bus Interface Registers

Register	Bit	RX72M (RIICa)/RX72N (RIICa)	RX74M (RI3C/RIICHS)/ RX74N (RI3C/RIICHS)
ICCR1	—	I²C-bus control register 1	—
ICCR2	—	I²C-bus control register 2	—
ICMR	—	—	Mode register
ICMR1	—	I²C-bus mode register 1	—
ICMR2	—	I²C-bus mode register 2	—
ICMR3	—	I²C-bus mode register 3	—
ICCR	—	—	Control register
ICCAR	—	—	Controller device address register
ICRCR	—	—	Reset control register
ICMMR	—	—	Operating mode monitor register
ICISR	—	—	Internal status register
ICISER	—	—	Internal status detection enable register
ICISIER	—	—	Internal status interrupt enable register
ICDCTIR	—	—	Device characteristics table index register
ICINCR	—	—	IBI notify control register
ICFER	TMOE	Timeout function enable bit	—
	NACKE	NACK reception transfer suspension enable bit	—
	NFE	Digital noise filter enable bit	—
	SMBS	—	SMBus/I²C-bus selection bit
	FMPE	Fast-mode plus enable bit 0: No Fm+ slope control circuit is used for the SCLn pin and SDAn pin. 1: An Fm+ slope control circuit is used for the SCLn pin and SDAn pin.	Fast-mode plus enable bit 0: No Fm+ slope control circuit is used for the SCL00 pin and SDA00 pin. 1: An Fm+ slope control circuit is used for the SCL00 pin and SDA00 pin.
	HSME	—	Hs-mode enable bit
ICTCR	—	—	Target mode control register
ICSCR	—	—	Slave mode control register
ICRCCR	—	—	Reference clock control register
ICSBR	—	—	Standard bitrate register
ICFBR	—	—	F/S-mode bitrate register
ICEBR	—	—	Extended bitrate register
ICHBR	—	—	Hs-mode bitrate register
ICBFTR	—	—	Bus free time setting register
ICBATR	—	—	Bus available time setting register
ICBITR	—	—	Bus idle time setting register
ICOCR	—	—	Output signal control register
ICICR	—	—	Input signal control register
ICTOR	—	—	Timeout control register
ICWUCR	—	—	Wake-up unit control register
ICACKR	—	—	Acknowledgment bit control register
ICCSCR	—	—	Clock stretch control register
ICSTCR	—	—	Clock stall control register
ICTDLR	—	—	Target transmit/receive data length register
ICSYTCR	—	—	Synchronous timing control register
ICASTCR	—	—	Asynchronous timing control register
ICASTTR	—	—	Asynchronous timing trigger register

Register	Bit	RX72M (RIICa)/RX72N (RIICa)	RX74M (RI3C/RIICHS)/ RX74N (RI3C/RIICHS)
ICASTCCR	—	—	Asynchronous timing counter control register
ICCGR	—	—	Condition generation request register
ICCQR	—	—	Command queue register
ICRQR	—	—	Response queue register
ICDR	—	—	Transmit/receive data register
ICIQR	—	—	IBI queue register
ICSQR	—	—	Receive status queue register
ICHCQR	—	—	High-priority command queue register
ICHRQR	—	—	High-priority response queue register
ICHDR	—	—	High-priority transmit/receive data register
ICQBTCR	—	—	Queue buffer threshold control register
ICDBTCR	—	—	Data buffer threshold control register
ICSQTCR	—	—	Receive status queue threshold control register
ICHQBTCR	—	—	High-priority queue buffer threshold control register
ICHDBTCR	—	—	High-priority data buffer threshold control register
ICIER	—	I²C-bus interrupt enable register	—
ICSR1	—	I²C-bus status register 1	—
ICSR2	TMOF	Timeout detection flag bit (b0)	Timeout detection flag bit (b20)
	AL	Arbitration-lost flag bit (b1)	Arbitration-lost flag bit (b16)
	START	Start condition detection flag bit (b2)	Start condition detection flag bit (b0)
	STOP	Stop condition detection flag bit (b3)	Stop condition detection flag bit (b1)
	RDRF	Receive data full flag bit (b5)	—
	TEND	Transmission end flag bit (b6)	Transmission end flag bit(b8)
	TDRE	Transmit data empty flag bit (b7)	—
	WUDF	—	Wake-up condition detection flag bit
SARLy	—	Slave address register Ly	—
SARUy	—	Slave address register Uy	—
ICBRL	—	I²C-bus bit rate low-level register	—
ICBRH	—	I²C-bus bit rate high-level register	—
ICDRT	—	I²C-bus transmit data register	—
ICDRR	—	I²C-bus receive data register	—
ICDRS	—	I²C-bus shift register	—
ICSER	—	I²C-bus status enable register	Status detection enable register
ICSIER	—	—	Status interrupt enable register
ICCSR	—	—	Communication status register
ICCSER	—	—	Communication status detection enable register
ICCSIER	—	—	Communication status interrupt enable register
ICHCSR	—	—	High-priority communication status register
ICHCSER	—	—	High-priority communication status detection enable register
ICHCSIER	—	—	High-priority communication status interrupt enable register
ICBSR	—	—	Bus status register
ICSSR	—	—	Slave mode status register
ICWUSR	—	—	Wake-up unit status register

Register	Bit	RX72M (RIICa)/RX72N (RIICa)	RX74M (RI3C/RIICHS)/ RX74N (RI3C/RIICHS)
ICCSCCR	—	—	C_SyncCNT capture register
ICTDATRm	—	—	Target device address table register m
ICEDATR	—	—	Extended target device address table register
ICDARy	—	—	Device address register y
SARy	—	—	Slave address register y
ICTDCTRm	—	—	Target device characteristics table register m
ICDCTR	—	—	Device characteristics table register
ICPIDLR	—	—	Provisioned ID low register
ICPIDHR	—	—	Provisioned ID high register
ICDAMRy	—	—	Device address monitor register y
SAMRy	—	—	Slave address monitor register y
ICTEVR	—	—	Target event register
ICASR	—	—	Activity state register
ICMWLR	—	—	Max write length register
ICMRLR	—	—	Max read length register
ICTMR	—	—	Test mode register
ICDSR	—	—	Device status register
ICMWSR	—	—	Max write speed register
ICMRSR	—	—	Max read speed register
ICMTTR	—	—	Maximum read turnaround time register
ICTSIR	—	—	Timing support information register
ICTSIR2	—	—	Timing support information register 2
ICBCR	—	—	Bit count register
ICQBSR	—	—	Queue buffer status register
ICDBSR	—	—	Data buffer status register
ICSQSR	—	—	Receive status queue status register
ICHQBSR	—	—	High-priority queue buffer status register
ICHDBSR	—	—	High-priority data buffer status register
ICIMR	—	—	Internal status monitor register
ICCECR	—	—	Controller error count register
ICTC1CR	—	—	T_C1 capture register
ICTC2CR	—	—	T_C2 capture register
ICCCR	—	—	Communication clock control register

2.33 CAN Module and CAN FD Module/CAN FD Module with Gateway Functionality

Table 2.76 is Comparative Overview of CAN Module and CANFD Module/CAN FD Module with Gateway Functionality, and Table 2.77 is Comparison of Registers of CAN Module and CAN FD Module/CAN FD Module with Gateway Functionality.

Table 2.76 Comparative Overview of CAN Module and CANFD Module/CAN FD Module with Gateway Functionality

Item	RX72M/RX72N (CAN)	RX74M/RX74N (CANFD/CANFDG)
Protocol	ISO 11898-1 compliant (standard and extended frames)	ISO 11898-1:2015 compliant
Number of channels	3	CANFDG: 2 CANFD: 1
Gateway function	—	CAN 2.0 ↔ CAN 2.0 CAN 2.0 ↔ CAN FD (only when the payload size is 8 bytes)*1 CAN FD ↔ CAN FD
Data transfer rate	Programmable bit rate up to 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source	Arbitration phase: up to 1 Mbps Data phase: up to 8 Mbps*1
Operating frequency	Peripheral module clock (PCLKB) or CANMCLK	Register block: up to 150 MHz (PCLKA) Message buffer RAM: up to 300 MHz (PCLKE)*1
Operating clock for data link layer (DLL clock)	—	Up to 80 MHz (either CANFDMCLK or CANFDCLK can be selected)
Frame types	• Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID) • Remote frame in base format (11-bit ID) • Remote frame in extended format (29-bit ID)	Classic CAN (CAN 2.0) • Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID) • Remote frame in base format (11-bit ID) • Remote frame in extended format (29-bit ID) CAN FD*1 • Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID)
Reception	• Data frame and remote frame can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable from overwrite mode (message overwritten) and overrun mode (message discarded) • The reception complete interrupt can be individually enabled or disabled for each mailbox.	• Data frames and remote frames can be received. • The ID format to be received (base ID only, extended ID only, or both base ID and extended ID) can be selected. • Receive message buffer interrupt can be enabled or disabled individually for each message buffer.
Data length	0 to 8 bytes	Classic CAN: 0 to 8 bytes CAN FD: 0 to 8, 12, 16, 20, 24, 32, 48, or 64 bytes*1

Item	RX72M/RX72N (CAN)	RX74M/RX74N (CANFD/CANFDG)
Acceptance filter	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox.	Filterable in the following fields: • IDE bit (base format, extended format, or both) • ID field • RTR bit (data frame or remote frame) (only for Classic CAN) • DLC field (data length) Protection function when the payload size is exceeded Acceptance filter list (AFL) entries can be updated during communication.
Receive message transfer function	• Routing function A function that transfers received messages to arbitrary destination buffers (Maximum number of destination buffers: 2) Transfer destination: Receive buffer, receive FIFO buffer, and transmit/receive FIFO buffer • Label addition function Label information can be stored together when storing a message in a receive buffer and FIFO buffer.	—
Transmission	• Data frame and remote frame can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable from ID priority mode and mailbox number priority mode • Transmission request can be aborted (the completion of abort can be confirmed with a flag) • The transmission complete interrupt can be individually enabled or disabled for each mailbox.	• Data frames and remote frames can be sent • The ID format to be sent (base ID only or extended ID only) can be selected. • The one-shot transmission function can be selected. • Either ID priority transmission mode or message buffer number priority transmission mode can be selected. • Transmission requests can be aborted. (Completion of abort can be confirmed with a flag.) • Channel transmission interrupts can be enabled or disabled.
Automatic transmission interval adjustment	The message transmission interval time can be set. (transmit mode of transmit/receive FIFO buffers)	Available when the common FIFO is configured as a transmit FIFO The interval between messages sent from the FIFO can be adjusted.
Error status monitoring	• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off entry, and bus-off recovery). • The error counters can be read.	—

Item	RX72M/RX72N (CAN)	RX74M/RX74N (CANFD/CANFDG)
Method of recovery from the bus-off state	Mode transition for the recovery from the bus-off state can be selected: • ISO 11898-1 Standards compliant • Automatic entry to CAN halt mode at bus-off entry • Automatic entry to CAN halt mode at bus-off end • Entry to CAN halt mode by a program • Transition into error-active state by a program	How to recover from the bus-off state can be selected. • Normal mode (ISO 11898-1 compliant) • Automatically enters CH_HALT mode when the bus-off state starts. • Automatically enters CH_HALT mode when the bus-off state ends. • Enters CH_HALT mode by software (during the period of recovery from the bus-off state). • The state programmatically changes to the Error Active state.
Timer	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.	Transmission and reception timestamp function
Interrupt function	Five types of interrupt sources — Reception complete interrupt — Transmission complete interrupt — Receive FIFO interrupt — Transmit FIFO interrupt — Error interrupt	Receive FIFO interrupt Global error interrupt Channel transmit interrupt Channel error interrupt Common FIFO receive interrupt Receive message buffer interrupt
Software support	Three software support units: — Acceptance filter support — Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) — Channel search support	Label information is automatically added to received messages.
Test mode	Three test modes available for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)	• Basic test mode • Listen-only mode • Self-test mode 0 (external loop-back mode) • Self-test mode 1 (internal loop-back mode)
Power consumption reducing function (RX72M/RX72N) Power down function (RX74M/RX74N)	Module-stop state can be set.	Module start/stop function for CAN node (CH_SLEEP and GL_SLEEP mode) Transition to module stop state is possible.
CAN sleep mode	Current consumption can be reduced by stopping the CAN clock.	—
RAM	—	RAM with ECC protection
Bus traffic measurement	—	CAN bus traffic measurement of each channel is possible
Protect Zone filter	—	Security attribute can be set.

Note: 1. This is only available for products that support the CAN FD protocol.

Table 2.77 Comparison of Registers of CAN Module and CAN FD Module/CAN FD Module with Gateway Functionality

Register	Bit	RX72M/RX72N (CAN)	RX74M/RX74N (CANFD/CANFDG)
CTRL	—	Control register	—
BCR	—	Bit configuration register	—
MKRk	—	Mask register k (k = 0 to 7)	—
FIDCR0 FIDCR1	—	FIFO received ID compare registers 0 and 1	—
MKIVLR	—	Mask invalid register	—
MBj	—	Mailbox register j (j = 0 to 31)	—
MIER	—	Mailbox interrupt enable register	—
MCTLj	—	Message control register j (j = 0 to 31)	—
RFCR	—	Receive FIFO control register	—
RFPCR	—	Receive FIFO pointer control register	—
TFCR	—	Transmit FIFO control register	—
TFPCR	—	Transmit FIFO pointer control register	—
STR	—	Status register	—
MSMR	—	Mailbox search mode register	—
MSSR	—	Mailbox search status register	—
CSSR	—	Channel search support register	—
AFSR	—	Acceptance filter support register	—
EIER	—	Error interrupt enable register	—
EIFR	—	Error interrupt factor judge register	—
RECR	—	Receive error count register	—
TECR	—	Transmit error count register	—
ECSR	—	Error code store register	—
TSR	—	Time stamp register	—
TCR	—	Test control register	—
NBCR	—	—	Nominal bit rate configuration register
CHCR	—	—	Channel control register
CHSR	—	—	Channel status register
CHESR	—	—	Channel error status register
DBCR	—	—	Data bit rate configuration register
FDCFG	—	—	CAN FD configuration register
FDCTR	—	—	CAN FD control register
FDSTS	—	—	CAN FD status register
FDCRC	—	—	CAN FD CRC register
GCFG	—	—	Global configuration register
GCR	—	—	Global control register
GSR	—	—	Global status register
GESR	—	—	Global error status register
TISR	—	—	Transmit interrupt status register
TSCR	—	—	Timestamp counter register
AFCR	—	—	Acceptance filter list control register
AFCFG	—	—	Acceptance filter list configuration register
AFLn.IDR	—	—	Acceptance filter list n ID register (n = 0 to 15)
AFLn.MASK	—	—	Acceptance filter list n mask register (n = 0 to 15)
AFLn.PTR0	—	—	Acceptance filter list n pointer register 0 (n = 0 to 15)
AFLn.PTR1	—	—	Acceptance filter list n pointer register 1 (n = 0 to 15)

Register	Bit	RX72M/RX72N (CAN)	RX74M/RX74N (CANFD/CANFDG)
RMCR	—	—	Receive message buffer configuration register
RMNDR	—	—	Receive message buffer new data register
RFCRn	—	—	Receive FIFO n configuration register (n = 0, 1)
RFSRn	—	—	Receive FIFO n status register (n = 0, 1)
RFPCRn	—	—	Receive FIFO n pointer control register (n = 0, 1)
CFCR0	—	—	Common FIFO 0 configuration register
CFECRn*1			Common FIFO n extended configuration register (n = 0 to 5)
CFSR0	—	—	Common FIFO 0 status register
CFPCR0	—	—	Common FIFO 0 pointer control register
FESR	—	—	FIFO empty status register
FFSR	—	—	FIFO full status register
FMLSR	—	—	FIFO message lost status register
RFISR	—	—	Receive FIFO interrupt status register
CFRISR*1	—	—	Common FIFO receive interrupt status register
CFTISR*1	—	—	Common FIFO transmit interrupt status register
FFISR*1	—	—	FIFO full interrupt status register
CFOWSR*1	—	—	Common FIFO message overwrite status register
CFORISR*1	—	—	Common FIFO one frame receive interrupt status register
CFOTISR*1	—	—	Common FIFO one frame transmit interrupt status register
DTCR	—	—	DMA transfer control register
DTSR	—	—	DMA transfer status register
TDTCR*1	—	—	Transmit DMA transfer control register
TDTSR*1	—	—	Transmit DMA transfer status register
RISR*1	—	—	Receive interrupt status register
TMCRn	—	—	Transmit message buffer n control register (n = 0 to 3)
TMSRn	—	—	Transmit message buffer n status register (n = 0 to 3)
TMTRSRm	—	—	Transmit message buffer transmission request status register m
TMARSRm	—	—	Transmit message buffer transmission abort request status register m
TMTCSRm	—	—	Transmit message buffer transmission completion status register m
TMTASRm	—	—	Transmit message buffer transmission abort status register m
TMIERm	—	—	Transmit message buffer interrupt enable register m
TQCRn	—	—	Transmit queue n configuration register
TQSRn	—	—	Transmit queue n status register
TQPCRn	—	—	Transmit queue n pointer control register
TQFISR*1	—	—	Transmit queue full interrupt status register

Register	Bit	RX72M/RX72N (CAN)	RX74M/RX74N (CANFD/CANFDG)
TQMLSR*1	—	—	Transmit queue message lost status register
TQISR*1	—	—	Transmit queue interrupt status register
TQOTISR*1	—	—	Transmit queue one frame transmit interrupt status register
TQORISR*1	—	—	Transmit queue one frame receive interrupt status register
TQFSR*1	—	—	Transmit queue full status register
THCR	—	—	Transmission history configuration register
THSR	—	—	Transmission history status register
THACR0	—	—	Transmission history access register 0
THACR1	—	—	Transmission history access register 1
THPCR	—	—	Transmission history pointer control register
GRCR	—	—	Global reset control register
GTMCR	—	—	Global test mode configuration register
GTMER	—	—	Global test mode enable register
GFDCFG	—	—	Global CAN FD configuration register
GTMLKR	—	—	Global test mode lock key register
RTPARk	—	—	RAM test page access register k (k = 0 to 63)
BLCCR*1	—	—	Bus load control register
BLCR*1	—	—	Bus load counter register
AFIGSR	—	—	Acceptance filter list ignore entry setting register
AFIGER	—	—	Acceptance filter list ignore entry enable register
RMIER	—	—	Receive message buffer interrupt enable register
ECCSR	—	—	ECC control/status register
ECTMR	—	—	ECC test mode register
ECTDR	—	—	ECC decoder test data register
ECEAR	—	—	ECC error address register

Note: 1. This is only available for the CANFDG channel.

2.34 Serial Peripheral Interface

Table 2.78 is Comparative Overview of Serial Peripheral Interfaces, and Table 2.79 is Comparison of Serial Peripheral Interface Registers.

Table 2.78 Comparative Overview of Serial Peripheral Interfaces

Item	RX72M (RSPIc)/RX72N (RSPIc)	RX74M (RSPIA)/RX74N (RSPIA)
Number of channels	3	3
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication mode: Full-duplex or simplex (transmit-only) can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Full-duplex or simplex (transmit-only or receive-only) communications can be selected. • Polarity of RSPCK can be selected. • Phase of RSPCK can be selected.
Data format	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable.	• MSB first/LSB first selectable • Transfer bit length can be changed to 4 through 32 bits. • Transmit buffer size/receive buffer size: 32 bits × 4 stages FIFO • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable. • Logic level of transmit and receive data can be inverted.
Operating clock	• Peripheral module clock (PCLKA)	• Selectable from peripheral module clock (PCLKA) or SPI clock (SPICLK)
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). Width at high level: 2 cycles of PCLK; width at low level: 2 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing TCLK. The division ratio ranges from divided by 2 to divided by 4096. • In slave mode, an external input clock is used as a serial clock. The maximum frequency of RSPCK is that of TCLK divided by 2 (width at high level: 1 cycle of TCLK; width at low level: 1 cycle of TCLK).
Buffer configuration	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers	• Transmit buffer and receive buffer are configured independently.
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection • Receive data ready detection

Item	RX72M (RSPIc)/RX72N (RSPIc)	RX74M (RSPIA)/RX74N (RSPIA)
SSL control function	• Four SSL pins (SSLx0 to SSLx3) for each channel • In single-master mode, SSLx0 to SSLx3 pins are output. • In multi-master mode: SSLx0 pin for input, and SSLx1 to SSLx3 pins for either output or unused. In slave mode: SSLx0 pin for input, and SSLx1 to SSLx3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity	[Motorola SPI] • Four SSL signals per RSPIA channel (SSLn0 to SSLn3) • In single-master mode, the SSLn0 to SSLn3 signals are output. • In multi-master mode: The SSLn0 signal is input and the SSLn1 to SSLn3 signals are output or Hi-Z. • In slave mode: The SSLn0 signal is input and the SSLn1 to SSLn3 signals are Hi-Z (not used). • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units • Function for changing SSL polarity [TI SSP] • Four SSL signals per RSPIA channel (SSLn0 to SSLn3) • In single-master mode, the SSLn0 to SSLn3 signals are output. • In multi-master mode: The SSLn0 signal is input and the SSLn1 to SSLn3 signals are output or Hi-Z. • In slave mode: The SSLn0 signal is input and the SSLn1 to SSLn3 signals are Hi-Z (not used). • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 0 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to OE output negation (OE negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Communication protocol	—	Motorola SPI TI SSP (synchronous serial protocol)

Item	RX72M (RSPIc)/RX72N (RSPIc)	RX74M (RSPIA)/RX74N (RSPIA)
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function	[Motorola SPI] • A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transmit data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function (enabled or disabled by setting) • Delay between data bytes under burst transfer can be reduced. [TI SSP] • A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transmit data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay (OE negation delay), and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function (enabled or disabled by setting) • Delay between data bytes under burst transfer can be reduced.
Interrupt sources	• Interrupt sources — Receive buffer full interrupt — Transmit buffer empty interrupt — Error interrupt (mode fault, overrun, underrun, or parity error) — Idle interrupt	• Five interrupt sources — Receive buffer full/receive data ready interrupt — Transmit buffer empty interrupt — Communication end interrupt — Error interrupt (mode fault error, underrun error, overrun error, parity error, or receive data ready) — Idle interrupt
Event link function (output)	• The following events can be output to the event link controller. (RSPI0) — Receive buffer full event — Transmit buffer empty event — Error event (mode fault, overrun, underrun, or parity error) — Idle event — Transmit end event	• Five event types can be output to the event link controller. — Receive buffer full/receive data ready event signal — Transmit buffer empty event signal — Mode fault error, underrun error, overrun error, parity error, or receive data ready event signal — Idle event signal — Communication end event signal

Item	RX72M (RSPIc)/RX72N (RSPIc)	RX74M (RSPIA)/RX74N (RSPIA)
Others	• Function for initializing the RSPI • Loopback mode	• Function for disabling (initializing) the RSPIA • Loopback mode • SPE bit status polling function
Low power consumption function	Module stop state can be set.	Module stop state can be set.
Protect Zone filter	—	Security attribution can be set for each channel.

Table 2.79 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX72M (RSPIc)/RX72N (RSPIc)	RX74M (RSPIA)/RX74N (RSPIA)
SPCR	—	RSPI control register SPCR is an 8-bit register.	RSPI control register SPCR is a 32-bit register.
	SPMS	RSPI mode select bit (b0)	RSPI mode select bit (b24)
	TXMD	Communications operating mode select bit	—
	MODFEN	Mode fault error detection enable bit (b2)	Mode fault error detection enable bit (b14)
	MSTR	RSPI master/slave mode select bit (b3)	RSPI master/slave mode select bit (b30)
	SPEIE	Error interrupt enable bit (b4)	Error interrupt enable bit (b16)
	SPTIE	Transmit buffer empty interrupt enable bit (b5)	Transmit buffer empty interrupt enable bit (b20)
	SPE	RSPI function enable bit (b6)	RSPI function enable bit (b0)
	SPRIE	Receive buffer full interrupt enable bit (b7)	Receive buffer full interrupt enable bit (b17)
	SPPE	—	Parity enable bit
	SPOE	—	Parity mode bit
	PTE	—	Parity self-diagnosis bit
	SCKASE	—	RSPCK auto-stop function enable bit
	SCKDDIS	—	RSPCK delay between frames disable bit
	SPIIE	—	Error interrupt enable bit
	RDRIS	—	Receive data ready interrupt select bit
	SPCIE	—	Communication end interrupt enable bit
	FRFS	—	Frame format select bit
	CMMD[1:0]	—	Communication mode select bits
	SYNDIS	—	Synchronizer disable bit
SSLP	SSL0P	SSL0 signal polarity setting bit 0: SSL0 signal is active low 1: SSL0 signal is active high	SSL0 signal polarity setting bit [Motorola SPI] 0: The SSLn0 signal is active low. 1: The SSLn0 signal is active high. [TI SSP] 0: The SSLn0 signal is active high. 1: The SSLn0 signal is active low.
	SSL1P	SSL1 signal polarity setting bit 0: SSL1 signal is active low 1: SSL1 signal is active high	SSL1 signal polarity setting bit [Motorola SPI] 0: The SSLn1 signal is active low. 1: The SSLn1 signal is active high. [TI SSP] 0: The SSLn1 signal is active high. 1: The SSLn1 signal is active low.

Register	Bit	RX72M (RSPIc)/RX72N (RSPIc)	RX74M (RSPIA)/RX74N (RSPIA)
SSLP	SSL2P	SSL2 signal polarity setting bit 0: SSL2 signal is active low 1: SSL2 signal is active high	SSL2 signal polarity setting bit [Motorola SPI] 0: The SSLn2 signal is active low. 1: The SSLn2 signal is active high. [TI SSP] 0: The SSLn2 signal is active high. 1: The SSLn2 signal is active low.
	SSL3P	SSL3 signal polarity setting bit 0: SSL3 signal is active low 1: SSL3 signal is active high	SSL3 signal polarity setting bit [Motorola SPI] 0: The SSLn3 signal is active low. 1: The SSLn3 signal is active high. [TI SSP] 0: The SSLn3 signal is active high. 1: The SSLn3 signal is active low.
SPSR	—	RSPI status register SPSR is an 8-bit register.	RSPI status register SPSR is a 16-bit register.
	OVRF	Overrun error flag (b0)	Overrun error flag (b8)
	IDLNF	Idle flag (b1)	Idle flag (b9)
	MODF	Mode fault error flag (b2)	Mode fault error flag (b10)
	PERF	Parity error flag (b3)	Parity error flag (b11)
	UDRF	Underrun error flag (b4) This flag is used with the MODF flag to check the state in terms of mode fault errors and underrun errors. b4 b2 0 0: Neither a mode fault error nor an underrun error occurs 0 1: A mode fault error occurs 1 1: An underrun error occurs	Underrun error flag (b12) This flag is used with the MODF flag to check the state in terms of mode fault errors and underrun errors. b10 b12 0 x: Neither a mode fault error nor an underrun error occurs 1 0: A mode fault error occurs 1 1: An underrun error occurs
	SPTEF	Transmit buffer empty flag (b5) 0: Transmit buffer has valid data 1: Transmit buffer has no valid data	Transmit buffer empty flag (b13) 0: The number of empty stages in the transmit FIFO ≤ the value set by the SPFCR.TTRG[1:0] bits 1: The number of empty stages in the transmit FIFO > the value set by the SPFCR.TTRG[1:0] bits
	SPRF	Receive buffer full flag (b7) 0: Receive buffer has no valid data 1: Receive buffer has valid data	Receive buffer full flag (b15) 0: The number of data stored in the receive FIFO ≤ number of frames set by the SPFCR.RTRG[1:0] bits 1: The number of data stored in the receive FIFO > number of frames set by the SPFCR.RTRG[1:0] bits
	RRDYF	—	Receive data ready flag
	SPCF	—	Communication end flag

Register	Bit	RX72M (RSPIc)/RX72N (RSPIc)	RX74M (RSPIA)/RX74N (RSPIA)
SPDCR	—	RSPI data control register SPDCR is an 8-bit register.	RSPI data control register SPCDR is a 16-bit register.
	SPCF[1:0]	Number of frames specification bits (b1, b0)	Number of frames setting bits (b9, b8)
	SPRDTD	RSPI receive/transmit data select bit (b4) 0: The SPDR values are read from the receive buffer 1: The SPDR values are read from the transmit buffer (but only if the transmit buffer is empty)	RSPI receive/transmit data select bit (b3) 0: SPDR values are read from the receive buffer 1: SPDR values are read from the transmit buffer
	SPLW	RSPI longword access/word access specification bit	—
	SPBYT	RSPI byte access specification bit	—
	BYSW	—	Byte swap bit
	DINV	—	Transfer data invert bit
SSLND	SLNDL[2:0]	RSPI slave select negation delay register b2 b0 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK	RSPI slave select negation delay register [In master mode] b2 b0 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK [In TI SSP slave mode] b2 b0 0 0 0: 1 TCLK 0 0 1: 2 TCLK 0 1 0: 3 TCLK 0 1 1: 4 TCLK 1 0 0: 5 TCLK 1 0 1: 6 TCLK 1 1 0: 7 TCLK 1 1 1: 8 TCLK
SPND	SPNDL[2:0]	RSPI next-access delay setting bits b2 b0 0 0 0: 1 RSPCK + 2 PCLK 0 0 1: 2 RSPCK + 2 PCLK 0 1 0: 3 RSPCK + 2 PCLK 0 1 1: 4 RSPCK + 2 PCLK 1 0 0: 5 RSPCK + 2 PCLK 1 0 1: 6 RSPCK + 2 PCLK 1 1 0: 7 RSPCK + 2 PCLK 1 1 1: 8 RSPCK + 2 PCLK	RSPI next-access delay setting bits b2 b0 0 0 0: 1 RSPCK + 5 TCLK 0 0 1: 2 RSPCK + 5 TCLK 0 1 0: 3 RSPCK + 5 TCLK 0 1 1: 4 RSPCK + 5 TCLK 1 0 0: 5 RSPCK + 5 TCLK 1 0 1: 6 RSPCK + 5 TCLK 1 1 0: 7 RSPCK + 5 TCLK 1 1 1: 8 RSPCK + 5 TCLK

Register	Bit	RX72M (RSPIc)/RX72N (RSPIc)	RX74M (RSPIA)/RX74N (RSPIA)
SPCR2	—	RSPI control register 2	—
SPCMDm	—	RSPI command register m (m = 0 to 7) The SPCMDm register is a 16-bit register.	RSPI command register m (m = 0 to 7) The SPCMDm register is a 32-bit register.
	SSLA[2:0]	SSL signal assertion setting bits (b6 to b4)	SSL signal assertion setting bits (b26 to b24)
	SPB[3:0] (RX72N/RX72M) SPB[4:0] (RX74M/RX74N)	RSPI data length setting bits (b11 to b8) b11 b8 0 0 0 0: 20 bits 0 0 0 1: 24 bits 0 0 1 0: 32 bits 0 0 1 1: 32 bits 0 1 0 0: 8 bits 0 1 0 1: 8 bits : : 0 1 1 1: 8 bits 1 0 0 0: 9 bits 1 0 0 1: 10 bits 1 0 1 0: 11 bits 1 0 1 1: 12 bits 1 1 0 0: 13 bits 1 1 0 1: 14 bits 1 1 1 0: 15 bits 1 1 1 1: 16 bits	RSPI data length setting bits (b20 to b16) b20 b16 0 0 0 1 1: 4 bits 0 0 1 0 0: 5 bits 0 0 1 0 1: 6 bits : : 0 0 1 1 1: 8 bits : : : : : : : : : : : : : : 0 1 1 1 1: 16 bits 1 0 0 0 0: 17 bits : : 1 1 1 1 0: 31 bits 1 1 1 1 1: 32 bits Settings other than above are prohibited.
	SPNDEN	RSPI next-access delay enable bit 0: A next-access delay of 1 RSPCK + 2 PCLK 1: A next-access delay is equal to the setting of the RSPI next-access delay register (SPND)	RSPI next-access delay enable bit 0: A next-access delay of 1 RSPCK + 5 TCLK 1: A next-access delay is equal to the setting of the RSPI next-access delay register (SPND)
	SLNDEN	SSL negation delay setting enable bit 0: An SSL negation delay of 1 RSPCK 1: An SSL negation delay is equal to the setting of the RSPI slave select negation delay register (SSLND)	SSL negation delay setting enable bit 0: In master mode, an SSL negation delay of 1 RSPCK In TI SSP slave mode, an SSL negation delay of 1 TCLK 1: An SSL negation delay is equal to the setting of the RSPI slave select negation delay register (SSLND)

Register	Bit	RX72M (RSPIc)/RX72N (RSPIc)	RX74M (RSPIA)/RX74N (RSPIA)
SPCMDm	SCKDEN	RSPCK delay setting enable bit 0: An RSPCK delay of 1 RSPCK 1: An RSPCK delay is equal to the setting of the RSPI clock delay register (SPCKD)	RSPCK delay setting enable bit 0: In Motorola SPI protocol, an RSPCK delay of 1 RSPCK In TI SSP protocol, an RSPCK delay of 0 RSPCK 1: An RSPCK delay is equal to the setting of the RSPI clock delay register (SPCKD)
SPDCR2	—	RSPI data control register 2	—
SPRMCR	—	—	RSPI receive-only mode control register
SPDRCSR	—	—	RSPI receive data ready detect condition setting register
SPPCR	—	—	RSPI Pin Control Register
SPFCR	—	—	RSPI FIFO control register
SPTFSR	—	—	RSPI transmit FIFO status register
SPRFSR	—	—	RSPI receive FIFO status register
SPPSR	—	—	RSPI polling status register
SPSCLR	—	—	RSPI status clear register
SPFCLR	—	—	RSPI FIFO clear register

2.35 CRC Calculator

Table 2.80 is Comparative Overview of CRC Calculators.

Table 2.80 Comparative Overview of CRC Calculators

Item	RX72M (CRCA)/RX72N (CRCA)		RX74M (CRCA)/RX74N (CRCA)	
Data size	8 bits	32 bits	8 bits	32 bits
Data for CRC calculation	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 32n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 32n-bit units (where n is a whole number)
CRC processor unit	8-bit parallel processing	32-bit parallel processing	8-bit parallel processing	32-bit parallel processing
CRC generating polynomial	• One of three generating polynomials is selectable — 8-bit CRC $X^8 + X^2 + X + 1$ — 16-bit CRC $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$	• One of two generating polynomials is selectable — 32-bit CRC $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$, $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$	• One of three generating polynomials is selectable — 8-bit CRC $X^8 + X^2 + X + 1$ — 16-bit CRC $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$	• One of two generating polynomials is selectable — 32-bit CRC $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$, $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$
CRC calculation switching	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication		The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication	
Low power consumption	Module stop state can be set.		Module stop state can be set.	
Protect Zone filter	—		Security attribute can be set.	

2.36 Serial Sound Interface

Table 2.81 is Comparative Overview of Serial Sound Interfaces, and Table 2.82 is Comparison of Serial Sound Interface Registers.

Table 2.81 Comparative Overview of Serial Sound Interfaces

Item		RX72M (SSIE)/ RX72N (SSIE)	RX74M (SSIE)/ RX74N (SSIE)
Number of channels		Two channels, SSIE0 and SSIE1	Two channels, SSIE0 and SSIE1
Transfer mode		• Master/slave • Transmission, reception, or transception (transception is only available on SSIE0)	• Master/slave • Transmission, reception, or transception
Data format		• I^2S format • Left-justified format • Right-justified format • Monaural format • TDM format	• I^2S format • Left-justified format • Right-justified format • Monaural format • TDM format
Serial data		• Fixed to MSB first • System word length: Selectable from among 8, 16, 24, 32, 48, 64, 128, or 256 bits • Data word length: Selectable from among 8, 16, 18, 20, 22, 24, or 32 bits • The level of padding bits is programmable. • Mute function	• Fixed to MSB first • System word length: Selectable from among 8, 16, 24, 32, 48, 64, 128, or 256 bits • Data word length: Selectable from among 8, 16, 18, 20, 22, 24, or 32 bits • The level of padding bits is programmable. • Mute function
Master clock (MCK)		Clock source: AUDIO_CLK	Clock source: AUDIO_CLK or GTIOC14A
Bit clock (BCK)	In master mode	• Frequency: Selectable from among 1/1, 1/2, 1/4, 1/6, 1/8, 1/12, 1/16, 1/24, 1/32, 1/48, 1/64, 1/96, or 1/128 of the AUDIO_CLK frequency • Continued supply or stopping while data transfer is halted is selectable.	• Frequency: Selectable from among 1/1, 1/2, 1/4, 1/6, 1/8, 1/12, 1/16, 1/24, 1/32, 1/48, 1/64, 1/96, or 1/128 of the MCK frequency • Continued supply or stopping while data transfer is halted is selectable.
	In master and slave modes	Polarity is selectable as rising edges or falling edges.	Polarity is selectable as rising edges or falling edges.
LR clock (LRCK)		• Polarity is selectable as low or high. • Continued supply or stopping while data transfer is halted is selectable.	• Polarity is selectable as low or high. • Continued supply or stopping while data transfer is halted is selectable.
FIFO	Capacity	• Transmit FIFO: 4 bytes × 32 stages • Receive FIFO: 4 bytes × 32 stages	• Transmit FIFO: 4 bytes × 32 stages • Receive FIFO: 4 bytes × 32 stages
	Data alignment	Alignment of data (left-justified or right-justified) in the FIFO is selectable.	Alignment of data (left-justified or right-justified) in the FIFO is selectable.

Item	RX72M (SSIE)/ RX72N (SSIE)	RX74M (SSIE)/ RX74N (SSIE)
Interrupts	• Data transfer error/idle state • Receive data full • Transmit data empty	• Data transfer error/idle state • Receive data full • Transmit data empty
Low power consumption function	• Module stop function • Master clock (MCK) supply stopping function	• Module stop function • Master clock (MCK) supply stopping function
Protect Zone filter	—	Security attribute can be set for each channel.

Table 2.82 Comparison of Serial Sound Interface Registers

Register	Bit	RX72M (SSIE)/RX72N (SSIE)	RX74M (SSIE)/RX74N (SSIE)
SSICR	CKS	—	Master clock select bit

2.37 SD/MMC Host Interface and SD Host Interface

Table 2.83 is Comparative Overview of SD Host Interfaces, and Table 2.84 is Comparison of SD Host Interface Registers.

Table 2.83 Comparative Overview of SD Host Interfaces

Item	RX72M (SDHI)/RX72N (SDHI)	RX74M (SDHIc)/RX74N (SDHIc)
SD bus interface	• Compatible with SD memory card and SDIO card • Transfer bus mode selectable from 4-bit wide bus mode or 1-bit default bus mode • Compatible with SD, SDHC, and SDXC formats	• Compatible with SD memory card and SDIO card • Transfer bus mode selectable from 4-bit wide bus mode or 1-bit default bus mode • Compatible with SD, SDHC, and SDXC formats
Transfer modes	Selectable from high-speed mode or default speed mode	Selectable from default speed mode, high-speed mode, SDR12, or SDR25
MMC bus interface	—	• Supports e•MMC device • Transfer bus width selectable from 1, 4, or 8 bits • Selectable from backward compatible mode or high-speed SDR mode
SDHI clock	The SDHI clock is generated by dividing peripheral module clock B (PCLKB) by *n*, where *n* = 1, 2, 4, 8, 16, 32, 64, 128, 256, or 512	The SDHI clock is generated by dividing peripheral module clock B (PCLKB) by *n*, where *n* = 1, 2, 4, 8, 16, 32, 64, 128, 256, or 512
Error check functions	• CRC7 (command/response) • CRC16 (transfer data)	• CRC7 (command/response) • CRC16 (transfer data)
Interrupt sources	• Card access interrupt (CACI) • SDIO access interrupt (SDACI) • Card detection interrupt (CDETI) • SD buffer access interrupt (SBFAI)	• Card access interrupt (CACI) • SDIO access interrupt (SDACI) • Card detection interrupt (CDETI) • SD buffer access interrupt (SBFAI)
DMA transfer sources	• DMAC and DTC triggerable by the SBFAI interrupt • SD buffer is read and write accessible using the DMAC and DTC	• DMAC and DTC triggerable by the SBFAI interrupt • SD buffer is read and write accessible using the DMAC and DTC
Other functions	• Card detection • Write protection	• Card detection • Write protection support
Low power consumption function	Module stop state can be set.	Module stop state can be set.
Protect Zone filter	—	Security attributes can be set.

Table 2.84 Comparison of SD Host Interface Registers

Register	Bit	RX72M (SDHI)/RX72N (SDHI)	RX74M (SDHIc)/RX74N (SDHIc)
SDOPT	TOUTMASK	—	Timeout mask bit
	WIDTH8	—	MMC bus width select bit
	WIDTH	SD bus width select bit 0: Wide bus mode (4 bits) 1: Default bus mode (1 bit)	SD bus width select bit 0: Selected by the WIDTH8 bit 1: Default bus mode (1 bit)
SDIFMD	—	—	SD/MMC interface mode register
SDVER	—	Version register	—

2.38 Parallel Data Capture Unit

Table 2.85 is Comparative Overview of Parallel Data Capture Units.

Table 2.85 Comparative Overview of Parallel Data Capture Units

Item	RX72M (PDC)/RX72N (PDC)	RX74M (PDC)/RX74N (PDC)
Capture range	• Desired amounts of parallel data within the following ranges in the vertical and horizontal directions. • Vertical direction: 1 to 4095 lines • Horizontal direction: 4 to 4095 bytes	• Desired amounts of parallel data within the following ranges in the vertical and horizontal directions. • Vertical direction: 1 to 4095 lines • Horizontal direction: 4 to 4095 bytes
Parallel data transfer clock (PIXCLK)	Operating frequency: 1 to 27 MHz	Operating frequency: 1 to 27 MHz
Interrupt sources	• Receive data ready • Frame end • Overrun • Underrun • Error in the setting for the number of lines • Error in setting for the number of bytes per line	• Receive data ready • Frame end • Overrun • Underrun • Error in the setting for the number of lines • Error in setting for the number of bytes per line
Startup of DTC/DMAC	The receive data ready interrupt is capable of starting the DTC or DMAC	The receive data ready interrupt is capable of starting the DTC or DMAC
Parallel data transfer clock output (PCKO)	• Operating frequency: 1 to 30 MHz • Clock source: Peripheral module clock B (PCLKB) • Frequency division ratio: Selectable from 2, 4, 6, 8, 10, 12, 14, and 16.	• Operating frequency: 1 to 37.5 MHz • Clock source: Peripheral module clock B (PCLKB) • Frequency division ratio: Selectable from 2, 4, 6, 8, 10, 12, 14, and 16.
Others	• PDC reset function • Selectable active sense for the VSYNC and HSYNC signals • Monitoring of the VSYNC and HSYNC signals • Endian selection	• PDC reset function • Selectable active sense for the VSYNC and HSYNC signals • Monitoring of the VSYNC and HSYNC signals • Endian selection
Reducing power consumption	The PDC can be placed in the module stop state.	The PDC can be placed in the module stop state.
Protect Zone filter	—	Security attribute can be set.

2.39 Boundary Scan

Table 2.86 is Comparative Overview of Boundary Scan.

Table 2.86 Comparative Overview of Boundary Scan

Item	RX72M	RX72N	RX74M/RX74N
Boundary scan enabled/disabled	Boundary scan is enabled when the RES# pin and the BSCANP pin are driven high and the EMLE pin is driven low.	Boundary scan is enabled when the RES# pin and the BSCANP pin are driven high and the EMLE pin is driven low.	When a low level is input to the RES# pin and the power-on reset is negated, the boundary scan function is enabled.
Dedicated boundary scan pins	The following pins are dedicated for the JTAG, when boundary scan function is enabled (TDO/TCK/TDI/TMS/TRST#). 224-pin LFBGA/176-pin LFBGA: PF0/PF1/PF2/PF3/PF4	The following pins are dedicated for the JTAG, when boundary scan function is enabled (TDO/TCK/TDI/TMS/TRST#). 224-pin LFBGA/176-pin LFBGA: PF0/PF1/PF2/PF3/PF4 145-pin TFLGA: P26/P27/P30/P31/P34	The following pins are dedicated for the JTAG, when boundary scan function is enabled (TDO/TCK/TDI/TMS). P302/P301/P303/P300
Six test modes	• BYPASS mode • EXTEST mode • SAMPLE/PRELOAD mode • CLAMP mode • HIGHZ mode • IDCODE mode	• BYPASS mode • EXTEST mode • SAMPLE/PRELOAD mode • CLAMP mode • HIGHZ mode • IDCODE mode	• BYPASS mode • EXTEST mode • SAMPLE/PRELOAD mode • CLAMP mode • HIGHZ mode • IDCODE mode

2.40 Arithmetic Unit for Trigonometric Functions

Table 2.87 is Comparative Overview of Arithmetic Units for Trigonometric Functions, Table 2.88 is Comparison of Registers of Arithmetic Unit for Trigonometric Functions, and Table 2.89 is Comparison of Range and Unit of Values.

Table 2.87 Comparative Overview of Arithmetic Units for Trigonometric Functions

Item	RX72M/RX72N (TFUv1)	RX74M/RX74N (TFUv2)
Arithmetic Processing	Calculation of sine, cosine, arctangent, and hypotenuse • A sine and cosine can be simultaneously calculated. • An arctangent and hypotenuse can be simultaneously calculated.	Calculation of sine, cosine, arctangent, and hypotenuse • A sine and cosine can be simultaneously calculated. • An arctangent and hypotenuse can be simultaneously calculated.
Data Type for Processing	Single-precision floating-point	Single-precision floating-point, fixed-point two's-complement
Number of cycles for calculation	Sine: 14 Cosine: 14 Arctangent: 14 Hypotenuse: 14 + 2 for software processing	Sine: 5 Cosine: 5 Arctangent: 14 Hypotenuse: 14
ProtectZone filter	—	Security attribute can be set.

Table 2.88 Comparison of Registers of Arithmetic Unit for Trigonometric Functions

Register	Bit	RX72M/RX72N (TFUv1)	RX74M/RX74N (TFUv2)
FXSCIOC	—	—	Fixed-point sincos input and output setting register
FXATIOC	—	—	Fixed-point atanhypot_k input and output setting register
TRGSTS	—	—	Trigonometric status register
FPSCDT0	—	—	Floating-point sincos data register 0
FPSCDT1	—	—	Floating-point sincos data register 1
FPATDT0	—	—	Floating-point atanhypot_k data register 0
FPATDT1	—	—	Floating-point atanhypot_k data register 1
FXSCDT0	—	—	Fixed-point sincos data register 0
FXSCDT1	—	—	Fixed-point sincos data register 1
FXATDT0	—	—	Fixed-point atanhypot_k data register 0
FXATDT1	—	—	Fixed-point atanhypot_k data register 1
DTSR0	—	—	Data saving and restoring register 0
DTSR1	—	—	Data saving and restoring register 1
TFUSAR	—	—	TFU security attribution register

Table 2.89 Comparison of Range and Unit of Values

Arithmetic Processing	I/O		Unit	Range	
				RX72M/RX72N (TFUv1)	RX74M/RX74N (TFUv2)
Input and output of floating-point numbers					
Calculating sine	Input	Angle θ	radians	$-float\_max \leq \theta \leq float\_max$	$-float\_max \leq \theta \leq float\_max$
	Output	sinθ	—	$-1.0 \leq sin(\theta) \leq 1.0$	$-1.0 \leq sin\theta \leq 1.0$
Calculating cosine	Input	Angle θ	radians	$-float\_max \leq \theta \leq float\_max$	$-float\_max \leq \theta \leq float\_max$
	Output	cosθ	—	$-1.0 \leqq cos(\theta) \leqq 1.0$	$-1.0 \leq cos\theta \leq 1.0$
Calculating arctangent	Input	x and y coordinates	—	$-float\_max \leq x \leq float\_max$ $-float\_max \leq y \leq float\_max$	$-float\_max \leq x \leq float\_max$ $-float\_max \leq y \leq float\_max$
	Output	atan(y/x)	radians	$-\pi \leq arctan(y/x) \leq \pi$	$-\pi \leq atan(y/x) \leq \pi$
Calculating hypotenuse	Input	x and y coordinates	—	$-float\_max \leq x \leq float\_max$ $-float\_max \leq y \leq float\_max$	—
	Output	$\sqrt{x^2+y^2}$	—	$0 \leq \sqrt{x^2+y^2} \leq \infty$	—
Calculating hypotenuse	Input	x and y coordinates	—	—	$-float\_max \leq x \leq float\_max$ $-float\_max \leq y \leq float\_max$
	Output	$\sqrt{x^2+y^2}/k$	—	—	$0 \leq \sqrt{x^2+y^2}/k \leq \infty$
Input and output of fixed-point numbers					
Calculating sine	Input	Angle θ	turns	—	$-1.0 \leq \theta \leq 1.0$
			radians	—	$-4.0 \leq \theta \leq 4.0$
	Output	sinθ	—	—	$-1.0 \leq sin\theta \leq 1.0$
Calculating cosine	Input	Angle θ	turns	—	$-1.0 \leq \theta \leq 1.0$
			radians	—	$-4.0 \leq \theta \leq 4.0$
	Output	cosθ	—	—	$-1.0 \leq cos\theta \leq 1.0$
Calculating arctangent	Input	x and y coordinates	—	—	$-1.0 \leq x < 1.0$ $-1.0 \leq y < 1.0$
	Output	atan(y/x)	turns	—	$-0.5 \leq atan(y/x) \leq 0.5$
			radians	—	$-\pi \leq atan(y/x) \leq \pi$
Calculating hypotenuse	Input	x and y coordinates	—	—	$-1.0 \leq x < 1.0$ $-1.0 \leq y < 1.0$
	Output	$\sqrt{x^2+y^2}/k$	—	—	$0 \leq \sqrt{x^2+y^2}/k \leq \sqrt{2}/k$

2.41 Delta-Sigma Modulator Interface

Table 2.90 is Comparative Overview of DSMIFs, and Table 2.91 is Comparison of DSMIF Registers.

Table 2.90 Comparative Overview of DSMIFs

Item	RX72M (DSMIF)	RX74M (DSMIFA)
Number of units	2	2
Number of channels	Three channels per unit (six channels in total)	Three channels per unit (six channels in total)
Core clock	PCLKB	Selectable from PCLKA, DSMIFCLK, or GPTCLK
Functions	• Capable of filtering 1-bit digital input data DSMDATm (m = 0 to 5) and converting them into 16-bit digital values. • The sinc filters are selectable as first-, second-, or third-order. • DSMCLKm (m = 0 to 5) can be output at up to 25 MHz in master operation and input at up to 25 MHz in slave operation. • Crests and troughs can trigger capture, allowing the capture of values for current with the same timing.	• Capable of filtering 1-bit digital input data DSMDATn (n = 0 to 5) and converting them into 16-bit digital values. • The sinc filters are selectable as first-, second-, or third-order. • The DSMCLKn pin can output at up to 25 MHz in master operation and input at up to 25 MHz in slave operation. • Crests and troughs can trigger capture, allowing the capture of values for current at the same timing. • Error detection function
Interrupt sources	Three sources per unit • Short-circuit detection • Overcurrent detection • Current sum error detection	Seven sources per unit • Current data register update (for each channel) • Current capture data register A update (for each channel) • Current capture data register B update (for each channel) • Current data register update (common) • Current capture data register A update (common) • Current capture data register B update (common) • Error detection — Short-circuit detection (for each channel) — Overcurrent lower limit detection 0 (for each channel) — Overcurrent upper limit detection 0 (for each channel) — Overcurrent lower limit detection 1 (for each channel) — Overcurrent upper limit detection 1 (for each channel) — Overcurrent lower limit detection 2 (for each channel) — Overcurrent upper limit detection 2 (for each channel) — Total-current lower limit detection — Total-current upper limit detection

Item	RX72M (DSMIF)	RX74M (DSMIFA)
Event link function (input)	Current capture function Two inputs per unit Measured data can be transferred to other registers in response to event signals used as triggers.	Current capture function Six inputs per unit Measured data can be transferred to other registers in response to event signals used as triggers.
	—	PWM synchronization function Three inputs per unit The decimation dividing counter for the differentiation stage of the sinc filter can be initialized using the output from the GPTW (set as an event signal) as a trigger.
Notification function (output)	—	Four outputs per channel Results of comparisons against upper and lower limits for overcurrent detection can be output to POEG as event notifications.
Low power consumption function	This module can be placed in the module stop state.	This module can be placed in the module-stop state.
Protect Zone filter	—	Security attribution can be set for each unit.

Table 2.91 Comparison of DSMIF Registers

Register	Bit	RX72M (DSMIF)	RX74M (DSMIFA)
DSCR	—	DSMIF control register	—
DSSR	—	DSMIF status register	—
OCLTR	—	Overcurrent detection low threshold register	—
OCHTR	—	Overcurrent detection high threshold register	—
SCLTR	—	Short-circuit detection low threshold register	—
SCHTR	—	Short-circuit detection high threshold register	—
SUMLTR	—	Current sum error detection low threshold register	—
SUMHTR	—	Current sum error detection high threshold register	—
CDRx	—	Channel x current data register	—
CCDRx	—	Channel x crest current data register	—
TCDRx	—	Channel x trough current data register	—
OCDRx	—	Channel x overcurrent detection data register	—
DSCCR	—	DSMIF control register	—
DSCHR	—	DSMIF channel control register	—
DSCCSCR	—	—	Core clock selection control register
DSSEICR	—	—	Overcurrent sum error detection interrupt control register
DSSECSR	—	—	Overcurrent sum error detection channel setting register
DSSELTR	—	—	Overcurrent sum error detection low threshold register

Register	Bit	RX72M (DSMIF)	RX74M (DSMIFA)
DSSEHTR	—	—	Overcurrent sum error detection high threshold register
DSSECR	—	—	Overcurrent sum error detection control register
DSSECDRn	—	—	Overcurrent sum error detection capture data register n
DSCMSR	—	—	Common mode setting register
DSCICR	—	—	Common interrupt control register
DSCSTRTR	—	—	Channel software start trigger register
DSCSTPTR	—	—	Channel software stop trigger register
DSCESR	—	—	Channel error status register
DSCOCESR	—	—	Channel overcurrent error status register
DSCOCNSR	—	—	Channel overcurrent notification status register
DSCOCRMR	—	—	Channel overcurrent comparator result monitor register
DSCSR	—	—	Channel status register
DSCSSR	—	—	Channel state status register
DSCESCR	—	—	Channel error status clear register
DSCOCESCR	—	—	Channel overcurrent error status clear register
DSCOCNSCR	—	—	Channel overcurrent notification status clear register
DSCSCR	—	—	Channel status clear register
DSICRCHn	—	—	Interrupt control register channel n
DSCMCCRCHn	—	—	Current-measurement clock control register channel n
DSCMFCRCHn	—	—	Current-measurement filter control register channel n
DSCMCTCRCHn	—	—	Current-measurement capture trigger control register channel n
DSEDCRCHn	—	—	Error detection control register channel n
DSSCTSRCHn	—	—	Short-circuit threshold setting register channel n
DSOCFCRCHn	—	—	Overcurrent-detection filter control register channel n
DSODCRCHn	—	—	Overcurrent-detection control register channel n
DSODWCRCHn	—	—	Overcurrent-detection window control register channel n
DSODWN0F	—	—	Overcurrent-detection window notification 0 suppression filter control register channel n
DSODWN1F	—	—	Overcurrent-detection window notification 1 suppression filter control register channel n
DSODWN2F	—	—	Overcurrent-detection window notification 2 suppression filter control register channel n
DSCLOCKCHn	—	—	Channel lock register channel n
DSOCLTR0CHn	—	—	Overcurrent low threshold register 0 channel n
DSOCHTR0CHn	—	—	Overcurrent high threshold register 0 channel n

Register	Bit	RX72M (DSMIF)	RX74M (DSMIFA)
DSOCLTR1CHn	—	—	Overcurrent low threshold register 1 channel n
DSOCHTR1CHn	—	—	Overcurrent high threshold register 1 channel n
DSOCLTR2CHn	—	—	Overcurrent low threshold register 2 channel n
DSOCHTR2CHn	—	—	Overcurrent high threshold register 2 channel n
DSCSTRTRCHn	—	—	Software start trigger register channel n
DSCSTPTRCHn	—	—	Software stop trigger register channel n
DSCDRCHn	—	—	Current data register channel n
DSCCDRACHn	—	—	Capture current data register a channel n
DSCCDRBCHn	—	—	Capture current data register b channel n
DSOCDRCHn	—	—	Overcurrent data register channel n
DSCOCDR0CHn	—	—	Capture overcurrent data register 0 channel n
DSCOCDR1CHn	—	—	Capture overcurrent data register 1 channel n
DSCOCDR2CHn	—	—	Capture overcurrent data register 2 channel n
DSCSRCHn	—	—	Status register channel n
DSCSCRCHn	—	—	Status clear register channel n
DSCCSCR	—	—	Core clock selection control register
DSSEICR	—	—	Overcurrent sum error detection interrupt control register
DSSECSR	—	—	Overcurrent sum error detection channel setting register
DSSELTR	—	—	Overcurrent sum error detection low threshold register
DSSEHTR	—	—	Overcurrent sum error detection high threshold register

2.42 12-Bit D/A Converter

Table 2.92 is Comparative Overview of 12-Bit D/A Converters, and Table 2.93 is Comparison of 12-Bit D/A Converter Registers.

Table 2.92 Comparative Overview of 12-Bit D/A Converters

Item	RX72M (R12DAa)/RX72N (R12DAa)	RX74M (R12DAB)/RX74N (R12DAB)
Resolution	12 bits	12 bits
Output channels	Two channels	Two channels
Measure against mutual interference between analog modules	• Measure against interference between D/A and A/D conversion D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable signal from the 12-bit A/D converter (unit 1). Therefore, the degradation of A/D conversion accuracy due to interference is reduced by controlling the timing in which the 12-bit D/A converter inrush current occurs, with the enable signal.	—
Low power consumption function	Module stop state can be set.	Module stop state can be set.
Event link function (input)	DA0 conversion can be started when an event signal is input.	D/A conversion of channels 0 and 1 can be started by an event signal input.
Output destination switching	Buffered output (gain = 1) or unbuffered output can be selected.	Independent control of output to the external pin and internal module (ADC) is possible.
Protect Zone filter	—	Security attribution can be set for each channel.

Table 2.93 Comparison of 12-Bit D/A Converter Registers

Register	Bit	RX72M (R12DAa)/RX72N (R12DAa)	RX74M (R12DAB)/RX74N (R12DAB)
DADRm (RX72M/ RX72N) DADR (RX74M/ RX74N)	—	D/A data register m (m = 0, 1)	D/A data register
DACR (RX72M/ RX72N) DACR0 (RX74M/ RX74N)	—	D/A control register	D/A control register 0
		The size of the register differs.	
	DACEN	—	D/A conversion enable bit
	DAE	D/A enable bit (b5)	Collective D/A conversion control bit (b15)
	DAOE0	D/A output enable 0 bit	—
	DAOE1	D/A output enable 1 bit	—
	DAOE	—	D/A output enable bit
	DAOUTDIS [1:0]	—	D/A output select bits

Register	Bit	RX72M (R12DAa)/RX72N (R12DAa)	RX74M (R12DAB)/RX74N (R12DAB)
DADPR (RX72M/ RX72N) DACR1 (RX74M/ RX74N)	—	Data register format select register	D/A control register 1
		The size of the register differs.	
	DPSEL	Format select bit (b7)	Format select bit (b16)
DAADSCR	—	D/A A/D synchronous start control register	—
DAAMPCR	—	D/A output amplifier control register	—
DAASWCR	—	D/A output amplifier stabilization wait control register	—
DAADUSR	—	D/A A/D synchronous unit select register	—
DACR2	—	—	D/A control register 2

2.43 Temperature Sensor

Table 2.94 is Comparative Overview of Temperature Sensors, and Table 2.95 is Comparison of Temperature Sensor Registers.

Table 2.94 Comparative Overview of Temperature Sensors

Item	RX72M/RX72N (TEMPS)	RX74M/RX74N (TEMPS)
Temperature sensor voltage output	Temperature sensor outputs a voltage to the 12-bit A/D converter unit 1.	Temperature sensor outputs a voltage to the A/D converter.
Low-power consumption function	Module stop state can be set.	Module stop state can be set.
Temperature sensor calibration data	Reference data measured for each chip at factory shipment is stored.	Reference data measured for each chip at factory shipment is stored.
Abnormal temperature detection	—	Abnormal high/low temperatures can be detected and a reset can be issued.
Protect Zone filter	—	Security attribution can be set.

Table 2.95 Comparison of Temperature Sensor Registers

Register	Bit	RX72M/RX72N (TEMPS)	RX74M/RX74N (TEMPS)
TSCR	TSOE	Temperature sensor output enable bit 0: Disables output from the temperature sensor to the 12-bit A/D converter unit 1. 1: Enables output from the temperature sensor to the 12-bit A/D converter unit 1.	Temperature sensor output enable bit 0: Disables output from the temperature sensor to the A/D converter. 1: Enables output from the temperature sensor to the A/D converter.
TSCDR2	—	—	Temperature sensor calibration data register 2

2.44 Data Operation Circuit

Table 2.96 is Comparative Overview of Data Operation Circuits, and Table 2.97 is Comparison of Data Operation Circuit Registers.

Table 2.96 Comparative Overview of Data Operation Circuits

Item	RX72M/RX72N (DOC)	RX74M/RX74N (DOCA)
Data operation function	16-bit data comparison, addition, and subtraction	• Comparison of 16- or 32-bit values (equal or not equal, greater or less than, or within or beyond a range) • Addition or subtraction of 16- or 32-bit values
Lower power consumption function	The DOC can be placed in a module-stop state.	The DOC can be placed in a module-stop state.
Interrupts	• The result of data comparison meets the detection condition. • The result of data addition is greater than FFFFh, which is an overflow. • The result of data subtraction is less than 0000h, which is an underflow.	• The result of data comparison meets the detection condition. • The result of data addition is greater than FFFFh (DOCR.DOPSZ = 0) or FFFF FFFFh (DOCR.DOPSZ = 1), which is an overflow. • The result of data subtraction is less than 0000h (DOCR.DOPSZ = 0) or 0000 0000h (DOCR.DOPSZ = 1), which is an underflow.
Event link function (output)	• The result of data comparison meets the detection condition. • The result of data addition is greater than FFFFh, which is an overflow. • The result of data subtraction is less than 0000h, which is an underflow.	• The result of data comparison meets the detection condition. • The result of data addition is greater than FFFFh (DOCR.DOPSZ = 0) or FFFF FFFFh (DOCR.DOPSZ = 1), which is an overflow. • The result of data subtraction is less than 0000h (DOCR.DOPSZ = 0) or 0000 0000h (DOCR.DOPSZ = 1), which is an underflow.

Table 2.97 Comparison of Data Operation Circuit Registers

Register	Bit	RX72M/RX72N (DOC)	RX74M/RX74N (DOCA)
DOCR	DCSEL (RX72M/ RX72N) DCSEL[2:0] (RX74M/ RX74N)	Detection condition select bits 0: 'Not equal to' is to be detected. 1: 'Equal to' is to be detected	Detection condition select bits b6 b4 0 0 0: Not equal to (DODIR ≠ DODSR0) 0 0 1: Equal to (DODIR = DODSR0) 0 1 0: Less than (DODIR < DODSR0) 0 1 1: Greater than (DODIR > DODSR0) 1 0 0: Within the range (DODSR0 < DODIR < DODSR1) 1 0 1: Beyond the range (DODIR < DODSR0, DODSR1 < DODIR) Settings other than above are prohibited.
	DOPSZ	—	Data operation size select bit
	DOPCIE	Data operation circuit interrupt enable bit (b4)	Data operation circuit interrupt enable bit (b7)
	DOPCF	Data operation result flag	—
	DOPCFCL	Data operation result clear bit	—
DODIR	—	DOC data input register	DOC data input register
		The size of the register differs.	
DODSR (RX72M/RX72N) DCSELn (RX74M/RX74N)	—	DOC data setting register	DOC data setting register n (n = 0, 1)
		The size of the register differs.	
DOSR	—	—	DOC status register
DOSCR	—	—	DOC status clear register

2.45 RAM and SRAM/LRAM

Table 2.98 is Comparative Overview of RAM and SRAM/LRAM, and Table 2.99 is Comparison of RAM and SRAM/LRAM Registers.

Table 2.98 Comparative Overview of RAM and SRAM/LRAM

Item	RX72M (RAM) /RX72N (RAM)		RX74M (SRAM/LRAM)/RX74N (SRAM/LRAM)	
	RAM	ECCRAM	LRAM0 and LRAM1	SRAM0 and SRAM1
Memory capacity	RAM 512 Kbytes Expansion RAM 512 ytes	32 Kbytes	LRAM0 128 Kbytes LRAM1 128 Kbytes	SRAM0 1 Mbyte SRAM1 512 Kbytes
Address	RAM: 0000 0000h to 0007 FFFFh Expansion RAM 0080 0000h to 0087 FFFFh	00FF 8000h to 00FF FFFFh	[Accsess from CPU] • Secure Area LRAM0: 8000 0000h to 8001 FFFFh LRAM1: 8002 0000h to 8003 FFFFh • Non-Secure Area LRAM0: 0000 0000h to 0001 FFFFh LRAM1: 0002 0000h to 0003 FFFFh [Access from Other Area] • Secure Area LRAM0: 8280 0000h to 8281 FFFFh LRAM1: 8282 0000h to 8283 FFFFh • Non-Secure Area LRAM0: 0280 0000h to 0281 FFFFh LRAM1: 0282 0000h to 0283 FFFFh	• Secure Area SRAM0 8200 0000h to 820F FFFFh SRAM1 8210 0000h to 8217 FFFFh • Non-secure Area SRAM0 0200 0000h to 020F FFFFh SRAM1 0210 0000h to 0217 FFFFh
Memory bus	RAM: Memory bus 1 Expansion RAM Memory bus 3	Memory bus 3	LRAM0BI and LRAM1BI	SRAM0BI and SRAM1BI

Item	RX72M (RAM) /RX72N (RAM)		RX74M (SRAM/LRAM)/RX74N (SRAM/LRAM)	
	RAM	ECCRAM	LRAM0 and LRAM1	SRAM0 and SRAM1
Access	RAM —Enabling or disabling of the RAM is selectable. —Access takes one cycle whether for reading or writing. Expansion RAM —Enabling or disabling of the expansion RAM is selectable. [When MEMWAIT is 0] —Access takes one cycle whether for reading or writing. [When MEMWAIT is 1] —Access takes two cycles whether for reading or writing.	Enabling or disabling of the ECCRAM is selectable. [When MEMWAIT is 0] • With the ECC function disabled: — Access takes two cycles whether for reading or writing. • With the ECC function enabled (and there are no errors): — Access takes two cycles whether for reading or writing. • With the ECC function enabled (and an error is found): — Access takes three cycles whether for reading or writing. [When MEMWAIT is 1] • With the ECC function disabled: — Access takes three cycles whether for reading or writing. • With the ECC function enabled (and there are no errors): — Reading takes three cycles and writing takes four cycles. • With the ECC function enabled (and an error is found): — Access takes five cycles whether for reading or writing.	Up to 600 MHz, no-wait access	Supports wait state function. Wait states are not inserted into the access cycle by default. If the ICLK frequency is greater than 150 MHz, a wait state is required. If the ICLK frequency is less than or equal to 150 MHz, a wait state is not required.
Data retention function	Data retention is not available on deep software standby.		Not available in deep software standby mode	
Low power consumption function	The RAM, expansion RAM, and ECCRAM are independently transferrable to the module stop state.		—	Transition to the module stop state is separately possible for the SRAM0 and SRAM1

Item	RX72M (RAM) /RX72N (RAM)		RX74M (SRAM/LRAM)/RX74N (SRAM/LRAM)	
	RAM	ECCRAM	LRAM0 and LRAM1	SRAM0 and SRAM1
Error checking	• Parity checking: 1-bit error detection • When an error is found, a non-maskable interrupt or an interrupt is generated.	• ECC error correction 1-bit error correction and 2-bit error detection • When an error is found, a non-maskable interrupt or an interrupt is generated.	SEC-DED (Single-Error Correction and Double-Error Detection Code: 32-bit data with 7-bit ECC code)	SEC-DED (Single-Error Correction and Double-Error Detection Code: 64-bit data with 8-bit ECC code)
Security	—		Protect Zone Filter is integrated for memory access and register access. Access to the memory space is controlled by setting the memory Security Attribution. And access to register space is controlled by setting the register Security Attribution. See section 57, Security Features.	

Table 2.99 Comparison of RAM and SRAM/LRAM Registers

Register	Bit	RX72M (RAM)/ RX72N (RAM)	RX74M (SRAM/LRAM)/ RX74N (SRAM/LRAM)
RAMMODE	—	RAM operating mode control register	—
RAMSTS	—	RAM error status register	—
RAMECAD	—	RAM error address capture register	—
RAMPRCR	—	RAM protection register	—
EXRAMMODE	—	Expansion RAM operating mode control register	—
EXRAMSTS	—	Expansion RAM error status register	—
EXRAMECAD	—	Expansion RAM error address capture register	—
EXRAMPRCR	—	Expansion RAM protection register	—
ECCRAMMODE	—	ECCRAM operating mode control register	—
ECCRAM2STS	—	ECCRAM 2-bit error status register	—
ECCRAM1STSEN	—	ECCRAM 1-bit error information update enable register	—
ECCRAM1STS	—	ECCRAM 1-bit error status register	—
ECCRAMPRCR	—	ECCRAM protection register	—
ECCRAM2ECAD	—	ECCRAM 2-bit error address capture register	—
ECCRAM1ECAD	—	ECCRAM 1-bit error address capture register	—
ECCRAMPRCR2	—	ECCRAM protection register 2	—
ECCRAMETST	—	ECCRAM test control register	—
SRAMSABARn	—	—	SRAMn security attribute boundary address register

Register	Bit	RX72M (RAM)/ RX72N (RAM)	RX74M (SRAM/LRAM)/ RX74N (SRAM/LRAM)
SRAMSAR	—	—	SRAM security attribution register
SRAMPRCR_S	—	—	SRAM protection control register for secure
SRAMPRCR_NS	—	—	SRAM protection control register for non-secure
SRAMWTSC	—	—	SRAM wait state control register
SRAMCRn	—	—	SRAM control register n
SRAMECCRGN0	—	—	SRAM ECC region control register 0
SRAMECCRGN1	—	—	SRAM ECC region control register 1
SRAMESR	—	—	SRAM error status register
SRAMESCLR	—	—	SRAM error status clear register
SRAMEARnm	—	—	SRAMn error address m register
LRMSAR	—	—	LRAM security attribute setting register
LRMSABARn	—	—	LRAMn boundary address setting register
LRMPRCR_S	—	—	LRAM protection control register for secure applications
LRMPRCR_NS	—	—	LRAM protection control register for non-secure applications
LRMCRn	—	—	LRAMn control register
LRMESR	—	—	LRAM error flag register
LRMESCLR	—	—	LRAM error flag clear register
LRMEARnm	—	—	LRAMn error address register m

2.46 Flash Memory and MRAM

Table 2.100 is Comparative Overview of Flash Memory and MRAM, and Table 2.101 is Comparison of Flash Memory and MRAM Registers, and Table 2.102 is Comparison of Address Boundary for Each of the Commands.

Table 2.100 Comparative Overview of Flash Memory and MRAM

Item	RX72M (FLASH)/RX72N (FLASH)		RX74M (MRAM)/RX74N (MRAM)	
	Code Flash Memory	Data Flash Memory	Code MRAM	Data MRAM
Memory capacity	• User area: 4 Mbytes max.	• Data area: 32 Kbytes	• User area: 1 Mbyte max	• Data area: 48 Kbytes
ROM cache	• Capacity: 8 Kbytes • Mapping method: direct mapping • Line size: 16 bytes	Not available	—	—
Read cycle	• While ROM cache operation is enabled: When the cache is hit, one cycle; When the cache is missed, one to two cycles if ICLK ≤ 120 MHz, two to three cycles if ICLK > 120 MHz. • When ROM cache operation is disabled: One cycle if ICLK ≤ 120 MHz Two cycles if ICLK > 120 MHz	Reading proceeds in every cycle of FCLK	Reading proceeds in every cycle at the frequency set in the code MRAM frequency notifications register (MRCFREQ)	Reading proceeds in every cycle at the frequency set in the extra MRAM frequency notifications register (MREFREQ)
Value after erasure	FFh	Undefined	—	—

Item	RX72M (FLASH)/RX72N (FLASH)		RX74M (MRAM)/RX74N (MRAM)	
	Code Flash Memory	Data Flash Memory	Code MRAM	Data MRAM
Programming/ erasing method (RX72M/RX72N) Programming method (RX74M/RX74N)	• Programming and erasing the code flash memory/data flash memory is handled by the FACI commands specified in the FACI command issuing area (007E 0000h). • Programming/erasure through transfer by a dedicated flash-memory programmer via a serial interface (serial programming)		Write page buffer (1 to 32 bytes)	Write page buffer (1 to 16 bytes)
Dual bank function	The dual-bank structure makes a safe update possible in cases where programming is suspended. • Linear mode: the code flash memory is used as one area • Dual mode: the code flash memory is divided into two areas	—	The dual-bank structure makes a safe update possible in cases where programming is suspended. • Linear mode: the code MRAM is used as one area • Dual mode: the code MRAM is divided into two areas	—
Block swap function	—		Block swap block size: 8 Kbytes Block swapping allows safe updates to code in operations by exchanging working sectors	—

Item	RX72M (FLASH)/RX72N (FLASH)		RX74M (MRAM)/RX74N (MRAM)	
	Code Flash Memory	Data Flash Memory	Code MRAM	Data MRAM
Security function	Protects against illicit tampering with or reading out of data in flash memory		• Protect against illicit tampering with or reading out of data in MRAM • OFS area protection • Startup area select setting protection — BTFLG and MSUACR register are protected by the FSPR bit. — BTSIZE is protected by the FSPRS bit. • Permanent block protect setting protection — User area is permanently protected from programming operation by permanent block protect function. • MRAM protection for Protect Zone — Protection for MRAM area (program) — Protection for MRAM area (read) — Protection for register • Extra MRAM program mode entry protection • Anti-rollback counter • HUK protection	
Protection	Protects against erroneous rewriting of the flash memory		Protects against erroneous rewriting of the MRAM	
Trusted memory (TM) function	Protects against illicit reading of the code flash memory • Linear mode: blocks 8 and 9 • Dual mode: blocks 8, 9, 78, and 79		—	
Background operations (BGOs)	• The code flash memory can be read while the code flash memory is being programmed or erased. • The data flash memory can be read while the code flash memory is being programmed or erased. • The code flash memory can be read while the data flash memory is being programmed or erased.		• A bank of the code MRAM can be read while another bank of the code MRAM is being programmed. • The extra MRAM can be read while the code MRAM is being programmed. • The code MRAM can be read while the extra MRAM is being programmed.	
Units of programming and erasure (RX72M/RX72N) Units of programming (RX74M/RX74N)	• Units of programming for the user area: 128 bytes • Units of erasure for the user area: Block units	• Unit of programming for the data area: 4 bytes • Unit of erasure for the data area: 64/128/256 bytes	• 1 to 32 bytes	• 1 to 16 bytes

Item	RX72M (FLASH)/RX72N (FLASH)		RX74M (MRAM)/RX74N (MRAM)	
	Code Flash Memory	Data Flash Memory	Code MRAM	Data MRAM
Other functions	• Interrupts can be accepted during self-programming. • In the initial settings of this MCU, an expansion area of the option-setting memory can be set.		—	
FACI Commands (RX72M/RX72N) MACI Commands (RX74M/74N)	• Program • Block erase • P/E suspend • P/E resume • Status clear • Forced stop • Blank check • Configuration set • Lock-bit program • Lock-bit read		—	— <Extra MRAM without Data MRAM> • Program • Status Clear • Forced Stop • Configuration Set • Increment Counter (secure access only) • Read Counter (secure access only)
On-board programming (Serial programming/ Self-programming)	• Programming/erasure in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The transfer rate is adjusted automatically. • Programming/erasure in boot mode (USB interface) — USB0 is used. — Dedicated hardware is not required, so direct connection to a PC is possible. • Program/erase in boot mode (FINE interface) — FINE is used • Programming/erasure in single-chip mode or on-chip ROM enabled extended mode — Programming or erasure by a routine for writing to code flash memory or data flash memory within the user program is possible.		—	
Off-board programming	Programming and erasure of the code flash memory and option-setting memory by using a parallel programmer is possible.	Programming or erasure of the data flash memory by a parallel programmer is not possible.	—	

Item	RX72M (FLASH)/RX72N (FLASH)		RX74M (MRAM)/RX74N (MRAM)	
	Code Flash Memory	Data Flash Memory	Code MRAM	Data MRAM
Unique ID	A 16-byte ID code provided for each MCU		A 16-byte ID code provided for each MCU	
Safety function	• Software Protection — Protection through FENTRYR — Protection through FWEPROR • Protection by Area Protection • Error Protection Error protection detects erroneous issuance of FACI commands, unauthorized access, and flash sequencer malfunction. FACI command acceptance is disabled (command-locked state) in response to the detection of these errors. • Start-Up Program Protection		• Software protection — MACI command protection by MENTRYR register — User area protection by MRCPCS and MRCPCNS registers — User area and data area protection by the block protect setting • Error protection Error is detected when unintended commands or prohibited settings occur. The MACI command is not accepted after an error detection. • Startup area protection The startup area select function allows the user to safely update the startup program, which is to be started after a reset. The size of the startup area can be selected from 8 Kbytes, 16 Kbytes or 32 Kbytes. • ECC support for double-bit error correction and triple-bit error detection.	

Item	RX72M (FLASH)/RX72N (FLASH)		RX74M (MRAM)/RX74N (MRAM)	
	Code Flash Memory	Data Flash Memory	Code MRAM	Data MRAM
Interrupt request	• FRDYI (flash ready) — Enabled by the FRDYIE bit • FIFERR (flash access error) — Enabled by the DFAEIE, CMDLKIE, or CFAEIE bit.		• MRCRDI (code MRAM ECC error) — Enabled by the INTENBTC and INTENBDC bits • MRERDI (Extra MRAM ECC error) — Enabled by the INTENBTE and INTENBDE bits • MRCPRI (code MRAM access error) — Enabled by the MRCAEIE bit • MRDPRI (data MRAM access error) — Enabled by the MRDAEIE bit • MREPRI (Extra MRAM access error) — Enabled by the CMDLKIEE and MREAEIE bits • MRDYI (Extra MRAM ready) — Enabled by the MRDYIE bit • MRPRRI (MRAM program ready) — Enabled by the MRCPRRIE or MRDPRRIE bit	

Table 2.101 Comparison of Flash Memory and MRAM Registers

Register	Bit	RX72M (FLASH)/RX72N (FLASH)	RX74M (MRAM)/RX74N (MRAM)
ROMCE	—	ROM cache enable register	—
ROMCIV	—	ROM cache invalidate register	—
NCRGn	—	Non-cacheable area n address register (n = 0, 1)	—
NCRCn	—	Non-cacheable area n setting register (n = 0, 1)	—
FWEPROR	—	Flash P/E protect register	—
FASTAT	—	Flash access status register	—
FAEINT	—	Flash access error interrupt enable register	—
FRDYIE	—	Flash ready interrupt enable register	—
FSADDR (RX72M/ RX72N) MSADDR (RX74M/ RX74N)	—	FACI command start address register	MACI command start address register
FEADDR	—	FACI command end address register	—
FSTATR (RX72M/ RX72N) MSTATR (RX74M/ RX74N)	—	Flash status register	Extra MRAM status register
	PROTERR	—	Protect error flag
	CFGSETERR	—	Configuration set error flag
	FLWEERR	Flash P/E protect error flag	—
	PRGSPD	Program suspend status flag	—
	ERSSPD	Erase suspend status flag	—
	DBFULL	Data buffer full flag	—
	SUSRDY	Suspend ready flag	—
	ERSERR	Erase error flag	—
	ILGLERR	Illegal error flag 0: The flash sequencer has not detected an illegal FACI command or illegal flash memory access. 1: The flash sequencer has detected an illegal FACI command or illegal flash memory access.	Illegal error flag 0: The extra MRAM sequencer has not detected an illegal MACI command or illegal extra MRAM access. 1: The extra MRAM sequencer has detected an illegal MACI command or illegal extra MRAM access.
	FRDY (RX72M/ RX72N) MRDY (RX74M/ RX74N)	Flash ready flag 0: Program, block erase, multi-block erase, P/E suspend, P/E resume, forced stop, blank check, or configuration set command processing is in progress. 1: None of the above is in progress.	Extra MRAM ready flag 0: Program, Configuration set, Increment Counter or Read Counter command processing is in progress. 1: None of the above is in progress.
		The initial value after reset differs.	
	PZFERR	—	Protect Zone filter error flag
	SECERR	Security error flag 0: Write protection by the FAW.FSPR bit is not violated 1: Write protection by the FAW.FSPR bit is violated	Security error flag 0: A write protection error against the MSUASMON.FSPR bit has not been detected. 1: A write protection error against the MSUASMON.FSPR bit has been detected.
	FESETERR	FENTRY setting error flag	—

Register	Bit	RX72M (FLASH)/RX72N (FLASH)	RX74M (MRAM)/RX74N (MRAM)
FSTATR (RX72M/ RX72N) MSTATR (RX74M/ RX74N)	ILGCOMERR	Illegal command error flag 0: The flash sequencer has not detected an illegal FACI command error. 1: The flash sequencer has detected an illegal FACI command error.	Illegal command error flag 0: An illegal MACI command error has not been detected. 1: An illegal MACI command error has been detected.
FENTRYR (RX72M/ RX72N) MENTRYR (RX74M/ RX74N)	—	Flash P/E mode entry register	Extra MRAM program mode entry register
	FENTRYC	Code flash memory P/E mode entry bit	—
	FENTRYD (RX72M/ RX72N) MENTRY (RX74M/ RX74N)	Data flash memory P/E mode entry bit 0: Data flash memory is in read mode. 1: Data flash memory is in P/E mode.	Extra MRAM program mode entry bit 0: Extra MRAM is in the read mode. 1: Extra MRAM is in the program mode.
FSUINITR (RX72M/ RX72N) MSUINITR (RX74M/ RX74N)	—	Flash sequencer set-up initialization register	Extra MRAM sequencer set-up initialization register
	SUINIT	Set-up initialization bit 0: The FEADDR, FCPSR, FSADDR, FENTRYR, and FBCCNT flash sequencer set-up registers keep their current values. 1: The FEADDR, FCPSR, FSADDR, FENTRYR, and FBCCNT flash sequencer set-up registers are initialized.	Set-up initialization bit 0: The extra MRAM sequencer setting register values of the MSADDR, MENTRYR, and MCNTSELR registers are retained. 1: Initializes the extra MRAM sequencer settings in the MSADDR, MENTRYR, and MCNTSELR registers
FCMDR (RX72M/ RX72N) MCMDR (RX74M/ RX74N)	—	FACI command register	MACI command register
	PCMDR[7:0]	Precommand flag	Pre-command flag
		The initial value after reset differs.	
	CMDR[7:0]	Command flag	Command flag
		The initial value after reset differs.	
FBCCNT	—	Data flash blank check control register	—
FBCSTAT	—	Data flash blank check status register	—
FPSADDR	—	Data flash programming start address register	—
FCPSR	—	Flash sequencer processing switching register	—
FPCKAR	—	Flash sequencer processing clock frequency notification register	—
FAWMON	—	Flash access window monitor register	—
FSUACR (RX72M/ RX72N) MSUACR (RX74M/ RX74N)	—	Start-up area control register	MRAM startup area control register

Register	Bit	RX72M (FLASH)/RX72N (FLASH)	RX74M (MRAM)/RX74N (MRAM)
FSUACR (RX72M/ RX72N) MSUACR (RX74M/ RX74N)	SAS[1:0]	Start-up area select bits b1 b0 0 x: A start-up area is selected based on the setting of the FAW.BTFLG bit. 1 0: The area from FFFF E000h to FFFF FFFFh is selected as the address range for startup area 0, and the area from FFFF C000h to FFFF DFFFh is selected as the address range for startup area 1, regardless of the setting of the FAW.BTFLG bit. 1 1: The area from FFFF E000h to FFFF FFFFh is selected as the address range for startup area 1, and the area from FFFF C000h to FFFF DFFFh is selected as the address range for startup area 0, regardless of the setting of the FAW.BTFLG bit.	Startup area select bits b1 b0 0 x: Startup area is selected by the SAS2.BTFLG bit 1 0: Startup area is temporarily switched to the default area regardless of the setting of the SAS2.BTFLG bit 1 1: Startup area is temporarily switched to the alternate area regardless of the setting of the SAS2.BTFLG bit
EEPFCLK	—	Data flash memory access frequency setting register	—
MRCPFB	—	—	Code MRAM prefetch buffer enable register
MRCFREQ	—	—	Code MRAM frequency notifications register
MREFREQ	—	—	Extra MRAM frequency notifications register
MRCDECC	—	—	Code MRAM ECC decoder control register
MRCRAEINT	—	—	Code MRAM read access error interrupt enable register
MRCRAES	—	—	Code MRAM read access error status register
MRCRTEA	—	—	Code MRAM TED error address register
MRCRDEA	—	—	Code MRAM DEC error address register
MREDECC	—	—	Extra MRAM ECC decoder control register
MRERAEINT	—	—	Extra MRAM read access error interrupt enable register
MRERAES	—	—	Extra MRAM read access error status register
MRERTEA	—	—	Extra MRAM TED error address register
MRERDEA	—	—	Extra MRAM DEC error address register
MSAR	—	—	MRAM security attribution register
MREZS	—	—	Extra MRAM zeroization status register
MREZC	—	—	Extra MRAM zeroization control register
MASTAT	—	—	Extra MRAM access status register
MPAEINT	—	—	Extra MRAM access error interrupt enable register
MRDYIE	—	—	Extra MRAM ready interrupt enable register
MCNTSELR	—	—	MRAM counter select register
MCNTDTRn	—	—	MRAM counter data register n (n = 0, 1)
MCTRCNTR	—	—	MRAM configuration update transfer control register

Register	Bit	RX72M (FLASH)/RX72N (FLASH)	RX74M (MRAM)/RX74N (MRAM)
MCTRSTATR	—	—	MRAM configuration update transfer status register
MSUASMON	—	—	MRAM startup area select monitor register
MRSTTRST	—	—	MACI reset transfer status register
MRPSC	—	—	MRAM program speed control register
MREEECC	—	—	Extra MRAM ECC encoder control register
MRCPCNS	—	—	Code MRAM program control register for non-secure application
MRCPCS	—	—	Code MRAM program control register for secure application
MRCBPROTNS	—	—	Code MRAM block protection register for non-secure application
MRCBPROTS	—	—	Code MRAM block protection register for secure application
MRCPS	—	—	Code MRAM program status register
MRCPAEINT	—	—	Code MRAM program access error interrupt enable register
MRCPEA	—	—	Code MRAM program error address register
MRCFLR	—	—	Code MRAM flush register
MRCPRICR	—	—	Code MRAM program ready interrupt control register
MRDPS	—	—	Data MRAM program status register
MRDPAEINT	—	—	Data MRAM program access error interrupt enable register
MRDPEA	—	—	Data MRAM program error address register
MRDFLR	—	—	Data MRAM flush register
MRDPRICR	—	—	Data MRAM program ready interrupt control register
MRCEECC	—	—	Code MRAM ECC encoder control register
PNRn	—	—	Part numbering register n (n = 0 to 3)
MCUVER	—	—	MCU version register
MWMCR	—	—	MRAM-OTP write mode control register

Table 2.102 Comparison of Address Boundary for Each of the Commands

Command	RX72M (FLASH)/ RX72N (FLASH)	RX74M (MRAM)/ RX74N (MRAM)
Program (code flash memory)	128-byte	—
Program (data flash memory)	4-byte	16-byte
Block erase (code flash memory)	8-Kbyte or 32-Kbyte	—
Block erase (data flash memory)	64-byte	—
Multi-block erase (data flash memory)	64-, 128-, or 256-byte	—
Blank check (data flash memory)	4-byte	—
Configuration set	16-byte	16-byte

2.47 Packages

As indicated in Table 2.103, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage. For details, refer to “Design Guide for Migration between RX Family: Differences in Package External form (R01AN4591EJ)”.

Table 2.103 Packages

Package Type	RENESAS Code			
	RX72M	**RX72N**	**RX74M**	**RX74N**
320-pin LFBGA	×	×	○	○
224-pin LFBGA	PLBG0224GA-A	PLBG0224GA-A	PLBG0224GE-A	PLBG0224GE-A
176-pin LFQFP	PLQP0176KB-C	PLQP0176KB-C	PLQP0176KJ-A	PLQP0176KJ-A
176-pin LFBGA	PLBG0176GA-A	PLBG0176GA-A	PLBG0176GG-A	PLBG0176GG-A
145-pin TFLGA	×	○	×	×
144-pin LFQFP	○	○	○	○
100-pin LFQFP	PLQP0100KB-B	PLQP0100KB-B	PLQP0100KP-A	PLQP0100KP-A

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exists on both groups with different specifications are indicated by **red text**. Black text indicates there is no differences in the item's specifications between groups.

3.1 224-Pin Package

Table 3.1 is Comparative Listing of RX72M/RX74M 224-Pin LFBGA Package Pin Functions, and Table 3.2 is Comparative Listing of RX72N/RX74N 224-Pin Package Pin Functions.

Table 3.1 Comparative Listing of RX72M/RX74M 224-Pin LFBGA Package Pin Functions

224-Pin LFBGA	RX72M	RX74M
A1	NC	VSS
A2	VREFH0	PC03/PIO_027/D4-A/GTOVLO-B/GTIOC8B/ TXD11-A/SMOSI11-A/SSDA11-A/TXDA11-A/ SDAHS1-C/ET0_TXD2-A/RGMII0_TXD2-A/ CAT0_ETXD2-A/SD0CLK-A/IRQ11/PCOUTA1
A3	VREFL0	ETHPHYCLK/PC07/PIO_031/D0-A/TMO2/TOC0/ CACREF/GTETRGD/GTADSM1/GTIOC15B/ POEGA/TXD8-A/SMOSI8-A/SSDA8-A/TXDA8-A/ MISO0-A/SSITXD0/RGMII0_TXC-A/ CATRESTOUT-A/SD0CD-A/IRQ14/ DSMDAT5-C/PDMDAT0-A
A4	P41/IRQ9-DS/AN001	CLKOUT/P801/PIO_057/EBCLK-A/GTIV-B/ GTIOC0B/POEGC/TXD10-B/SMOSI10-B/ SSDA10-B/TXDA10-B/ET0_CRS-B/ CATSYNC0-A/IRQ9/ADCNV1-B/DSMDAT4-C
A5	P92/D18/A18/POE4#/RXD7/SMISO7/SSCL7/ ET1_CRS/RMII1_CRS_DV/CAT1_RX_DV/AN116/ DSMCLK4	P802/PIO_058/CS2#-A/WR#-B/WR0#-B/ GTIW-B/GTIOC1A/POEGB/SCK10-B/CTS10#-B/ TXDB10-B/CRX2-D/USB0_EXICEN/ ET0_MDIO-B/CAT0_MDIO-B/IRQ2/ADCNV2-B/ DSMCLK3-C
A6	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108	VLO
A7	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/ET1_EXOUT/QIO2-B/ SDHI_D2-B/MMC_D2-B/LCD_DATA22-B/IRQ2/ AN110	VSS_DCDC
A8	TRDATA5/P96/D22/A22/ET1_ERXD2/ CAT1_ERXD2	VCC_DCDC
A9	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/ET1_WOL/QIO3-B/ SDHI_D3-B/MMC_D3-B/LCD_DATA21-B/IRQ3/ AN111	P103/PIO_011/TMO3/GTADSM1/GTIOC13B/ CTS2#-B/SDA00-A/ET0_CRS-D/ CATI2CDATA-A/IRQ3
A10	TRDATA6/PG0/D24/ET1_RX_CLK/REF50CK1/ CAT1_RX_CLK	P104/PIO_012/TMRI2/GTIW-E/GTIOC14A/ RXD2-B/SMISO2-B/SSCL2-B/CTS3#-B/RTS3#-B/ SS3#-B/DE3-B/TXDB3-B/CTX2-A/ USB0_OVRCURA-DS/USBHS_VBUS/ ET0_TXD0-B/RMII0_TXD0-B/CAT0_ETXD0-B/ CATLEDSTER-C/PIXD0-A/IRQ4/ADST0-A/ DSMCLK1-C/PCINA0
A11	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ ET1_RX_ER/RMII1_RX_ER/CAT1_RX_ER/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B/IRQ7/AN107	CLKOUT/P106/PIO_014/TMO2/RTCOUT/GTIU-D/ GTIOC15A/POEGB/RXD3-B/SMISO3-B/ SSCL3-B/SCLHS2-A/ET0_TXD2-B/ CAT0_ETXD2-B/CATI2CCLK-B/SD0DAT2-C/ PIXD2-A/IRQ30-DS/ADTRG0#/PCINA1

224-Pin LFBGA	RX72M	RX74M
A12	P61/SDCS#/D0[A0/D0]/CS1#/ET1_ERXD1/ RMII1_RXD1/CAT1_ERXD1	P200/PIO_016/TMRI0/GTETRGA/GTIOC3A/ GTIOC14A/CTS6#-A/RTS6#-A/SS6#-A/ DE6-A/TXDB6-A/MOSI0-C/SDAHS1-A/ USB0_ID/SSIRXD0/ET0_TX_EN-B/ RMII0_TX_EN-B/CAT0_TX_EN-B/ SD0CMD-C/PIXD4-A/IRQ8/ADTRG2#/PCINZ1
A13	P62/RAS#/D1[A1/D1]/CS2#/ET1_ERXD0/ RMII1_RXD0/CAT1_ERXD0	TCK/SWCLK/P301/PIO_025/TMCI3/GTCPPO11/ SCK0-A/CTS0#-A/TXDB0-A/SCK1-A/CTS1#-A/ TXDB1-A/RSPCK1-C/ET1_WOL-D/IRQ7
A14	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/MTIOC3B/ PO18/GTIOC1B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1	TDO/P302/PIO_026/TMRI3/GTCPPO12/TXD0-A/ SMOSI0-A/SSDA0-A/TXDA0-A/TXD1-A/ SMOSI1-A/SSDA1-A/TXDA1-A/MOSI1-C/ ET1_COL-D/IRQ4
A15	P70/SDCLK/CATLINKACT0	VSS
B1	AVSS0	PC04/PIO_028/D3-A/TMCI1/GTOWUP-B/ GTIOC9A/CTS8#-A/RTS8#-A/SS8#-A/DE8-A/ TXDB8-A/CTS11#-A/SSL00-A/AUDIO_CLK/ ET0_TXD3-A/RGMII0_TXD3-A/CAT0_ETXD3-A/ SD0DAT0-A/IRQ12/PCOUTB1
B2	AVCC0	PC01/PIO_025/D6-A/GTOULO-B/GTIOC7B/ SCK11-A/CTS11#-A/TXDB11-A/SSL02-A/ SDA00-C/ET0_TXD0-A/RMII0_TXD0-A/ RGMII0_TXD0-A/CAT0_ETXD0-A/SD0DAT3-A/ IRQ12/PCOUTB0
B3	P42/IRQ10-DS/AN002	PC05/PIO_029/D2-A/TMRI2/GTOWLO-B/ GTIOC9B/SCK8-A/CTS8#-A/TXDB8-A/ RSPCK0-A/SSIBCK0/ET0_TX_EN-A/ RMII0_TX_EN-A/RGMII0_TX_CTL-A/ CAT0_TX_EN-A/SD0DAT1-A/IRQ5/PCOUTZ1
B4	P46/IRQ14-DS/AN006	PC06/PIO_030/D1-A/TMCI2/TIC0/GTETRGC/ GTCPPO7/GTIOC15A/POEGB/RXD8-A/ SMISO8-A/SSCL8-A/MOSI0-A/SSILRCK0/ ET0_TX_ER-A/CATLINKACT0-A/SD0WP-A/ IRQ13/DSMCLK5-C/PDMCLK0-A
B5	P91/D17/A17/SCK7/ET1_COL/AN115/DSMDAT5	P803/PIO_059/CS3#-A/WR1#-B/BC1#-B/ GTIOC1B/POEGA/CTS10#-B/RTS10#-B/SS10#-B/ DE10-B/TXDB10-B/CTX2-D/USB0_ID/ ET0_MDC-B/CAT0_MDC-B/IRQ3/ADSYNC-B/ DSMDAT3-C
B6	VCC	VLO
B7	P94/D20/A20/ET1_ERXD0/RMII1_RXD0/ CAT1_ERXD0	VSS_DCDC
B8	TRDATA4/P95/D21/A21/ET1_ERXD1/ RMII1_RXD1/CAT1_ERXD1	VCC_DCDC
B9	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0-A/ ET1_MDIO/PMGI1_MDIO/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112	P102/PIO_010/TMCI1/GTADSM0/GTIOC13A/ SCL00-A/ET0_COL-D/CATI2CCLK-A/IRQ2
B10	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/ET1_RX_CLK/REF50CK1/ CAT1_RX_CLK/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/IRQ6/AN106	P105/PIO_013/TMCI2/GTIV-E/GTIOC14B/ TXD2-B/SMOSI2-B/SSDA2-B/TXDA2-B/SCK3-B/ CTS3#-B/TXDB3-B/CRX2-A/USB0_VBUS/ USBHS_OVRCURB/SSILRCK1/ET0_TXD1-B/ RMII0_TXD1-B/CAT0_ETXD1-B/CATLEDRUN-C/ PIXD1-A/IRQ29-DS/ADST1-A/DSMDAT1-C/ PCINB0
B11	VCC	P107/PIO_015/TMO1/GTIV-D/GTIOC15B/ POEGA/TXD3-B/SMOSI3-B/SSDA3-B/TXDA3-B/ SDAHS2-A/SSITXD0/ET0_TXD3-B/ CAT0_ETXD3-B/CATI2CDATA-B/SD0DAT3-C/ PIXD3-A/IRQ31-DS/ADTRG1#/PCINB1

224-Pin LFBGA	RX72M	RX74M
B12	P63/CAS#/D2[A2/D2]/CS3#/ET1_ETXD1/ RMII1_TXD1/CAT1_ETXD1	P201/PIO_017/TMCI0/GTIW-D/GTIOC3B/ GTIOC14B/SCK6-A/CTS6#-A/TXDB6-A/ MISO0-C/SCLHS1-A/USB0_EXICEN/SSILRCK0/ ET0_RX_ER-B/RMII0_RX_ER-B/ CAT0_RX_ER-B/SD0CLK-C/PIXD5-A/IRQ9/ PCINZ0
B13	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/PO23/ TIC3/GTIOC0B/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/MMC_D6-B/LCD_DATA14-B/ IRQ7-DS/AN100	TMS/SWDIO/P300/PIO_024/TMO1/GTCPPO10/ CTS0#-A/RTS0#-A/SS0#-A/DE0-A/TXDB0-A/ CTS1#-A/RTS1#-A/SS1#-A/DE1-A/TXDB1-A/ SSL10-C/ET0_WOL-D/IRQ6
B14	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/CAT0_ERXD2/LCD_DATA12-B/ AN102	TDI/P303/PIO_027/TMCI2/GTCPPO13/RXD0-A/ SMISO0-A/SSCL0-A/RXD1-A/SMISO1-A/ SSCL1-A/MISO1-C/ET1_CRS-D/IRQ1
B15	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105	ETHPHYCLK/P304/PIO_028/ALE-C/WAIT#-B/ TMCI3/GTETRGD/GTCPPO0/POEGA/CTS0#-A/ CTS1#-A/USB0_VBUSEN/USBHS_ID/ ET0_INT-E/CATRESTOUT-D/IRQ0-DS/ADTRG0#
C1	AVSS1	PC00/PIO_024/D7-A/GTOUUP-B/GTIOC7A/ CTS11#-A/RTS11#-A/SS11#-A/DE11-A/ TXDB11-A/SSL01-A/SCL00-C/ET0_TX_CLK-A/ CAT0_TX_CLK-A/SD0DAT2-A/IRQ14/PCOUTA0
C2	AVCC1	PC02/PIO_026/D5-A/GTOVUP-B/GTIOC8A/ RXD11-A/SMISO11-A/SSCL11-A/SSL03-A/ SCLHS1-C/ET0_TXD1-A/RMII0_TXD1-A/ RGMII0_TXD1-A/CAT0_ETXD1-A/SD0CMD-A/ IRQ10/PCOUTZ0
C3	P05/SSILRCK1/IRQ13/DA1	PB06/PIO_022/D9-A/GTOWUP-A/GTIOC6A/ RXD9-A/SMISO9-A/SSCL9-A/ET0_RX_ER-A/ RMII0_RX_ER-A/CAT0_RX_ER-A/IRQ6
C4	P44/IRQ12-DS/AN004	PB05/PIO_021/D10-A/TMRI1/GTOVLO-A/ GTIOC5B/SCK9-A/CTS9#-A/TXDB9-A/ ET0_RX_DV-A/RMII0_CRS_DV-A/ RGMII0_RX_CTL-A/CAT0_RX_DV-A/IRQ13
C5	VSS	P800/PIO_056/CS1#-A/DQM0-B/GTIU-B/ GTIOC0A/POEGD/RXD10-B/SMISO10-B/ SSCL10-B/ET0_COL-B/CATLATCH0-A/ IRQ8/ADCNV0-B/DSMCLK4-C
C6	P90/D16/A16/TXD7/SMOSI7/SSDA7/ ET1_RX_DV/CAT1_RX_DV/AN114/DSMCLK5	VLO
C7	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/AN109	P100/PIO_008/CS1#-B/WAIT#-A/TMRI3/ CACREF/GTIU-E/GTADSM0/GTIOC12A/ CTS2#-B/RTS2#-B/SS2#-B/DE2-B/TXDB2-B/ CTS5#-B/USB0_OVRCURB-DS/USBHS_VBUS/ ET0_TX_ER-B/CATLINKACT0-B/CATLEDERR-C/ IRQ0/ADTRG2#/DSMCLK0-C
C8	VCC	VCC_DCDC
C9	TRSYNC1/P97/D23/A23/ET1_ERXD3/ CAT1_ERXD3	P804/PIO_060/GTADSM0/GTIOC15A/CTS5#-B/ RTS5#-B/SS5#-B/DE5-B/TXDB5-B/SSL21-B/ CTX0-D/USB0_OVRCURA/USBHS_OVRCURA/ ET0_TX_EN-C/RMII0_TX_EN-C/CAT0_TX_EN-C/ PCKO-D/IRQ4/DSMCLK0-F/PCINA0
C10	P60/CS0#/ET1_TX_EN/RMII1_TXD_EN/ CAT1_TX_EN	P805/PIO_061/GTADSM1/GTIOC15B/SCK5-B/ CTS5#-B/TXDB5-B/SSL22-B/CRX0-D/ USB0_VBUSEN/USBHS_VBUSEN/ET0_TXD0-C/ RMII0_TXD0-C/CAT0_ETXD0-C/HSYNC-D/ IRQ5/ADSYNC-C/DSMDAT0-F/PCINB0

224-Pin LFBGA	RX72M	RX74M
C11	P64/WE#/D3[A3/D3]/CS4#/ET1_ETXD0/ RMII1_TXD0/CAT1_ETXD0	P114/PIO_046/GTCPPO14/TXD12-B/SMOSI12-B/ SSDA12-B/TXDA12-B/SSL23-C/ET1_TX_ER-C/ CATLINKACT1-C/PIXD6-D/IRQ22/ADST2-D/ DSMCLK0-H
C12	VSS	P111/PIO_043/GTCPPO11/CTS12#-B/CTS9#-C/ RTS9#-C/SS9#-C/DE9-C/TXDB9-C/SSL20-C/ ET0_RXD1-C/RMII0_RXD1-C/CAT0_ERXD1-C/ SD0DAT7-C/PIXD3-D/IRQ19
C13	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ET0_RX_CLK/ REF50CK0/CAT0_RX_CLK/LCD_DATA11-B/ IRQ5/AN103	P108/PIO_040/TIC0/GTCPPO8/SCK9-C/CTS9#-C/ TXDB9-C/RSPCK2-C/ET0_RX_DV-C/ RMII0_CRS_DV-C/CAT0_RX_DV-C/SD0DAT4-C/ PIXD0-D/IRQ16/ADCNV0-D/DSMCLK2-F
C14	P65/CKE/CS5#	P110/PIO_042/GTCPPO10/TXD9-C/SMOSI9-C/ SSDA9-C/TXDA9-C/MISO2-C/ET0_RXD0-C/ RMII0_RXD0-C/CAT0_ERXD0-C/SD0DAT6-C/ PIXD2-D/IRQ18/ADCNV2-D
C15	P66/DQM0/CS6#/MTIOC7D/GTIOC2B/CTX2	P113/PIO_045/GTCPPO13/SCK12-B/CTS12#-B/ TXDB12-B/SSL22-C/ET0_RXD3-C/ CAT0_ERXD3-C/PIXD5-D/IRQ21/ADST1-D/ DSMDAT1-H/PDMDAT0-D
D1	P45/IRQ13-DS/AN005	PG00/PIO_056/DQM1-A/WR1#-C/BC1#-C/ GTCPPO0/SCK8-C/CTS8#-C/TXDB8-C/ ET1_RX_CLK-A/RMII1_REF50CK-A/ RGMII1_RXC-A/CAT1_RX_CLK-A/IRQ8/ DSMCLK2-D
D2	P47/IRQ15-DS/AN007	PG02/PIO_058/DQM3-A/WR3#-C/BC3#-C/ GTIOC11A/TXD8-C/SMOSI8-C/SSDA8-C/ TXDA8-C/ET1_RX_ER-A/RMII1_RX_ER-A/ CAT1_RX_ER-A/IRQ10/DSMCLK1-D
D3	P03/SSIDATA1/IRQ11/DA0	PB04/PIO_020/D11-A/GTOVUP-A/GTIOC5A/ CTS4#-A/CTS9#-A/RTS9#-A/SS9#-A/DE9-A/ TXDB9-A/ET0_RX_CLK-A/RMII0_REF50CK-A/ RGMII0_RXC-A/CAT0_RX_CLK-A/IRQ4
D4	P40/IRQ8-DS/AN000	PB07/PIO_023/D8-A/GTOWLO-A/GTIOC6B/ TXD9-A/SMOSI9-A/SSDA9-A/TXDA9-A/ ET0_LINKSTA-A/CAT0_LINKSTA-A/IRQ15
D5	P01/TMCI0/RXD6/SMISO6/SSCL6/SSIBCK0/ CATLEDERR/QIO3-C/IRQ9/AN119	P502/PIO_034/WR2#-A/BC2#-A/A18-C/GTIOC3A/ TXD2-C/SMOSI2-C/SSDA2-C/TXDA2-C/SSL13-C/ CTX1-C/ET0_WOL-B/CATLEDRUN-A/ SD0DAT6-A/IRQ2/ADST2-C/DSMCLK1-E
D6	P02/TMCI1/SCK6/SSIBCK1/CATLEDSTER/ IRQ10/AN120	P500/PIO_032/WR#-A/WR0#-A/A16-C/ GTIOC2A/CTS2#-C/RTS2#-C/SS2#-C/DE2-C/ TXDB2-C/CTS7#-B/SSL11-C/CTX0-C/ ET0_LINKSTA-B/CAT0_LINKSTA-B/SD0DAT4-A/ IRQ0/ADST0-C/DSMCLK2-E
D7	P93/D19/A19/POE0#/CTS7#/RTS7#/SS7#/ ET1_LINKSTA/CAT1_LINKSTA/AN117/ DSMDAT4	P101/PIO_009/CS0#-A/ALE-B/TMCI3/GTETRGC/ GTADSM1/GTIOC12B/SCK2-B/CTS2#-B/ TXDB2-B/USB0_VBUS-DS/USBHS_EXICEN/ ET0_TX_CLK-B/CAT0_TX_CLK-B/ CAT0_LINKSTA-D/IRQ1/ADTRG1#/DSMDAT0-C
D8	VSS	P504/PIO_036/TMCI1/GTETRGA/GTIOC4A/ CTS2#-C/RXD7-B/SMISO7-B/SSCL7-B/MOSI2-B/ ET0_TX_ER-C/GPTP_CAPTURE0/ CATLINKACT0-C/IRQ4/DSMCLK0-E
D9	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/MTCLKA/ POE10#/SSLC1-A/ET1_MDC/PMGI1_MDC/ QSPCLK-B/SDHI_CLK-B/MMC_CLK-B/ LCD_DATA19-B/IRQ5/AN113	P506/PIO_038/GTETRGC/GTIOC5A/POEGD/ SCK7-B/CTS7#-B/TXDB7-B/RSPCK2-B/ ET0_TXD2-C/GPTP0_PPS/CAT0_ETXD2-C/IRQ6

224-Pin LFBGA	RX72M	RX74M
D10	TRDATA7/PG1/D25/ET1_RX_ER/RMII1_RX_ER/ CAT1_RX_ER	P806/PIO_062/GTCPPO7/GTIOC14A/RXD5-B/ SMISO5-B/SSCL5-B/SSL23-B/CTX1-D/ ET0_TXD1-C/RMII0_TXD1-C/CAT0_ETXD1-C/ VSYNC-D/IRQ14/DSMCLK1-F/PCINA1
D11	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/GTIOC2B/ SCK12/SSLB1-B/MMC_D4-B/LCD_DATA16-B/ ANEX0	P109/PIO_041/TOC0/GTCPPO9/RXD9-C/ SMISO9-C/SSCL9-C/MOSI2-C/ET0_RX_CLK-C/ RMII0_REF50CK-C/CAT0_RX_CLK-C/ SD0DAT5-C/PIXD1-D/IRQ17/ADCNV1-D/ DSMDAT2-F
D12	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/CTS12#/RTS12#/SS12#/ ET0_ERXD3/CAT0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101	P115/PIO_047/GTCPPO15/RXD12-B/ SMISO12-B/SSCL12-B/ET1_TX_CLK-C/ CAT1_TX_CLK-C/PIXD7-D/IRQ23/DSMDAT0-H
D13	VSS	P112/PIO_044/GTCPPO12/CTS12#-B/RTS12#-B/ SS12#-B/DE12-B/TXDB12-B/CTS9#-C/SSL21-C/ ET0_RXD2-C/CAT0_ERXD2-C/PIXD4-D/IRQ20/ ADST0-D/DSMCLK1-H/PDMCLK0-D
D14	TRDATA0/PG2/D26/ET1_TX_CLK/ CAT1_TX_CLK	VSS
D15	P67/DQM1/CS7#/MTIOC7C/GTIOC1B/CRX2/ EPLSOUT1/CATSYNC1/IRQ15	VCC
E1	VCL	PG01/PIO_057/DQM0-A/WR#-C/WR0#-C/ GTCPPO1/RXD8-C/SMISO8-C/SSCL8-C/ ET1_RX_DV-A/RMII1_CRS_DV-A/ RGMII1_RX_CTL-A/CAT1_RX_DV-A/IRQ9/ DSMDAT2-D
E2	VSS	PG03/PIO_059/DQM2-A/WR2#-C/BC2#-C/ GTIOC11B/CTS8#-C/RTS8#-C/SS8#-C/DE8-C/ TXDB8-C/ET0_INT-A/GPTP_MATCH1/IRQ11/ DSMDAT1-D
E3	P00/TMRI0/TXD6/SMOSI6/SSDA6/AUDIO_CLK/ CATLATCH1/QIO2-C/IRQ8/AN118	PB02/PIO_018/D13-A/GTOUUP-A/GTIOC4A/ CTS4#-A/RTS4#-A/SS4#-A/DE4-A/TXDB4-A/ CTS9#-A/ET0_RXD2-A/RGMII0_RXD2-A/ CAT0_ERXD2-A/IRQ2
E4	P43/IRQ11-DS/AN003	PB03/PIO_019/D12-A/TMO0/GTOULO-A/ GTIOC4B/SCK4-A/CTS4#-A/TXDB4-A/ ET0_RXD3-A/RGMII0_RXD3-A/CAT0_ERXD3-A/ IRQ3
E5	P07/IRQ15/ADTRG0#	VCC
E6	PN0/ET1_ETXD2/CAT1_ETXD2	P501/PIO_033/WR1#-A/BC1#-A/A17-C/ GTIOC2B/SCK2-C/CTS2#-C/TXDB2-C/SSL12-C/ CRX0-C/ET0_INT-B/CATLEDSTER-A/ SD0DAT5-A/IRQ1/ADST1-C/DSMDAT2-E
E7	PQ0/SCK11/ET1_CRS/RMII1_CRS_DV/ CAT1_RX_DV	P503/PIO_035/WR3#-A/BC3#-A/A19-C/ GTIOC3B/RXD2-C/SMISO2-C/SSCL2-C/CRX1-C/ USB0_OVRCURB/SSIRXD0/ET1_WOL-B/ CATLEDERR-A/SD0DAT7-A/IRQ3/DSMDAT1-E
E8	PQ1/SMISO11/SSCL11/RXD11/ET1_COL	P505/PIO_037/TMO3/GTETRGB/GTIOC4B/ TXD7-B/SMOSI7-B/SSDA7-B/TXDA7-B/MISO2-B/ ET0_TX_CLK-C/GPTP_MATCH0/ CAT0_TX_CLK-C/IRQ10/DSMDAT0-E
E9	PQ3/RTS11#/CTS11#/SS11#/ET1_TX_ER	P507/PIO_039/GTETRGD/GTIOC5B/POEGC/ CTS7#-B/RTS7#-B/SS7#-B/DE7-B/TXDB7-B/ SSL20-B/ET0_TXD3-C/GPTP1_PPS/ CAT0_ETXD3-C/IRQ7

224-Pin LFBGA	RX72M	RX74M
E10	PQ5/ET1_ETXD0/RMII1_TXD0/CAT1_ETXD0	P807/PIO_063/GTCPPO4/GTIOC14B/POEGD/ TXD5-B/SMOSI5-B/SSDA5-B/TXDA5-B/CRX1-D/ ET0_RX_ER-C/RMII0_RX_ER-C/ CAT0_RX_ER-C/PIXCLK-D/IRQ15/ DSMDAT1-F/PCINB1
E11	PQ4/ET1_RX_CLK/REF50CK1/CAT1_RX_CLK	PF02/PIO_050/CS6#-B/BREQ#-C/GTCPPO1/ GTIOC7A/RXD0-C/SMISO0-C/SSCL0-C/RXD7-C/ SMISO7-C/SSCL7-C/ET1_TXD2-C/ CAT1_ETXD2-C/IRQ2/ADSYNC-D/DSMCLK3-F
E12	VCC	PF04/PIO_052/CS4#-B/GTCPPO3/GTIOC8A/ SCK0-C/CTS0#-C/TXDB0-C/SCK7-C/CTS7#-C/ TXDB7-C/ET1_TXD0-C/RMII1_TXD0-C/ CAT1_ETXD0-C/IRQ4/DSMCLK4-F
E13	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/AN104	PF03/PIO_051/CS7#-B/BACK#-C/GTCPPO2/ GTIOC7B/TXD0-C/SMOSI0-C/SSDA0-C/ TXDA0-C/TXD7-C/SMOSI7-C/SSDA7-C/ TXDA7-C/ET1_TXD3-C/CAT1_ETXD3-C/IRQ3/ DSMDAT3-F
E14	TRCLK/PG5/D29/ET1_ETXD2/CAT1_ETXD2	PF00/PIO_048/GTCPPO14/USB0_DP/IRQ0
E15	TRSYNC/PG4/D28/ET1_ETXD1/RMII1_TXD1/ CAT1_ETXD1	PF01/PIO_049/GTCPPO15/USB0_DM/IRQ1
F1	XCIN	PA05/PIO_013/A2-A/GTIOC2B/GTIOC12B/ SCK10-A/CTS10#-A/TXDB10-A/RSPCK0-B/ ET1_TXD2-A/RGMII1_TXD2-A/CAT1_ETXD2-A/ IRQ5/PCINA0
F2	VBATT	ETHPHYCLK/PA07/PIO_015/A0-A/BC0#-A/ DQM1-B/GTIOC3B/GTIOC13B/RXD10-A/ SMISO10-A/SSCL10-A/MISO0-B/ET1_TX_ER-A/ CATLINKACT1-A/IRQ7/PCINB0
F3	TRST#/PF4	PB01/PIO_017/D14-A/TMCI0/GTETRGB/ GTCPPO4/GTIOC14B/POEGA/TXD4-A/ SMOSI4-A/SSDA4-A/TXDA4-A/ET0_RXD1-A/ RMII0_RXD1-A/RGMII0_RXD1-A/ CAT0_ERXD1-A/IRQ4-DS/DSMDAT2-A/PCINB1
F4	PK4/GTADSM0/SSLB1/ET0_ERXD2/ CAT0_ERXD2	PB00/PIO_016/D15-A/GTETRGA/GTADSM0/ GTIOC14A/POEGC/RXD4-A/SMISO4-A/ SSCL4-A/ET0_RXD0-A/RMII0_RXD0-A/ RGMII0_RXD0-A/CAT0_ERXD0-A/IRQ12/ ADST2-A/DSMCLK2-A/PCINA1
F5	PK5/GTADSM1/SSLB2/ET0_ERXD3/ CAT0_ERXD3	VSS
F6	EMLE	VCL
F7	PK6/GTIOC1A/SSLB3/CATLINKACT0	VSS
F8	PN1/ET1_ETXD3/CAT1_ETXD3	VCC
F9	PQ6/ET1_ETXD1/RMII1_TXD1/CAT1_ETXD1	VSS
F10	VSS	VSS
F11	PM1/TOC3/GTETRGB/SMISO10/SSCL10/ RXD10/ET1_ERXD1/RMII1_RXD1/CAT1_ERXD1/ SDHI_CMD-D/QSSL-A	PF05/PIO_053/CS5#-B/GTCPPO5/GTIOC8B/ POEGD/CTS7#-C/RTS7#-C/SS7#-C/DE7-C/ TXDB7-C/SSL01-C/ET1_TXD1-C/RMII1_TXD1-C/ CAT1_ETXD1-C/IRQ5/DSMDAT4-F
F12	PA0/DQM2/BC0#/A0/MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/CAT0_TX_EN/ CATLEDRUN/LCD_DATA8-B	P202/PIO_018/CS3#-B/BREQ#-A/TMO0/ GTOUUP-D/GTIOC0A/GTIOC4A/TXD6-A/ SMOSI6-A/SSDA6-A/TXDA6-A/RSPCK0-C/ SCL00-B/CTX2-B/USB0_OVRCURA/ USBHS_EXICEN/AUDIO_CLK/ET0_RX_DV-B/ RMII0_CRS_DV-B/CAT0_RX_DV-B/ CATI2CCLK-C/SD0DAT0-C/PIXD6-A/IRQ15/ DSMCLK3-B/PDMCLK0-B

224-Pin LFBGA	RX72M	RX74M
F13	TRDATA1/PG3/D27/ET1_ETXD0/RMII1_TXD0/ CAT1_ETXD0	P203/PIO_019/CS2#-B/BACK#-A/GTOULO-D/ GTIOC0B/GTIOC4B/RXD6-A/SMISO6-A/ SSCL6-A/CTS3#-B/SSL00-C/SDA00-B/CRX2-B/ USB0_OVRCURB/USBHS_ID/SSIBCK0/ ET0_RX_CLK-B/RMII0_REF50CK-B/ CAT0_RX_CLK-B/CATI2CDATA-C/SD0DAT1-C/ PIXD7-A/IRQ3/DSMDAT3-B/PDMDAT0-B
F14	TRDATA2/PG6/D30/ET1_ETXD3/CAT1_ETXD3	VCC_USB
F15	TRDATA3/PG7/D31/ET1_TX_ER	VSS_USB
G1	XCOUT	PA04/PIO_012/A3-A/TMRI0/GTIOC2A/ GTIOC12A/CTS10#-A/RTS10#-A/SS10#-A/ DE10-A/TXDB10-A/SSL00-B/ET1_TXD1-A/ RMII1_TXD1-A/RGMII1_TXD1-A/CAT1_ETXD1-A/ IRQ5-DS/PCINZ0
G2	VSS	PA06/PIO_014/A1-A/DQM2-B/TMCI3/GTIOC3A/ GTIOC13A/TXD10-A/SMOSI10-A/SSDA10-A/ TXDA10-A/MOSI0-B/ET1_TXD3-A/ RGMII1_TXD3-A/CAT1_ETXD3-A/IRQ14/PCINZ1
G3	VCC	PG05/PIO_061/A10-A/GTIOC12B/RXD3-C/ SMISO3-C/SSCL3-C/ET0_MDIO-A/ CAT0_MDIO-A/IRQ13
G4	MD/FINED	PG07/PIO_063/A8-A/GTIOC13B/CTS3#-C/ RTS3#-C/SS3#-C/DE3-C/TXDB3-C/ET0_CRS-A/ IRQ15
G5	PJ5/POE8#/CTS2#/RTS2#/SS2#/SSIRXD0/ EPLSOUT0/CATSYNC0/QMI-C/QIO1-C	PF09/PIO_017/A20-A/A16-D/CTS12#-C/ GPTP_CAPTURE1/XSPI1_INT0#-A/ XSPI1_ECS0#-A/IRQ17
G6	PF5/WAIT#/SSILRCK0/CATLATCH0/IRQ4	VSS
G7	RES#	VCL
G8	PQ2/SMOSI11/SSDA11/TXD11/ET1_RX_DV/ CAT1_RX_DV	VSS
G9	PN2/ET1_TX_CLK/CAT1_TX_CLK	VCL
G10	VCC	VCL
G11	PM0/TIC3/GTETRGA/SCK10/ET1_ERXD0/ RMII1_RXD0/CAT1_ERXD0/SDHI_CLK-D/ QSPCLK-A	CLKOUT/P205/PIO_021/A21-C/CS6#-C/ GTOVLO-D/GTIOC1B/GTIOC5B/SCK1-B/ CTS1#-B/TXDB1-B/RSPCK1-B/SDAHS1-B/ CRX0-A/USB0_VBUS/USBHS_VBUSEN/ SSIRXD1/ET0_RXD1-B/RMII0_RXD1-B/ CAT0_ERXD1-B/SD0CD-C/HSYNC-A/IRQ5/ ADTRG0#/DSMDAT4-B/PCOUTB1
G12	PA1/DQM3/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/IRQ11	ETHPHYCLK/P204/PIO_020/A20-C/CS7#-C/ TMRI1/GTOVUP-D/GTIOC1A/GTIOC5A/ CTS1#-B/RTS1#-B/SS1#-B/DE1-B/TXDB1-B/ SSL10-B/SCLHS1-B/CTX0-A/USB0_VBUSEN/ USBHS_VBUS-DS/SSIBCK1/ET0_RXD0-B/ RMII0_RXD0-B/CAT0_ERXD0-B/SD0WP-C/ PIXCLK-A/IRQ12/DSMCLK4-B/PCOUTA1
G13	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/CATLINKACT1/ LCD_DATA6-B	VCC_USBHS
G14	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/ CAT0_MDIO/PMGI0_MDIO/LCD_DATA5-B/ IRQ6-DS	USBHS_DP
G15	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/ TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC/ CAT0_MDC/CATIRQ/PMGI0_MDC/ LCD_DATA4-B/IRQ5-DS	USBHS_DM

224-Pin LFBGA	RX72M	RX74M
H1	XTAL/P37	PA02/PIO_010/A5-A/GTIW-A/GTIOC1A/ GTIOC11A/TXD5-A/SMOSI5-A/SSDA5-A/ TXDA5-A/SSL03-B/ET1_TX_CLK-A/ CAT1_TX_CLK-A/IRQ10/ADCNV2-A/DSMCLK1-A
H2	P34/MTIOC0A/TMCI3/PO12/POE10#/SCK6/ SCK0/ET0_LINKSTA/CAT0_LINKSTA/IRQ4/ DSMDAT0	PA03/PIO_011/A4-A/GTIOC1B/GTIOC11B/ RXD5-A/SMISO5-A/SSCL5-A/ET1_TXD0-A/ RMII1_TXD0-A/RGMII1_TXD0-A/CAT1_ETXD0-A/ IRQ6-DS/ADSYNC-A/DSMDAT1-A
H3	UPSEL/P35/NMI	PG06/PIO_062/A9-A/GTIOC13A/TXD3-C/ SMOSI3-C/SSDA3-C/TXDA3-C/ET0_COL-A/ IRQ14
H4	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/ POE4#/POE11#/RXD6/SMISO6/SSCL6/RXD0/ SMISO0/SSCL0/CRX0/PCKO/IRQ3-DS/ DSMCLK0	PG04/PIO_060/A11-A/GTIOC12A/SCK3-C/ CTS3#-C/TXDB3-C/ET0_MDC-A/CAT0_MDC-A/ IRQ12
H5	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCIC2/ RTCOUT/POE0#/POE10#/TXD6/SMOSI6/SSDA6/ TXD0/SMOSI0/SSDA0/CTX0/USB0_VBUSEN/ VSYNC/IRQ2-DS	PF08/PIO_016/A21-A/A17-D/GTCPPO12/ POEGA/XSPI1_RESET0#-A/IRQ16
H6	BSCANP	VCC
H7	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/SS6#/ CTS0#/RTS0#/SS0#/SSITXD0/ET0_EXOUT/ CATRESTOUT/QMO-C/QIO0-C	VSS
H8	PQ7/ET1_TX_EN/RMII1_TXD_EN/CAT1_TX_EN	VCL
H9	PN3/ET1_RX_ER/RMII1_RX_ER/CAT1_RX_ER	VSS
H10	P73/CS3#/PO16/ET0_WOL/LCD_EXTCLK-A	VCL
H11	PL0/TIC2/GTETRGA/SCK9/RSPCKC/ ET0_ERXD0/RMII0_RXD0/CAT0_ERXD0	P206/PIO_022/A22-C/CS5#-C/TMO3/RTCOUT/ GTOWUP-D/GTIOC2A/GTIOC6A/CTS6#-A/ TXD1-B/SMOSI1-B/SSDA1-B/TXDA1-B/MOSI1-B/ SCLHS2-B/CTX1-A/USB0_EXICEN/ USBHS_OVRCURA-DS/SSITXD1/ET0_RXD2-B/ CAT0_ERXD2-B/VSYNC-A/IRQ2-DS/ADTRG1#/ DSMCLK5-B/PCOUTZ1
H12	VCC	AVSS_USBHS
H13	VSS	USBHS_RREF
H14	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/RTS5#/SS5#/ MOSIA-B/ET0_EXOUT/CATRESTOUT/ LCD_DATA2-B	VSS_USBHS
H15	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/CAT0_LINKSTA/ LCD_DATA3-B	VCC
J1	EXTAL/P36	ETHPHYCLK/PA00/PIO_008/A7-A/CACREF/ GTIU-A/GTIOC0A/GTIOC10A/CTS10#-A/ CTS5#-A/RTS5#-A/SS5#-A/DE5-A/TXDB5-A/ SSL01-B/RGMII1_TXC-A/CATIRQ-A/IRQ1-DS/ ADCNV0-A/DSMCLK0-A
J2	TDI/PF2/RXD1/SMISO1/SSCL1/CATI2CCLK	PA01/PIO_009/A6-A/GTIV-A/GTIOC0B/ GTIOC10B/SCK5-A/CTS5#-A/TXDB5-A/SSL02-B/ ET1_TX_EN-A/RMII1_TX_EN-A/ RGMII1_TX_CTL-A/CAT1_TX_EN-A/IRQ11/ ADCNV1-A/DSMDAT0-A
J3	TMS/PF3	P703/PIO_051/ALE-A/WR2#-B/BC2#-B/CACREF/ GTETRGB/GTIOC11B/CTS4#-B/RTS4#-B/ SS4#-B/DE4-B/TXDB4-B/ET1_LINKSTA-A/ CAT1_LINKSTA-A/XSPI1_RESET0#-B/PCKO-C/ IRQ8/DSMDAT4-D

224-Pin LFBGA	RX72M	RX74M
J4	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/ RTS1#/SS1#/SSLB0-A/ET1_MDC/PMGI1_MDC/ IRQ1-DS	PF06/PIO_054/A23-A/A19-D/GTCPPO6/ GTIOC9A/POEGC/CTS0#-C/RTS0#-C/SS0#-C/ DE0-C/TXDB0-C/CTS7#-C/SSL02-C/ XSPI1_CS1#-A/XSPI1_WP0#-A/IRQ6/ DSMCLK5-F
J5	P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/MISOB-A/ET1_MDIO/ PMGI1_MDIO/IRQ0-DS	PF07/PIO_055/A22-A/A18-D/GTCPPO11/ GTIOC9B/SSL03-C/XSPI1_RSTO0#-A/IRQ7/ DSMDAT5-F
J6	PH2/GTETRGC/SMOSI7/SSDA7/TXD7/MISOA/ CATI2CDATA	VSS
J7	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/ PO13/GTETRGA/RXD1/SMISO1/SSCL1/SCK3/ CRX1-DS/SSILRCK1/CATLEDRUN/PIXD0/IRQ5	VCL
J8	P53*1/BCLK	VSS
J9	PK3/GTETRGD/RTS8#/CTS8#/SS8#/SSLB0/ ET0_TX_ER	VCL
J10	PL1/TOC2/GTETRGB/SMISO9/SSCL9/RXD9/ MOSIC/ET0_ERXD1/RMII0_RXD1/CAT0_ERXD1	VSS
J11	PN5/ET1_MDC/PMGI1_MDC/QSSL-C	P207/PIO_023/A23-C/CS4#-C/TMRI3/ GTOWLO-D/GTIOC2B/GTIOC6B/RXD1-B/ SMISO1-B/SSCL1-B/MISO1-B/SDAHS2-B/ CRX1-A/USB0_ID/USBHS_OVRCURB-DS/ ET0_RXD3-B/CAT0_ERXD3-B/PCKO-A/ IRQ3-DS/ADTRG2#/DSMDAT5-B
J12	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/ PO25/TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/ SSDA6/ET0_ERXD0/RMII0_RXD0/CAT0_ERXD0/ LCD_TCON3-B/IRQ4-DS	P305/NMI/IRQ0
J13	P71/A18/CS1#/ET0_MDIO/CAT0_MDIO/ PMGI0_MDIO/DSMCLK3	AVCC_USBHS
J14	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/ET0_ERXD1/ RMII0_RXD1/CAT0_ERXD1/LCD_DATA0-B/ IRQ12	XTAL/P307
J15	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B	EXTAL/P306
K1	CLKOUT25M/PH7/GTIOC0B	P707/PIO_055/WE#-A/CS7#-A/GTIOC13B/ TXD11-B/SMOSI11-B/SSDA11-B/TXDA11-B/ ET1_RXD3-A/RGMII1_RXD3-A/CAT1_ERXD3-A/ XSPI1_RESET1#-B/IRQ7/DSMDAT0-D
K2	CLKOUT/PH6/GTIOC0A/SSLA3/CATLATCH1	P706/PIO_054/CAS#-A/CS6#-A/GTIOC13A/ RXD11-B/SMISO11-B/SSCL11-B/ET1_RXD2-A/ RGMII1_RXD2-A/CAT1_ERXD2-A/ XSPI1_WP1#-B/IRQ14/ADCNV2-C/DSMCLK0-D
K3	PH4/GTADSM0/SSLA1/CATLEDSTER	P702/PIO_050/RD#-A/DQM3-B/GTETRGA/ GTIOC11A/SCK4-B/CTS4#-B/TXDB4-B/ ET1_CRS-E/CATSYNC1-A/XSPI1_WP0#-B/ XSPI1_RESET1#-C/HSYNC-C/IRQ10/ADST2-B/ DSMCLK4-D
K4	PH5/GTADSM1/SSLA2/CATLATCH0	P605/PIO_013/CS2#-C/D18-B/GTIOC6B/RXD9-B/ SMISO9-B/SSCL9-B/SSL02-D/ET1_TXD3-B/ ET_TAS_STA1/CAT1_ETXD3-B/XSPI0_INT0#-A/ XSPI0_ECS0#-A/IRQ13/DSMDAT4-A
K5	TDO/PF0/TXD1/SMOSI1/SSDA1/CATI2CDATA	VSS
K6	PH1/TOC0/GTETRGB/SMISO7/SSCL7/RXD7/ MOSIA/CATI2CCLK	VCC
K7	P10/ALE/MTIC5W/TMRI3/IRQ0	VSS
K8	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A/CATLEDERR	VCC2

224-Pin LFBGA	RX72M	RX74M
K9	PK1/TOC1/GTETRGB/SMISO8/SSCL8/RXD8/ MOSIB/ET0_COL	VCL
K10	PL3/GTETRGD/RTS9#/CTS9#/SS9#/SSLC0/ ET0_RX_CLK/REF50CK0/CAT0_RX_CLK	VSS
K11	PM2/GTETRGC/SMOSI10/SSDA10/TXD10/ ET1_ERXD2/CAT1_ERXD2/SDHI_D0-D/ QMO-A/QIO0-A	P310/PIO_058/RTCIC0/CACREF/GTETRGB/ GTCPPO1/POEGC/CTS0#-C/CTS1#-B/SSL11-B/ SSITXD0/ET1_INT-E/CATIRQ-D/IRQ18/ ADTRG0#/TAMPI0
K12	VSS	P311/PIO_059/BREQ#-B/RTCIC1/GTETRGC/ GTCPPO14/POEGD/CTS7#-A/SSL12-B/ SSIRXD0/ET0_WOL-C/IRQ19/ADTRG1#/ DSMCLK2-C/TAMPI1
K13	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/SCK11/ET0_ETXD0/ RMII0_TXD0/CAT0_ETXD0/LCD_CLK-B	MD/P315
K14	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK4/SCK6/ET0_RX_ER/ RMII0_RX_ER/CAT0_RX_ER/LCD_TCON1-B	VSS
K15	P72/A19/CS2#/ET0_MDC/CAT0_MDC/ PMGI0_MDC/LCD_DATA23-A/DSMDAT3	VSS
L1	PH3/GTETRGD/RTS7#/CTS7#/SS7#/SSLA0/ CATLEDERR	P705/PIO_053/RAS#-A/CS5#-A/GTIOC12B/ SCK11-B/CTS11#-B/TXDB11-B/ET1_RXD1-A/ RMII1_RXD1-A/RGMII1_RXD1-A/ CAT1_ERXD1-A/XSPI1_RSTO1#-B/IRQ13/ ADCNV1-C/DSMDAT5-D
L2	P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A/ET1_WOL/CATIRQ	P704/PIO_052/SDCS#-A/CS4#-A/GTIOC12A/ CTS4#-B/CTS11#-B/RTS11#-B/SS11#-B/DE11-B/ TXDB11-B/ET1_RXD0-A/RMII1_RXD0-A/ RGMII1_RXD0-A/CAT1_ERXD0-A/ XSPI1_INT1#-B/XSPI1_ECS1#-B/IRQ12/ ADCNV0-C/DSMCLK5-D
L3	TCK/PF1/SCK1	P604/PIO_012/CS3#-C/D19-B/GTIOC6A/ TXD9-B/SMOSI9-B/SSDA9-B/TXDA9-B/SSL01-D/ ET1_TXD2-B/ET_TAS_STA0/CAT1_ETXD2-B/ XSPI0_CS1#-A/XSPI0_RSTO0#-B/IRQ4/ DSMCLK4-A
L4	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/ TMRI1/PO4/SCK3/USB0_VBUSEN/SSIBCK1/ SDHI_WP/PIXCLK	P606/PIO_014/CS1#-C/D17-B/GTETRGA/ GTCPPO4/GTIOC15A/POEGC/SCK9-B/CTS9#-B/ TXDB9-B/SSL03-D/CTX2-C/ET1_TX_ER-B/ ET_TAS_STA2/CATLINKACT1-B/ XSPI0_RESET0#-A/IRQ14/DSMCLK5-A
L5	VCC	VCC2
L6	CLKOUT25M/PJ2/TXD8/SMOSI8/SSDA8/ SSLC3-B/LCD_TCON2-A	P904/PIO_004/GTCPPO0/POEGC/TXD6-B/ SMOSI6-B/SSDA6-B/TXDA6-B/ET0_COL-E/ GPTP_PTPOUT0/IRQ12
L7	VCC	P906/PIO_006/GTCPPO2/POEGA/SCK6-B/ CTS6#-B/TXDB6-B/ET0_MDC-C/ GPTP_PTPOUT2/IRQ14
L8	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A/ CATLEDSTER	P407/PIO_055/IRQ15-DS/AN007
L9	P81/EDACK0/MTIOC3D/PO27/GTIOC0B/ SMISO10/SSCL10/RXD10/ET0_ETXD0/ RMII0_TXD0/CAT0_ETXD0/CATI2CCLK/QIO3-A/ SDHI_CD/MMC_D3-A/LCD_DATA13-A	P406/PIO_054/IRQ14-DS/AN006
L10	PL7/GTIOC2B/ET0_MDIO/CAT0_MDIO/ PMGI0_MDIO	P215/PIO_055/GTCPPO13/CTS4#-C/CTS5#-C/ RTS5#-C/SS5#-C/DE5-C/TXDB5-C/USBHS_ID/ ET1_RXD3-C/CAT1_ERXD3-C/IRQ31/ PDMDAT0-E/PCINZ0

224-Pin LFBGA	RX72M	RX74M
L11	P77/CS7#/PO23/SMOSI11/SSDA11/TXD11/ET0_RX_ER/RMII0_RX_ER/CAT0_RX_ER/QSPCLK-A/SDHI_CLK-A/MMC_CLK-A/LCD_DATA17-A	P209/PIO_049/TOC1/GTETRGB/RXD4-C/SMISO4-C/SSCL4-C/MOSI1-D/ET1_RX_CLK-C/RMII1_REF50CK-C/CAT1_RX_CLK-C/IRQ25/PCINB1
L12	PN4/ET1_MDIO/PMGI1_MDIO/QSPCLK-C	P312/PIO_060/BACK#-B/RTCIC2/GTETRGD/GTCPPO15/POEGA/SSL13-B/SSILRCK0/ET1_WOL-C/IRQ20/ADTRG2#/DSMDAT2-C/TAMPI2
L13	VCC	VCC
L14	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/SS4#/CTS6#/RTS6#/SS6#/ET0_RX_CLK/REF50CK0/CAT0_RX_CLK/LCD_TCON2-B	XCIN/EXCIN/P309
L15	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/SS11#/CTS11#/RTS11#/ET0_TX_EN/RMII0_TXD_EN/CAT0_TX_EN/LCD_TCON0-B	XCOUT/P308
M1	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A/ET1_EXOUT/CATLINKACT1	ETHPHYCLK/P700/PIO_048/SDCLK-A/GTIOC10A/TXD4-B/SMOSI4-B/SSDA4-B/TXDA4-B/ET1_INT-A/CATRESTOUT-F/XSPI1_INT0#-B/XSPI1_ECS0#-B/PIXCLK-C/IRQ0/ADST0-B/DSMCLK3-D
M2	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/SDHI_D1-C/PIXD7	P701/PIO_049/CKE-A/WR3#-B/BC3#-B/GTIOC10B/RXD4-B/SMISO4-B/SSCL4-B/ET1_COL-E/CATLATCH1-A/XSPI1_RSTO0#-B/XSPI1_RESET0#-B/VSYNC-C/IRQ1/ADST1-B/DSMDAT3-D
M3	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/SSIDATA1/SDHI_CD/HSYNC/ADTRG0#	P607/PIO_015/CS0#-B/D16-B/GTETRGB/GTADSM0/GTIOC15B/POEGA/CTS8#-B/CTS9#-B/RTS9#-B/SS9#-B/DE9-B/TXDB9-B/CRX2-C/ET1_INT-B/ET_TAS_STA3/CATIRQ-B/XSPI0_RSTO0#-A/IRQ15/DSMDAT5-A
M4	VSS	P603/PIO_011/WE#-B/D20-B/GTIOC5B/CTS8#-B/RTS8#-B/SS8#-B/DE8-B/TXDB8-B/CTS9#-B/MISO0-D/ET1_TXD1-B/RMII1_TXD1-B/GPTP_PTPOUT3/CAT1_ETXD1-B/CATSYNC0-B/XSPI0_IO7-A/PCKO-B/IRQ3/DSMDAT3-A
M5	PJ0/MTIOC6B/SCK8/SSLC1-B/EPLSOUT0/CATSYNC0/LCD_DATA0-A	P907/PIO_007/GTCPPO3/POEGD/CTS6#-B/RTS6#-B/SS6#-B/DE6-B/TXDB6-B/CTS1#-C/ET0_MDIO-C/GPTP_PTPOUT3/XSPI0_WP0#-A/IRQ15
M6	P84/MTIOC6D/ET1_LINKSTA/CAT1_LINKSTA/LCD_DATA2-A	P905/PIO_005/GTCPPO1/POEGB/RXD6-B/SMISO6-B/SSCL6-B/ET0_CRS-E/GPTP_PTPOUT1/IRQ13
M7	VSS	P902/PIO_002/GTETRGC/GTCPPO8/SCK1-C/CTS1#-C/TXDB1-C/ET1_MDC-B/ET_TAS_STA2/CATRESTOUT-B/XSPI0_RESET1#-A/IRQ10/AN034
M8	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	P900/PIO_000/GTETRGA/GTCPPO5/RXD1-C/SMISO1-C/SSCL1-C/ET1_COL-B/ET_TAS_STA0/CATSYNC1-B/XSPI0_INT1#-A/XSPI0_ECS1#-A/IRQ0/AN032
M9	P83/EDACK1/MTIOC4C/GTIOC0A/SCK10/SS10#/CTS10#/ET0_CRS/RMII0_CRS_DV/CAT0_RX_DV/LCD_DATA8-A/DSMCLK1	P405/PIO_053/IRQ13-DS/AN005
M10	PK0/TIC1/GTETRGA/SCK8/RSPCKB/ET0_MDC/CAT0_MDC/PMGI0_MDC	P415/PIO_063/IRQ31/AN015/DA1
M11	PL5/GTADSM1/SSLC2/ET0_ETXD1/RMII0_TXD1/CAT0_ETXD1	P212/PIO_052/GTCPPO10/SCK5-C/CTS5#-C/TXDB5-C/SSL11-D/USBHS_OVRCURA/ET1_RX_DV-C/RMII1_CRS_DV-C/CAT1_RX_DV-C/IRQ28/ADTRG0#

224-Pin LFBGA	RX72M	RX74M
M12	PL6/GTIOC2A/SSLC3/ET0_TX_EN/ RMII0_TXD_EN/CAT0_TX_EN	P214/PIO_054/GTCPPO12/TXD5-C/SMOSI5-C/ SSDA5-C/TXDA5-C/SSL13-D/USBHS_EXICEN/ ET1_RXD2-C/CAT1_ERXD2-C/IRQ30/ADTRG2#/ PDMCLK0-E/PCINB0
M13	PM7/GTIOC3B/ET0_CRS/RMII0_CRS_DV/ CAT0_RX_DV/SDHI_WP	RES#
M14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/ SS5#/SSLA1-A/ET0_ERXD3/CAT0_ERXD3/ IRQ14	VSS
M15	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1/CAT0_ETXD1	VBATT/VCC
N1	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/GTIOC1A/SCK0/USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/PIXD6	PE07/PIO_047/A8-B/A20-C/TOC1/GTETRGD/ GTCPPO7/GTIOC10B/POEGD/ET1_LINKSTA-E/ CAT1_LINKSTA-D/CATRESTOUT-C/ XSPI1_CS0#-A/PIXD7-C/IRQ7
N2	PH0/TIC0/GTETRGA/SCK7/RSPCKA/ CATLEDRUN	PE04/PIO_044/A11-B/A23-C/GTOWUP-C/ GTIOC9A/CTS12#-A/SSL11-A/ET1_RXD2-D/ CAT1_ERXD2-D/CATLEDSTER-B/XSPI1_IO2-A/ XSPI1_WP0#-C/PIXD4-C/IRQ12
N3	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/ SSCL10/RXD10/CATLINKACT0/PIXD1	PE06/PIO_046/A9-B/A21-C/TIC1/GTETRGC/ GTADSM1/GTIOC10A/POEGB/SSL13-A/ ET1_RX_CLK-D/RMII1_REF50CK-D/ CAT1_RX_CLK-D/CATLEDERR-B/XSPI1_DS-A/ PIXD6-C/IRQ6
N4	P85/MTIOC6C/TIOCC0/LCD_DATA1-A	P602/PIO_010/CAS#-B/D21-B/GTIOC5A/SCK8-B/ CTS8#-B/TXDB8-B/MOSI0-D/ET1_TXD0-B/ RMII1_TXD0-B/GPTP_PTPOUT2/ CAT1_ETXD0-B/CATLATCH0-B/XSPI0_IO6-A/ HSYNC-B/IRQ2/ADTRG2#/DSMCLK3-A
N5	P13/WR2#/BC2#/MTIOC0B/TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/SSDA2/SDA0[FM+]/ LCD_TCON0-A/IRQ3/ADTRG1#	P601/PIO_009/RAS#-B/D22-B/GTIOC4B/RXD8-B/ SMISO8-B/SSCL8-B/RSPCK0-D/ET1_TX_EN-B/ RMII1_TX_EN-B/GPTP_PTPOUT1/ CAT1_TX_EN-B/CATSYNC1-D/XSPI0_IO5-A/ VSYNC-B/IRQ1/ADTRG1#
N6	PJ1/MTIOC6A/RXD8/SMISO8/SSCL8/SSLC2-B/ EPLSOUT1/CATSYNC1/LCD_TCON3-A	P600/PIO_008/SDCS#-B/D23-B/GTIOC4A/ TXD8-B/SMOSI8-B/SSDA8-B/TXDA8-B/SSL00-D/ ET1_TX_CLK-B/GPTP_PTPOUT0/ CAT1_TX_CLK-B/CATLATCH1-D/XSPI0_IO4-A/ PIXCLK-B/IRQ0/ADTRG0#
N7	CLKOUT25M/P56/EDACK1/MTIOC3C/TIOCA1/ SCK7/RSPCKC-B/LCD_DATA4-A/DSMDAT1	P903/PIO_003/GTETRGD/GTCPPO9/POEGD/ CTS6#-B/CTS1#-C/RTS1#-C/SS1#-C/DE1-C/ TXDB1-C/ET1_MDIO-B/ET_TAS_STA3/ CATIRQ-C/XSPI0_WP1#-A/IRQ11/AN035
N8	VCC	P901/PIO_001/GTETRGB/GTCPPO6/TXD1-C/ SMOSI1-C/SSDA1-C/TXDA1-C/ET1_CRS-B/ ET_TAS_STA1/CATLATCH1-B/ XSPI0_RSTO1#-A/XSPI0_RESET0#-B/IRQ9/ AN033
N9	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/ ET0_COL/MMC_D7-A/LCD_DATA9-A/IRQ14	P404/PIO_052/IRQ12-DS/AN004
N10	P80/EDREQ0/MTIOC3B/PO26/SCK10/RTS10#/ ET0_TX_EN/RMII0_TXD_EN/CAT0_TX_EN/ CATLATCH0/QIO2-A/SDHI_WP/MMC_D2-A/ LCD_DATA14-A	P414/PIO_062/IRQ30/AN014/DA0

224-Pin LFBGA	RX72M	RX74M
N11	PK2/GTETRGC/SMOSI8/SSDA8/TXD8/MISOB/ ET0_RX_DV/CAT0_RX_DV	P210/PIO_050/GTETRGC/TXD4-C/SMOSI4-C/ SSDA4-C/TXDA4-C/MISO1-D/ET1_RXD0-C/ RMII1_RXD0-C/CAT1_ERXD0-C/IRQ26/PCINZ1
N12	P76/CS6#/PO22/SMISO11/SSCL11/RXD11/ ET0_RX_CLK/REF50CK0/CAT0_RX_CLK/ QSSL-A/SDHI_CMD-A/MMC_CMD-A/ LCD_DATA18-A	P213/PIO_053/GTCPPO11/RXD5-C/SMISO5-C/ SSCL5-C/SSL12-D/USBHS_VBUSEN/ ET1_RX_ER-C/RMII1_RX_ER-C/ CAT1_RX_ER-C/IRQ29/ADTRG1#/PCINA0
N13	PM6/GTIOC3A/ET0_TX_CLK/CAT0_TX_CLK/ SDHI_CD	P208/PIO_048/TIC1/GTETRGA/SCK4-C/ CTS4#-C/TXDB4-C/RSPCK1-D/ET1_TX_EN-C/ RMII1_TX_EN-C/CAT1_TX_EN-C/IRQ24/PCINA1
N14	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/CAT0_ERXD2/ LCD_DATA22-A/IRQ12	P211/PIO_051/GTETRGD/CTS4#-C/RTS4#-C/ SS4#-C/DE4-C/TXDB4-C/CTS5#-C/SSL10-D/ USBHS_OVRCURB/ET1_RXD1-C/ RMII1_RXD1-C/CAT1_ERXD1-C/IRQ27
N15	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV/CAT0_RX_DV	P000/PIO_000/TMRI0/GTCPPO7/GTIOC10A/ POEGB/CTS0#-B/CTS7#-A/RTS7#-A/SS7#-A/ DE7-A/TXDB7-A/AUDIO_CLK/ET0_INT-D/ CATRESTOUT-E/IRQ16-DS/AN016/DSMCLK0-B
P1	PK7/GTIOC1B/CATLINKACT1	PE05/PIO_045/A10-B/A22-C/GTOWLO-C/ GTIOC9B/SSL12-A/ET1_RXD3-D/ CAT1_ERXD3-D/CATLEDRUN-B/ XSPI1_IO3-A/PIXD5-C/IRQ5
P2	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/SCK1/ TXD3/SMOSI3/SSDA3/SDA2-DS/SSITXD0/ EPLSOUT0/CATSYNC0/SDHI_D3-C/PIXD3/IRQ7/ ADTRG1#	PE03/PIO_043/A12-B/TOC3/GTOVLO-C/ GTIOC8B/CTS12#-A/RTS12#-A/SS12#-A/ DE12-A/TXDB12-A/MISO1-A/ET1_RXD1-D/ RMII1_RXD1-D/CAT1_ERXD1-D/SD0DAT7-B/ XSPI1_IO1-A/PIXD3-C/IRQ11
P3	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMD-C/PIXD4/IRQ8	PE02/PIO_042/A13-B/TIC3/GTOVUP-C/ GTIOC8A/RXD12-A/SMISO12-A/SSCL12-A/ MOSI1-A/ET1_RXD0-D/RMII1_RXD0-D/ CAT1_ERXD0-D/SD0DAT6-B/XSPI1_IO0-A/ PIXD2-C/IRQ7-DS
P4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/ PO15/GTETRGD/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/LCD_CLK-A/IRQ4	PD07/PIO_039/A16-B/D24-B/GTIW-C/ GTIOC3B/POEGA/TXD3-A/SMOSI3-A/SSDA3-A/ TXDA3-A/CTX1-B/ET1_LINKSTA-B/ CAT1_LINKSTA-B/SD0CD-B/XSPI0_CS0#-A/ XSPI0_RESET1#-B/PIXD7-B/IRQ7/AN031
P5	VCC_USB	PD05/PIO_037/A18-B/D26-B/GTIU-C/GTIOC2B/ POEGD/SCK3-A/CTS3#-A/TXDB3-A/SSL22-A/ CTX0-B/ET1_RX_DV-B/RMII1_CRS_DV-B/ CAT1_RX_DV-B/CATLEDSTER-D/SD0DAT1-B/ XSPI0_IO3-A/PIXD5-B/IRQ5/AN029
P6	VSS_USB	PD03/PIO_035/A20-B/D28-B/TOC2/GTIOC1B/ POEGA/TXD2-A/SMOSI2-A/SSDA2-A/TXDA2-A/ MISO2-A/ET1_RXD3-B/CAT1_ERXD3-B/ CAT0_MDIO-D/SD0CLK-B/XSPI0_IO1-A/ PIXD3-B/IRQ3/AN027
P7	P57/RXD7/SMISO7/SSCL7/SSLC0-B/ LCD_DATA3-A	PD02/PIO_034/A21-B/D29-B/TIC2/GTETRGB/ GTIOC1A/POEGB/RXD2-A/SMISO2-A/SSCL2-A/ MOSI2-A/ET1_RXD2-B/CAT1_ERXD2-B/ CAT0_MDC-D/SD0CMD-B/XSPI0_IO0-A/ PIXD2-B/IRQ2/AN026
P8	P11/MTIC5V/TMCI3/SCK2/EPLSOUT1/ CATSYNC1/LCD_DATA7-A/IRQ1	AVSS0
P9	VSS	VREFL0
P10	P82/EDREQ1/MTIOC4A/PO28/GTIOC2A/ SMOSI10/SSDA10/TXD10/ET0_ETXD1/ RMII0_TXD1/CAT0_ETXD1/CATI2CDATA/ MMC_D4-A/LCD_DATA12-A	P403/PIO_051/IRQ11-DS/AN003

224-Pin LFBGA	RX72M	RX74M
P11	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/ POE0#/GTETRGC/SCK5/CTS8#/SS8#/SS10#/ CTS10#/RTS10#/SSLA0-A/ET0_TX_CLK/ CAT0_TX_CLK/CATSYNC0/QMI-A/QIO1-A/ SDHI_D1-A/MMC_D1-A/LCD_DATA15-A	P401/PIO_049/IRQ9-DS/AN001
P12	PL2/GTETRGC/SMOSI9/SSDA9/TXD9/MISOC/ ET0_RX_ER/RMII0_RX_ER/CAT0_RX_ER	P006/PIO_006/GTCPPO5/GTIOC13A/GTIOC9B/ SCK0-B/CTS0#-B/TXDB0-B/ET1_LINKSTA-D/ CAT1_LINKSTA-E/IRQ22-DS/ADTRG1#/AN022/ PDMCLK0-C/PCOUTZ1
P13	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ET0_RX_DV/ CAT0_RX_DV/SDHI_D3-A/MMC_CD-A/ LCD_DATA19-A	P004/PIO_004/GTCPPO3/GTIOC12A/GTIOC8B/ TXD0-B/SMOSI0-B/SSDA0-B/TXDA0-B/ SSITXD1/ET1_MDC-D/CATSYNC0-E/IRQ20-DS/ AN020/DSMCLK2-B/PCOUTA1
P14	PM4/GTADSM0/ET0_ETXD2/CAT0_ETXD2/ SDHI_D2-D/QIO2-A	P003/PIO_003/GTCPPO2/GTIOC11B/GTIOC8A/ RXD7-A/SMISO7-A/SSCL7-A/SSIRXD1/ ET0_MDIO-D/CAT0_MDIO-E/IRQ19-DS/AN019/ DSMDAT1-B/PCOUTB0
P15	PM3/GTETRGD/RTS10#/CTS10#/SS10#/ ET1_ERXD3/CAT1_ERXD3/SDHI_D1-D/ QMI-A/QIO1-A	P001/PIO_001/TMCI0/GTCPPO0/GTIOC10B/ GTIOC7A/SCK7-A/CTS7#-A/TXDB7-A/ SSIBCK0/ET0_LINKSTA-D/CAT0_LINKSTA-E/ IRQ17-DS/AN017/DSMDAT0-B/PCOUTZ0
R1	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/ GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/PIXD5/ IRQ9	VSS
R2	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/ SSDA10/TXD10/EPLSOUT1/CATSYNC1/ SDHI_D2-C/PIXD2	CLKOUT/PE01/PIO_041/A14-B/GTOULO-C/ GTIOC7B/TXD12-A/SMOSI12-A/SSDA12-A/ TXDA12-A/RSPCK1-A/ET1_RX_DV-D/ RMII1_CRS_DV-D/CAT1_RX_DV-D/SD0DAT5-B/ XSPI1_CK-A/PIXD1-C/IRQ9
R3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/ PO14/RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/ SMISO3/SSCL3/SCL2-DS/USB0_VBUSEN/ USB0_VBUS/USB0_OVRCURB/IRQ6/ADTRG0#	ETHPHYCLK/PE00/PIO_040/A15-B/GTOUUP-C/ GTIOC7A/SCK12-A/CTS12#-A/TXDB12-A/ SSL10-A/ET1_RX_ER-D/RMII1_RX_ER-D/ CAT1_RX_ER-D/SD0DAT4-B/XSPI1_CKN#-A/ XSPI1_CS1#-B/PIXD0-C/IRQ8
R4	P12/WR3#/BC3#/MTIC5U/TMCI1/GTADSM0/ RXD2/SMISO2/SSCL2/SCL0[FM+]/ LCD_TCON1-A/IRQ2	PD06/PIO_038/A17-B/D25-B/GTIV-C/GTIOC3A/ POEGB/RXD3-A/SMISO3-A/SSCL3-A/SSL23-A/ CRX1-B/ET1_RX_ER-B/RMII1_RX_ER-B/ CAT1_RX_ER-B/CATLEDERR-D/SD0WP-B/ XSPI0_DS-A/PIXD6-B/IRQ6/AN030
R5	USB0_DM	PD04/PIO_036/A19-B/D27-B/GTETRGA/ GTIOC2A/POEGC/CTS2#-A/CTS3#-A/RTS3#-A/ SS3#-A/DE3-A/TXDB3-A/SSL21-A/CRX0-B/ ET1_RX_CLK-B/RMII1_REF50CK-B/ CAT1_RX_CLK-B/CATLEDRUN-D/SD0DAT0-B/ XSPI0_IO2-A/XSPI0_WP0#-B/PIXD4-B/IRQ4/ AN028
R6	USB0_DP	PD00/PIO_032/A23-B/D31-B/GTETRGD/ GTIOC0A/POEGD/CTS2#-A/RTS2#-A/SS2#-A/ DE2-A/TXDB2-A/CTS3#-A/SSL20-A/ ET1_RXD0-B/RMII1_RXD0-B/CAT1_ERXD0-B/ CATLATCH0-D/SD0DAT2-B/XSPI0_CKN#-A/ XSPI0_CS1#-B/PIXD0-B/IRQ0/AN024
R7	P54/D1[A1/D1]/EDACK0/ALE/MTIOC4B/TMCI1/ CTS2#/RTS2#/SS2#/MOSIC-B/CTX1/ ET0_LINKSTA/CAT0_LINKSTA/LCD_DATA6-A	PD01/PIO_033/A22-B/D30-B/GTETRGC/ GTIOC0B/POEGC/SCK2-A/CTS2#-A/TXDB2-A/ RSPCK2-A/ET1_RXD1-B/RMII1_RXD1-B/ CAT1_ERXD1-B/CATSYNC0-D/SD0DAT3-B/ XSPI0_CK-A/PIXD1-B/IRQ1/AN025

224-Pin LFBGA	RX72M	RX74M
R8	P55/D0[A0/D0]/EDREQ0/WAIT#/MTIOC4D/ TMO3/TXD7/SMOSI7/SSDA7/MISOC-B/CRX1/ ET0_EXOUT/LCD_DATA5-A/IRQ10	AVCC0
R9	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/MTCLKA/ TMCI2/PO30/TIC0/GTIOC3B/RXD8/SMISO8/ SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ ET0_ETXD3/CAT0_ETXD3/CATLATCH1/ MMC_D6-A/LCD_DATA10-A/IRQ13	VREFH0
R10	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/RTS8#/ SCK10/RSPCKA-A/ET0_ETXD2/CAT0_ETXD2/ MMC_D5-A/LCD_DATA11-A	P402/PIO_050/IRQ10-DS/AN002
R11	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/MMC_D0-A/LCD_DATA16-A	P400/PIO_048/IRQ8-DS/AN000
R12	PL4/GTADSM0/SSLC1/ET0_ETXD0/ RMII0_TXD0/CAT0_ETXD0	P007/PIO_007/GTCPPO6/GTIOC13B/POEGA/ CTS0#-B/RTS0#-B/SS0#-B/DE0-B/TXDB0-B/ ET1_INT-D/CATIRQ-E/IRQ23-DS/ADTRG0#/ AN023/PDMDAT0-C
R13	P75/CS5#/PO20/SCK11/RTS11#/ET0_ERXD0/ RMII0_RXD0/CAT0_ERXD0/SDHI_D2-A/ MMC_RES#-A/LCD_DATA20-A/DSMDAT2	P005/PIO_005/GTCPPO4/GTIOC12B/GTIOC9A/ RXD0-B/SMISO0-B/SSCL0-B/SSILRCK1/ ET1_MDIO-D/CATLATCH0-E/IRQ21-DS/ ADTRG2#/AN021/DSMDAT2-B/PCOUTB1
R14	P74/A20/CS4#/PO19/SS11#/CTS11#/ ET0_ERXD1/RMII0_RXD1/CAT0_ERXD1/ LCD_DATA21-A/DSMCLK2	P002/PIO_002/TMCI1/GTCPPO1/GTIOC11A/ GTIOC7B/TXD7-A/SMOSI7-A/SSDA7-A/ TXDA7-A/SSIBCK1/ET0_MDC-D/CAT0_MDC-E/ IRQ18-DS/AN018/DSMCLK1-B/PCOUTA0
R15	PM5/GTADSM1/ET0_ETXD3/CAT0_ETXD3/ SDHI_D3-D/QIO3-A	NC

Note: 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

Table 3.2 Comparative Listing of RX72N/RX74N 224-Pin Package Pin Functions

224-Pin	RX72N (224-Pin LFBGA)	RX74N (224-Pin LFBGA)
A1	NC	VSS
A2	VREFH0	PC03/PIO_027/D4-A/GTOVLO-B/GTIOC8B/ TXD11-A/SMOSI11-A/SSDA11-A/TXDA11-A/ SDAHS1-C/ET0_TXD2-A/RGMII0_TXD2-A/ SD0CLK-A/IRQ11/PCOUTA1
A3	VREFL0	ETHPHYCLK/PC07/PIO_031/D0-A/TMO2/TOC0/ CACREF/GTETRGD/GTADSM1/GTIOC15B/ POEGA/TXD8-A/SMOSI8-A/SSDA8-A/TXDA8-A/ MISO0-A/SSITXD0/RGMII0_TXC-A/SD0CD-A/ IRQ14/PDMDAT0-A
A4	P41/IRQ9-DS/AN001	CLKOUT/P801/PIO_057/EBCLK-A/GTIV-B/ GTIOC0B/POEGC/TXD10-B/SMOSI10-B/ SSDA10-B/TXDA10-B/ET0_CRS-B/IRQ9/ ADCNV1-B
A5	P92/D18/A18/POE4#/RXD7/SMISO7/SSCL7/ ET1_CRS/RMII1_CRS_DV/AN116	P802/PIO_058/CS2#-A/WR#-B/WR0#-B/GTIW-B/ GTIOC1A/POEGB/SCK10-B/CTS10#-B/ TXDB10-B/CRX2-D/USB0_EXICEN/ ET0_MDIO-B/IRQ2/ADCNV2-B

224-Pin	RX72N (224-Pin LFBGA)	RX74N (224-Pin LFBGA)
A6	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108	VLO
A7	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/ET1_EXOUT/QIO2-B/ SDHI_D2-B/MMC_D2-B/LCD_DATA22-B/IRQ2/ AN110	VSS_DCDC
A8	TRDATA5/P96/D22/A22/ET1_ERXD2	VCC_DCDC
A9	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/ET1_WOL/QIO3-B/ SDHI_D3-B/MMC_D3-B/LCD_DATA21-B/IRQ3/ AN111	P103/PIO_011/TMO3/GTADSM1/GTIOC13B/ CTS2#-B/SDA00-A/ET0_CRS-D/IRQ3
A10	TRDATA6/PG0/D24/ET1_RX_CLK/REF50CK1	P104/PIO_012/TMRI2/GTIW-E/GTIOC14A/ RXD2-B/SMISO2-B/SSCL2-B/CTS3#-B/RTS3#-B/ SS3#-B/DE3-B/TXDB3-B/CTX2-A/ USB0_OVRCURA-DS/USBHS_VBUS/ ET0_TXD0-B/RMII0_TXD0-B/PIXD0-A/IRQ4/ ADST0-A/PCINA0
A11	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ ET1_RX_ER/RMII1_RX_ER/QMI-B/QIO1-B/ SDHI_D1-B/MMC_D1-B/LCD_DATA17-B/IRQ7/ AN107	CLKOUT/P106/PIO_014/TMO2/RTCOUT/ GTIU-D/GTIOC15A/POEGB/RXD3-B/SMISO3-B/ SSCL3-B/SCLHS2-A/ET0_TXD2-B/SD0DAT2-C/ PIXD2-A/IRQ30-DS/ADTRG0#/PCINA1
A12	P61/SDCS#/D0[A0/D0]/CS1#/ET1_ERXD1/ RMII1_RXD1	P200/PIO_016/TMRI0/GTETRGA/GTIOC3A/ GTIOC14A/CTS6#-A/RTS6#-A/SS6#-A/DE6-A/ TXDB6-A/MOSI0-C/SDAHS1-A/USB0_ID/ SSIRXD0/ET0_TX_EN-B/RMII0_TX_EN-B/ SD0CMD-C/PIXD4-A/IRQ8/ADTRG2#/PCINZ1
A13	P62/RAS#/D1[A1/D1]/CS2#/ET1_ERXD0/ RMII1_RXD0	TCK/SWCLK/P301/PIO_025/TMCI3/GTCPPO11/ SCK0-A/CTS0#-A/TXDB0-A/SCK1-A/CTS1#-A/ TXDB1-A/RSPCK1-C/IRQ7
A14	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/MTIOC3B/ PO18/GTIOC1B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1	TDO/P302/PIO_026/TMRI3/GTCPPO12/TXD0-A/ SMOSI0-A/SSDA0-A/TXDA0-A/TXD1-A/ SMOSI1-A/SSDA1-A/TXDA1-A/MOSI1-C/IRQ4
A15	P70/SDCLK	VSS
B1	AVSS0	PC04/PIO_028/D3-A/TMCI1/GTOWUP-B/ GTIOC9A/CTS8#-A/RTS8#-A/SS8#-A/DE8-A/ TXDB8-A/CTS11#-A/SSL00-A/AUDIO_CLK/ ET0_TXD3-A/RGMII0_TXD3-A/SD0DAT0-A/ IRQ12/PCOUTB1
B2	AVCC0	PC01/PIO_025/D6-A/GTOULO-B/GTIOC7B/ SCK11-A/CTS11#-A/TXDB11-A/SSL02-A/ SDA00-C/ET0_TXD0-A/RMII0_TXD0-A/ RGMII0_TXD0-A/SD0DAT3-A/IRQ12/PCOUTB0
B3	P42/IRQ10-DS/AN002	PC05/PIO_029/D2-A/TMRI2/GTOWLO-B/ GTIOC9B/SCK8-A/CTS8#-A/TXDB8-A/ RSPCK0-A/SSIBCK0/ET0_TX_EN-A/ RMII0_TX_EN-A/RGMII0_TX_CTL-A/ SD0DAT1-A/IRQ5/PCOUTZ1
B4	P46/IRQ14-DS/AN006	PC06/PIO_030/D1-A/TMCI2/TIC0/GTETRGC/ GTCPPO7/GTIOC15A/POEGB/RXD8-A/ SMISO8-A/SSCL8-A/MOSI0-A/SSILRCK0/ ET0_TX_ER-A/SD0WP-A/IRQ13/PDMCLK0-A

224-Pin	RX72N (224-Pin LFBGA)	RX74N (224-Pin LFBGA)
B5	P91/D17/A17/SCK7/ET1_COL/AN115	P803/PIO_059/CS3#-A/WR1#-B/BC1#-B/ GTIOC1B/POEGA/CTS10#-B/RTS10#-B/ SS10#-B/DE10-B/TXDB10-B/CTX2-D/USB0_ID/ ET0_MDC-B/IRQ3/ADSYNC-B
B6	VCC	VLO
B7	P94/D20/A20/ET1_ERXD0/RMII1_RXD0	VSS_DCDC
B8	TRDATA4/P95/D21/A21/ET1_ERXD1/ RMII1_RXD1	VCC_DCDC
B9	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0-A/ ET1_MDIO/PMGI1_MDIO/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112	P102/PIO_010/TMCI1/GTADSM0/GTIOC13A/ SCL00-A/ET0_COL-D/IRQ2
B10	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/ET1_RX_CLK/REF50CK1/QMO-B/ QIO0-B/SDHI_D0-B/MMC_D0-B/LCD_DATA18-B/ IRQ6/AN106	P105/PIO_013/TMCI2/GTIV-E/GTIOC14B/ TXD2-B/SMOSI2-B/SSDA2-B/TXDA2-B/SCK3-B/ CTS3#-B/TXDB3-B/CRX2-A/USB0_VBUS/ USBHS_OVRCURB/SSILRCK1/ET0_TXD1-B/ RMII0_TXD1-B/PIXD1-A/IRQ29-DS/ADST1-A/ PCINB0
B11	VCC	P107/PIO_015/TMO1/GTIV-D/GTIOC15B/ POEGA/TXD3-B/SMOSI3-B/SSDA3-B/TXDA3-B/ SDAHS2-A/SSITXD0/ET0_TXD3-B/SD0DAT3-C/ PIXD3-A/IRQ31-DS/ADTRG1#/PCINB1
B12	P63/CAS#/D2[A2/D2]/CS3#/ET1_ETXD1/ RMII1_TXD1	P201/PIO_017/TMCI0/GTIW-D/GTIOC3B/ GTIOC14B/SCK6-A/CTS6#-A/TXDB6-A/ MISO0-C/SCLHS1-A/USB0_EXICEN/SSILRCK0/ ET0_RX_ER-B/RMII0_RX_ER-B/SD0CLK-C/ PIXD5-A/IRQ9/PCINZ0
B13	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/PO23/ TIC3/GTIOC0B/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/MMC_D6-B/LCD_DATA14-B/ IRQ7-DS/AN100	TMS/SWDIO/P300/PIO_024/TMO1/GTCPPO10/ CTS0#-A/RTS0#-A/SS0#-A/DE0-A/TXDB0-A/ CTS1#-A/RTS1#-A/SS1#-A/DE1-A/TXDB1-A/ SSL10-C/ET0_WOL-D/IRQ6
B14	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/LCD_DATA12-B/AN102	TDI/P303/PIO_027/TMCI2/GTCPPO13/RXD0-A/ SMISO0-A/SSCL0-A/RXD1-A/SMISO1-A/ SSCL1-A/MISO1-C/IRQ1
B15	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105	ETHPHYCLK/P304/PIO_028/ALE-C/WAIT#-B/ TMCI3/GTETRGD/GTCPPO0/POEGA/CTS0#-A/ CTS1#-A/USB0_VBUSEN/USBHS_ID/ ET0_INT-E/IRQ0-DS/ADTRG0#
C1	AVSS1	PC00/PIO_024/D7-A/GTOUUP-B/GTIOC7A/ CTS11#-A/RTS11#-A/SS11#-A/DE11-A/ TXDB11-A/SSL01-A/SCL00-C/ET0_TX_CLK-A/ SD0DAT2-A/IRQ14/PCOUTA0
C2	AVCC1	PC02/PIO_026/D5-A/GTOVUP-B/GTIOC8A/ RXD11-A/SMISO11-A/SSCL11-A/SSL03-A/ SCLHS1-C/ET0_TXD1-A/RMII0_TXD1-A/ RGMII0_TXD1-A/SD0CMD-A/IRQ10/PCOUTZ0
C3	P05/SSILRCK1/IRQ13/DA1	PB06/PIO_022/D9-A/GTOWUP-A/GTIOC6A/ RXD9-A/SMISO9-A/SSCL9-A/ET0_RX_ER-A/ RMII0_RX_ER-A/IRQ6
C4	P44/IRQ12-DS/AN004	PB05/PIO_021/D10-A/TMRI1/GTOVLO-A/ GTIOC5B/SCK9-A/CTS9#-A/TXDB9-A/ ET0_RX_DV-A/RMII0_CRS_DV-A/ RGMII0_RX_CTL-A/IRQ13

224-Pin	RX72N (224-Pin LFBGA)	RX74N (224-Pin LFBGA)
C5	VSS	P800/PIO_056/CS1#-A/DQM0-B/GTIU-B/ GTIOC0A/POEGD/RXD10-B/SMISO10-B/ SSCL10-B/ET0_COL-B/IRQ8/ADCNV0-B
C6	P90/D16/A16/TXD7/SMOSI7/SSDA7/ ET1_RX_DV/AN114	VLO
C7	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/AN109	P100/PIO_008/CS1#-B/WAIT#-A/TMRI3/ CACREF/GTIU-E/GTADSM0/GTIOC12A/ CTS2#-B/RTS2#-B/SS2#-B/DE2-B/TXDB2-B/ CTS5#-B/USB0_OVRCURB-DS/USBHS_VBUS/ ET0_TX_ER-B/IRQ0/ADTRG2#
C8	VCC	VCC_DCDC
C9	TRSYNC1/P97/D23/A23/ET1_ERXD3	P804/PIO_060/GTADSM0/GTIOC15A/CTS5#-B/ RTS5#-B/SS5#-B/DE5-B/TXDB5-B/SSL21-B/ CTX0-D/USB0_OVRCURA/USBHS_OVRCURA/ ET0_TX_EN-C/RMII0_TX_EN-C/PCKO-D/IRQ4/ PCINA0
C10	P60/CS0#/ET1_TX_EN/RMII1_TXD_EN	P805/PIO_061/GTADSM1/GTIOC15B/SCK5-B/ CTS5#-B/TXDB5-B/SSL22-B/CRX0-D/ USB0_VBUSEN/USBHS_VBUSEN/ET0_TXD0-C/ RMII0_TXD0-C/HSYNC-D/IRQ5/ADSYNC-C/ PCINB0
C11	P64/WE#/D3[A3/D3]/CS4#/ET1_ETXD0/ RMII1_TXD0	P114/PIO_046/GTCPPO14/TXD12-B/ SMOSI12-B/SSDA12-B/TXDA12-B/SSL23-C/ PIXD6-D/IRQ22/ADST2-D
C12	VSS	P111/PIO_043/GTCPPO11/CTS12#-B/CTS9#-C/ RTS9#-C/SS9#-C/DE9-C/TXDB9-C/SSL20-C/ ET0_RXD1-C/RMII0_RXD1-C/SD0DAT7-C/ PIXD3-D/IRQ19
C13	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ET0_RX_CLK/ REF50CK0/LCD_DATA11-B/IRQ5/AN103	P108/PIO_040/TIC0/GTCPPO8/SCK9-C/ CTS9#-C/TXDB9-C/RSPCK2-C/ET0_RX_DV-C/ RMII0_CRS_DV-C/SD0DAT4-C/PIXD0-D/IRQ16/ ADCNV0-D
C14	P65/CKE/CS5#	P110/PIO_042/GTCPPO10/TXD9-C/SMOSI9-C/ SSDA9-C/TXDA9-C/MISO2-C/ET0_RXD0-C/ RMII0_RXD0-C/SD0DAT6-C/PIXD2-D/IRQ18/ ADCNV2-D
C15	P66/DQM0/CS6#/MTIOC7D/GTIOC2B/CTX2	P113/PIO_045/GTCPPO13/SCK12-B/CTS12#-B/ TXDB12-B/SSL22-C/ET0_RXD3-C/PIXD5-D/ IRQ21/ADST1-D/PDMDAT0-D
D1	P45/IRQ13-DS/AN005	PG00/PIO_056/DQM1-A/WR1#-C/BC1#-C/ GTCPPO0/SCK8-C/CTS8#-C/TXDB8-C/IRQ8
D2	P47/IRQ15-DS/AN007	PG02/PIO_058/DQM3-A/WR3#-C/BC3#-C/ GTIOC11A/TXD8-C/SMOSI8-C/SSDA8-C/ TXDA8-C/IRQ10
D3	P03/SSIDATA1/IRQ11/DA0	PB04/PIO_020/D11-A/GTOVUP-A/GTIOC5A/ CTS4#-A/CTS9#-A/RTS9#-A/SS9#-A/DE9-A/ TXDB9-A/ET0_RX_CLK-A/RMII0_REF50CK-A/ RGMII0_RXC-A/IRQ4
D4	P40/IRQ8-DS/AN000	PB07/PIO_023/D8-A/GTOWLO-A/GTIOC6B/ TXD9-A/SMOSI9-A/SSDA9-A/TXDA9-A/ ET0_LINKSTA-A/IRQ15

224-Pin	RX72N (224-Pin LFBGA)	RX74N (224-Pin LFBGA)
D5	P01/TMCI0/RXD6/SMISO6/SSCL6/SSIBCK0/ QIO3-C/IRQ9/AN119	P502/PIO_034/WR2#-A/BC2#-A/A18-C/ GTIOC3A/TXD2-C/SMOSI2-C/SSDA2-C/ TXDA2-C/SSL13-C/CTX1-C/ET0_WOL-B/ SD0DAT6-A/IRQ2/ADST2-C
D6	P02/TMCI1/SCK6/SSIBCK1/IRQ10/AN120	P500/PIO_032/WR#-A/WR0#-A/A16-C/GTIOC2A/ CTS2#-C/RTS2#-C/SS2#-C/DE2-C/TXDB2-C/ CTS7#-B/SSL11-C/CTX0-C/ET0_LINKSTA-B/ SD0DAT4-A/IRQ0/ADST0-C
D7	P93/D19/A19/POE0#/CTS7#/RTS7#/SS7#/ ET1_LINKSTA/AN117	P101/PIO_009/CS0#-A/ALE-B/TMCI3/GTETRGC/ GTADSM1/GTIOC12B/SCK2-B/CTS2#-B/ TXDB2-B/USB0_VBUS-DS/USBHS_EXICEN/ ET0_TX_CLK-B/IRQ1/ADTRG1#
D8	VSS	P504/PIO_036/TMCI1/GTETRGA/GTIOC4A/ CTS2#-C/RXD7-B/SMISO7-B/SSCL7-B/MOSI2-B/ ET0_TX_ER-C/GPTP_CAPTURE0/IRQ4
D9	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/MTCLKA/ POE10#/SSLC1-A/ET1_MDC/PMGI1_MDC/ QSPCLK-B/SDHI_CLK-B/MMC_CLK-B/ LCD_DATA19-B/IRQ5/AN113	P506/PIO_038/GTETRGC/GTIOC5A/POEGD/ SCK7-B/CTS7#-B/TXDB7-B/RSPCK2-B/ ET0_TXD2-C/GPTP0_PPS/IRQ6
D10	TRDATA7/PG1/D25/ET1_RX_ER/RMII1_RX_ER	P806/PIO_062/GTCPPO7/GTIOC14A/RXD5-B/ SMISO5-B/SSCL5-B/SSL23-B/CTX1-D/ ET0_TXD1-C/RMII0_TXD1-C/VSYNC-D/IRQ14/ PCINA1
D11	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/GTIOC2B/ SCK12/SSLB1-B/MMC_D4-B/LCD_DATA16-B/ ANEX0	P109/PIO_041/TOC0/GTCPPO9/RXD9-C/ SMISO9-C/SSCL9-C/MOSI2-C/ET0_RX_CLK-C/ RMII0_REF50CK-C/SD0DAT5-C/PIXD1-D/IRQ17/ ADCNV1-D
D12	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/CTS12#/RTS12#/SS12#/ ET0_ERXD3/MMC_D7-B/LCD_DATA13-B/AN101	P115/PIO_047/GTCPPO15/RXD12-B/ SMISO12-B/SSCL12-B/PIXD7-D/IRQ23
D13	VSS	P112/PIO_044/GTCPPO12/CTS12#-B/RTS12#-B/ SS12#-B/DE12-B/TXDB12-B/CTS9#-C/SSL21-C/ ET0_RXD2-C/PIXD4-D/IRQ20/ADST0-D/ PDMCLK0-D
D14	TRDATA0/PG2/D26/ET1_TX_CLK	VSS
D15	P67/DQM1/CS7#/MTIOC7C/GTIOC1B/CRX2/ EPLSOUT1/IRQ15	VCC
E1	VCL	PG01/PIO_057/DQM0-A/WR#-C/WR0#-C/ GTCPPO1/RXD8-C/SMISO8-C/SSCL8-C/IRQ9
E2	VSS	PG03/PIO_059/DQM2-A/WR2#-C/BC2#-C/ GTIOC11B/CTS8#-C/RTS8#-C/SS8#-C/DE8-C/ TXDB8-C/ET0_INT-A/GPTP_MATCH1/IRQ11
E3	P00/TMRI0/TXD6/SMOSI6/SSDA6/AUDIO_CLK/ QIO2-C/IRQ8/AN118	PB02/PIO_018/D13-A/GTOUUP-A/GTIOC4A/ CTS4#-A/RTS4#-A/SS4#-A/DE4-A/TXDB4-A/ CTS9#-A/ET0_RXD2-A/RGMII0_RXD2-A/IRQ2
E4	P43/IRQ11-DS/AN003	PB03/PIO_019/D12-A/TMO0/GTOULO-A/ GTIOC4B/SCK4-A/CTS4#-A/TXDB4-A/ ET0_RXD3-A/RGMII0_RXD3-A/IRQ3
E5	P07/IRQ15/ADTRG0#	VCC
E6	PN0/ET1_ETXD2	P501/PIO_033/WR1#-A/BC1#-A/A17-C/ GTIOC2B/SCK2-C/CTS2#-C/TXDB2-C/SSL12-C/ CRX0-C/ET0_INT-B/SD0DAT5-A/IRQ1/ADST1-C

224-Pin	RX72N (224-Pin LFBGA)	RX74N (224-Pin LFBGA)
E7	PQ0/SCK11/ET1_CRS/RMII1_CRS_DV	P503/PIO_035/WR3#-A/BC3#-A/A19-C/ GTIOC3B/RXD2-C/SMISO2-C/SSCL2-C/CRX1-C/ USB0_OVRCURB/SSIRXD0/SD0DAT7-A/IRQ3
E8	PQ1/SMISO11/SSCL11/RXD11/ET1_COL	P505/PIO_037/TMO3/GTETRGB/GTIOC4B/ TXD7-B/SMOSI7-B/SSDA7-B/TXDA7-B/MISO2-B/ ET0_TX_CLK-C/GPTP_MATCH0/IRQ10
E9	PQ3/RTS11#/CTS11#/SS11#/ET1_TX_ER	P507/PIO_039/GTETRGD/GTIOC5B/POEGC/ CTS7#-B/RTS7#-B/SS7#-B/DE7-B/TXDB7-B/ SSL20-B/ET0_TXD3-C/IRQ7
E10	PQ5/ET1_ETXD0/RMII1_TXD0	P807/PIO_063/GTCPPO4/GTIOC14B/POEGD/ TXD5-B/SMOSI5-B/SSDA5-B/TXDA5-B/CRX1-D/ ET0_RX_ER-C/RMII0_RX_ER-C/PIXCLK-D/ IRQ15/PCINB1
E11	PQ4/ET1_RX_CLK/REF50CK1	PF02/PIO_050/CS6#-B/BREQ#-C/GTCPPO1/ GTIOC7A/RXD0-C/SMISO0-C/SSCL0-C/RXD7-C/ SMISO7-C/SSCL7-C/IRQ2/ADSYNC-D
E12	VCC	PF04/PIO_052/CS4#-B/GTCPPO3/GTIOC8A/ SCK0-C/CTS0#-C/TXDB0-C/SCK7-C/CTS7#-C/ TXDB7-C/IRQ4
E13	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/AN104	PF03/PIO_051/CS7#-B/BACK#-C/GTCPPO2/ GTIOC7B/TXD0-C/SMOSI0-C/SSDA0-C/ TXDA0-C/TXD7-C/SMOSI7-C/SSDA7-C/ TXDA7-C/IRQ3
E14	TRCLK/PG5/D29/ET1_ETXD2	PF00/PIO_048/GTCPPO14/USB0_DP/IRQ0
E15	TRSYNC/PG4/D28/ET1_ETXD1/RMII1_TXD1	PF01/PIO_049/GTCPPO15/USB0_DM/IRQ1
F1	XCIN	PA05/PIO_013/A2-A/GTIOC2B/GTIOC12B/ SCK10-A/CTS10#-A/TXDB10-A/RSPCK0-B/IRQ5/ PCINA0
F2	VBATT	ETHPHYCLK/PA07/PIO_015/A0-A/BC0#-A/ DQM1-B/GTIOC3B/GTIOC13B/RXD10-A/ SMISO10-A/SSCL10-A/MISO0-B/IRQ7/PCINB0
F3	TRST#/PF4	PB01/PIO_017/D14-A/TMCI0/GTETRGB/ GTCPPO4/GTIOC14B/POEGA/TXD4-A/ SMOSI4-A/SSDA4-A/TXDA4-A/ET0_RXD1-A/ RMII0_RXD1-A/RGMII0_RXD1-A/IRQ4-DS/ PCINB1
F4	PK4/GTADSM0/SSLB1/ET0_ERXD2	PB00/PIO_016/D15-A/GTETRGA/GTADSM0/ GTIOC14A/POEGC/RXD4-A/SMISO4-A/ SSCL4-A/ET0_RXD0-A/RMII0_RXD0-A/ RGMII0_RXD0-A/IRQ12/ADST2-A/PCINA1
F5	PK5/GTADSM1/SSLB2/ET0_ERXD3	VSS
F6	EMLE	VCL
F7	PK6/GTIOC1A/SSLB3	VSS
F8	PN1/ET1_ETXD3	VCC
F9	PQ6/ET1_ETXD1/RMII1_TXD1	VSS
F10	VSS	VSS
F11	PM1/TOC3/GTETRGB/SMISO10/SSCL10/ RXD10/ET1_ERXD1/RMII1_RXD1/SDHI_CMD-D/ QSSL-A	PF05/PIO_053/CS5#-B/GTCPPO5/GTIOC8B/ POEGD/CTS7#-C/RTS7#-C/SS7#-C/DE7-C/ TXDB7-C/SSL01-C/IRQ5

224-Pin	RX72N (224-Pin LFBGA)	RX74N (224-Pin LFBGA)
F12	PA0/DQM2/BC0#/A0/MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/LCD_DATA8-B	P202/PIO_018/CS3#-B/BREQ#-A/TMO0/ GTOUUP-D/GTIOC0A/GTIOC4A/TXD6-A/ SMOSI6-A/SSDA6-A/TXDA6-A/RSPCK0-C/ SCL00-B/CTX2-B/USB0_OVRCURA/ USBHS_EXICEN/AUDIO_CLK/ET0_RX_DV-B/ RMII0_CRS_DV-B/SD0DAT0-C/PIXD6-A/IRQ15/ PDMCLK0-B
F13	TRDATA1/PG3/D27/ET1_ETXD0/RMII1_TXD0	P203/PIO_019/CS2#-B/BACK#-A/GTOULO-D/ GTIOC0B/GTIOC4B/RXD6-A/SMISO6-A/ SSCL6-A/CTS3#-B/SSL00-C/SDA00-B/CRX2-B/ USB0_OVRCURB/USBHS_ID/SSIBCK0/ ET0_RX_CLK-B/RMII0_REF50CK-B/ SD0DAT1-C/PIXD7-A/IRQ3/PDMDAT0-B
F14	TRDATA2/PG6/D30/ET1_ETXD3	VCC_USB
F15	TRDATA3/PG7/D31/ET1_TX_ER	VSS_USB
G1	XCOUT	PA04/PIO_012/A3-A/TMRI0/GTIOC2A/ GTIOC12A/CTS10#-A/RTS10#-A/SS10#-A/ DE10-A/TXDB10-A/SSL00-B/IRQ5-DS/PCINZ0
G2	VSS	PA06/PIO_014/A1-A/DQM2-B/TMCI3/GTIOC3A/ GTIOC13A/TXD10-A/SMOSI10-A/SSDA10-A/ TXDA10-A/MOSI0-B/IRQ14/PCINZ1
G3	VCC	PG05/PIO_061/A10-A/GTIOC12B/RXD3-C/ SMISO3-C/SSCL3-C/ET0_MDIO-A/IRQ13
G4	MD/FINED	PG07/PIO_063/A8-A/GTIOC13B/CTS3#-C/ RTS3#-C/SS3#-C/DE3-C/TXDB3-C/ET0_CRS-A/ IRQ15
G5	PJ5/POE8#/CTS2#/RTS2#/SS2#/SSIRXD0/ EPLSOUT0/QMI-C/QIO1-C	PF09/PIO_017/A20-A/A16-D/CTS12#-C/ GPTP_CAPTURE1/XSPI1_INT0#-A/ XSPI1_ECS0#-A/IRQ17
G6	PF5/WAIT#/SSILRCK0/IRQ4	VSS
G7	RES#	VCL
G8	PQ2/SMOSI11/SSDA11/TXD11/ET1_RX_DV	VSS
G9	PN2/ET1_TX_CLK	VCL
G10	VCC	VCL
G11	PM0/TIC3/GTETRGA/SCK10/ET1_ERXD0/ RMII1_RXD0/SDHI_CLK-D/QSPCLK-A	CLKOUT/P205/PIO_021/A21-C/CS6#-C/ GTOVLO-D/GTIOC1B/GTIOC5B/SCK1-B/ CTS1#-B/TXDB1-B/RSPCK1-B/SDAHS1-B/ CRX0-A/USB0_VBUS/USBHS_VBUSEN/ SSIRXD1/ET0_RXD1-B/RMII0_RXD1-B/ SD0CD-C/HSYNC-A/IRQ5/ADTRG0#/PCOUTB1
G12	PA1/DQM3/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/IRQ11	ETHPHYCLK/P204/PIO_020/A20-C/CS7#-C/ TMRI1/GTOVUP-D/GTIOC1A/GTIOC5A/ CTS1#-B/RTS1#-B/SS1#-B/DE1-B/TXDB1-B/ SSL10-B/SCLHS1-B/CTX0-A/USB0_VBUSEN/ USBHS_VBUS-DS/SSIBCK1/ET0_RXD0-B/ RMII0_RXD0-B/SD0WP-C/PIXCLK-A/IRQ12/ PCOUTA1
G13	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B	VCC_USBHS
G14	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/ PMGI0_MDIO/LCD_DATA5-B/IRQ6-DS	USBHS_DP

224-Pin	RX72N (224-Pin LFBGA)	RX74N (224-Pin LFBGA)
G15	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/ TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC/ PMGI0_MDC/LCD_DATA4-B/IRQ5-DS	USBHS_DM
H1	XTAL/P37	PA02/PIO_010/A5-A/GTIW-A/GTIOC1A/ GTIOC11A/TXD5-A/SMOSI5-A/SSDA5-A/ TXDA5-A/SSL03-B/IRQ10/ADCNV2-A
H2	P34/MTIOC0A/TMCI3/PO12/POE10#/SCK6/ SCK0/ET0_LINKSTA/IRQ4	PA03/PIO_011/A4-A/GTIOC1B/GTIOC11B/ RXD5-A/SMISO5-A/SSCL5-A/IRQ6-DS/ ADSYNC-A
H3	UPSEL/P35/NMI	PG06/PIO_062/A9-A/GTIOC13A/TXD3-C/ SMOSI3-C/SSDA3-C/TXDA3-C/ET0_COL-A/ IRQ14
H4	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/ POE4#/POE11#/RXD6/SMISO6/SSCL6/RXD0/ SMISO0/SSCL0/CRX0/PCKO/IRQ3-DS	PG04/PIO_060/A11-A/GTIOC12A/SCK3-C/ CTS3#-C/TXDB3-C/ET0_MDC-A/IRQ12
H5	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCIC2/ RTCOUT/POE0#/POE10#/TXD6/SMOSI6/ SSDA6/TXD0/SMOSI0/SSDA0/CTX0/ USB0_VBUSEN/VSYNC/IRQ2-DS	PF08/PIO_016/A21-A/A17-D/GTCPPO12/ POEGA/XSPI1_RESET0#-A/IRQ16
H6	BSCANP	VCC
H7	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/SS6#/ CTS0#/RTS0#/SS0#/SSITXD0/ET0_EXOUT/ QMO-C/QIO0-C	VSS
H8	PQ7/ET1_TX_EN/RMII1_TXD_EN	VCL
H9	PN3/ET1_RX_ER/RMII1_RX_ER	VSS
H10	P73/CS3#/PO16/ET0_WOL/LCD_EXTCLK-A	VCL
H11	PL0/TIC2/GTETRGA/SCK9/RSPCKC/ ET0_ERXD0/RMII0_RXD0	P206/PIO_022/A22-C/CS5#-C/TMO3/RTCOUT/ GTOWUP-D/GTIOC2A/GTIOC6A/CTS6#-A/ TXD1-B/SMOSI1-B/SSDA1-B/TXDA1-B/MOSI1-B/ SCLHS2-B/CTX1-A/USB0_EXICEN/ USBHS_OVRCURA-DS/SSITXD1/ET0_RXD2-B/ VSYNC-A/IRQ2-DS/ADTRG1#/PCOUTZ1
H12	VCC	AVSS_USBHS
H13	VSS	USBHS_RREF
H14	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/RTS5#/SS5#/ MOSIA-B/ET0_EXOUT/LCD_DATA2-B	VSS_USBHS
H15	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/LCD_DATA3-B	VCC
J1	EXTAL/P36	ETHPHYCLK/PA00/PIO_008/A7-A/CACREF/ GTIU-A/GTIOC0A/GTIOC10A/CTS10#-A/ CTS5#-A/RTS5#-A/SS5#-A/DE5-A/TXDB5-A/ SSL01-B/IRQ1-DS/ADCNV0-A
J2	TDI/PF2/RXD1/SMISO1/SSCL1	PA01/PIO_009/A6-A/GTIV-A/GTIOC0B/ GTIOC10B/SCK5-A/CTS5#-A/TXDB5-A/SSL02-B/ IRQ11/ADCNV1-A
J3	TMS/PF3	P703/PIO_051/ALE-A/WR2#-B/BC2#-B/CACREF/ GTETRGB/GTIOC11B/CTS4#-B/RTS4#-B/ SS4#-B/DE4-B/TXDB4-B/XSPI1_RESET0#-B/ PCKO-C/IRQ8

224-Pin	RX72N (224-Pin LFBGA)	RX74N (224-Pin LFBGA)
J4	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/ RTS1#/SS1#/SSLB0-A/ET1_MDC/PMGI1_MDC/ IRQ1-DS	PF06/PIO_054/A23-A/A19-D/GTCPPO6/ GTIOC9A/POEGC/CTS0#-C/RTS0#-C/SS0#-C/ DE0-C/TXDB0-C/CTS7#-C/SSL02-C/ XSPI1_CS1#-A/XSPI1_WP0#-A/IRQ6
J5	P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/MISOB-A/ET1_MDIO/ PMGI1_MDIO/IRQ0-DS	PF07/PIO_055/A22-A/A18-D/GTCPPO11/ GTIOC9B/SSL03-C/XSPI1_RSTO0#-A/IRQ7
J6	PH2/GTETRGC/SMOSI7/SSDA7/TXD7/MISOA	VSS
J7	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/ PO13/GTETRGA/RXD1/SMISO1/SSCL1/SCK3/ CRX1-DS/SSILRCK1/PIXD0/IRQ5	VCL
J8	P53*1/BCLK	VSS
J9	PK3/GTETRGD/RTS8#/CTS8#/SS8#/SSLB0/ ET0_TX_ER	VCL
J10	PL1/TOC2/GTETRGB/SMISO9/SSCL9/RXD9/ MOSIC/ET0_ERXD1/RMII0_RXD1	VSS
J11	PN5/ET1_MDC/PMGI1_MDC/QSSL-C	P207/PIO_023/A23-C/CS4#-C/TMRI3/ GTOWLO-D/GTIOC2B/GTIOC6B/RXD1-B/ SMISO1-B/SSCL1-B/MISO1-B/SDAHS2-B/ CRX1-A/USB0_ID/USBHS_OVRCURB-DS/ ET0_RXD3-B/PCKO-A/IRQ3-DS/ADTRG2#
J12	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/ PO25/TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/ SSDA6/ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS	P305/NMI/IRQ0
J13	P71/A18/CS1#/ET0_MDIO/PMGI0_MDIO	AVCC_USBHS
J14	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/ET0_ERXD1/ RMII0_RXD1/LCD_DATA0-B/IRQ12	XTAL/P307
J15	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B	EXTAL/P306
K1	CLKOUT25M/PH7/GTIOC0B	P707/PIO_055/WE#-A/CS7#-A/GTIOC13B/ TXD11-B/SMOSI11-B/SSDA11-B/TXDA11-B/ XSPI1_RESET1#-B/IRQ7
K2	CLKOUT/PH6/GTIOC0A/SSLA3	P706/PIO_054/CAS#-A/CS6#-A/GTIOC13A/ RXD11-B/SMISO11-B/SSCL11-B/ XSPI1_WP1#-B/IRQ14/ADCNV2-C
K3	PH4/GTADSM0/SSLA1	P702/PIO_050/RD#-A/DQM3-B/GTETRGA/ GTIOC11A/SCK4-B/CTS4#-B/TXDB4-B/ XSPI1_WP0#-B/XSPI1_RESET1#-C/HSYNC-C/ IRQ10/ADST2-B
K4	PH5/GTADSM1/SSLA2	P605/PIO_013/CS2#-C/D18-B/GTIOC6B/ RXD9-B/SMISO9-B/SSCL9-B/SSL02-D/ XSPI0_INT0#-A/XSPI0_ECS0#-A/IRQ13
K5	TDO/PF0/TXD1/SMOSI1/SSDA1	VSS
K6	PH1/TOC0/GTETRGB/SMISO7/SSCL7/RXD7/ MOSIA	VCC
K7	P10/ALE/MTIC5W/TMRI3/IRQ0	VSS
K8	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A	VCC2
K9	PK1/TOC1/GTETRGB/SMISO8/SSCL8/RXD8/ MOSIB/ET0_COL	VCL

224-Pin	RX72N (224-Pin LFBGA)	RX74N (224-Pin LFBGA)
K10	PL3/GTETRGD/RTS9#/CTS9#/SS9#/SSLC0/ ET0_RX_CLK/REF50CK0	VSS
K11	PM2/GTETRGC/SMOSI10/SSDA10/TXD10/ ET1_ERXD2/SDHI_D0-D/QMO-A/QIO0-A	P310/PIO_058/RTCIC0/CACREF/GTETRGB/ GTCPPO1/POEGC/CTS0#-C/CTS1#-B/SSL11-B/ SSITXD0/IRQ18/ADTRG0#/TAMPI0
K12	VSS	P311/PIO_059/BREQ#-B/RTCIC1/GTETRGC/ GTCPPO14/POEGD/CTS7#-A/SSL12-B/ SSIRXD0/ET0_WOL-C/IRQ19/ADTRG1#/TAMPI1
K13	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/SCK11/ET0_ETXD0/ RMII0_TXD0/LCD_CLK-B	MD/P315
K14	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK4/SCK6/ET0_RX_ER/ RMII0_RX_ER/LCD_TCON1-B	VSS
K15	P72/A19/CS2#/ET0_MDC/PMGI0_MDC/ LCD_DATA23-A	VSS
L1	PH3/GTETRGD/RTS7#/CTS7#/SS7#/SSLA0	P705/PIO_053/RAS#-A/CS5#-A/GTIOC12B/ SCK11-B/CTS11#-B/TXDB11-B/ XSPI1_RSTO1#-B/IRQ13/ADCNV1-C
L2	P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A/ET1_WOL	P704/PIO_052/SDCS#-A/CS4#-A/GTIOC12A/ CTS4#-B/CTS11#-B/RTS11#-B/SS11#-B/DE11-B/ TXDB11-B/XSPI1_INT1#-B/XSPI1_ECS1#-B/ IRQ12/ADCNV0-C
L3	TCK/PF1/SCK1	P604/PIO_012/CS3#-C/D19-B/GTIOC6A/TXD9-B/ SMOSI9-B/SSDA9-B/TXDA9-B/SSL01-D/ XSPI0_CS1#-A/XSPI0_RSTO0#-B/IRQ4
L4	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/ TMRI1/PO4/SCK3/USB0_VBUSEN/SSIBCK1/ SDHI_WP/PIXCLK	P606/PIO_014/CS1#-C/D17-B/GTETRGA/ GTCPPO4/GTIOC15A/POEGC/SCK9-B/ CTS9#-B/TXDB9-B/SSL03-D/CTX2-C/ XSPI0_RESET0#-A/IRQ14
L5	VCC	VCC2
L6	CLKOUT25M/PJ2/TXD8/SMOSI8/SSDA8/ SSLC3-B/LCD_TCON2-A	P904/PIO_004/GTCPPO0/POEGC/TXD6-B/ SMOSI6-B/SSDA6-B/TXDA6-B/ET0_COL-E/ GPTP_PTPOUT0/IRQ12
L7	VCC	P906/PIO_006/GTCPPO2/POEGA/SCK6-B/ CTS6#-B/TXDB6-B/ET0_MDC-C/IRQ14
L8	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A	P407/PIO_055/IRQ15-DS/AN007
L9	P81/EDACK0/MTIOC3D/PO27/GTIOC0B/ SMISO10/SSCL10/RXD10/ET0_ETXD0/ RMII0_TXD0/QIO3-A/SDHI_CD/MMC_D3-A/ LCD_DATA13-A	P406/PIO_054/IRQ14-DS/AN006
L10	PL7/GTIOC2B/ET0_MDIO/PMGI0_MDIO	P215/PIO_055/GTCPPO13/CTS4#-C/CTS5#-C/ RTS5#-C/SS5#-C/DE5-C/TXDB5-C/USBHS_ID/ IRQ31/PDMDAT0-E/PCINZ0
L11	P77/CS7#/PO23/SMOSI11/SSDA11/TXD11/ ET0_RX_ER/RMII0_RX_ER/QSPCLK-A/ SDHI_CLK-A/MMC_CLK-A/LCD_DATA17-A	P209/PIO_049/TOC1/GTETRGB/RXD4-C/ SMISO4-C/SSCL4-C/MOSI1-D/IRQ25/PCINB1
L12	PN4/ET1_MDIO/PMGI1_MDIO/QSPCLK-C	P312/PIO_060/BACK#-B/RTCIC2/GTETRGD/ GTCPPO15/POEGA/SSL13-B/SSILRCK0/IRQ20/ ADTRG2#/TAMPI2
L13	VCC	VCC

224-Pin	RX72N (224-Pin LFBGA)	RX74N (224-Pin LFBGA)
L14	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/SS4#/CTS6#/RTS6#/SS6#/ET0_RX_CLK/REF50CK0/LCD_TCON2-B	XCIN/EXCIN/P309
L15	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/SS11#/CTS11#/RTS11#/ET0_TX_EN/RMII0_TXD_EN/LCD_TCON0-B	XCOUT/P308
M1	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A/ET1_EXOUT	ETHPHYCLK/P700/PIO_048/SDCLK-A/GTIOC10A/TXD4-B/SMOSI4-B/SSDA4-B/TXDA4-B/XSPI1_INT0#-B/XSPI1_ECS0#-B/PIXCLK-C/IRQ0/ADST0-B
M2	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/SDHI_D1-C/PIXD7	P701/PIO_049/CKE-A/WR3#-B/BC3#-B/GTIOC10B/RXD4-B/SMISO4-B/SSCL4-B/XSPI1_RSTO0#-B/XSPI1_RESET0#-B/VSYNC-C/IRQ1/ADST1-B
M3	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/SSIDATA1/SDHI_CD/HSYNC/ADTRG0#	P607/PIO_015/CS0#-B/D16-B/GTETRGB/GTADSM0/GTIOC15B/POEGA/CTS8#-B/CTS9#-B/RTS9#-B/SS9#-B/DE9-B/TXDB9-B/CRX2-C/XSPI0_RSTO0#-A/IRQ15
M4	VSS	P603/PIO_011/WE#-B/D20-B/GTIOC5B/CTS8#-B/RTS8#-B/SS8#-B/DE8-B/TXDB8-B/CTS9#-B/MISO0-D/XSPI0_IO7-A/PCKO-B/IRQ3
M5	PJ0/MTIOC6B/SCK8/SSLC1-B/EPLSOUT0/LCD_DATA0-A	P907/PIO_007/GTCPPO3/POEGD/CTS6#-B/RTS6#-B/SS6#-B/DE6-B/TXDB6-B/CTS1#-C/ET0_MDIO-C/XSPI0_WP0#-A/IRQ15
M6	P84/MTIOC6D/ET1_LINKSTA/LCD_DATA2-A	P905/PIO_005/GTCPPO1/POEGB/RXD6-B/SMISO6-B/SSCL6-B/ET0_CRS-E/GPTP_PTPOUT1/IRQ13
M7	VSS	P902/PIO_002/GTETRGC/GTCPPO8/SCK1-C/CTS1#-C/TXDB1-C/XSPI0_RESET1#-A/IRQ10/AN034
M8	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	P900/PIO_000/GTETRGA/GTCPPO5/RXD1-C/SMISO1-C/SSCL1-C/XSPI0_INT1#-A/XSPI0_ECS1#-A/IRQ0/AN032
M9	P83/EDACK1/MTIOC4C/GTIOC0A/SCK10/SS10#/CTS10#/ET0_CRS/RMII0_CRS_DV/LCD_DATA8-A	P405/PIO_053/IRQ13-DS/AN005
M10	PK0/TIC1/GTETRGA/SCK8/RSPCKB/ET0_MDC/PMGI0_MDC	P415/PIO_063/IRQ31/AN015/DA1
M11	PL5/GTADSM1/SSLC2/ET0_ETXD1/RMII0_TXD1	P212/PIO_052/GTCPPO10/SCK5-C/CTS5#-C/TXDB5-C/SSL11-D/USBHS_OVRCURA/IRQ28/ADTRG0#
M12	PL6/GTIOC2A/SSLC3/ET0_TX_EN/RMII0_TXD_EN	P214/PIO_054/GTCPPO12/TXD5-C/SMOSI5-C/SSDA5-C/TXDA5-C/SSL13-D/USBHS_EXICEN/IRQ30/ADTRG2#/PDMCLK0-E/PCINB0
M13	PM7/GTIOC3B/ET0_CRS/RMII0_CRS_DV/SDHI_WP	RES#
M14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14	VSS
M15	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ET0_ETXD1/RMII0_TXD1	VBATT/VCC

224-Pin	RX72N (224-Pin LFBGA)	RX74N (224-Pin LFBGA)
N1	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/GTIOC1A/SCK0/USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/PIXD6	PE07/PIO_047/A8-B/A20-C/TOC1/GTETRGD/ GTCPPO7/GTIOC10B/POEGD/XSPI1_CS0#-A/ PIXD7-C/IRQ7
N2	PH0/TIC0/GTETRGA/SCK7/RSPCKA	PE04/PIO_044/A11-B/A23-C/GTOWUP-C/ GTIOC9A/CTS12#-A/SSL11-A/XSPI1_IO2-A/ XSPI1_WP0#-C/PIXD4-C/IRQ12
N3	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/ SSCL10/RXD10/PIXD1	PE06/PIO_046/A9-B/A21-C/TIC1/GTETRGC/ GTADSM1/GTIOC10A/POEGB/SSL13-A/ XSPI1_DS-A/PIXD6-C/IRQ6
N4	P85/MTIOC6C/TIOCC0/LCD_DATA1-A	P602/PIO_010/CAS#-B/D21-B/GTIOC5A/ SCK8-B/CTS8#-B/TXDB8-B/MOSI0-D/ XSPI0_IO6-A/HSYNC-B/IRQ2/ADTRG2#
N5	P13/WR2#/BC2#/MTIOC0B/TIOCA5/TMO3/ PO13/GTADSM1/TXD2/SMOSI2/SSDA2/ SDA0[FM+]/LCD_TCON0-A/IRQ3/ADTRG1#	P601/PIO_009/RAS#-B/D22-B/GTIOC4B/ RXD8-B/SMISO8-B/SSCL8-B/RSPCK0-D/ GPTP_PTPOUT1/XSPI0_IO5-A/VSYNC-B/IRQ1/ ADTRG1#
N6	PJ1/MTIOC6A/RXD8/SMISO8/SSCL8/SSLC2-B/ EPLSOUT1/LCD_TCON3-A	P600/PIO_008/SDCS#-B/D23-B/GTIOC4A/ TXD8-B/SMOSI8-B/SSDA8-B/TXDA8-B/SSL00-D/ GPTP_PTPOUT0/XSPI0_IO4-A/PIXCLK-B/IRQ0/ ADTRG0#
N7	CLKOUT25M/P56/EDACK1/MTIOC3C/TIOCA1/ SCK7/RSPCKC-B/LCD_DATA4-A	P903/PIO_003/GTETRGD/GTCPPO9/POEGD/ CTS6#-B/CTS1#-C/RTS1#-C/SS1#-C/DE1-C/ TXDB1-C/XSPI0_WP1#-A/IRQ11/AN035
N8	VCC	P901/PIO_001/GTETRGB/GTCPPO6/TXD1-C/ SMOSI1-C/SSDA1-C/TXDA1-C/ XSPI0_RSTO1#-A/XSPI0_RESET0#-B/IRQ9/ AN033
N9	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/ ET0_COL/MMC_D7-A/LCD_DATA9-A/IRQ14	P404/PIO_052/IRQ12-DS/AN004
N10	P80/EDREQ0/MTIOC3B/PO26/SCK10/RTS10#/ ET0_TX_EN/RMII0_TXD_EN/QIO2-A/SDHI_WP/ MMC_D2-A/LCD_DATA14-A	P414/PIO_062/IRQ30/AN014/DA0
N11	PK2/GTETRGC/SMOSI8/SSDA8/TXD8/MISOB/ ET0_RX_DV	P210/PIO_050/GTETRGC/TXD4-C/SMOSI4-C/ SSDA4-C/TXDA4-C/MISO1-D/IRQ26/PCINZ1
N12	P76/CS6#/PO22/SMISO11/SSCL11/RXD11/ ET0_RX_CLK/REF50CK0/QSSL-A/SDHI_CMD-A/ MMC_CMD-A/LCD_DATA18-A	P213/PIO_053/GTCPPO11/RXD5-C/SMISO5-C/ SSCL5-C/SSL12-D/USBHS_VBUSEN/IRQ29/ ADTRG1#/PCINA0
N13	PM6/GTIOC3A/ET0_TX_CLK/SDHI_CD	P208/PIO_048/TIC1/GTETRGA/SCK4-C/ CTS4#-C/TXDB4-C/RSPCK1-D/IRQ24/PCINA1
N14	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/LCD_DATA22-A/IRQ12	P211/PIO_051/GTETRGD/CTS4#-C/RTS4#-C/ SS4#-C/DE4-C/TXDB4-C/CTS5#-C/SSL10-D/ USBHS_OVRCURB/IRQ27
N15	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV	P000/PIO_000/TMRI0/GTCPPO7/GTIOC10A/ POEGB/CTS0#-B/CTS7#-A/RTS7#-A/SS7#-A/ DE7-A/TXDB7-A/AUDIO_CLK/ET0_INT-D/ IRQ16-DS/AN016
P1	PK7/GTIOC1B	PE05/PIO_045/A10-B/A22-C/GTOWLO-C/ GTIOC9B/SSL12-A/XSPI1_IO3-A/PIXD5-C/IRQ5

224-Pin	RX72N (224-Pin LFBGA)	RX74N (224-Pin LFBGA)
P2	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/SCK1/ TXD3/SMOSI3/SSDA3/SDA2-DS/SSITXD0/ EPLSOUT0/SDHI_D3-C/PIXD3/IRQ7/ADTRG1#	PE03/PIO_043/A12-B/TOC3/GTOVLO-C/ GTIOC8B/CTS12#-A/RTS12#-A/SS12#-A/ DE12-A/TXDB12-A/MISO1-A/SD0DAT7-B/ XSPI1_IO1-A/PIXD3-C/IRQ11
P3	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMD-C/PIXD4/IRQ8	PE02/PIO_042/A13-B/TIC3/GTOVUP-C/ GTIOC8A/RXD12-A/SMISO12-A/SSCL12-A/ MOSI1-A/SD0DAT6-B/XSPI1_IO0-A/PIXD2-C/ IRQ7-DS
P4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/ PO15/GTETRGD/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/LCD_CLK-A/IRQ4	PD07/PIO_039/A16-B/D24-B/GTIW-C/GTIOC3B/ POEGA/TXD3-A/SMOSI3-A/SSDA3-A/TXDA3-A/ CTX1-B/SD0CD-B/XSPI0_CS0#-A/ XSPI0_RESET1#-B/PIXD7-B/IRQ7/AN031
P5	VCC_USB	PD05/PIO_037/A18-B/D26-B/GTIU-C/GTIOC2B/ POEGD/SCK3-A/CTS3#-A/TXDB3-A/SSL22-A/ CTX0-B/SD0DAT1-B/XSPI0_IO3-A/PIXD5-B/ IRQ5/AN029
P6	VSS_USB	PD03/PIO_035/A20-B/D28-B/TOC2/GTIOC1B/ POEGA/TXD2-A/SMOSI2-A/SSDA2-A/TXDA2-A/ MISO2-A/SD0CLK-B/XSPI0_IO1-A/PIXD3-B/ IRQ3/AN027
P7	P57/RXD7/SMISO7/SSCL7/SSLC0-B/ LCD_DATA3-A	PD02/PIO_034/A21-B/D29-B/TIC2/GTETRGB/ GTIOC1A/POEGB/RXD2-A/SMISO2-A/SSCL2-A/ MOSI2-A/SD0CMD-B/XSPI0_IO0-A/PIXD2-B/ IRQ2/AN026
P8	P11/MTIC5V/TMCI3/SCK2/EPLSOUT1/ LCD_DATA7-A/IRQ1	AVSS0
P9	VSS	VREFL0
P10	P82/EDREQ1/MTIOC4A/PO28/GTIOC2A/ SMOSI10/SSDA10/TXD10/ET0_ETXD1/ RMII0_TXD1/MMC_D4-A/LCD_DATA12-A	P403/PIO_051/IRQ11-DS/AN003
P11	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/ POE0#/GTETRGC/SCK5/CTS8#/SS8#/SS10#/ CTS10#/RTS10#/SSLA0-A/ET0_TX_CLK/QMI-A/ QIO1-A/SDHI_D1-A/MMC_D1-A/LCD_DATA15-A	P401/PIO_049/IRQ9-DS/AN001
P12	PL2/GTETRGC/SMOSI9/SSDA9/TXD9/MISOC/ ET0_RX_ER/RMII0_RX_ER	P006/PIO_006/GTCPPO5/GTIOC13A/GTIOC9B/ SCK0-B/CTS0#-B/TXDB0-B/IRQ22-DS/ ADTRG1#/AN022/PDMCLK0-C/PCOUTZ1
P13	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ET0_RX_DV/ SDHI_D3-A/MMC_CD-A/LCD_DATA19-A	P004/PIO_004/GTCPPO3/GTIOC12A/GTIOC8B/ TXD0-B/SMOSI0-B/SSDA0-B/TXDA0-B/ SSITXD1/IRQ20-DS/AN020/PCOUTA1
P14	PM4/GTADSM0/ET0_ETXD2/SDHI_D2-D/QIO2-A	P003/PIO_003/GTCPPO2/GTIOC11B/GTIOC8A/ RXD7-A/SMISO7-A/SSCL7-A/SSIRXD1/ ET0_MDIO-D/IRQ19-DS/AN019/PCOUTB0
P15	PM3/GTETRGD/RTS10#/CTS10#/SS10#/ ET1_ERXD3/SDHI_D1-D/QMI-A/QIO1-A	P001/PIO_001/TMCI0/GTCPPO0/GTIOC10B/ GTIOC7A/SCK7-A/CTS7#-A/TXDB7-A/SSIBCK0/ ET0_LINKSTA-D/IRQ17-DS/AN017/PCOUTZ0
R1	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/ GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/PIXD5/ IRQ9	VSS

224-Pin	RX72N (224-Pin LFBGA)	RX74N (224-Pin LFBGA)
R2	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/ SSDA10/TXD10/EPLSOUT1/SDHI_D2-C/PIXD2	CLKOUT/PE01/PIO_041/A14-B/GTOULO-C/ GTIOC7B/TXD12-A/SMOSI12-A/SSDA12-A/ TXDA12-A/RSPCK1-A/SD0DAT5-B/XSPI1_CK-A/ PIXD1-C/IRQ9
R3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/ PO14/RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/ SMISO3/SSCL3/SCL2-DS/USB0_VBUSEN/ USB0_VBUS/USB0_OVRCURB/IRQ6/ADTRG0#	ETHPHYCLK/PE00/PIO_040/A15-B/GTOUUP-C/ GTIOC7A/SCK12-A/CTS12#-A/TXDB12-A/ SSL10-A/SD0DAT4-B/XSPI1_CKN#-A/ XSPI1_CS1#-B/PIXD0-C/IRQ8
R4	P12/WR3#/BC3#/MTIC5U/TMCI1/GTADSM0/ RXD2/SMISO2/SSCL2/SCL0[FM+]/ LCD_TCON1-A/IRQ2	PD06/PIO_038/A17-B/D25-B/GTIV-C/GTIOC3A/ POEGB/RXD3-A/SMISO3-A/SSCL3-A/SSL23-A/ CRX1-B/SD0WP-B/XSPI0_DS-A/PIXD6-B/IRQ6/ AN030
R5	USB0_DM	PD04/PIO_036/A19-B/D27-B/GTETRGA/ GTIOC2A/POEGC/CTS2#-A/CTS3#-A/RTS3#-A/ SS3#-A/DE3-A/TXDB3-A/SSL21-A/CRX0-B/ SD0DAT0-B/XSPI0_IO2-A/XSPI0_WP0#-B/ PIXD4-B/IRQ4/AN028
R6	USB0_DP	PD00/PIO_032/A23-B/D31-B/GTETRGD/ GTIOC0A/POEGD/CTS2#-A/RTS2#-A/SS2#-A/ DE2-A/TXDB2-A/CTS3#-A/SSL20-A/SD0DAT2-B/ XSPI0_CKN#-A/XSPI0_CS1#-B/PIXD0-B/IRQ0/ AN024
R7	P54/D1[A1/D1]/EDACK0/ALE/MTIOC4B/TMCI1/ CTS2#/RTS2#/SS2#/MOSIC-B/CTX1/ ET0_LINKSTA/LCD_DATA6-A	PD01/PIO_033/A22-B/D30-B/GTETRGC/ GTIOC0B/POEGC/SCK2-A/CTS2#-A/TXDB2-A/ RSPCK2-A/SD0DAT3-B/XSPI0_CK-A/PIXD1-B/ IRQ1/AN025
R8	P55/D0[A0/D0]/EDREQ0/WAIT#/MTIOC4D/ TMO3/TXD7/SMOSI7/SSDA7/MISOC-B/CRX1/ ET0_EXOUT/LCD_DATA5-A/IRQ10	AVCC0
R9	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/MTCLKA/ TMCI2/PO30/TIC0/GTIOC3B/RXD8/SMISO8/ SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ ET0_ETXD3/MMC_D6-A/LCD_DATA10-A/IRQ13	VREFH0
R10	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/RTS8#/ SCK10/RSPCKA-A/ET0_ETXD2/MMC_D5-A/ LCD_DATA11-A	P402/PIO_050/IRQ10-DS/AN002
R11	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/MMC_D0-A/LCD_DATA16-A	P400/PIO_048/IRQ8-DS/AN000
R12	PL4/GTADSM0/SSLC1/ET0_ETXD0/RMII0_TXD0	P007/PIO_007/GTCPPO6/GTIOC13B/POEGA/ CTS0#-B/RTS0#-B/SS0#-B/DE0-B/TXDB0-B/ IRQ23-DS/ADTRG0#/AN023/PDMDAT0-C
R13	P75/CS5#/PO20/SCK11/RTS11#/ET0_ERXD0/ RMII0_RXD0/SDHI_D2-A/MMC_RES#-A/ LCD_DATA20-A	P005/PIO_005/GTCPPO4/GTIOC12B/GTIOC9A/ RXD0-B/SMISO0-B/SSCL0-B/SSILRCK1/ IRQ21-DS/ADTRG2#/AN021/PCOUTB1
R14	P74/A20/CS4#/PO19/SS11#/CTS11#/ ET0_ERXD1/RMII0_RXD1/LCD_DATA21-A	P002/PIO_002/TMCI1/GTCPPO1/GTIOC11A/ GTIOC7B/TXD7-A/SMOSI7-A/SSDA7-A/ TXDA7-A/SSIBCK1/ET0_MDC-D/IRQ18-DS/ AN018/PCOUTA0
R15	PM5/GTADSM1/ET0_ETXD3/SDHI_D3-D/QIO3-A	NC

Note: 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

3.2 176-Pin LFBGA Package

Table 3.3 is Comparative Listing of RX72M/RX74M 176-Pin LFBGA Package Pin Functions, and Table 3.4 is Comparative Listing of RX72N/RX74N 176-Pin LFBGA Package Pin Functions.

Table 3.3 Comparative Listing of RX72M/RX74M 176-Pin LFBGA Package Pin Functions

176-Pin LFBGA	RX72M	RX74M
A1	AVSS0	PC01/PIO_025/D6-A/GTOULO-B/GTIOC7B/ SCK11-A/CTS11#-A/TXDB11-A/SSL02-A/ SDA00-C/ET0_TXD0-A/RMII0_TXD0-A/ RGMII0_TXD0-A/CAT0_ETXD0-A/SD0DAT3-A/ IRQ12/PCOUTB0
A2	AVCC0	PC03/PIO_027/D4-A/GTOVLO-B/GTIOC8B/ TXD11-A/SMOSI11-A/SSDA11-A/TXDA11-A/ SDAHS1-C/ET0_TXD2-A/RGMII0_TXD2-A/ CAT0_ETXD2-A/SD0CLK-A/IRQ11/PCOUTA1
A3	VREFL0	PC05/PIO_029/D2-A/TMRI2/GTOWLO-B/ GTIOC9B/SCK8-A/CTS8#-A/TXDB8-A/ RSPCK0-A/SSIBCK0/ET0_TX_EN-A/ RMII0_TX_EN-A/RGMII0_TX_CTL-A/ CAT0_TX_EN-A/SD0DAT1-A/IRQ5/PCOUTZ1
A4	P42/IRQ10-DS/AN002	ETHPHYCLK/PC07/PIO_031/D0-A/TMO2/TOC0/ CACREF/GTETRGD/GTADSM1/GTIOC15B/ POEGA/TXD8-A/SMOSI8-A/SSDA8-A/TXDA8-A/ MISO0-A/SSITXD0/RGMII0_TXC-A/ CATRESTOUT-A/SD0CD-A/IRQ14/DSMDAT5-C/ PDMDAT0-A
A5	P46/IRQ14-DS/AN006	CLKOUT/P801/PIO_057/EBCLK-A/GTIV-B/ GTIOC0B/POEGC/TXD10-B/SMOSI10-B/ SSDA10-B/TXDA10-B/ET0_CRS-B/ CATSYNC0-A/IRQ9/ADCNV1-B/DSMDAT4-C
A6	VCC	P503/PIO_035/WR3#-A/BC3#-A/A19-C/GTIOC3B/ RXD2-C/SMISO2-C/SSCL2-C/CRX1-C/ USB0_OVRCURB/SSIRXD0/ET1_WOL-B/ CATLEDERR-A/SD0DAT7-A/IRQ3/DSMDAT1-E
A7	VSS	VLO
A8	P94/D20/A20/ET1_ERXD0/RMII1_RXD0/ CAT1_ERXD0	VSS_DCDC
A9	VCC	VCC_DCDC
A10	TRSYNC1/P97/D23/A23/ET1_ERXD3/ CAT1_ERXD3	P102/PIO_010/TMCI1/GTADSM0/GTIOC13A/ SCL00-A/ET0_COL-D/CATI2CCLK-A/IRQ2
A11	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/ET1_RX_CLK/REF50CK1/ CAT1_RX_CLK/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/IRQ6/AN106	CLKOUT/P106/PIO_014/TMO2/RTCOUT/GTIU-D/ GTIOC15A/POEGB/RXD3-B/SMISO3-B/ SSCL3-B/SCLHS2-A/ET0_TXD2-B/ CAT0_ETXD2-B/CATI2CCLK-B/SD0DAT2-C/ PIXD2-A/IRQ30-DS/ADTRG0#/PCINA1
A12	P60/CS0#/ET1_TX_EN/RMII1_TXD_EN/ CAT1_TX_EN	P200/PIO_016/TMRI0/GTETRGA/GTIOC3A/ GTIOC14A/CTS6#-A/RTS6#-A/SS6#-A/DE6-A/ TXDB6-A/MOSI0-C/SDAHS1-A/ USB0_ID/SSIRXD0/ET0_TX_EN-B/ RMII0_TX_EN-B/CAT0_TX_EN-B/ SD0CMD-C/PIXD4-A/IRQ8/ADTRG2#/PCINZ1
A13	P63/CAS#/D2[A2/D2]/CS3#/ET1_ETXD1/ RMII1_TXD1/CAT1_ETXD1	P805/PIO_061/GTADSM1/GTIOC15B/SCK5-B/ CTS5#-B/TXDB5-B/SSL22-B/CRX0-D/ USB0_VBUSEN/USBHS_VBUSEN/ET0_TXD0-C/ RMII0_TXD0-C/CAT0_ETXD0-C/HSYNC-D/ IRQ5/ADSYNC-C/DSMDAT0-F/PCINB0

176-Pin LFBGA	RX72M	RX74M
A14	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/MTIOC3B/PO18/GTIOC1B/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/MMC_D5-B/LCD_DATA15-B/ANEX1	TCK/SWCLK/P301/PIO_025/TMCI3/GTCPPO11/SCK0-A/CTS0#-A/TXDB0-A/SCK1-A/CTS1#-A/TXDB1-A/RSPCK1-C/ET1_WOL-D/IRQ7
A15	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/PO23/TIC3/GTIOC0B/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/MMC_D6-B/LCD_DATA14-B/IRQ7-DS/AN100	TDO/P302/PIO_026/TMRI3/GTCPPO12/TXD0-A/SMOSI0-A/SSDA0-A/TXDA0-A/TXD1-A/SMOSI1-A/SSDA1-A/TXDA1-A/MOSI1-C/ET1_COL-D/IRQ4
B1	P05/SSILRCK1/IRQ13/DA1	PC00/PIO_024/D7-A/GTOUUP-B/GTIOC7A/CTS11#-A/RTS11#-A/SS11#-A/DE11-A/TXDB11-A/SSL01-A/SCL00-C/ET0_TX_CLK-A/CAT0_TX_CLK-A/SD0DAT2-A/IRQ14/PCOUTA0
B2	P07/IRQ15/ADTRG0#	PC02/PIO_026/D5-A/GTOVUP-B/GTIOC8A/RXD11-A/SMISO11-A/SSCL11-A/SSL03-A/SCLHS1-C/ET0_TXD1-A/RMII0_TXD1-A/RGMII0_TXD1-A/CAT0_ETXD1-A/SD0CMD-A/IRQ10/PCOUTZ0
B3	P40/IRQ8-DS/AN000	PC04/PIO_028/D3-A/TMCI1/GTOWUP-B/GTIOC9A/CTS8#-A/RTS8#-A/SS8#-A/DE8-A/TXDB8-A/CTS11#-A/SSL00-A/AUDIO_CLK/ET0_TXD3-A/RGMII0_TXD3-A/CAT0_ETXD3-A/SD0DAT0-A/IRQ12/PCOUTB1
B4	P41/IRQ9-DS/AN001	PC06/PIO_030/D1-A/TMCI2/TIC0/GTETRGC/GTCPPO7/GTIOC15A/POEGB/RXD8-A/SMISO8-A/SSCL8-A/MOSI0-A/SSILRCK0/ET0_TX_ER-A/CATLINKACT0-A/SD0WP-A/IRQ13/DSMCLK5-C/PDMCLK0-A
B5	P47/IRQ15-DS/AN007	P803/PIO_059/CS3#-A/WR1#-B/BC1#-B/GTIOC1B/POEGA/CTS10#-B/RTS10#-B/SS10#-B/DE10-B/TXDB10-B/CTX2-D/USB0_ID/ET0_MDC-B/CAT0_MDC-B/IRQ3/ADSYNC-B/DSMDAT3-C
B6	P91/D17/A17/SCK7/ET1_COL/AN115/DSMDAT5	P502/PIO_034/WR2#-A/BC2#-A/A18-C/GTIOC3A/TXD2-C/SMOSI2-C/SSDA2-C/TXDA2-C/SSL13-C/CTX1-C/ET0_WOL-B/CATLEDRUN-A/SD0DAT6-A/IRQ2/ADST2-C/DSMCLK1-E
B7	P92/D18/A18/POE4#/RXD7/SMISO7/SSCL7/ET1_CRS/RMII1_CRS_DV/CAT1_RX_DV/AN116/DSMCLK4	VLO
B8	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/AN109	VSS_DCDC
B9	TRDATA5/P96/D22/A22/ET1_ERXD2/CAT1_ERXD2	VCC_DCDC
B10	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0-A/ET1_MDIO/PMGI1_MDIO/QSSL-B/SDHI_CMD-B/MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112	P103/PIO_011/TMO3/GTADSM1/GTIOC13B/CTS2#-B/SDA00-A/ET0_CRS-D/CATI2CDATA-A/IRQ3
B11	TRDATA7/PG1/D25/ET1_RX_ER/RMII1_RX_ER/CAT1_RX_ER	P107/PIO_015/TMO1/GTIV-D/GTIOC15B/POEGA/TXD3-B/SMOSI3-B/SSDA3-B/TXDA3-B/SDAHS2-A/SSITXD0/ET0_TXD3-B/CAT0_ETXD3-B/CATI2CDATA-B/SD0DAT3-C/PIXD3-A/IRQ31-DS/ADTRG1#/PCINB1
B12	VSS	P201/PIO_017/TMCI0/GTIW-D/GTIOC3B/GTIOC14B/SCK6-A/CTS6#-A/TXDB6-A/MISO0-C/SCLHS1-A/USB0_EXICEN/SSILRCK0/ET0_RX_ER-B/RMII0_RX_ER-B/CAT0_RX_ER-B/SD0CLK-C/PIXD5-A/IRQ9/PCINZ0

176-Pin LFBGA	RX72M	RX74M
B13	P64/WE#/D3[A3/D3]/CS4#/ET1_ETXD0/ RMII1_TXD0/CAT1_ETXD0	P804/PIO_060/GTADSM0/GTIOC15A/CTS5#-B/ RTS5#-B/SS5#-B/DE5-B/TXDB5-B/SSL21-B/ CTX0-D/USB0_OVRCURA/USBHS_OVRCURA/ ET0_TX_EN-C/RMII0_TX_EN-C/CAT0_TX_EN-C/ PCKO-D/IRQ4/DSMCLK0-F/PCINA0
B14	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/GTIOC2B/ SCK12/SSLB1-B/MMC_D4-B/LCD_DATA16-B/ ANEX0	TMS/SWDIO/P300/PIO_024/TMO1/GTCPPO10/ CTS0#-A/RTS0#-A/SS0#-A/DE0-A/TXDB0-A/ CTS1#-A/RTS1#-A/SS1#-A/DE1-A/TXDB1-A/ SSL10-C/ET0_WOL-D/IRQ6
B15	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/CTS12#/RTS12#/SS12#/ ET0_ERXD3/CAT0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101	TDI/P303/PIO_027/TMCI2/GTCPPO13/RXD0-A/ SMISO0-A/SSCL0-A/RXD1-A/SMISO1-A/ SSCL1-A/MISO1-C/ET1_CRS-D/IRQ1
C1	AVSS1	PB06/PIO_022/D9-A/GTOWUP-A/GTIOC6A/ RXD9-A/SMISO9-A/SSCL9-A/ET0_RX_ER-A/ RMII0_RX_ER-A/CAT0_RX_ER-A/IRQ6
C2	AVCC1	PB07/PIO_023/D8-A/GTOWLO-A/GTIOC6B/ TXD9-A/SMOSI9-A/SSDA9-A/TXDA9-A/ ET0_LINKSTA-A/CAT0_LINKSTA-A/IRQ15
C3	VREFH0	P802/PIO_058/CS2#-A/WR#-B/WR0#-B/GTIW-B/ GTIOC1A/POEGB/SCK10-B/CTS10#-B/TXDB10-B/ CRX2-D/USB0_EXICEN/ET0_MDIO-B/ CAT0_MDIO-B/IRQ2/ADCNV2-B/DSMCLK3-C
C4	P43/IRQ11-DS/AN003	VCC
C5	P45/IRQ13-DS/AN005	P500/PIO_032/WR#-A/WR0#-A/A16-C/GTIOC2A/ CTS2#-C/RTS2#-C/SS2#-C/DE2-C/TXDB2-C/ CTS7#-B/SSL11-C/CTX0-C/ET0_LINKSTA-B/ CAT0_LINKSTA-B/SD0DAT4-A/IRQ0/ADST0-C/ DSMCLK2-E
C6	P90/D16/A16/TXD7/SMOSI7/SSDA7/ ET1_RX_DV/CAT1_RX_DV/AN114/DSMCLK5	P501/PIO_033/WR1#-A/BC1#-A/A17-C/GTIOC2B/ SCK2-C/CTS2#-C/TXDB2-C/SSL12-C/CRX0-C/ ET0_INT-B/CATLEDSTER-A/SD0DAT5-A/IRQ1/ ADST1-C/DSMDAT2-E
C7	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108	VLO
C8	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/ET1_EXOUT/QIO2-B/ SDHI_D2-B/MMC_D2-B/LCD_DATA22-B/IRQ2/ AN110	VCC_DCDC
C9	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/ET1_WOL/QIO3-B/ SDHI_D3-B/MMC_D3-B/LCD_DATA21-B/IRQ3/ AN111	VCC
C10	TRDATA6/PG0/D24/ET1_RX_CLK/REF50CK1/ CAT1_RX_CLK	P100/PIO_008/CS1#-B/WAIT#-A/TMRI3/CACREF/ GTIU-E/GTADSM0/GTIOC12A/CTS2#-B/RTS2#-B/ SS2#-B/DE2-B/TXDB2-B/CTS5#-B/ USB0_OVRCURB-DS/USBHS_VBUS/ ET0_TX_ER-B/CATLINKACT0-B/CATLEDERR-C/ IRQ0/ADTRG2#/DSMCLK0-C
C11	VCC	P104/PIO_012/TMRI2/GTIW-E/GTIOC14A/ RXD2-B/SMISO2-B/SSCL2-B/CTS3#-B/RTS3#-B/ SS3#-B/DE3-B/TXDB3-B/CTX2-A/ USB0_OVRCURA-DS/USBHS_VBUS/ ET0_TXD0-B/RMII0_TXD0-B/CAT0_ETXD0-B/ CATLEDSTER-C/PIXD0-A/IRQ4/ADST0-A/ DSMCLK1-C/PCINA0

176-Pin LFBGA	RX72M	RX74M
C12	P62/RAS#/D1[A1/D1]/CS2#/ET1_ERXD0/ RMII1_RXD0/CAT1_ERXD0	CLKOUT/P205/PIO_021/A21-C/CS6#-C/ GTOVLO-D/GTIOC1B/GTIOC5B/SCK1-B/ CTS1#-B/TXDB1-B/RSPCK1-B/SDAHS1-B/ CRX0-A/USB0_VBUS/USBHS_VBUSEN/ SSIRXD1/ET0_RXD1-B/RMII0_RXD1-B/ CAT0_ERXD1-B/SD0CD-C/HSYNC-A/IRQ5/ ADTRG0#/DSMDAT4-B/PCOUTB1
C13	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/CAT0_ERXD2/LCD_DATA12-B/ AN102	ETHPHYCLK/P304/PIO_028/ALE-C/WAIT#-B/ TMCI3/GTETRGD/GTCPPO0/POEGA/CTS0#-A/ CTS1#-A/USB0_VBUSEN/USBHS_ID/ET0_INT-E/ CATRESTOUT-D/IRQ0-DS/ADTRG0#
C14	VSS	P202/PIO_018/CS3#-B/BREQ#-A/TMO0/ GTOUUP-D/GTIOC0A/GTIOC4A/TXD6-A/ SMOSI6-A/SSDA6-A/TXDA6-A/RSPCK0-C/ SCL00-B/CTX2-B/USB0_OVRCURA/ USBHS_EXICEN/AUDIO_CLK/ET0_RX_DV-B/ RMII0_CRS_DV-B/CAT0_RX_DV-B/ CATI2CCLK-C/SD0DAT0-C/PIXD6-A/IRQ15/ DSMCLK3-B/PDMCLK0-B
C15	P70/SDCLK/CATLINKACT0	P203/PIO_019/CS2#-B/BACK#-A/GTOULO-D/ GTIOC0B/GTIOC4B/RXD6-A/SMISO6-A/ SSCL6-A/CTS3#-B/SSL00-C/SDA00-B/CRX2-B/ USB0_OVRCURB/USBHS_ID/SSIBCK0/ ET0_RX_CLK-B/RMII0_REF50CK-B/ CAT0_RX_CLK-B/CATI2CDATA-C/SD0DAT1-C/ PIXD7-A/IRQ3/DSMDAT3-B/PDMDAT0-B
D1	P01/TMCI0/RXD6/SMISO6/SSCL6/SSIBCK0/ CATLEDERR/IRQ9/AN119	PB04/PIO_020/D11-A/GTOVUP-A/GTIOC5A/ CTS4#-A/CTS9#-A/RTS9#-A/SS9#-A/DE9-A/ TXDB9-A/ET0_RX_CLK-A/RMII0_REF50CK-A/ RGMII0_RXC-A/CAT0_RX_CLK-A/IRQ4
D2	P02/TMCI1/SCK6/SSIBCK1/CATLEDSTER/ IRQ10/AN120	PB05/PIO_021/D10-A/TMRI1/GTOVLO-A/ GTIOC5B/SCK9-A/CTS9#-A/TXDB9-A/ ET0_RX_DV-A/RMII0_CRS_DV-A/ RGMII0_RX_CTL-A/CAT0_RX_DV-A/IRQ13
D3	P03/SSIDATA1/IRQ11/DA0	PG01/PIO_057/DQM0-A/WR#-C/WR0#-C/ GTCPPO1/RXD8-C/SMISO8-C/SSCL8-C/ ET1_RX_DV-A/RMII1_CRS_DV-A/ RGMII1_RX_CTL-A/CAT1_RX_DV-A/IRQ9/ DSMDAT2-D
D4	P00/TMRI0/TXD6/SMOSI6/SSDA6/AUDIO_CLK/ CATLATCH1/IRQ8/AN118	P800/PIO_056/CS1#-A/DQM0-B/GTIU-B/ GTIOC0A/POEGD/RXD10-B/SMISO10-B/ SSCL10-B/ET0_COL-B/CATLATCH0-A/IRQ8/ ADCNV0-B/DSMCLK4-C
D5	P44/IRQ12-DS/AN004	VCC
D6	P93/D19/A19/POE0#/CTS7#/RTS7#/SS7#/ ET1_LINKSTA/CAT1_LINKSTA/AN117/ DSMDAT4	VSS
D7	TRDATA4/P95/D21/A21/ET1_ERXD1/ RMII1_RXD1/CAT1_ERXD1	VCL
D8	VSS	P101/PIO_009/CS0#-A/ALE-B/TMCI3/GTETRGC/ GTADSM1/GTIOC12B/SCK2-B/CTS2#-B/ TXDB2-B/USB0_VBUS-DS/USBHS_EXICEN/ ET0_TX_CLK-B/CAT0_TX_CLK-B/ CAT0_LINKSTA-D/IRQ1/ADTRG1#/DSMDAT0-C
D9	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/MTCLKA/ POE10#/SSLC1-A/ET1_MDC/PMGI1_MDC/ QSPCLK-B/SDHI_CLK-B/MMC_CLK-B/ LCD_DATA19-B/IRQ5/AN113	VSS

176-Pin LFBGA	RX72M	RX74M
D10	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ ET1_RX_ER/RMII1_RX_ER/CAT1_RX_ER/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B/IRQ7/AN107	VCL
D11	P61/SDCS#/D0[A0/D0]/CS1#/ET1_ERXD1/ RMII1_RXD1/CAT1_ERXD1	P105/PIO_013/TMCI2/GTIV-E/GTIOC14B/ TXD2-B/SMOSI2-B/SSDA2-B/TXDA2-B/SCK3-B/ CTS3#-B/TXDB3-B/CRX2-A/USB0_VBUS/ USBHS_OVRCURB/SSILRCK1/ET0_TXD1-B/ RMII0_TXD1-B/CAT0_ETXD1-B/CATLEDRUN-C/ PIXD1-A/IRQ29-DS/ADST1-A/DSMDAT1-C/ PCINB0
D12	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ET0_RX_CLK/ REF50CK0/CAT0_RX_CLK/LCD_DATA11-B/ IRQ5/AN103	VCC
D13	VCC	ETHPHYCLK/P204/PIO_020/A20-C/CS7#-C/ TMRI1/GTOVUP-D/GTIOC1A/GTIOC5A/ CTS1#-B/RTS1#-B/SS1#-B/DE1-B/TXDB1-B/ SSL10-B/SCLHS1-B/CTX0-A/USB0_VBUSEN/ USBHS_VBUS-DS/SSIBCK1/ET0_RXD0-B/ RMII0_RXD0-B/CAT0_ERXD0-B/SD0WP-C/ PIXCLK-A/IRQ12/DSMCLK4-B/PCOUTA1
D14	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105	PF00/PIO_048/GTCPPO14/USB0_DP/IRQ0
D15	P65/CKE/CS5#	PF01/PIO_049/GTCPPO15/USB0_DM/IRQ1
E1	PJ5/POE8#/CTS2#/RTS2#/SS2#/SSIRXD0/ EPLSOUT0/CATSYNC0	PB02/PIO_018/D13-A/GTOUUP-A/GTIOC4A/ CTS4#-A/RTS4#-A/SS4#-A/DE4-A/TXDB4-A/ CTS9#-A/ET0_RXD2-A/RGMII0_RXD2-A/ CAT0_ERXD2-A/IRQ2
E2	EMLE	PB03/PIO_019/D12-A/TMO0/GTOULO-A/ GTIOC4B/SCK4-A/CTS4#-A/TXDB4-A/ ET0_RXD3-A/RGMII0_RXD3-A/CAT0_ERXD3-A/ IRQ3
E3	PF5/WAIT#/SSILRCK0/CATLATCH0/IRQ4	PG00/PIO_056/DQM1-A/WR1#-C/BC1#-C/ GTCPPO0/SCK8-C/CTS8#-C/TXDB8-C/ ET1_RX_CLK-A/RMII1_REF50CK-A/ RGMII1_RXC-A/CAT1_RX_CLK-A/IRQ8/ DSMCLK2-D
E4	VSS	VSS
E12	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/AN104	VSS
E13	TRDATA0/PG2/D26/ET1_TX_CLK/ CAT1_TX_CLK	P206/PIO_022/A22-C/CS5#-C/TMO3/RTCOUT/ GTOWUP-D/GTIOC2A/GTIOC6A/CTS6#-A/ TXD1-B/SMOSI1-B/SSDA1-B/TXDA1-B/ MOSI1-B/SCLHS2-B/CTX1-A/USB0_EXICEN/ USBHS_OVRCURA-DS/SSITXD1/ET0_RXD2-B/ CAT0_ERXD2-B/VSYNC-A/IRQ2-DS/ADTRG1#/ DSMCLK5-B/PCOUTZ1
E14	TRDATA1/PG3/D27/ET1_ETXD0/RMII1_TXD0/ CAT1_ETXD0	VSS_USB
E15	P67/DQM1/CS7#/MTIOC7C/GTIOC1B/CRX2/ EPLSOUT1/CATSYNC1/IRQ15	VCC_USB
F1	VBATT	PB00/PIO_016/D15-A/GTETRGA/GTADSM0/ GTIOC14A/POEGC/RXD4-A/SMISO4-A/ SSCL4-A/ET0_RXD0-A/RMII0_RXD0-A/ RGMII0_RXD0-A/CAT0_ERXD0-A/IRQ12/ ADST2-A/DSMCLK2-A/PCINA1

176-Pin LFBGA	RX72M	RX74M
F2	VCL	PB01/PIO_017/D14-A/TMCI0/GTETRGB/ GTCPPO4/GTIOC14B/POEGA/TXD4-A/ SMOSI4-A/SSDA4-A/TXDA4-A/ET0_RXD1-A/ RMII0_RXD1-A/RGMII0_RXD1-A/ CAT0_ERXD1-A/IRQ4-DS/DSMDAT2-A/PCINB1
F3	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/SS6#/ CTS0#/RTS0#/SS0#/SSITXD0/ET0_EXOUT/ CATRESTOUT	PG02/PIO_058/DQM3-A/WR3#-C/BC3#-C/ GTIOC11A/TXD8-C/SMOSI8-C/SSDA8-C/ TXDA8-C/ET1_RX_ER-A/RMII1_RX_ER-A/ CAT1_RX_ER-A/IRQ10/DSMCLK1-D
F4	BSCANP	VCL
F12	P66/DQM0/CS6#/MTIOC7D/GTIOC2B/CTX2	VCL
F13	TRSYNC/PG4/D28/ET1_ETXD1/RMII1_TXD1/ CAT1_ETXD1	AVSS_USBHS
F14	PA0/DQM2/BC0#/A0/MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/CAT0_TX_EN/ CATLEDRUN/LCD_DATA8-B	USBHS_DP
F15	VSS	USBHS_DM
G1	XCIN	PA06/PIO_014/A1-A/DQM2-B/TMCI3/GTIOC3A/ GTIOC13A/TXD10-A/SMOSI10-A/SSDA10-A/ TXDA10-A/MOSI0-B/ET1_TXD3-A/ RGMII1_TXD3-A/CAT1_ETXD3-A/IRQ14/PCINZ1
G2	XCOUT	ETHPHYCLK/PA07/PIO_015/A0-A/BC0#-A/ DQM1-B/GTIOC3B/GTIOC13B/RXD10-A/ SMISO10-A/SSCL10-A/MISO0-B/ET1_TX_ER-A/ CATLINKACT1-A/IRQ7/PCINB0
G3	MD/FINED	P706/PIO_054/CAS#-A/CS6#-A/GTIOC13A/ RXD11-B/SMISO11-B/SSCL11-B/ET1_RXD2-A/ RGMII1_RXD2-A/CAT1_ERXD2-A/ XSPI1_WP1#-B/IRQ14/ADCNV2-C/DSMCLK0-D
G4	TRST#/PF4	VCC
G12	TRCLK/PG5/D29/ET1_ETXD2/CAT1_ETXD2	AVCC_USBHS
G13	TRDATA2/PG6/D30/ET1_ETXD3/CAT1_ETXD3	USBHS_RREF
G14	PA1/DQM3/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/IRQ11	VSS_USBHS
G15	VCC	VCC_USBHS
H1	XTAL/P37	PA04/PIO_012/A3-A/TMRI0/GTIOC2A/ GTIOC12A/CTS10#-A/RTS10#-A/SS10#-A/ DE10-A/TXDB10-A/SSL00-B/ET1_TXD1-A/ RMII1_TXD1-A/RGMII1_TXD1-A/CAT1_ETXD1-A/ IRQ5-DS/PCINZ0
H2	VSS	PA05/PIO_013/A2-A/GTIOC2B/GTIOC12B/ SCK10-A/CTS10#-A/TXDB10-A/RSPCK0-B/ ET1_TXD2-A/RGMII1_TXD2-A/CAT1_ETXD2-A/ IRQ5/PCINA0
H3	RES#	P707/PIO_055/WE#-A/CS7#-A/GTIOC13B/ TXD11-B/SMOSI11-B/SSDA11-B/TXDA11-B/ ET1_RXD3-A/RGMII1_RXD3-A/CAT1_ERXD3-A/ XSPI1_RESET1#-B/IRQ7/DSMDAT0-D
H4	UPSEL/P35/NMI	VSS
H12	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/ TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC/ CAT0_MDC/CATIRQ/PMGI0_MDC/ LCD_DATA4-B/IRQ5-DS	P207/PIO_023/A23-C/CS4#-C/TMRI3/ GTOWLO-D/GTIOC2B/GTIOC6B/RXD1-B/ SMISO1-B/SSCL1-B/MISO1-B/SDAHS2-B/ CRX1-A/USB0_ID/USBHS_OVRCURB-DS/ ET0_RXD3-B/CAT0_ERXD3-B/PCKO-A/ IRQ3-DS/ADTRG2#/DSMDAT5-B

176-Pin LFBGA	RX72M	RX74M
H13	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/ CAT0_MDIO/PMGI0_MDIO/LCD_DATA5-B/ IRQ6-DS	VSS
H14	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/CATLINKACT1/ LCD_DATA6-B	EXTAL/P306
H15	TRDATA3/PG7/D31/ET1_TX_ER	XTAL/P307
J1	EXTAL/P36	PA02/PIO_010/A5-A/GTIW-A/GTIOC1A/ GTIOC11A/TXD5-A/SMOSI5-A/SSDA5-A/ TXDA5-A/SSL03-B/ET1_TX_CLK-A/ CAT1_TX_CLK-A/IRQ10/ADCNV2-A/DSMCLK1-A
J2	VCC	PA03/PIO_011/A4-A/GTIOC1B/GTIOC11B/ RXD5-A/SMISO5-A/SSCL5-A/ET1_TXD0-A/ RMII1_TXD0-A/RGMII1_TXD0-A/CAT1_ETXD0-A/ IRQ6-DS/ADSYNC-A/DSMDAT1-A
J3	P34/MTIOC0A/TMCI3/PO12/POE10#/SCK6/ SCK0/ET0_LINKSTA/CAT0_LINKSTA/IRQ4/ DSMDAT0	P705/PIO_053/RAS#-A/CS5#-A/GTIOC12B/ SCK11-B/CTS11#-B/TXDB11-B/ET1_RXD1-A/ RMII1_RXD1-A/RGMII1_RXD1-A/ CAT1_ERXD1-A/XSPI1_RSTO1#-B/IRQ13/ ADCNV1-C/DSMDAT5-D
J4	TMS/PF3	VCL
J12	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/CAT0_LINKSTA/ LCD_DATA3-B	VCL
J13	VSS	P305/NMI/IRQ0
J14	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B	VSS
J15	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/RTS5#/SS5#/ MOSIA-B/ET0_EXOUT/CATRESTOUT/ LCD_DATA2-B	VCC
K1	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/ POE4#/POE11#/RXD6/SMISO6/SSCL6/RXD0/ SMISO0/SSCL0/CRX0/PCKO/IRQ3-DS/ DSMCLK0	ETHPHYCLK/PA00/PIO_008/A7-A/CACREF/ GTIU-A/GTIOC0A/GTIOC10A/CTS10#-A/ CTS5#-A/RTS5#-A/SS5#-A/DE5-A/TXDB5-A/ SSL01-B/RGMII1_TXC-A/CATIRQ-A/IRQ1-DS/ ADCNV0-A/DSMCLK0-A
K2	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCIC2/ RTCOUT/POE0#/POE10#/TXD6/SMOSI6/SSDA6/ TXD0/SMOSI0/SSDA0/CTX0/USB0_VBUSEN/ VSYNC/IRQ2-DS	PA01/PIO_009/A6-A/GTIV-A/GTIOC0B/ GTIOC10B/SCK5-A/CTS5#-A/TXDB5-A/SSL02-B/ ET1_TX_EN-A/RMII1_TX_EN-A/ RGMII1_TX_CTL-A/CAT1_TX_EN-A/IRQ11/ ADCNV1-A/DSMDAT0-A
K3	TDI/PF2/RXD1/SMISO1/SSCL1/CATI2CCLK	P702/PIO_050/RD#-A/DQM3-B/GTETRGA/ GTIOC11A/SCK4-B/CTS4#-B/TXDB4-B/ ET1_CRS-E/CATSYNC1-A/XSPI1_WP0#-B/ XSPI1_RESET1#-C/HSYNC-C/IRQ10/ADST2-B/ DSMCLK4-D
K4	TCK/PF1/SCK1	VCC
K12	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/ SS4#/CTS6#/RTS6#/SS6#/ET0_RX_CLK/ REF50CK0/CAT0_RX_CLK/LCD_TCON2-B	VSS
K13	P71/A18/CS1#/ET0_MDIO/CAT0_MDIO/ PMGI0_MDIO/DSMCLK3	P310/PIO_058/RTCIC0/CACREF/GTETRGB/ GTCPPO1/POEGC/CTS0#-C/CTS1#-B/SSL11-B/ SSITXD0/ET1_INT-E/CATIRQ-D/IRQ18/ ADTRG0#/TAMPI0
K14	VCC	XCIN/EXCIN/P309

176-Pin LFBGA	RX72M	RX74M
K15	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/SMISO4/SSCL4/RXD6/SMISO6/SSCL6/ET0_ERXD1/RMII0_RXD1/CAT0_ERXD1/LCD_DATA0-B/IRQ12	XCOUT/P308
L1	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/ET1_MDC/PMGI1_MDC/IRQ1-DS	ETHPHYCLK/P700/PIO_048/SDCLK-A/GTIOC10A/TXD4-B/SMOSI4-B/SSDA4-B/TXDA4-B/ET1_INT-A/CATRESTOUT-F/XSPI1_INT0#-B/XSPI1_ECS0#-B/PIXCLK-C/IRQ0/ADST0-B/DSMCLK3-D
L2	P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ET1_MDIO/PMGI1_MDIO/IRQ0-DS	P701/PIO_049/CKE-A/WR3#-B/BC3#-B/GTIOC10B/RXD4-B/SMISO4-B/SSCL4-B/ET1_COL-E/CATLATCH1-A/XSPI1_RSTO0#-B/XSPI1_RESET0#-B/VSYNC-C/IRQ1/ADST1-B/DSMDAT3-D
L3	TDO/PF0/TXD1/SMOSI1/SSDA1/CATI2CDATA	P703/PIO_051/ALE-A/WR2#-B/BC2#-B/CACREF/GTETRGB/GTIOC11B/CTS4#-B/RTS4#-B/SS4#-B/DE4-B/TXDB4-B/ET1_LINKSTA-A/CAT1_LINKSTA-A/XSPI1_RESET0#-B/PCKO-C/IRQ8/DSMDAT4-D
L4	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/SSIDATA1/SDHI_CD/HSYNC/ADTRG0#	P704/PIO_052/SDCS#-A/CS4#-A/GTIOC12A/CTS4#-B/CTS11#-B/RTS11#-B/SS11#-B/DE11-B/TXDB11-B/ET1_RXD0-A/RMII1_RXD0-A/RGMII1_RXD0-A/CAT1_ERXD0-A/XSPI1_INT1#-B/XSPI1_ECS1#-B/IRQ12/ADCNV0-C/DSMCLK5-D
L12	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ET0_ETXD1/RMII0_TXD1/CAT0_ETXD1	P312/PIO_060/BACK#-B/RTCIC2/GTETRGD/GTCPPO15/POEGA/SSL13-B/SSILRCK0/ET1_WOL-C/IRQ20/ADTRG2#/DSMDAT2-C/TAMPI2
L13	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ET0_RX_ER/RMII0_RX_ER/CAT0_RX_ER/LCD_TCON1-B	P311/PIO_059/BREQ#-B/RTCIC1/GTETRGC/GTCPPO14/POEGD/CTS7#-A/SSL12-B/SSIRXD0/ET0_WOL-C/IRQ19/ADTRG1#/DSMCLK2-C/TAMPI1
L14	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/ET0_ERXD0/RMII0_RXD0/CAT0_ERXD0/LCD_TCON3-B/IRQ4-DS	VCC
L15	P72/A19/CS2#/ET0_MDC/CAT0_MDC/PMGI0_MDC/LCD_DATA23-A/DSMDAT3	VBATT/VCC
M1	P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A/ET1_WOL/CATIRQ	PE07/PIO_047/A8-B/A20-C/TOC1/GTETRGD/GTCPPO7/GTIOC10B/POEGD/ET1_LINKSTA-E/CAT1_LINKSTA-D/CATRESTOUT-C/XSPI1_CS0#-A/PIXD7-C/IRQ7
M2	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A/ET1_EXOUT/CATLINKACT1	PE03/PIO_043/A12-B/TOC3/GTOVLO-C/GTIOC8B/CTS12#-A/RTS12#-A/SS12#-A/DE12-A/TXDB12-A/MISO1-A/ET1_RXD1-D/RMII1_RXD1-D/CAT1_ERXD1-D/SD0DAT7-B/XSPI1_IO1-A/PIXD3-C/IRQ11
M3	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/SSIBCK1/SDHI_WP/PIXCLK	PD04/PIO_036/A19-B/D27-B/GTETRGA/GTIOC2A/POEGC/CTS2#-A/CTS3#-A/RTS3#-A/SS3#-A/DE3-A/TXDB3-A/SSL21-A/CRX0-B/ET1_RX_CLK-B/RMII1_REF50CK-B/CAT1_RX_CLK-B/CATLEDRUN-D/SD0DAT0-B/XSPI0_IO2-A/XSPI0_WP0#-B/PIXD4-B/IRQ4/AN028
M4	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/SSCL10/RXD10/CATLINKACT0/PIXD1	PD06/PIO_038/A17-B/D25-B/GTIV-C/GTIOC3A/POEGB/RXD3-A/SMISO3-A/SSCL3-A/SSL23-A/CRX1-B/ET1_RX_ER-B/RMII1_RX_ER-B/CAT1_RX_ER-B/CATLEDERR-D/SD0WP-B/XSPI0_DS-A/PIXD6-B/IRQ6/AN030

176-Pin LFBGA	RX72M	RX74M
M5	CLKOUT25M/PJ2/TXD8/SMOSI8/SSDA8/ SSLC3-B/LCD_TCON2-A	VSS
M6	PJ1/MTIOC6A/RXD8/SMISO8/SSCL8/SSLC2-B/ EPLSOUT1/CATSYNC1/LCD_TCON3-A	VCL
M7	P85/MTIOC6C/TIOCC0/LCD_DATA1-A	VCC2
M8	P55/D0[A0/D0]/EDREQ0/WAIT#/MTIOC4D/ TMO3/TXD7/SMOSI7/SSDA7/MISOC-B/CRX1/ ET0_EXOUT/LCD_DATA5-A/IRQ10	VSS
M9	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A/CATLEDERR	VCL
M10	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/RTS8#/ SCK10/RSPCKA-A/ET0_ETXD2/CAT0_ETXD2/ MMC_D5-A/LCD_DATA11-A	P407/PIO_055/IRQ15-DS/AN007
M11	P81/EDACK0/MTIOC3D/PO27/GTIOC0B/ SMISO10/SSCL10/RXD10/ET0_ETXD0/ RMII0_TXD0/CAT0_ETXD0/CATI2CCLK/QIO3-A/ SDHI_CD/MMC_D3-A/LCD_DATA13-A	P404/PIO_052/IRQ12-DS/AN004
M12	P77/CS7#/PO23/SMOSI11/SSDA11/TXD11/ ET0_RX_ER/RMII0_RX_ER/CAT0_RX_ER/ QSPCLK-A/SDHI_CLK-A/MMC_CLK-A/ LCD_DATA17-A	MD/P315
M13	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV/CAT0_RX_DV	RES#
M14	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/SCK11/ET0_ETXD0/ RMII0_TXD0/CAT0_ETXD0/LCD_CLK-B	P001/PIO_001/TMCI0/GTCPPO0/GTIOC10B/ GTIOC7A/SCK7-A/CTS7#-A/TXDB7-A/SSIBCK0/ ET0_LINKSTA-D/CAT0_LINKSTA-E/IRQ17-DS/ AN017/DSMDAT0-B/PCOUTZ0
M15	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/SS11#/ CTS11#/RTS11#/ET0_TX_EN/RMII0_TXD_EN/ CAT0_TX_EN/LCD_TCON0-B	P000/PIO_000/TMRI0/GTCPPO7/GTIOC10A/ POEGB/CTS0#-B/CTS7#-A/RTS7#-A/SS7#-A/ DE7-A/TXDB7-A/AUDIO_CLK/ET0_INT-D/ CATRESTOUT-E/IRQ16-DS/AN016/DSMCLK0-B
N1	VCC	PE05/PIO_045/A10-B/A22-C/GTOWLO-C/ GTIOC9B/SSL12-A/ET1_RXD3-D/ CAT1_ERXD3-D/CATLEDRUN-B/XSPI1_IO3-A/ PIXD5-C/IRQ5
N2	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/ GTIOC0A/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/ SS0#/CTX1/SSIBCK0/SDHI_D1-C/PIXD7	PE04/PIO_044/A11-B/A23-C/GTOWUP-C/ GTIOC9A/CTS12#-A/SSL11-A/ET1_RXD2-D/ CAT1_ERXD2-D/CATLEDSTER-B/XSPI1_IO2-A/ XSPI1_WP0#-C/PIXD4-C/IRQ12
N3	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/GTIOC1A/SCK0/USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/PIXD6	P607/PIO_015/CS0#-B/D16-B/GTETRGB/ GTADSM0/GTIOC15B/POEGA/CTS8#-B/ CTS9#-B/RTS9#-B/SS9#-B/DE9-B/TXDB9-B/ CRX2-C/ET1_INT-B/ET_TAS_STA3/CATIRQ-B/ XSPI0_RSTO0#-A/IRQ15/DSMDAT5-A
N4	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/ PO13/GTETRGA/RXD1/SMISO1/SSCL1/SCK3/ CRX1-DS/SSILRCK1/CATLEDRUN/PIXD0/IRQ5	P604/PIO_012/CS3#-C/D19-B/GTIOC6A/TXD9-B/ SMOSI9-B/SSDA9-B/TXDA9-B/SSL01-D/ ET1_TXD2-B/ET_TAS_STA0/CAT1_ETXD2-B/ XSPI0_CS1#-A/XSPI0_RSTO0#-B/IRQ4/ DSMCLK4-A
N5	P12/WR3#/BC3#/MTIC5U/TMCI1/GTADSM0/ RXD2/SMISO2/SSCL2/SCL0[FM+]/ LCD_TCON1-A/IRQ2	PD07/PIO_039/A16-B/D24-B/GTIW-C/GTIOC3B/ POEGA/TXD3-A/SMOSI3-A/SSDA3-A/TXDA3-A/ CTX1-B/ET1_LINKSTA-B/CAT1_LINKSTA-B/ SD0CD-B/XSPI0_CS0#-A/XSPI0_RESET1#-B/ PIXD7-B/IRQ7/AN031

176-Pin LFBGA	RX72M	RX74M
N6	PJ0/MTIOC6B/SCK8/SSLC1-B/EPLSOUT0/ CATSYNC0/LCD_DATA0-A	PD05/PIO_037/A18-B/D26-B/GTIU-C/GTIOC2B/ POEGD/SCK3-A/CTS3#-A/TXDB3-A/SSL22-A/ CTX0-B/ET1_RX_DV-B/RMII1_CRS_DV-B/ CAT1_RX_DV-B/CATLEDSTER-D/SD0DAT1-B/ XSPI0_IO3-A/PIXD5-B/IRQ5/AN029
N7	P84/MTIOC6D/ET1_LINKSTA/CAT1_LINKSTA/ LCD_DATA2-A	VCC2
N8	P54/D1[A1/D1]/EDACK0/ALE/MTIOC4B/TMCI1/ CTS2#/RTS2#/SS2#/MOSIC-B/CTX1/ ET0_LINKSTA/CAT0_LINKSTA/LCD_DATA6-A	VSS
N9	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	VCL
N10	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/ ET0_COL/MMC_D7-A/LCD_DATA9-A/IRQ14	P406/PIO_054/IRQ14-DS/AN006
N11	P82/EDREQ1/MTIOC4A/PO28/GTIOC2A/ SMOSI10/SSDA10/TXD10/ET0_ETXD1/ RMII0_TXD1/CAT0_ETXD1/CATI2CDATA/ MMC_D4-A/LCD_DATA12-A	P405/PIO_053/IRQ13-DS/AN005
N12	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/MMC_D0-A/LCD_DATA16-A	P415/PIO_063/IRQ31/AN015/DA1
N13	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/ SS5#/SSLA1-A/ET0_ERXD3/CAT0_ERXD3/ IRQ14	P414/PIO_062/IRQ30/AN014/DA0
N14	P73/CS3#/PO16/ET0_WOL/LCD_EXTCLK-A	P003/PIO_003/GTCPPO2/GTIOC11B/GTIOC8A/ RXD7-A/SMISO7-A/SSCL7-A/SSIRXD1/ ET0_MDIO-D/CAT0_MDIO-E/IRQ19-DS/AN019/ DSMDAT1-B/PCOUTB0
N15	VSS	P002/PIO_002/TMCI1/GTCPPO1/GTIOC11A/ GTIOC7B/TXD7-A/SMOSI7-A/SSDA7-A/ TXDA7-A/SSIBCK1/ET0_MDC-D/CAT0_MDC-E/ IRQ18-DS/AN018/DSMCLK1-B/PCOUTA0
P1	VSS	CLKOUT/PE01/PIO_041/A14-B/GTOULO-C/ GTIOC7B/TXD12-A/SMOSI12-A/SSDA12-A/ TXDA12-A/RSPCK1-A/ET1_RX_DV-D/ RMII1_CRS_DV-D/CAT1_RX_DV-D/SD0DAT5-B/ XSPI1_CK-A/PIXD1-C/IRQ9
P2	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/SCK1/ TXD3/SMOSI3/SSDA3/SDA2-DS/SSITXD0/ EPLSOUT0/CATSYNC0/SDHI_D3-C/PIXD3/IRQ7/ ADTRG1#	PE02/PIO_042/A13-B/TIC3/GTOVUP-C/ GTIOC8A/RXD12-A/SMISO12-A/SSCL12-A/ MOSI1-A/ET1_RXD0-D/RMII1_RXD0-D/ CAT1_ERXD0-D/SD0DAT6-B/XSPI1_IO0-A/ PIXD2-C/IRQ7-DS
P3	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/ SSDA10/TXD10/EPLSOUT1/CATSYNC1/ SDHI_D2-C/PIXD2	P606/PIO_014/CS1#-C/D17-B/GTETRGA/ GTCPPO4/GTIOC15A/POEGC/SCK9-B/CTS9#-B/ TXDB9-B/SSL03-D/CTX2-C/ET1_TX_ER-B/ ET_TAS_STA2/CATLINKACT1-B/ XSPI0_RESET0#-A/IRQ14/DSMCLK5-A
P4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/ PO15/GTETRGD/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/LCD_CLK-A/IRQ4	P603/PIO_011/WE#-B/D20-B/GTIOC5B/CTS8#-B/ RTS8#-B/SS8#-B/DE8-B/TXDB8-B/CTS9#-B/ MISO0-D/ET1_TXD1-B/RMII1_TXD1-B/ GPTP_PTPOUT3/CAT1_ETXD1-B/CATSYNC0-B/ XSPI0_IO7-A/PCKO-B/IRQ3/DSMDAT3-A
P5	VCC_USB	P601/PIO_009/RAS#-B/D22-B/GTIOC4B/RXD8-B/ SMISO8-B/SSCL8-B/RSPCK0-D/ET1_TX_EN-B/ RMII1_TX_EN-B/GPTP_PTPOUT1/ CAT1_TX_EN-B/CATSYNC1-D/XSPI0_IO5-A/ VSYNC-B/IRQ1/ADTRG1#

176-Pin LFBGA	RX72M	RX74M
P6	VSS_USB	PD03/PIO_035/A20-B/D28-B/TOC2/GTIOC1B/ POEGA/TXD2-A/SMOSI2-A/SSDA2-A/TXDA2-A/ MISO2-A/ET1_RXD3-B/CAT1_ERXD3-B/ CAT0_MDIO-D/SD0CLK-B/XSPI0_IO1-A/ PIXD3-B/IRQ3/AN027
P7	P57/RXD7/SMISO7/SSCL7/SSLC0-B/ LCD_DATA3-A	PD00/PIO_032/A23-B/D31-B/GTETRGD/ GTIOC0A/POEGD/CTS2#-A/RTS2#-A/SS2#-A/ DE2-A/TXDB2-A/CTS3#-A/SSL20-A/ ET1_RXD0-B/RMII1_RXD0-B/CAT1_ERXD0-B/ CATLATCH0-D/SD0DAT2-B/XSPI0_CKN#-A/ XSPI0_CS1#-B/PIXD0-B/IRQ0/AN024
P8	P10/ALE/MTIC5W/TMRI3/IRQ0	P902/PIO_002/GTETRGC/GTCPPO8/SCK1-C/ CTS1#-C/TXDB1-C/ET1_MDC-B/ET_TAS_STA2/ CATRESTOUT-B/XSPI0_RESET1#-A/IRQ10/ AN034
P9	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A/ CATLEDSTER	P900/PIO_000/GTETRGA/GTCPPO5/RXD1-C/ SMISO1-C/SSCL1-C/ET1_COL-B/ET_TAS_STA0/ CATSYNC1-B/XSPI0_INT1#-A/XSPI0_ECS1#-A/ IRQ0/AN032
P10	P83/EDACK1/MTIOC4C/GTIOC0A/SCK10/ SS10#/CTS10#/ET0_CRS/RMII0_CRS_DV/ CAT0_RX_DV/LCD_DATA8-A/DSMCLK1	AVSS0
P11	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/MTCLKA/ TMCI2/PO30/TIC0/GTIOC3B/RXD8/SMISO8/ SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ ET0_ETXD3/CAT0_ETXD3/CATLATCH1/ MMC_D6-A/LCD_DATA10-A/IRQ13	VREFL0
P12	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/ POE0#/GTETRGC/SCK5/CTS8#/SS8#/SS10#/ CTS10#/RTS10#/SSLA0-A/ET0_TX_CLK/ CAT0_TX_CLK/CATSYNC0/QMI-A/QIO1-A/ SDHI_D1-A/MMC_D1-A/LCD_DATA15-A	P402/PIO_050/IRQ10-DS/AN002
P13	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ET0_RX_DV/ CAT0_RX_DV/SDHI_D3-A/MMC_CD-A/ LCD_DATA19-A	P400/PIO_048/IRQ8-DS/AN000
P14	P75/CS5#/PO20/SCK11/RTS11#/ET0_ERXD0/ RMII0_RXD0/CAT0_ERXD0/SDHI_D2-A/ MMC_RES#-A/LCD_DATA20-A/DSMDAT2	P005/PIO_005/GTCPPO4/GTIOC12B/GTIOC9A/ RXD0-B/SMISO0-B/SSCL0-B/SSILRCK1/ ET1_MDIO-D/CATLATCH0-E/IRQ21-DS/ ADTRG2#/AN021/DSMDAT2-B/PCOUTB1
P15	VCC	P004/PIO_004/GTCPPO3/GTIOC12A/GTIOC8B/ TXD0-B/SMOSI0-B/SSDA0-B/TXDA0-B/SSITXD1/ ET1_MDC-D/CATSYNC0-E/IRQ20-DS/AN020/ DSMCLK2-B/PCOUTA1
R1	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/ GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/PIXD5/ IRQ9	ETHPHYCLK/PE00/PIO_040/A15-B/GTOUUP-C/ GTIOC7A/SCK12-A/CTS12#-A/TXDB12-A/ SSL10-A/ET1_RX_ER-D/RMII1_RX_ER-D/ CAT1_RX_ER-D/SD0DAT4-B/XSPI1_CKN#-A/ XSPI1_CS1#-B/PIXD0-C/IRQ8
R2	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMD-C/PIXD4/IRQ8	PE06/PIO_046/A9-B/A21-C/TIC1/GTETRGC/ GTADSM1/GTIOC10A/POEGB/SSL13-A/ ET1_RX_CLK-D/RMII1_REF50CK-D/ CAT1_RX_CLK-D/CATLEDERR-B/XSPI1_DS-A/ PIXD6-C/IRQ6
R3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/ PO14/RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/ SMISO3/SSCL3/SCL2-DS/USB0_VBUSEN/ USB0_VBUS/USB0_OVRCURB/IRQ6/ADTRG0#	P605/PIO_013/CS2#-C/D18-B/GTIOC6B/ RXD9-B/SMISO9-B/SSCL9-B/SSL02-D/ ET1_TXD3-B/ET_TAS_STA1/CAT1_ETXD3-B/ XSPI0_INT0#-A/XSPI0_ECS0#-A/IRQ13/ DSMDAT4-A

176-Pin LFBGA	RX72M	RX74M
R4	P13/WR2#/BC2#/MTIOC0B/TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/SSDA2/SDA0[FM+]/ LCD_TCON0-A/IRQ3/ADTRG1#	P602/PIO_010/CAS#-B/D21-B/GTIOC5A/ SCK8-B/CTS8#-B/TXDB8-B/MOSI0-D/ ET1_TXD0-B/RMII1_TXD0-B/GPTP_PTPOUT2/ CAT1_ETXD0-B/CATLATCH0-B/XSPI0_IO6-A/ HSYNC-B/IRQ2/ADTRG2#/DSMCLK3-A
R5	USB0_DM	P600/PIO_008/SDCS#-B/D23-B/GTIOC4A/ TXD8-B/SMOSI8-B/SSDA8-B/TXDA8-B/SSL00-D/ ET1_TX_CLK-B/GPTP_PTPOUT0/ CAT1_TX_CLK-B/CATLATCH1-D/ XSPI0_IO4-A/PIXCLK-B/IRQ0/ADTRG0#
R6	USB0_DP	PD02/PIO_034/A21-B/D29-B/TIC2/GTETRGB/ GTIOC1A/POEGB/RXD2-A/SMISO2-A/SSCL2-A/ MOSI2-A/ET1_RXD2-B/CAT1_ERXD2-B/ CAT0_MDC-D/SD0CMD-B/XSPI0_IO0-A/ PIXD2-B/IRQ2/AN026
R7	CLKOUT25M/P56/EDACK1/MTIOC3C/TIOCA1/ SCK7/RSPCKC-B/LCD_DATA4-A/DSMDAT1	PD01/PIO_033/A22-B/D30-B/GTETRGC/ GTIOC0B/POEGC/SCK2-A/CTS2#-A/TXDB2-A/ RSPCK2-A/ET1_RXD1-B/RMII1_RXD1-B/ CAT1_ERXD1-B/CATSYNC0-D/SD0DAT3-B/ XSPI0_CK-A/PIXD1-B/IRQ1/AN025
R8	P11/MTIC5V/TMCI3/SCK2/EPLSOUT1/ CATSYNC1/LCD_DATA7-A/IRQ1	P903/PIO_003/GTETRGD/GTCPPO9/POEGD/ CTS6#-B/CTS1#-C/RTS1#-C/SS1#-C/DE1-C/ TXDB1-C/ET1_MDIO-B/ET_TAS_STA3/ CATIRQ-C/XSPI0_WP1#-A/IRQ11/AN035
R9	P53*1/BCLK	P901/PIO_001/GTETRGB/GTCPPO6/TXD1-C/ SMOSI1-C/SSDA1-C/TXDA1-C/ET1_CRS-B/ ET_TAS_STA1/CATLATCH1-B/ XSPI0_RSTO1#-A/XSPI0_RESET0#-B/IRQ9/ AN033
R10	VSS	AVCC0
R11	VCC	VREFH0
R12	P80/EDREQ0/MTIOC3B/PO26/SCK10/RTS10#/ ET0_TX_EN/RMII0_TXD_EN/CAT0_TX_EN/ CATLATCH0/QIO2-A/SDHI_WP/MMC_D2-A/ LCD_DATA14-A	P403/PIO_051/IRQ11-DS/AN003
R13	P76/CS6#/PO22/SMISO11/SSCL11/RXD11/ ET0_RX_CLK/REF50CK0/CAT0_RX_CLK/ QSSL-A/SDHI_CMD-A/MMC_CMD-A/ LCD_DATA18-A	P401/PIO_049/IRQ9-DS/AN001
R14	P74/A20/CS4#/PO19/SS11#/CTS11#/ ET0_ERXD1/RMII0_RXD1/CAT0_ERXD1/ LCD_DATA21-A/DSMCLK2	P007/PIO_007/GTCPPO6/GTIOC13B/POEGA/ CTS0#-B/RTS0#-B/SS0#-B/DE0-B/TXDB0-B/ ET1_INT-D/CATIRQ-E/IRQ23-DS/ADTRG0#/ AN023/PDMDAT0-C
R15	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/CAT0_ERXD2/ LCD_DATA22-A/IRQ12	P006/PIO_006/GTCPPO5/GTIOC13A/GTIOC9B/ SCK0-B/CTS0#-B/TXDB0-B/ET1_LINKSTA-D/ CAT1_LINKSTA-E/IRQ22-DS/ADTRG1#/AN022/ PDMCLK0-C/PCOUTZ1

Table 3.4 Comparative Listing of RX72N/RX74N 176-Pin LFBGA Package Pin Functions

176-Pin	RX72N (176-Pin LFBGA)	RX74N (176-Pin LFBGA)
A1	AVSS0	PC01/PIO_025/D6-A/GTOULO-B/GTIOC7B/ SCK11-A/CTS11#-A/TXDB11-A/SSL02-A/ SDA00-C/ET0_TXD0-A/RMII0_TXD0-A/ RGMII0_TXD0-A/SD0DAT3-A/IRQ12/PCOUTB0
A2	AVCC0	PC03/PIO_027/D4-A/GTOVLO-B/GTIOC8B/ TXD11-A/SMOSI11-A/SSDA11-A/TXDA11-A/ SDAHS1-C/ET0_TXD2-A/RGMII0_TXD2-A/ SD0CLK-A/IRQ11/PCOUTA1
A3	VREFL0	PC05/PIO_029/D2-A/TMRI2/GTOWLO-B/ GTIOC9B/SCK8-A/CTS8#-A/TXDB8-A/ RSPCK0-A/SSIBCK0/ET0_TX_EN-A/ RMII0_TX_EN-A/RGMII0_TX_CTL-A/ SD0DAT1-A/IRQ5/PCOUTZ1
A4	P42/IRQ10-DS/AN002	ETHPHYCLK/PC07/PIO_031/D0-A/TMO2/TOC0/ CACREF/GTETRGD/GTADSM1/GTIOC15B/ POEGA/TXD8-A/SMOSI8-A/SSDA8-A/TXDA8-A/ MISO0-A/SSITXD0/RGMII0_TXC-A/SD0CD-A/ IRQ14/PDMDAT0-A
A5	P46/IRQ14-DS/AN006	CLKOUT/P801/PIO_057/EBCLK-A/GTIV-B/ GTIOC0B/POEGC/TXD10-B/SMOSI10-B/ SSDA10-B/TXDA10-B/ET0_CRS-B/IRQ9/ ADCNV1-B
A6	VCC	P503/PIO_035/WR3#-A/BC3#-A/A19-C/ GTIOC3B/RXD2-C/SMISO2-C/SSCL2-C/CRX1-C/ USB0_OVRCURB/SSIRXD0/SD0DAT7-A/IRQ3
A7	VSS	VLO
A8	P94/D20/A20/ET1_ERXD0/RMII1_RXD0	VSS_DCDC
A9	VCC	VCC_DCDC
A10	TRSYNC1/P97/D23/A23/ET1_ERXD3	P102/PIO_010/TMCI1/GTADSM0/GTIOC13A/ SCL00-A/ET0_COL-D/IRQ2
A11	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/ET1_RX_CLK/REF50CK1/QMO-B/ QIO0-B/SDHI_D0-B/MMC_D0-B/LCD_DATA18-B/ IRQ6/AN106	CLKOUT/P106/PIO_014/TMO2/RTCOUT/ GTIU-D/GTIOC15A/POEGB/RXD3-B/SMISO3-B/ SSCL3-B/SCLHS2-A/ET0_TXD2-B/SD0DAT2-C/ PIXD2-A/IRQ30-DS/ADTRG0#/PCINA1
A12	P60/CS0#/ET1_TX_EN/RMII1_TXD_EN	P200/PIO_016/TMRI0/GTETRGA/GTIOC3A/ GTIOC14A/CTS6#-A/RTS6#-A/SS6#-A/DE6-A/ TXDB6-A/MOSI0-C/SDAHS1-A/USB0_ID/ SSIRXD0/ET0_TX_EN-B/RMII0_TX_EN-B/ SD0CMD-C/PIXD4-A/IRQ8/ADTRG2#/PCINZ1
A13	P63/CAS#/D2[A2/D2]/CS3#/ET1_ETXD1/ RMII1_TXD1	P805/PIO_061/GTADSM1/GTIOC15B/SCK5-B/ CTS5#-B/TXDB5-B/SSL22-B/CRX0-D/ USB0_VBUSEN/USBHS_VBUSEN/ET0_TXD0-C/ RMII0_TXD0-C/HSYNC-D/IRQ5/ADSYNC-C/ PCINB0
A14	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/MTIOC3B/ PO18/GTIOC1B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1	TCK/SWCLK/P301/PIO_025/TMCI3/GTCPPO11/ SCK0-A/CTS0#-A/TXDB0-A/SCK1-A/CTS1#-A/ TXDB1-A/RSPCK1-C/IRQ7

176-Pin	RX72N (176-Pin LFBGA)	RX74N (176-Pin LFBGA)
A15	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/PO23/ TIC3/GTIOC0B/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/MMC_D6-B/LCD_DATA14-B/ IRQ7-DS/AN100	TDO/P302/PIO_026/TMRI3/GTCPPO12/TXD0-A/ SMOSI0-A/SSDA0-A/TXDA0-A/TXD1-A/ SMOSI1-A/SSDA1-A/TXDA1-A/MOSI1-C/IRQ4
B1	P05/SSILRCK1/IRQ13/DA1	PC00/PIO_024/D7-A/GTOUUP-B/GTIOC7A/ CTS11#-A/RTS11#-A/SS11#-A/DE11-A/ TXDB11-A/SSL01-A/SCL00-C/ET0_TX_CLK-A/ SD0DAT2-A/IRQ14/PCOUTA0
B2	P07/IRQ15/ADTRG0#	PC02/PIO_026/D5-A/GTOVUP-B/GTIOC8A/ RXD11-A/SMISO11-A/SSCL11-A/SSL03-A/ SCLHS1-C/ET0_TXD1-A/RMII0_TXD1-A/ RGMII0_TXD1-A/SD0CMD-A/IRQ10/PCOUTZ0
B3	P40/IRQ8-DS/AN000	PC04/PIO_028/D3-A/TMCI1/GTOWUP-B/ GTIOC9A/CTS8#-A/RTS8#-A/SS8#-A/DE8-A/ TXDB8-A/CTS11#-A/SSL00-A/AUDIO_CLK/ ET0_TXD3-A/RGMII0_TXD3-A/SD0DAT0-A/ IRQ12/PCOUTB1
B4	P41/IRQ9-DS/AN001	PC06/PIO_030/D1-A/TMCI2/TIC0/GTETRGC/ GTCPPO7/GTIOC15A/POEGB/RXD8-A/ SMISO8-A/SSCL8-A/MOSI0-A/SSILRCK0/ ET0_TX_ER-A/SD0WP-A/IRQ13/PDMCLK0-A
B5	P47/IRQ15-DS/AN007	P803/PIO_059/CS3#-A/WR1#-B/BC1#-B/ GTIOC1B/POEGA/CTS10#-B/RTS10#-B/ SS10#-B/DE10-B/TXDB10-B/CTX2-D/USB0_ID/ ET0_MDC-B/IRQ3/ADSYNC-B
B6	P91/D17/A17/SCK7/ET1_COL/AN115	P502/PIO_034/WR2#-A/BC2#-A/A18-C/ GTIOC3A/TXD2-C/SMOSI2-C/SSDA2-C/ TXDA2-C/SSL13-C/CTX1-C/ET0_WOL-B/ SD0DAT6-A/IRQ2/ADST2-C
B7	P92/D18/A18/POE4#/RXD7/SMISO7/SSCL7/ ET1_CRS/RMII1_CRS_DV/AN116	VLO
B8	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/AN109	VSS_DCDC
B9	TRDATA5/P96/D22/A22/ET1_ERXD2	VCC_DCDC
B10	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0-A/ ET1_MDIO/PMGI1_MDIO/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112	P103/PIO_011/TMO3/GTADSM1/GTIOC13B/ CTS2#-B/SDA00-A/ET0_CRS-D/IRQ3
B11	TRDATA7/PG1/D25/ET1_RX_ER/RMII1_RX_ER	P107/PIO_015/TMO1/GTIV-D/GTIOC15B/ POEGA/TXD3-B/SMOSI3-B/SSDA3-B/TXDA3-B/ SDAHS2-A/SSITXD0/ET0_TXD3-B/SD0DAT3-C/ PIXD3-A/IRQ31-DS/ADTRG1#/PCINB1
B12	VSS	P201/PIO_017/TMCI0/GTIW-D/GTIOC3B/ GTIOC14B/SCK6-A/CTS6#-A/TXDB6-A/ MISO0-C/SCLHS1-A/USB0_EXICEN/SSILRCK0/ ET0_RX_ER-B/RMII0_RX_ER-B/SD0CLK-C/ PIXD5-A/IRQ9/PCINZ0
B13	P64/WE#/D3[A3/D3]/CS4#/ET1_ETXD0/ RMII1_TXD0	P804/PIO_060/GTADSM0/GTIOC15A/CTS5#-B/ RTS5#-B/SS5#-B/DE5-B/TXDB5-B/SSL21-B/ CTX0-D/USB0_OVRCURA/USBHS_OVRCURA/ ET0_TX_EN-C/RMII0_TX_EN-C/PCKO-D/IRQ4/ PCINA0

176-Pin	RX72N (176-Pin LFBGA)	RX74N (176-Pin LFBGA)
B14	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/GTIOC2B/ SCK12/SSLB1-B/MMC_D4-B/LCD_DATA16-B/ ANEX0	TMS/SWDIO/P300/PIO_024/TMO1/GTCPPO10/ CTS0#-A/RTS0#-A/SS0#-A/DE0-A/TXDB0-A/ CTS1#-A/RTS1#-A/SS1#-A/DE1-A/TXDB1-A/ SSL10-C/ET0_WOL-D/IRQ6
B15	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/CTS12#/RTS12#/SS12#/ ET0_ERXD3/MMC_D7-B/LCD_DATA13-B/AN101	TDI/P303/PIO_027/TMCI2/GTCPPO13/RXD0-A/ SMISO0-A/SSCL0-A/RXD1-A/SMISO1-A/ SSCL1-A/MISO1-C/IRQ1
C1	AVSS1	PB06/PIO_022/D9-A/GTOWUP-A/GTIOC6A/ RXD9-A/SMISO9-A/SSCL9-A/ET0_RX_ER-A/ RMII0_RX_ER-A/IRQ6
C2	AVCC1	PB07/PIO_023/D8-A/GTOWLO-A/GTIOC6B/ TXD9-A/SMOSI9-A/SSDA9-A/TXDA9-A/ ET0_LINKSTA-A/IRQ15
C3	VREFH0	P802/PIO_058/CS2#-A/WR#-B/WR0#-B/GTIW-B/ GTIOC1A/POEGB/SCK10-B/CTS10#-B/ TXDB10-B/CRX2-D/USB0_EXICEN/ ET0_MDIO-B/IRQ2/ADCNV2-B
C4	P43/IRQ11-DS/AN003	VCC
C5	P45/IRQ13-DS/AN005	P500/PIO_032/WR#-A/WR0#-A/A16-C/GTIOC2A/ CTS2#-C/RTS2#-C/SS2#-C/DE2-C/TXDB2-C/ CTS7#-B/SSL11-C/CTX0-C/ET0_LINKSTA-B/ SD0DAT4-A/IRQ0/ADST0-C
C6	P90/D16/A16/TXD7/SMOSI7/SSDA7/ ET1_RX_DV/AN114	P501/PIO_033/WR1#-A/BC1#-A/A17-C/ GTIOC2B/SCK2-C/CTS2#-C/TXDB2-C/SSL12-C/ CRX0-C/ET0_INT-B/SD0DAT5-A/IRQ1/ADST1-C
C7	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108	VLO
C8	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/ET1_EXOUT/QIO2-B/ SDHI_D2-B/MMC_D2-B/LCD_DATA22-B/IRQ2/ AN110	VCC_DCDC
C9	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/ET1_WOL/QIO3-B/ SDHI_D3-B/MMC_D3-B/LCD_DATA21-B/IRQ3/ AN111	VCC
C10	TRDATA6/PG0/D24/ET1_RX_CLK/REF50CK1	P100/PIO_008/CS1#-B/WAIT#-A/TMRI3/ CACREF/GTIU-E/GTADSM0/GTIOC12A/ CTS2#-B/RTS2#-B/SS2#-B/DE2-B/TXDB2-B/ CTS5#-B/USB0_OVRCURB-DS/USBHS_VBUS/ ET0_TX_ER-B/IRQ0/ADTRG2#
C11	VCC	P104/PIO_012/TMRI2/GTIW-E/GTIOC14A/ RXD2-B/SMISO2-B/SSCL2-B/CTS3#-B/RTS3#-B/ SS3#-B/DE3-B/TXDB3-B/CTX2-A/ USB0_OVRCURA-DS/USBHS_VBUS/ ET0_TXD0-B/RMII0_TXD0-B/PIXD0-A/IRQ4/ ADST0-A/PCINA0
C12	P62/RAS#/D1[A1/D1]/CS2#/ET1_ERXD0/ RMII1_RXD0	CLKOUT/P205/PIO_021/A21-C/CS6#-C/ GTOVLO-D/GTIOC1B/GTIOC5B/SCK1-B/ CTS1#-B/TXDB1-B/RSPCK1-B/SDAHS1-B/ CRX0-A/USB0_VBUS/USBHS_VBUSEN/ SSIRXD1/ET0_RXD1-B/RMII0_RXD1-B/ SD0CD-C/HSYNC-A/IRQ5/ADTRG0#/PCOUTB1

176-Pin	RX72N (176-Pin LFBGA)	RX74N (176-Pin LFBGA)
C13	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/LCD_DATA12-B/AN102	ETHPHYCLK/P304/PIO_028/ALE-C/WAIT#-B/ TMCI3/GTETRGD/GTCPPO0/POEGA/CTS0#-A/ CTS1#-A/USB0_VBUSEN/USBHS_ID/ ET0_INT-E/IRQ0-DS/ADTRG0#
C14	VSS	P202/PIO_018/CS3#-B/BREQ#-A/TMO0/ GTOUUP-D/GTIOC0A/GTIOC4A/TXD6-A/ SMOSI6-A/SSDA6-A/TXDA6-A/RSPCK0-C/ SCL00-B/CTX2-B/USB0_OVRCURA/ USBHS_EXICEN/AUDIO_CLK/ET0_RX_DV-B/ RMII0_CRS_DV-B/SD0DAT0-C/PIXD6-A/ IRQ15/PDMCLK0-B
C15	P70/SDCLK	P203/PIO_019/CS2#-B/BACK#-A/GTOULO-D/ GTIOC0B/GTIOC4B/RXD6-A/SMISO6-A/ SSCL6-A/CTS3#-B/SSL00-C/SDA00-B/CRX2-B/ USB0_OVRCURB/USBHS_ID/SSIBCK0/ ET0_RX_CLK-B/RMII0_REF50CK-B/ SD0DAT1-C/PIXD7-A/IRQ3/PDMDAT0-B
D1	P01/TMCI0/RXD6/SMISO6/SSCL6/SSIBCK0/ IRQ9/AN119	PB04/PIO_020/D11-A/GTOVUP-A/GTIOC5A/ CTS4#-A/CTS9#-A/RTS9#-A/SS9#-A/DE9-A/ TXDB9-A/ET0_RX_CLK-A/RMII0_REF50CK-A/ RGMII0_RXC-A/IRQ4
D2	P02/TMCI1/SCK6/SSIBCK1/IRQ10/AN120	PB05/PIO_021/D10-A/TMRI1/GTOVLO-A/ GTIOC5B/SCK9-A/CTS9#-A/TXDB9-A/ ET0_RX_DV-A/RMII0_CRS_DV-A/ RGMII0_RX_CTL-A/IRQ13
D3	P03/SSIDATA1/IRQ11/DA0	PG01/PIO_057/DQM0-A/WR#-C/WR0#-C/ GTCPPO1/RXD8-C/SMISO8-C/SSCL8-C/IRQ9
D4	P00/TMRI0/TXD6/SMOSI6/SSDA6/AUDIO_CLK/ IRQ8/AN118	P800/PIO_056/CS1#-A/DQM0-B/GTIU-B/ GTIOC0A/POEGD/RXD10-B/SMISO10-B/ SSCL10-B/ET0_COL-B/IRQ8/ADCNV0-B
D5	P44/IRQ12-DS/AN004	VCC
D6	P93/D19/A19/POE0#/CTS7#/RTS7#/SS7#/ ET1_LINKSTA/AN117	VSS
D7	TRDATA4/P95/D21/A21/ET1_ERXD1/ RMII1_RXD1	VCL
D8	VSS	P101/PIO_009/CS0#-A/ALE-B/TMCI3/GTETRGC/ GTADSM1/GTIOC12B/SCK2-B/CTS2#-B/ TXDB2-B/USB0_VBUS-DS/USBHS_EXICEN/ ET0_TX_CLK-B/IRQ1/ADTRG1#
D9	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/MTCLKA/ POE10#/SSLC1-A/ET1_MDC/PMGI1_MDC/ QSPCLK-B/SDHI_CLK-B/MMC_CLK-B/ LCD_DATA19-B/IRQ5/AN113	VSS
D10	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ ET1_RX_ER/RMII1_RX_ER/QMI-B/QIO1-B/ SDHI_D1-B/MMC_D1-B/LCD_DATA17-B/IRQ7/ AN107	VCL

176-Pin	RX72N (176-Pin LFBGA)	RX74N (176-Pin LFBGA)
D11	P61/SDCS#/D0[A0/D0]/CS1#/ET1_ERXD1/ RMII1_RXD1	P105/PIO_013/TMCI2/GTIV-E/GTIOC14B/ TXD2-B/SMOSI2-B/SSDA2-B/TXDA2-B/SCK3-B/ CTS3#-B/TXDB3-B/CRX2-A/USB0_VBUS/ USBHS_OVRCURB/SSILRCK1/ET0_TXD1-B/ RMII0_TXD1-B/PIXD1-A/IRQ29-DS/ADST1-A/ PCINB0
D12	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ET0_RX_CLK/ REF50CK0/LCD_DATA11-B/IRQ5/AN103	VCC
D13	VCC	ETHPHYCLK/P204/PIO_020/A20-C/CS7#-C/ TMRI1/GTOVUP-D/GTIOC1A/GTIOC5A/ CTS1#-B/RTS1#-B/SS1#-B/DE1-B/TXDB1-B/ SSL10-B/SCLHS1-B/CTX0-A/USB0_VBUSEN/ USBHS_VBUS-DS/SSIBCK1/ET0_RXD0-B/ RMII0_RXD0-B/SD0WP-C/PIXCLK-A/IRQ12/ PCOUTA1
D14	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105	PF00/PIO_048/GTCPPO14/USB0_DP/IRQ0
D15	P65/CKE/CS5#	PF01/PIO_049/GTCPPO15/USB0_DM/IRQ1
E1	PJ5/POE8#/CTS2#/RTS2#/SS2#/SSIRXD0/ EPLSOUT0	PB02/PIO_018/D13-A/GTOUUP-A/GTIOC4A/ CTS4#-A/RTS4#-A/SS4#-A/DE4-A/TXDB4-A/ CTS9#-A/ET0_RXD2-A/RGMII0_RXD2-A/IRQ2
E2	EMLE	PB03/PIO_019/D12-A/TMO0/GTOULO-A/ GTIOC4B/SCK4-A/CTS4#-A/TXDB4-A/ ET0_RXD3-A/RGMII0_RXD3-A/IRQ3
E3	PF5/WAIT#/SSILRCK0/IRQ4	PG00/PIO_056/DQM1-A/WR1#-C/BC1#-C/ GTCPPO0/SCK8-C/CTS8#-C/TXDB8-C/IRQ8
E4	VSS	VSS
E12	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/AN104	VSS
E13	TRDATA0/PG2/D26/ET1_TX_CLK	P206/PIO_022/A22-C/CS5#-C/TMO3/RTCOUT/ GTOWUP-D/GTIOC2A/GTIOC6A/CTS6#-A/ TXD1-B/SMOSI1-B/SSDA1-B/TXDA1-B/MOSI1-B/ SCLHS2-B/CTX1-A/USB0_EXICEN/ USBHS_OVRCURA-DS/SSITXD1/ET0_RXD2-B/ VSYNC-A/IRQ2-DS/ADTRG1#/PCOUTZ1
E14	TRDATA1/PG3/D27/ET1_ETXD0/RMII1_TXD0	VSS_USB
E15	P67/DQM1/CS7#/MTIOC7C/GTIOC1B/CRX2/ EPLSOUT1/IRQ15	VCC_USB
F1	VBATT	PB00/PIO_016/D15-A/GTETRGA/GTADSM0/ GTIOC14A/POEGC/RXD4-A/SMISO4-A/ SSCL4-A/ET0_RXD0-A/RMII0_RXD0-A/ RGMII0_RXD0-A/IRQ12/ADST2-A/PCINA1
F2	VCL	PB01/PIO_017/D14-A/TMCI0/GTETRGB/ GTCPPO4/GTIOC14B/POEGA/TXD4-A/ SMOSI4-A/SSDA4-A/TXDA4-A/ET0_RXD1-A/ RMII0_RXD1-A/RGMII0_RXD1-A/IRQ4-DS/ PCINB1

176-Pin	RX72N (176-Pin LFBGA)	RX74N (176-Pin LFBGA)
F3	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/SS6#/ CTS0#/RTS0#/SS0#/SSITXD0/ET0_EXOUT	PG02/PIO_058/DQM3-A/WR3#-C/BC3#-C/ GTIOC11A/TXD8-C/SMOSI8-C/SSDA8-C/ TXDA8-C/IRQ10
F4	BSCANP	VCL
F12	P66/DQM0/CS6#/MTIOC7D/GTIOC2B/CTX2	VCL
F13	TRSYNC/PG4/D28/ET1_ETXD1/RMII1_TXD1	AVSS_USBHS
F14	PA0/DQM2/BC0#/A0/MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/LCD_DATA8-B	USBHS_DP
F15	VSS	USBHS_DM
G1	XCIN	PA06/PIO_014/A1-A/DQM2-B/TMCI3/GTIOC3A/ GTIOC13A/TXD10-A/SMOSI10-A/SSDA10-A/ TXDA10-A/MOSI0-B/IRQ14/PCINZ1
G2	XCOUT	ETHPHYCLK/PA07/PIO_015/A0-A/BC0#-A/ DQM1-B/GTIOC3B/GTIOC13B/RXD10-A/ SMISO10-A/SSCL10-A/MISO0-B/IRQ7/PCINB0
G3	MD/FINED	P706/PIO_054/CAS#-A/CS6#-A/GTIOC13A/ RXD11-B/SMISO11-B/SSCL11-B/ XSPI1_WP1#-B/IRQ14/ADCNV2-C
G4	TRST#/PF4	VCC
G12	TRCLK/PG5/D29/ET1_ETXD2	AVCC_USBHS
G13	TRDATA2/PG6/D30/ET1_ETXD3	USBHS_RREF
G14	PA1/DQM3/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/IRQ11	VSS_USBHS
G15	VCC	VCC_USBHS
H1	XTAL/P37	PA04/PIO_012/A3-A/TMRI0/GTIOC2A/ GTIOC12A/CTS10#-A/RTS10#-A/SS10#-A/ DE10-A/TXDB10-A/SSL00-B/IRQ5-DS/PCINZ0
H2	VSS	PA05/PIO_013/A2-A/GTIOC2B/GTIOC12B/ SCK10-A/CTS10#-A/TXDB10-A/RSPCK0-B/IRQ5/ PCINA0
H3	RES#	P707/PIO_055/WE#-A/CS7#-A/GTIOC13B/ TXD11-B/SMOSI11-B/SSDA11-B/TXDA11-B/ XSPI1_RESET1#-B/IRQ7
H4	UPSEL/P35/NMI	VSS
H12	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/ TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC/ PMGI0_MDC/LCD_DATA4-B/IRQ5-DS	P207/PIO_023/A23-C/CS4#-C/TMRI3/ GTOWLO-D/GTIOC2B/GTIOC6B/RXD1-B/ SMISO1-B/SSCL1-B/MISO1-B/SDAHS2-B/ CRX1-A/USB0_ID/USBHS_OVRCURB-DS/ ET0_RXD3-B/PCKO-A/IRQ3-DS/ADTRG2#
H13	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/ PMGI0_MDIO/LCD_DATA5-B/IRQ6-DS	VSS
H14	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B	EXTAL/P306
H15	TRDATA3/PG7/D31/ET1_TX_ER	XTAL/P307
J1	EXTAL/P36	PA02/PIO_010/A5-A/GTIW-A/GTIOC1A/ GTIOC11A/TXD5-A/SMOSI5-A/SSDA5-A/ TXDA5-A/SSL03-B/IRQ10/ADCNV2-A

176-Pin	RX72N (176-Pin LFBGA)	RX74N (176-Pin LFBGA)
J2	VCC	PA03/PIO_011/A4-A/GTIOC1B/GTIOC11B/ RXD5-A/SMISO5-A/SSCL5-A/IRQ6-DS/ ADSYNC-A
J3	P34/MTIOC0A/TMCI3/PO12/POE10#/SCK6/ SCK0/ET0_LINKSTA/IRQ4	P705/PIO_053/RAS#-A/CS5#-A/GTIOC12B/ SCK11-B/CTS11#-B/TXDB11-B/ XSPI1_RSTO1#-B/IRQ13/ADCNV1-C
J4	TMS/PF3	VCL
J12	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/LCD_DATA3-B	VCL
J13	VSS	P305/NMI/IRQ0
J14	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B	VSS
J15	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/RTS5#/SS5#/ MOSIA-B/ET0_EXOUT/LCD_DATA2-B	VCC
K1	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/ POE4#/POE11#/RXD6/SMISO6/SSCL6/RXD0/ SMISO0/SSCL0/CRX0/PCKO/IRQ3-DS	ETHPHYCLK/PA00/PIO_008/A7-A/CACREF/ GTIU-A/GTIOC0A/GTIOC10A/CTS10#-A/ CTS5#-A/RTS5#-A/SS5#-A/DE5-A/TXDB5-A/ SSL01-B/IRQ1-DS/ADCNV0-A
K2	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCIC2/ RTCOUT/POE0#/POE10#/TXD6/SMOSI6/ SSDA6/TXD0/SMOSI0/SSDA0/CTX0/ USB0_VBUSEN/VSYNC/IRQ2-DS	PA01/PIO_009/A6-A/GTIV-A/GTIOC0B/ GTIOC10B/SCK5-A/CTS5#-A/TXDB5-A/SSL02-B/ IRQ11/ADCNV1-A
K3	TDI/PF2/RXD1/SMISO1/SSCL1	P702/PIO_050/RD#-A/DQM3-B/GTETRGA/ GTIOC11A/SCK4-B/CTS4#-B/TXDB4-B/ XSPI1_WP0#-B/XSPI1_RESET1#-C/HSYNC-C/ IRQ10/ADST2-B
K4	TCK/PF1/SCK1	VCC
K12	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/ SS4#/CTS6#/RTS6#/SS6#/ET0_RX_CLK/ REF50CK0/LCD_TCON2-B	VSS
K13	P71/A18/CS1#/ET0_MDIO/PMGI0_MDIO	P310/PIO_058/RTCIC0/CACREF/GTETRGB/ GTCPPO1/POEGC/CTS0#-C/CTS1#-B/SSL11-B/ SSITXD0/IRQ18/ADTRG0#/TAMPI0
K14	VCC	XCIN/EXCIN/P309
K15	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/ET0_ERXD1/ RMII0_RXD1/LCD_DATA0-B/IRQ12	XCOUT/P308
L1	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/ RTS1#/SS1#/SSLB0-A/ET1_MDC/PMGI1_MDC/ IRQ1-DS	ETHPHYCLK/P700/PIO_048/SDCLK-A/ GTIOC10A/TXD4-B/SMOSI4-B/SSDA4-B/ TXDA4-B/XSPI1_INT0#-B/XSPI1_ECS0#-B/ PIXCLK-C/IRQ0/ADST0-B
L2	P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/MISOB-A/ET1_MDIO/ PMGI1_MDIO/IRQ0-DS	P701/PIO_049/CKE-A/WR3#-B/BC3#-B/ GTIOC10B/RXD4-B/SMISO4-B/SSCL4-B/ XSPI1_RSTO0#-B/XSPI1_RESET0#-B/ VSYNC-C/IRQ1/ADST1-B
L3	TDO/PF0/TXD1/SMOSI1/SSDA1	P703/PIO_051/ALE-A/WR2#-B/BC2#-B/CACREF/ GTETRGB/GTIOC11B/CTS4#-B/RTS4#-B/ SS4#-B/DE4-B/TXDB4-B/XSPI1_RESET0#-B/ PCKO-C/IRQ8

176-Pin	RX72N (176-Pin LFBGA)	RX74N (176-Pin LFBGA)
L4	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SSIDATA1/SDHI_CD/HSYNC/ADTRG0#	P704/PIO_052/SDCS#-A/CS4#-A/GTIOC12A/ CTS4#-B/CTS11#-B/RTS11#-B/SS11#-B/DE11-B/ TXDB11-B/XSPI1_INT1#-B/XSPI1_ECS1#-B/ IRQ12/ADCNV0-C
L12	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1	P312/PIO_060/BACK#-B/RTCIC2/GTETRGD/ GTCPPO15/POEGA/SSL13-B/SSILRCK0/IRQ20/ ADTRG2#/TAMPI2
L13	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK4/SCK6/ET0_RX_ER/ RMII0_RX_ER/LCD_TCON1-B	P311/PIO_059/BREQ#-B/RTCIC1/GTETRGC/ GTCPPO14/POEGD/CTS7#-A/SSL12-B/ SSIRXD0/ET0_WOL-C/IRQ19/ADTRG1#/TAMPI1
L14	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/ PO25/TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/ SSDA6/ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS	VCC
L15	P72/A19/CS2#/ET0_MDC/PMGI0_MDC/ LCD_DATA23-A	VBATT/VCC
M1	P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A/ET1_WOL	PE07/PIO_047/A8-B/A20-C/TOC1/GTETRGD/ GTCPPO7/GTIOC10B/POEGD/XSPI1_CS0#-A/ PIXD7-C/IRQ7
M2	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/ SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A/ ET1_EXOUT	PE03/PIO_043/A12-B/TOC3/GTOVLO-C/ GTIOC8B/CTS12#-A/RTS12#-A/SS12#-A/ DE12-A/TXDB12-A/MISO1-A/SD0DAT7-B/ XSPI1_IO1-A/PIXD3-C/IRQ11
M3	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/ TMRI1/PO4/SCK3/USB0_VBUSEN/SSIBCK1/ SDHI_WP/PIXCLK	PD04/PIO_036/A19-B/D27-B/GTETRGA/ GTIOC2A/POEGC/CTS2#-A/CTS3#-A/RTS3#-A/ SS3#-A/DE3-A/TXDB3-A/SSL21-A/CRX0-B/ SD0DAT0-B/XSPI0_IO2-A/XSPI0_WP0#-B/ PIXD4-B/IRQ4/AN028
M4	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/ SSCL10/RXD10/PIXD1	PD06/PIO_038/A17-B/D25-B/GTIV-C/GTIOC3A/ POEGB/RXD3-A/SMISO3-A/SSCL3-A/SSL23-A/ CRX1-B/SD0WP-B/XSPI0_DS-A/PIXD6-B/IRQ6/ AN030
M5	CLKOUT25M/PJ2/TXD8/SMOSI8/SSDA8/ SSLC3-B/LCD_TCON2-A	VSS
M6	PJ1/MTIOC6A/RXD8/SMISO8/SSCL8/SSLC2-B/ EPLSOUT1/LCD_TCON3-A	VCL
M7	P85/MTIOC6C/TIOCC0/LCD_DATA1-A	VCC2
M8	P55/D0[A0/D0]/EDREQ0/WAIT#/MTIOC4D/ TMO3/TXD7/SMOSI7/SSDA7/MISOC-B/CRX1/ ET0_EXOUT/LCD_DATA5-A/IRQ10	VSS
M9	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A	VCL
M10	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/RTS8#/ SCK10/RSPCKA-A/ET0_ETXD2/MMC_D5-A/ LCD_DATA11-A	P407/PIO_055/IRQ15-DS/AN007
M11	P81/EDACK0/MTIOC3D/PO27/GTIOC0B/ SMISO10/SSCL10/RXD10/ET0_ETXD0/ RMII0_TXD0/QIO3-A/SDHI_CD/MMC_D3-A/ LCD_DATA13-A	P404/PIO_052/IRQ12-DS/AN004
M12	P77/CS7#/PO23/SMOSI11/SSDA11/TXD11/ ET0_RX_ER/RMII0_RX_ER/QSPCLK-A/ SDHI_CLK-A/MMC_CLK-A/LCD_DATA17-A	MD/P315

176-Pin	RX72N (176-Pin LFBGA)	RX74N (176-Pin LFBGA)
M13	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV	RES#
M14	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/SCK11/ET0_ETXD0/ RMII0_TXD0/LCD_CLK-B	P001/PIO_001/TMCI0/GTCPPO0/GTIOC10B/ GTIOC7A/SCK7-A/CTS7#-A/TXDB7-A/SSIBCK0/ ET0_LINKSTA-D/IRQ17-DS/AN017/PCOUTZ0
M15	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/SS11#/ CTS11#/RTS11#/ET0_TX_EN/RMII0_TXD_EN/ LCD_TCON0-B	P000/PIO_000/TMRI0/GTCPPO7/GTIOC10A/ POEGB/CTS0#-B/CTS7#-A/RTS7#-A/SS7#-A/ DE7-A/TXDB7-A/AUDIO_CLK/ET0_INT-D/ IRQ16-DS/AN016
N1	VCC	PE05/PIO_045/A10-B/A22-C/GTOWLO-C/ GTIOC9B/SSL12-A/XSPI1_IO3-A/PIXD5-C/IRQ5
N2	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/ GTIOC0A/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/ SS0#/CTX1/SSIBCK0/SDHI_D1-C/PIXD7	PE04/PIO_044/A11-B/A23-C/GTOWUP-C/ GTIOC9A/CTS12#-A/SSL11-A/XSPI1_IO2-A/ XSPI1_WP0#-C/PIXD4-C/IRQ12
N3	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/GTIOC1A/SCK0/USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/PIXD6	P607/PIO_015/CS0#-B/D16-B/GTETRGB/ GTADSM0/GTIOC15B/POEGA/CTS8#-B/ CTS9#-B/RTS9#-B/SS9#-B/DE9-B/TXDB9-B/ CRX2-C/XSPI0_RSTO0#-A/IRQ15
N4	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/ PO13/GTETRGA/RXD1/SMISO1/SSCL1/SCK3/ CRX1-DS/SSILRCK1/PIXD0/IRQ5	P604/PIO_012/CS3#-C/D19-B/GTIOC6A/TXD9-B/ SMOSI9-B/SSDA9-B/TXDA9-B/SSL01-D/ XSPI0_CS1#-A/XSPI0_RSTO0#-B/IRQ4
N5	P12/WR3#/BC3#/MTIC5U/TMCI1/GTADSM0/ RXD2/SMISO2/SSCL2/SCL0[FM+]/ LCD_TCON1-A/IRQ2	PD07/PIO_039/A16-B/D24-B/GTIW-C/GTIOC3B/ POEGA/TXD3-A/SMOSI3-A/SSDA3-A/TXDA3-A/ CTX1-B/SD0CD-B/XSPI0_CS0#-A/ XSPI0_RESET1#-B/PIXD7-B/IRQ7/AN031
N6	PJ0/MTIOC6B/SCK8/SSLC1-B/EPLSOUT0/ LCD_DATA0-A	PD05/PIO_037/A18-B/D26-B/GTIU-C/GTIOC2B/ POEGD/SCK3-A/CTS3#-A/TXDB3-A/SSL22-A/ CTX0-B/SD0DAT1-B/XSPI0_IO3-A/PIXD5-B/ IRQ5/AN029
N7	P84/MTIOC6D/ET1_LINKSTA/LCD_DATA2-A	VCC2
N8	P54/D1[A1/D1]/EDACK0/ALE/MTIOC4B/TMCI1/ CTS2#/RTS2#/SS2#/MOSIC-B/CTX1/ ET0_LINKSTA/LCD_DATA6-A	VSS
N9	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	VCL
N10	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/ ET0_COL/MMC_D7-A/LCD_DATA9-A/IRQ14	P406/PIO_054/IRQ14-DS/AN006
N11	P82/EDREQ1/MTIOC4A/PO28/GTIOC2A/ SMOSI10/SSDA10/TXD10/ET0_ETXD1/ RMII0_TXD1/MMC_D4-A/LCD_DATA12-A	P405/PIO_053/IRQ13-DS/AN005
N12	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/MMC_D0-A/LCD_DATA16-A	P415/PIO_063/IRQ31/AN015/DA1
N13	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/ SS5#/SSLA1-A/ET0_ERXD3/IRQ14	P414/PIO_062/IRQ30/AN014/DA0
N14	P73/CS3#/PO16/ET0_WOL/LCD_EXTCLK-A	P003/PIO_003/GTCPPO2/GTIOC11B/GTIOC8A/ RXD7-A/SMISO7-A/SSCL7-A/SSIRXD1/ ET0_MDIO-D/IRQ19-DS/AN019/PCOUTB0

176-Pin	RX72N (176-Pin LFBGA)	RX74N (176-Pin LFBGA)
N15	VSS	P002/PIO_002/TMCI1/GTCPPO1/GTIOC11A/ GTIOC7B/TXD7-A/SMOSI7-A/SSDA7-A/ TXDA7-A/SSIBCK1/ET0_MDC-D/IRQ18-DS/ AN018/PCOUTA0
P1	VSS	CLKOUT/PE01/PIO_041/A14-B/GTOULO-C/ GTIOC7B/TXD12-A/SMOSI12-A/SSDA12-A/ TXDA12-A/RSPCK1-A/SD0DAT5-B/XSPI1_CK-A/ PIXD1-C/IRQ9
P2	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/SCK1/ TXD3/SMOSI3/SSDA3/SDA2-DS/SSITXD0/ EPLSOUT0/SDHI_D3-C/PIXD3/IRQ7/ADTRG1#	PE02/PIO_042/A13-B/TIC3/GTOVUP-C/ GTIOC8A/RXD12-A/SMISO12-A/SSCL12-A/ MOSI1-A/SD0DAT6-B/XSPI1_IO0-A/PIXD2-C/ IRQ7-DS
P3	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/ SSDA10/TXD10/EPLSOUT1/SDHI_D2-C/ PIXD2	P606/PIO_014/CS1#-C/D17-B/GTETRGA/ GTCPPO4/GTIOC15A/POEGC/SCK9-B/ CTS9#-B/TXDB9-B/SSL03-D/CTX2-C/ XSPI0_RESET0#-A/IRQ14
P4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/ PO15/GTETRGD/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/LCD_CLK-A/IRQ4	P603/PIO_011/WE#-B/D20-B/GTIOC5B/ CTS8#-B/RTS8#-B/SS8#-B/DE8-B/TXDB8-B/ CTS9#-B/MISO0-D/XSPI0_IO7-A/PCKO-B/IRQ3
P5	VCC_USB	P601/PIO_009/RAS#-B/D22-B/GTIOC4B/ RXD8-B/SMISO8-B/SSCL8-B/RSPCK0-D/ GPTP_PTPOUT1/XSPI0_IO5-A/VSYNC-B/IRQ1/ ADTRG1#
P6	VSS_USB	PD03/PIO_035/A20-B/D28-B/TOC2/GTIOC1B/ POEGA/TXD2-A/SMOSI2-A/SSDA2-A/TXDA2-A/ MISO2-A/SD0CLK-B/XSPI0_IO1-A/PIXD3-B/ IRQ3/AN027
P7	P57/RXD7/SMISO7/SSCL7/SSLC0-B/ LCD_DATA3-A	PD00/PIO_032/A23-B/D31-B/GTETRGD/ GTIOC0A/POEGD/CTS2#-A/RTS2#-A/SS2#-A/ DE2-A/TXDB2-A/CTS3#-A/SSL20-A/SD0DAT2-B/ XSPI0_CKN#-A/XSPI0_CS1#-B/PIXD0-B/IRQ0/ AN024
P8	P10/ALE/MTIC5W/TMRI3/IRQ0	P902/PIO_002/GTETRGC/GTCPPO8/SCK1-C/ CTS1#-C/TXDB1-C/XSPI0_RESET1#-A/IRQ10/ AN034
P9	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A	P900/PIO_000/GTETRGA/GTCPPO5/RXD1-C/ SMISO1-C/SSCL1-C/XSPI0_INT1#-A/ XSPI0_ECS1#-A/IRQ0/AN032
P10	P83/EDACK1/MTIOC4C/GTIOC0A/SCK10/ SS10#/CTS10#/ET0_CRS/RMII0_CRS_DV/ LCD_DATA8-A	AVSS0
P11	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/MTCLKA/ TMCI2/PO30/TIC0/GTIOC3B/RXD8/SMISO8/ SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ ET0_ETXD3/MMC_D6-A/LCD_DATA10-A/IRQ13	VREFL0
P12	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/ POE0#/GTETRGC/SCK5/CTS8#/SS8#/SS10#/ CTS10#/RTS10#/SSLA0-A/ET0_TX_CLK/QMI-A/ QIO1-A/SDHI_D1-A/MMC_D1-A/LCD_DATA15-A	P402/PIO_050/IRQ10-DS/AN002
P13	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ET0_RX_DV/ SDHI_D3-A/MMC_CD-A/LCD_DATA19-A	P400/PIO_048/IRQ8-DS/AN000

176-Pin	RX72N (176-Pin LFBGA)	RX74N (176-Pin LFBGA)
P14	P75/CS5#/PO20/SCK11/RTS11#/ET0_ERXD0/ RMII0_RXD0/SDHI_D2-A/MMC_RES#-A/ LCD_DATA20-A	P005/PIO_005/GTCPPO4/GTIOC12B/GTIOC9A/ RXD0-B/SMISO0-B/SSCL0-B/SSILRCK1/ IRQ21-DS/ADTRG2#/AN021/PCOUTB1
P15	VCC	P004/PIO_004/GTCPPO3/GTIOC12A/GTIOC8B/ TXD0-B/SMOSI0-B/SSDA0-B/TXDA0- B/SSITXD1/IRQ20-DS/AN020/PCOUTA1
R1	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/ GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/PIXD5/ IRQ9	ETHPHYCLK/PE00/PIO_040/A15-B/GTOUUP-C/ GTIOC7A/SCK12-A/CTS12#-A/TXDB12-A/ SSL10-A/SD0DAT4-B/XSPI1_CKN#-A/ XSPI1_CS1#-B/PIXD0-C/IRQ8
R2	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMD-C/PIXD4/IRQ8	PE06/PIO_046/A9-B/A21-C/TIC1/GTETRGC/ GTADSM1/GTIOC10A/POEGB/SSL13-A/ XSPI1_DS-A/PIXD6-C/IRQ6
R3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/ PO14/RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/ SMISO3/SSCL3/SCL2-DS/USB0_VBUSEN/ USB0_VBUS/USB0_OVRCURB/IRQ6/ADTRG0#	P605/PIO_013/CS2#-C/D18-B/GTIOC6B/ RXD9-B/SMISO9-B/SSCL9-B/SSL02-D/ XSPI0_INT0#-A/XSPI0_ECS0#-A/IRQ13
R4	P13/WR2#/BC2#/MTIOC0B/TIOCA5/TMO3/ PO13/GTADSM1/TXD2/SMOSI2/SSDA2/ SDA0[FM+]/LCD_TCON0-A/IRQ3/ADTRG1#	P602/PIO_010/CAS#-B/D21-B/GTIOC5A/ SCK8-B/CTS8#-B/TXDB8-B/MOSI0-D/ XSPI0_IO6-A/HSYNC-B/IRQ2/ADTRG2#
R5	USB0_DM	P600/PIO_008/SDCS#-B/D23-B/GTIOC4A/ TXD8-B/SMOSI8-B/SSDA8-B/TXDA8-B/SSL00-D/ GPTP_PTPOUT0/XSPI0_IO4-A/PIXCLK-B/IRQ0/ ADTRG0#
R6	USB0_DP	PD02/PIO_034/A21-B/D29-B/TIC2/GTETRGB/ GTIOC1A/POEGB/RXD2-A/SMISO2-A/SSCL2-A/ MOSI2-A/SD0CMD-B/XSPI0_IO0-A/PIXD2-B/ IRQ2/AN026
R7	CLKOUT25M/P56/EDACK1/MTIOC3C/TIOCA1/ SCK7/RSPCKC-B/LCD_DATA4-A	PD01/PIO_033/A22-B/D30-B/GTETRGC/ GTIOC0B/POEGC/SCK2-A/CTS2#-A/TXDB2-A/ RSPCK2-A/SD0DAT3-B/XSPI0_CK-A/PIXD1-B/ IRQ1/AN025
R8	P11/MTIC5V/TMCI3/SCK2/EPLSOUT1/ LCD_DATA7-A/IRQ1	P903/PIO_003/GTETRGD/GTCPPO9/POEGD/ CTS6#-B/CTS1#-C/RTS1#-C/SS1#-C/DE1-C/ TXDB1-C/XSPI0_WP1#-A/IRQ11/AN035
R9	P53[*1]/BCLK	P901/PIO_001/GTETRGB/GTCPPO6/TXD1-C/ SMOSI1-C/SSDA1-C/TXDA1-C/ XSPI0_RSTO1#-A/XSPI0_RESET0#-B/IRQ9/ AN033
R10	VSS	AVCC0
R11	VCC	VREFH0
R12	P80/EDREQ0/MTIOC3B/PO26/SCK10/RTS10#/ ET0_TX_EN/RMII0_TXD_EN/QIO2-A/SDHI_WP/ MMC_D2-A/LCD_DATA14-A	P403/PIO_051/IRQ11-DS/AN003
R13	P76/CS6#/PO22/SMISO11/SSCL11/RXD11/ ET0_RX_CLK/REF50CK0/QSSL-A/SDHI_CMD-A/ MMC_CMD-A/LCD_DATA18-A	P401/PIO_049/IRQ9-DS/AN001
R14	P74/A20/CS4#/PO19/SS11#/CTS11#/ ET0_ERXD1/RMII0_RXD1/LCD_DATA21-A	P007/PIO_007/GTCPPO6/GTIOC13B/POEGA/ CTS0#-B/RTS0#-B/SS0#-B/DE0-B/TXDB0-B/ IRQ23-DS/ADTRG0#/AN023/PDMDAT0-C

176-Pin	RX72N (176-Pin LFBGA)	RX74N (176-Pin LFBGA)
R15	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/LCD_DATA22-A/IRQ12	P006/PIO_006/GTCPPO5/GTIOC13A/GTIOC9B/ SCK0-B/CTS0#-B/TXDB0-B/IRQ22-DS/ ADTRG1#/AN022/PDMCLK0-C/PCOUTZ1

Note: 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

3.3 176-Pin LFQFP Package

Table 3.5 is Comparative Listing of RX72M/RX74M 176-Pin LFQFP Package Pin Functions, and Table 3.6 is Comparative Listing of RX72N/RX74N 176-Pin LFQFP Package Pin Functions

Table 3.5 Comparative Listing of RX72M/RX74M 176-Pin LFQFP Package Pin Functions

176-Pin LFQFP	RX72M	RX74M
1	AVSS0	P003/PIO_003/GTCPPO2/GTIOC11B/GTIOC8A/ RXD7-A/SMISO7-A/SSCL7-A/SSIRXD1/ ET0_MDIO-D/CAT0_MDIO-E/IRQ19-DS/AN019/ DSMDAT1-B/PCOUTB0
2	P05/SSILRCK1/IRQ13/DA1	P002/PIO_002/TMCI1/GTCPPO1/GTIOC11A/ GTIOC7B/TXD7-A/SMOSI7-A/SSDA7-A/ TXDA7-A/SSIBCK1/ET0_MDC-D/CAT0_MDC-E/ IRQ18-DS/AN018/DSMCLK1-B/PCOUTA0
3	AVCC1	P001/PIO_001/TMCI0/GTCPPO0/GTIOC10B/ GTIOC7A/SCK7-A/CTS7#-A/TXDB7-A/SSIBCK0/ ET0_LINKSTA-D/CAT0_LINKSTA-E/IRQ17-DS/ AN017/DSMDAT0-B/PCOUTZ0
4	P03/SSIDATA1/IRQ11/DA0	P000/PIO_000/TMRI0/GTCPPO7/GTIOC10A/ POEGB/CTS0#-B/CTS7#-A/RTS7#-A/SS7#-A/ DE7-A/TXDB7-A/AUDIO_CLK/ET0_INT-D/ CATRESTOUT-E/IRQ16-DS/AN016/DSMCLK0-B
5	AVSS1	VCC
6	P02/TMCI1/SCK6/SSIBCK1/CATLEDSTER/ IRQ10/AN120	VSS
7	P01/TMCI0/RXD6/SMISO6/SSCL6/SSIBCK0/ CATLEDERR/IRQ9/AN119	VSS
8	P00/TMRI0/TXD6/SMOSI6/SSDA6/AUDIO_CLK/ CATLATCH1/IRQ8/AN118	VCL
9	PF5/WAIT#/SSILRCK0/CATLATCH0/IRQ4	RES#
10	EMLE	MD/P315
11	PJ5/POE8#/CTS2#/RTS2#/SS2#/SSIRXD0/ EPLSOUT0/CATSYNC0	P312/PIO_060/BACK#-B/RTCIC2/GTETRGD/ GTCPPO15/POEGA/SSL13-B/SSILRCK0/ ET1_WOL-C/IRQ20/ADTRG2#/DSMDAT2-C/TAMPI2
12	VSS	P311/PIO_059/BREQ#-B/RTCIC1/GTETRGC/ GTCPPO14/POEGD/CTS7#-A/SSL12-B/ SSIRXD0/ET0_WOL-C/IRQ19/ADTRG1#/ DSMCLK2-C/TAMPI1
13	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/SS6#/ CTS0#/RTS0#/SS0#/SSITXD0/ET0_EXOUT/ CATRESTOUT	P310/PIO_058/RTCIC0/CACREF/GTETRGB/ GTCPPO1/POEGC/CTS0#-C/CTS1#-B/SSL11-B/ SSITXD0/ET1_INT-E/CATIRQ-D/IRQ18/ ADTRG0#/TAMPI0
14	VCL	VBATT/VCC
15	VBATT	XCIN/EXCIN/P309
16	NC	XCOUT/P308
17	TRST#/PF4	VSS
18	MD/FINED	XTAL/P307
19	XCIN	EXTAL/P306
20	XCOUT	VCC
21	RES#	P305/NMI/IRQ0
22	XTAL/P37	AVCC_USBHS

176-Pin LFQFP	RX72M	RX74M
23	VSS	USBHS_RREF
24	EXTAL/P36	AVSS_USBHS
25	VCC	USBHS_DM
26	UPSEL/P35/NMI	USBHS_DP
27	P34/MTIOC0A/TMCI3/PO12/POE10#/SCK6/SCK0/ET0_LINKSTA/CAT0_LINKSTA/IRQ4/DSMDAT0	VSS_USBHS
28	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/SMISO6/SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/IRQ3-DS/DSMCLK0	VCC_USBHS
29	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCIC2/RTCOUT/POE0#/POE10#/TXD6/SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS	VCC_USB
30	TMS/PF3	PF01/PIO_049/GTCPPO15/USB0_DM/IRQ1
31	TDI/PF2/RXD1/SMISO1/SSCL1/CATI2CCLK	PF00/PIO_048/GTCPPO14/USB0_DP/IRQ0
32	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/ET1_MDC/PMGI1_MDC/IRQ1-DS	VSS_USB
33	P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ET1_MDIO/PMGI1_MDIO/IRQ0-DS	P207/PIO_023/A23-C/CS4#-C/TMRI3/GTOWLO-D/GTIOC2B/GTIOC6B/RXD1-B/SMISO1-B/SSCL1-B/MISO1-B/SDAHS2-B/CRX1-A/USB0_ID/USBHS_OVRCURB-DS/ET0_RXD3-B/CAT0_ERXD3-B/PCKO-A/IRQ3-DS/ADTRG2#/DSMDAT5-B
34	TCK/PF1/SCK1	P206/PIO_022/A22-C/CS5#-C/TMO3/RTCOUT/GTOWUP-D/GTIOC2A/GTIOC6A/CTS6#-A/TXD1-B/SMOSI1-B/SSDA1-B/TXDA1-B/MOSI1-B/SCLHS2-B/CTX1-A/USB0_EXICEN/USBHS_OVRCURA-DS/SSITXD1/ET0_RXD2-B/CAT0_ERXD2-B/VSYNC-A/IRQ2-DS/ADTRG1#/DSMCLK5-B/PCOUTZ1
35	TDO/PF0/TXD1/SMOSI1/SSDA1/CATI2CDATA	CLKOUT/P205/PIO_021/A21-C/CS6#-C/GTOVLO-D/GTIOC1B/GTIOC5B/SCK1-B/CTS1#-B/TXDB1-B/RSPCK1-B/SDAHS1-B/CRX0-A/USB0_VBUS/USBHS_VBUSEN/SSIRXD1/ET0_RXD1-B/RMII0_RXD1-B/CAT0_ERXD1-B/SD0CD-C/HSYNC-A/IRQ5/ADTRG0#/DSMDAT4-B/PCOUTB1
36	P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A/ET1_WOL/CATIRQ	ETHPHYCLK/P204/PIO_020/A20-C/CS7#-C/TMRI1/GTOVUP-D/GTIOC1A/GTIOC5A/CTS1#-B/RTS1#-B/SS1#-B/DE1-B/TXDB1-B/SSL10-B/SCLHS1-B/CTX0-A/USB0_VBUSEN/USBHS_VBUS-DS/SSIBCK1/ET0_RXD0-B/RMII0_RXD0-B/CAT0_ERXD0-B/SD0WP-C/PIXCLK-A/IRQ12/DSMCLK4-B/PCOUTA1
37	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A/ET1_EXOUT/CATLINKACT1	VCL
38	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/SSIDATA1/SDHI_CD/HSYNC/ADTRG0#	VSS
39	VCC	VCC

176-Pin LFQFP	RX72M	RX74M
40	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/SSIBCK1/SDHI_WP/PIXCLK	P203/PIO_019/CS2#-B/BACK#-A/GTOULO-D/GTIOC0B/GTIOC4B/RXD6-A/SMISO6-A/SSCL6-A/CTS3#-B/SSL00-C/SDA00-B/CRX2-B/USB0_OVRCURB/USBHS_ID/SSIBCK0/ET0_RX_CLK-B/RMII0_REF50CK-B/CAT0_RX_CLK-B/CATI2CDATA-C/SD0DAT1-C/PIXD7-A/IRQ3/DSMDAT3-B/PDMDAT0-B
41	VSS	P202/PIO_018/CS3#-B/BREQ#-A/TMO0/GTOUUP-D/GTIOC0A/GTIOC4A/TXD6-A/SMOSI6-A/SSDA6-A/TXDA6-A/RSPCK0-C/SCL00-B/CTX2-B/USB0_OVRCURA/USBHS_EXICEN/AUDIO_CLK/ET0_RX_DV-B/RMII0_CRS_DV-B/CAT0_RX_DV-B/CATI2CCLK-C/SD0DAT0-C/PIXD6-A/IRQ15/DSMCLK3-B/PDMCLK0-B
42	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/SDHI_D1-C/PIXD7	ETHPHYCLK/P304/PIO_028/ALE-C/WAIT#-B/TMCI3/GTETRGD/GTCPPO0/POEGA/CTS0#-A/CTS1#-A/USB0_VBUSEN/USBHS_ID/ET0_INT-E/CATRESTOUT-D/IRQ0-DS/ADTRG0#
43	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/GTIOC1A/SCK0/USB0_OVRCURB/AUDIO_CLK/SDHI_D0-C/PIXD6	TDI/P303/PIO_027/TMCI2/GTCPPO13/RXD0-A/SMISO0-A/SSCL0-A/RXD1-A/SMISO1-A/SSCL1-A/MISO1-C/ET1_CRS-D/IRQ1
44	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/USB0_EXICEN/SSILRCK0/SDHI_CLK-C/PIXD5/IRQ9	TDO/P302/PIO_026/TMRI3/GTCPPO12/TXD0-A/SMOSI0-A/SSDA0-A/TXDA0-A/TXD1-A/SMOSI1-A/SSDA1-A/TXDA1-A/MOSI1-C/ET1_COL-D/IRQ4
45	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/SDHI_CMD-C/PIXD4/IRQ8	TCK/SWCLK/P301/PIO_025/TMCI3/GTCPPO11/SCK0-A/CTS0#-A/TXDB0-A/SCK1-A/CTS1#-A/TXDB1-A/RSPCK1-C/ET1_WOL-D/IRQ7
46	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/GTIOC0B/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/SSITXD0/EPLSOUT0/CATSYNC0/SDHI_D3-C/PIXD3/IRQ7/ADTRG1#	TMS/SWDIO/P300/PIO_024/TMO1/GTCPPO10/CTS0#-A/RTS0#-A/SS0#-A/DE0-A/TXDB0-A/CTS1#-A/RTS1#-A/SS1#-A/DE1-A/TXDB1-A/SSL10-C/ET0_WOL-D/IRQ6
47	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/SSDA10/TXD10/EPLSOUT1/CATSYNC1/SDHI_D2-C/PIXD2	P805/PIO_061/GTADSM1/GTIOC15B/SCK5-B/CTS5#-B/TXDB5-B/SSL22-B/CRX0-D/USB0_VBUSEN/USBHS_VBUSEN/ET0_TXD0-C/RMII0_TXD0-C/CAT0_ETXD0-C/HSYNC-D/IRQ5/ADSYNC-C/DSMDAT0-F/PCINB0
48	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/USB0_VBUSEN/USB0_VBUS/USB0_OVRCURB/IRQ6/ADTRG0#	P804/PIO_060/GTADSM0/GTIOC15A/CTS5#-B/RTS5#-B/SS5#-B/DE5-B/TXDB5-B/SSL21-B/CTX0-D/USB0_OVRCURA/USBHS_OVRCURA/ET0_TX_EN-C/RMII0_TX_EN-C/CAT0_TX_EN-C/PCKO-D/IRQ4/DSMCLK0-F/PCINA0
49	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/SSCL10/RXD10/CATLINKACT0/PIXD1	P201/PIO_017/TMCI0/GTIW-D/GTIOC3B/GTIOC14B/SCK6-A/CTS6#-A/TXDB6-A/MISO0-C/SCLHS1-A/USB0_EXICEN/SSILRCK0/ET0_RX_ER-B/RMII0_RX_ER-B/CAT0_RX_ER-B/SD0CLK-C/PIXD5-A/IRQ9/PCINZ0
50	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/GTETRGA/RXD1/SMISO1/SSCL1/SCK3/CRX1-DS/SSILRCK1/CATLEDRUN/PIXD0/IRQ5	P200/PIO_016/TMRI0/GTETRGA/GTIOC3A/GTIOC14A/CTS6#-A/RTS6#-A/SS6#-A/DE6-A/TXDB6-A/MOSI0-C/SDAHS1-A/USB0_ID/SSIRXD0/ET0_TX_EN-B/RMII0_TX_EN-B/CAT0_TX_EN-B/SD0CMD-C/PIXD4-A/IRQ8/ADTRG2#/PCINZ1

176-Pin LFQFP	RX72M	RX74M
51	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/ PO15/GTETRGD/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/LCD_CLK-A/IRQ4	P107/PIO_015/TMO1/GTIV-D/GTIOC15B/ POEGA/TXD3-B/SMOSI3-B/SSDA3-B/TXDA3-B/ SDAHS2-A/SSITXD0/ET0_TXD3-B/ CAT0_ETXD3-B/CATI2CDATA-B/SD0DAT3-C/ PIXD3-A/IRQ31-DS/ADTRG1#/PCINB1
52	P13/WR2#/BC2#/MTIOC0B/TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/SSDA2/SDA0[FM+]/ LCD_TCON0-A/IRQ3/ADTRG1#	CLKOUT/P106/PIO_014/TMO2/RTCOUT/GTIU-D/ GTIOC15A/POEGB/RXD3-B/SMISO3-B/ SSCL3-B/SCLHS2-A/ET0_TXD2-B/ CAT0_ETXD2-B/CATI2CCLK-B/SD0DAT2-C/ PIXD2-A/IRQ30-DS/ADTRG0#/PCINA1
53	P12/WR3#/BC3#/MTIC5U/TMCI1/GTADSM0/ RXD2/SMISO2/SSCL2/SCL0[FM+]/ LCD_TCON1-A/IRQ2	P105/PIO_013/TMCI2/GTIV-E/GTIOC14B/ TXD2-B/SMOSI2-B/SSDA2-B/TXDA2-B/SCK3-B/ CTS3#-B/TXDB3-B/CRX2-A/USB0_VBUS/ USBHS_OVRCURB/SSILRCK1/ET0_TXD1-B/ RMII0_TXD1-B/CAT0_ETXD1-B/CATLEDRUN-C/ PIXD1-A/IRQ29-DS/ADST1-A/DSMDAT1-C/ PCINB0
54	VCC_USB	P104/PIO_012/TMRI2/GTIW-E/GTIOC14A/ RXD2-B/SMISO2-B/SSCL2-B/CTS3#-B/RTS3#-B/ SS3#-B/DE3-B/TXDB3-B/CTX2-A/ USB0_OVRCURA-DS/USBHS_VBUS/ ET0_TXD0-B/RMII0_TXD0-B/CAT0_ETXD0-B/ CATLEDSTER-C/PIXD0-A/IRQ4/ADST0-A/ DSMCLK1-C/PCINA0
55	USB0_DM	VCL
56	USB0_DP	VSS
57	VSS_USB	VCC
58	CLKOUT25M/PJ2/TXD8/SMOSI8/SSDA8/ SSLC3-B/LCD_TCON2-A	P103/PIO_011/TMO3/GTADSM1/GTIOC13B/ CTS2#-B/SDA00-A/ET0_CRS-D/CATI2CDATA-A/ IRQ3
59	PJ1/MTIOC6A/RXD8/SMISO8/SSCL8/SSLC2-B/ EPLSOUT1/CATSYNC1/LCD_TCON3-A	P102/PIO_010/TMCI1/GTADSM0/GTIOC13A/ SCL00-A/ET0_COL-D/CATI2CCLK-A/IRQ2
60	PJ0/MTIOC6B/SCK8/SSLC1-B/EPLSOUT0/ CATSYNC0/LCD_DATA0-A	P101/PIO_009/CS0#-A/ALE-B/TMCI3/ GTETRGC/GTADSM1/GTIOC12B/SCK2-B/ CTS2#-B/TXDB2-B/USB0_VBUS-DS/ USBHS_EXICEN/ET0_TX_CLK-B/ CAT0_TX_CLK-B/CAT0_LINKSTA-D/IRQ1/ ADTRG1#/DSMDAT0-C
61	P85/MTIOC6C/TIOCC0/LCD_DATA1-A	P100/PIO_008/CS1#-B/WAIT#-A/TMRI3/ CACREF/GTIU-E/GTADSM0/GTIOC12A/ CTS2#-B/RTS2#-B/SS2#-B/DE2-B/TXDB2-B/ CTS5#-B/USB0_OVRCURB-DS/USBHS_VBUS/ ET0_TX_ER-B/CATLINKACT0-B/CATLEDERR-C/ IRQ0/ADTRG2#/DSMCLK0-C
62	P84/MTIOC6D/ET1_LINKSTA/CAT1_LINKSTA/ LCD_DATA2-A	VCC_DCDC
63	P57/RXD7/SMISO7/SSCL7/SSLC0-B/ LCD_DATA3-A	VCC_DCDC
64	CLKOUT25M/P56/EDACK1/MTIOC3C/TIOCA1/ SCK7/RSPCKC-B/LCD_DATA4-A/DSMDAT1	VCC_DCDC
65	P55/D0[A0/D0]/EDREQ0/WAIT#/MTIOC4D/ TMO3/TXD7/SMOSI7/SSDA7/MISOC-B/CRX1/ ET0_EXOUT/LCD_DATA5-A/IRQ10	VLO
66	P54/D1[A1/D1]/EDACK0/ALE/MTIOC4B/TMCI1/C TS2#/RTS2#/SS2#/MOSIC-B/CTX1/ ET0_LINKSTA/CAT0_LINKSTA/LCD_DATA6-A	VLO

176-Pin LFQFP	RX72M	RX74M
67	P11/MTIC5V/TMCI3/SCK2/EPLSOUT1/ CATSYNC1/LCD_DATA7-A/IRQ1	VLO
68	P10/ALE/MTIC5W/TMRI3/IRQ0	VSS_DCDC
69	P53*1/BCLK	VSS_DCDC
70	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A/ CATLEDSTER	P503/PIO_035/WR3#-A/BC3#-A/A19-C/ GTIOC3B/RXD2-C/SMISO2-C/SSCL2-C/CRX1-C/ USB0_OVRCURB/SSIRXD0/ET1_WOL-B/ CATLEDERR-A/SD0DAT7-A/IRQ3/DSMDAT1-E
71	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	P502/PIO_034/WR2#-A/BC2#-A/A18-C/ GTIOC3A/TXD2-C/SMOSI2-C/SSDA2-C/ TXDA2-C/SSL13-C/CTX1-C/ET0_WOL-B/ CATLEDRUN-A/SD0DAT6-A/IRQ2/ADST2-C/ DSMCLK1-E
72	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A/CATLEDERR	P501/PIO_033/WR1#-A/BC1#-A/A17-C/ GTIOC2B/SCK2-C/CTS2#-C/TXDB2-C/SSL12-C/ CRX0-C/ET0_INT-B/CATLEDSTER-A/ SD0DAT5-A/IRQ1/ADST1-C/DSMDAT2-E
73	VSS	P500/PIO_032/WR#-A/WR0#-A/A16-C/ GTIOC2A/CTS2#-C/RTS2#-C/SS2#-C/DE2-C/ TXDB2-C/CTS7#-B/SSL11-C/CTX0-C/ ET0_LINKSTA-B/CAT0_LINKSTA-B/SD0DAT4-A/ IRQ0/ADST0-C/DSMCLK2-E
74	P83/EDACK1/MTIOC4C/GTIOC0A/SCK10/ SS10#/CTS10#/ET0_CRS/RMII0_CRS_DV/ CAT0_RX_DV/LCD_DATA8-A/DSMCLK1	P803/PIO_059/CS3#-A/WR1#-B/BC1#-B/ GTIOC1B/POEGA/CTS10#-B/RTS10#-B/ SS10#-B/DE10-B/TXDB10-B/CTX2-D/USB0_ID/ ET0_MDC-B/CAT0_MDC-B/IRQ3/ADSYNC-B/ DSMDAT3-C
75	VCC	P802/PIO_058/CS2#-A/WR#-B/WR0#-B/GTIW-B/ GTIOC1A/POEGB/SCK10-B/CTS10#-B/ TXDB10-B/CRX2-D/USB0_EXICEN/ ET0_MDIO-B/CAT0_MDIO-B/IRQ2/ADCNV2-B/ DSMCLK3-C
76	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/ ET0_COL/MMC_D7-A/LCD_DATA9-A/IRQ14	VCL
77	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/MTCLKA/ TMCI2/PO30/TIC0/GTIOC3B/RXD8/SMISO8/ SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ ET0_ETXD3/CAT0_ETXD3/CATLATCH1/ MMC_D6-A/LCD_DATA10-A/IRQ13	VSS
78	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/RTS8#/ SCK10/RSPCKA-A/ET0_ETXD2/CAT0_ETXD2/ MMC_D5-A/LCD_DATA11-A	VCC
79	P82/EDREQ1/MTIOC4A/PO28/GTIOC2A/ SMOSI10/SSDA10/TXD10/ET0_ETXD1/ RMII0_TXD1/CAT0_ETXD1/CATI2CDATA/ MMC_D4-A/LCD_DATA12-A	CLKOUT/P801/PIO_057/EBCLK-A/GTIV-B/ GTIOC0B/POEGC/TXD10-B/SMOSI10-B/ SSDA10-B/TXDA10-B/ET0_CRS-B/ CATSYNC0-A/IRQ9/ADCNV1-B/DSMDAT4-C
80	P81/EDACK0/MTIOC3D/PO27/GTIOC0B/ SMISO10/SSCL10/RXD10/ET0_ETXD0/ RMII0_TXD0/CAT0_ETXD0/CATI2CCLK/QIO3-A/ SDHI_CD/MMC_D3-A/LCD_DATA13-A	P800/PIO_056/CS1#-A/DQM0-B/GTIU-B/ GTIOC0A/POEGD/RXD10-B/SMISO10-B/ SSCL10-B/ET0_COL-B/CATLATCH0-A/IRQ8/ ADCNV0-B/DSMCLK4-C

176-Pin LFQFP	RX72M	RX74M
81	P80/EDREQ0/MTIOC3B/PO26/SCK10/RTS10#/ ET0_TX_EN/RMII0_TXD_EN/CAT0_TX_EN/ CATLATCH0/QIO2-A/SDHI_WP/MMC_D2-A/ LCD_DATA14-A	ETHPHYCLK/PC07/PIO_031/D0-A/TMO2/TOC0/ CACREF/GTETRGD/GTADSM1/GTIOC15B/ POEGA/TXD8-A/SMOSI8-A/SSDA8-A/TXDA8-A/ MISO0-A/SSITXD0/CATRESTOUT-A/SD0CD-A/ IRQ14/DSMDAT5-C/PDMDAT0-A
82	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/ POE0#/GTETRGC/SCK5/CTS8#/SS8#/SS10#/ CTS10#/RTS10#/SSLA0-A/ET0_TX_CLK/ CAT0_TX_CLK/CATSYNC0/QMI-A/QIO1-A/ SDHI_D1-A/MMC_D1-A/LCD_DATA15-A	PC06/PIO_030/D1-A/TMCI2/TIC0/GTETRGC/ GTCPPO7/GTIOC15A/POEGB/RXD8-A/ SMISO8-A/SSCL8-A/MOSI0-A/SSILRCK0/ ET0_TX_ER-A/CATLINKACT0-A/SD0WP-A/ IRQ13/DSMCLK5-C/PDMCLK0-A
83	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER/ QMO-A/QIO0-A/SDHI_D0-A/MMC_D0-A/ LCD_DATA16-A	PC05/PIO_029/D2-A/TMRI2/GTOWLO-B/ GTIOC9B/SCK8-A/CTS8#-A/TXDB8-A/ RSPCK0-A/SSIBCK0/ET0_TX_EN-A/ RMII0_TX_EN-A/CAT0_TX_EN-A/SD0DAT1-A/ IRQ5/PCOUTZ1
84	P77/CS7#/PO23/SMOSI11/SSDA11/TXD11/ ET0_RX_ER/RMII0_RX_ER/CAT0_RX_ER/ QSPCLK-A/SDHI_CLK-A/MMC_CLK-A/ LCD_DATA17-A	PC04/PIO_028/D3-A/TMCI1/GTOWUP-B/ GTIOC9A/CTS8#-A/RTS8#-A/SS8#-A/DE8-A/ TXDB8-A/CTS11#-A/SSL00-A/AUDIO_CLK/ ET0_TXD3-A/CAT0_ETXD3-A/SD0DAT0-A/ IRQ12/PCOUTB1
85	P76/CS6#/PO22/SMISO11/SSCL11/RXD11/ ET0_RX_CLK/REF50CK0/CAT0_RX_CLK/ QSSL-A/SDHI_CMD-A/MMC_CMD-A/ LCD_DATA18-A	PC03/PIO_027/D4-A/GTOVLO-B/GTIOC8B/ TXD11-A/SMOSI11-A/SSDA11-A/TXDA11-A/ SDAHS1-C/ET0_TXD2-A/CAT0_ETXD2-A/ SD0CLK-A/IRQ11/PCOUTA1
86	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ET0_RX_DV/ CAT0_RX_DV/SDHI_D3-A/MMC_CD-A/ LCD_DATA19-A	PC02/PIO_026/D5-A/GTOVUP-B/GTIOC8A/ RXD11-A/SMISO11-A/SSCL11-A/SSL03-A/ SCLHS1-C/ET0_TXD1-A/RMII0_TXD1-A/ CAT0_ETXD1-A/SD0CMD-A/IRQ10/PCOUTZ0
87	P75/CS5#/PO20/SCK11/RTS11#/ET0_ERXD0/ RMII0_RXD0/CAT0_ERXD0/SDHI_D2-A/ MMC_RES#-A/LCD_DATA20-A/DSMDAT2	PC01/PIO_025/D6-A/GTOULO-B/GTIOC7B/ SCK11-A/CTS11#-A/TXDB11-A/SSL02-A/ SDA00-C/ET0_TXD0-A/RMII0_TXD0-A/ CAT0_ETXD0-A/SD0DAT3-A/IRQ12/PCOUTB0
88	P74/A20/CS4#/PO19/SS11#/CTS11#/ ET0_ERXD1/RMII0_RXD1/CAT0_ERXD1/ LCD_DATA21-A/DSMCLK2	PC00/PIO_024/D7-A/GTOUUP-B/GTIOC7A/ CTS11#-A/RTS11#-A/SS11#-A/DE11-A/ TXDB11-A/SSL01-A/SCL00-C/ET0_TX_CLK-A/ CAT0_TX_CLK-A/SD0DAT2-A/IRQ14/PCOUTA0
89	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/CAT0_ERXD2/ LCD_DATA22-A/IRQ12	PB07/PIO_023/D8-A/GTOWLO-A/GTIOC6B/ TXD9-A/SMOSI9-A/SSDA9-A/TXDA9-A/ ET0_LINKSTA-A/CAT0_LINKSTA-A/IRQ15
90	VCC	PB06/PIO_022/D9-A/GTOWUP-A/GTIOC6A/ RXD9-A/SMISO9-A/SSCL9-A/ET0_RX_ER-A/ RMII0_RX_ER-A/CAT0_RX_ER-A/IRQ6
91	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/ SS5#/SSLA1-A/ET0_ERXD3/CAT0_ERXD3/ IRQ14	PB05/PIO_021/D10-A/TMRI1/GTOVLO-A/ GTIOC5B/SCK9-A/CTS9#-A/TXDB9-A/ ET0_RX_DV-A/RMII0_CRS_DV-A/ CAT0_RX_DV-A/IRQ13
92	VSS	PB04/PIO_020/D11-A/GTOVUP-A/GTIOC5A/ CTS4#-A/CTS9#-A/RTS9#-A/SS9#-A/DE9-A/ TXDB9-A/ET0_RX_CLK-A/RMII0_REF50CK-A/ CAT0_RX_CLK-A/IRQ4
93	P73/CS3#/PO16/ET0_WOL/LCD_EXTCLK-A	VCC
94	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV/CAT0_RX_DV	VSS
95	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1/CAT0_ETXD1	VCL

176-Pin LFQFP	RX72M	RX74M
96	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/SCK11/ET0_ETXD0/ RMII0_TXD0/CAT0_ETXD0/LCD_CLK-B	PB03/PIO_019/D12-A/TMO0/GTOULO-A/ GTIOC4B/SCK4-A/CTS4#-A/TXDB4-A/ ET0_RXD3-A/CAT0_ERXD3-A/IRQ3
97	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/SS11#/ CTS11#/RTS11#/ET0_TX_EN/RMII0_TXD_EN/ CAT0_TX_EN/LCD_TCON0-B	PB02/PIO_018/D13-A/GTOUUP-A/GTIOC4A/ CTS4#-A/RTS4#-A/SS4#-A/DE4-A/TXDB4-A/ CTS9#-A/ET0_RXD2-A/CAT0_ERXD2-A/IRQ2
98	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK4/SCK6/ET0_RX_ER/ RMII0_RX_ER/CAT0_RX_ER/LCD_TCON1-B	PB01/PIO_017/D14-A/TMCI0/GTETRGB/ GTCPPO4/GTIOC14B/POEGA/TXD4-A/ SMOSI4-A/SSDA4-A/TXDA4-A/ET0_RXD1-A/ RMII0_RXD1-A/CAT0_ERXD1-A/IRQ4-DS/ DSMDAT2-A/PCINB1
99	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/ SS4#/CTS6#/RTS6#/SS6#/ET0_RX_CLK/ REF50CK0/CAT0_RX_CLK/LCD_TCON2-B	PB00/PIO_016/D15-A/GTETRGA/GTADSM0/ GTIOC14A/POEGC/RXD4-A/SMISO4-A/ SSCL4-A/ET0_RXD0-A/RMII0_RXD0-A/ CAT0_ERXD0-A/IRQ12/ADST2-A/DSMCLK2-A/ PCINA1
100	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/ PO25/TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/ SSDA6/ET0_ERXD0/RMII0_RXD0/ CAT0_ERXD0/LCD_TCON3-B/IRQ4-DS	PG02/PIO_058/DQM3-A/WR3#-C/BC3#-C/ GTIOC11A/TXD8-C/SMOSI8-C/SSDA8-C/ TXDA8-C/ET1_RX_ER-A/RMII1_RX_ER-A/ CAT1_RX_ER-A/IRQ10/DSMCLK1-D
101	P72/A19/CS2#/ET0_MDC/CAT0_MDC/ PMGI0_MDC/LCD_DATA23-A/DSMDAT3	PG01/PIO_057/DQM0-A/WR#-C/WR0#-C/ GTCPPO1/RXD8-C/SMISO8-C/SSCL8-C/ ET1_RX_DV-A/RMII1_CRS_DV-A/ CAT1_RX_DV-A/IRQ9/DSMDAT2-D
102	P71/A18/CS1#/ET0_MDIO/CAT0_MDIO/ PMGI0_MDIO/DSMCLK3	PG00/PIO_056/DQM1-A/WR1#-C/BC1#-C/ GTCPPO0/SCK8-C/CTS8#-C/TXDB8-C/ ET1_RX_CLK-A/RMII1_REF50CK-A/ CAT1_RX_CLK-A/IRQ8/DSMCLK2-D
103	VCC	ETHPHYCLK/PA07/PIO_015/A0-A/BC0#-A/ DQM1-B/GTIOC3B/GTIOC13B/RXD10-A/ SMISO10-A/SSCL10-A/MISO0-B/ET1_TX_ER-A/ CATLINKACT1-A/IRQ7/PCINB0
104	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/ET0_ERXD1/ RMII0_RXD1/CAT0_ERXD1/LCD_DATA0-B/ IRQ12	PA06/PIO_014/A1-A/DQM2-B/TMCI3/GTIOC3A/ GTIOC13A/TXD10-A/SMOSI10-A/SSDA10-A/ TXDA10-A/MOSI0-B/ET1_TXD3-A/ CAT1_ETXD3-A/IRQ14/PCINZ1
105	VSS	PA05/PIO_013/A2-A/GTIOC2B/GTIOC12B/ SCK10-A/CTS10#-A/TXDB10-A/RSPCK0-B/ ET1_TXD2-A/CAT1_ETXD2-A/IRQ5/PCINA0
106	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B	PA04/PIO_012/A3-A/TMRI0/GTIOC2A/ GTIOC12A/CTS10#-A/RTS10#-A/SS10#-A/ DE10-A/TXDB10-A/SSL00-B/ET1_TXD1-A/ RMII1_TXD1-A/CAT1_ETXD1-A/IRQ5-DS/ PCINZ0
107	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/RTS5#/SS5#/ MOSIA-B/ET0_EXOUT/CATRESTOUT/ LCD_DATA2-B	VCC
108	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/RSP CKA-B/ET0_LINKSTA/CAT0_LINKSTA/ LCD_DATA3-B	VSS
109	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/ TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC/ CAT0_MDC/CATIRQ/PMGI0_MDC/ LCD_DATA4-B/IRQ5-DS	VCL
110	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/ CAT0_MDIO/PMGI0_MDIO/LCD_DATA5-B/ IRQ6-DS	PA03/PIO_011/A4-A/GTIOC1B/GTIOC11B/ RXD5-A/SMISO5-A/SSCL5-A/ET1_TXD0-A/ RMII1_TXD0-A/CAT1_ETXD0-A/IRQ6-DS/ ADSYNC-A/DSMDAT1-A

176-Pin LFQFP	RX72M	RX74M
111	TRDATA3/PG7/D31/ET1_TX_ER	PA02/PIO_010/A5-A/GTIW-A/GTIOC1A/ GTIOC11A/TXD5-A/SMOSI5-A/SSDA5-A/ TXDA5-A/SSL03-B/ET1_TX_CLK-A/ CAT1_TX_CLK-A/IRQ10/ADCNV2-A/DSMCLK1-A
112	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/CATLINKACT1/ LCD_DATA6-B	PA01/PIO_009/A6-A/GTIV-A/GTIOC0B/ GTIOC10B/SCK5-A/CTS5#-A/TXDB5-A/SSL02-B/ ET1_TX_EN-A/RMII1_TX_EN-A/CAT1_TX_EN-A/ IRQ11/ADCNV1-A/DSMDAT0-A
113	TRDATA2/PG6/D30/ET1_ETXD3/CAT1_ETXD3	ETHPHYCLK/PA00/PIO_008/A7-A/CACREF/ GTIU-A/GTIOC0A/GTIOC10A/CTS10#-A/ CTS5#-A/RTS5#-A/SS5#-A/DE5-A/TXDB5-A/ SSL01-B/CATIRQ-A/IRQ1-DS/ADCNV0-A/ DSMCLK0-A
114	PA1/DQM3/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/IRQ11	P707/PIO_055/WE#-A/CS7#-A/GTIOC13B/ TXD11-B/SMOSI11-B/SSDA11-B/TXDA11-B/ ET1_RXD3-A/CAT1_ERXD3-A/ XSPI1_RESET1#-B/IRQ7/DSMDAT0-D
115	VCC	P706/PIO_054/CAS#-A/CS6#-A/GTIOC13A/ RXD11-B/SMISO11-B/SSCL11-B/ET1_RXD2-A/ CAT1_ERXD2-A/XSPI1_WP1#-B/IRQ14/ ADCNV2-C/DSMCLK0-D
116	TRCLK/PG5/D29/ET1_ETXD2/CAT1_ETXD2	P705/PIO_053/RAS#-A/CS5#-A/GTIOC12B/ SCK11-B/CTS11#-B/TXDB11-B/ET1_RXD1-A/ RMII1_RXD1-A/CAT1_ERXD1-A/ XSPI1_RSTO1#-B/IRQ13/ADCNV1-C/ DSMDAT5-D
117	VSS	P704/PIO_052/SDCS#-A/CS4#-A/GTIOC12A/ CTS4#-B/CTS11#-B/RTS11#-B/SS11#-B/DE11-B/ TXDB11-B/ET1_RXD0-A/RMII1_RXD0-A/ CAT1_ERXD0-A/XSPI1_INT1#-B/ XSPI1_ECS1#-B/IRQ12/ADCNV0-C/DSMCLK5-D
118	PA0/DQM2/BC0#/A0/MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/CAT0_TX_EN/ CATLEDRUN/LCD_DATA8-B	P703/PIO_051/ALE-A/WR2#-B/BC2#-B/CACREF/ GTETRGB/GTIOC11B/CTS4#-B/RTS4#-B/ SS4#-B/DE4-B/TXDB4-B/ET1_LINKSTA-A/ CAT1_LINKSTA-A/XSPI1_RESET0#-B/PCKO-C/ IRQ8/DSMDAT4-D
119	TRSYNC/PG4/D28/ET1_ETXD1/RMII1_TXD1/ CAT1_ETXD1	P702/PIO_050/RD#-A/DQM3-B/GTETRGA/ GTIOC11A/SCK4-B/CTS4#-B/TXDB4-B/ ET1_CRS-E/CATSYNC1-A/XSPI1_WP0#-B/ XSPI1_RESET1#-C/HSYNC-C/IRQ10/ADST2-B/ DSMCLK4-D
120	P67/DQM1/CS7#/MTIOC7C/GTIOC1B/CRX2/ EPLSOUT1/CATSYNC1/IRQ15	P701/PIO_049/CKE-A/WR3#-B/BC3#-B/ GTIOC10B/RXD4-B/SMISO4-B/SSCL4-B/ ET1_COL-E/CATLATCH1-A/XSPI1_RSTO0#-B/ XSPI1_RESET0#-B/VSYNC-C/IRQ1/ADST1-B/ DSMDAT3-D
121	TRDATA1/PG3/D27/ET1_ETXD0/RMII1_TXD0/ CAT1_ETXD0	ETHPHYCLK/P700/PIO_048/SDCLK-A/ GTIOC10A/TXD4-B/SMOSI4-B/SSDA4-B/ TXDA4-B/ET1_INT-A/CATRESTOUT-F/ XSPI1_INT0#-B/XSPI1_ECS0#-B/PIXCLK-C/ IRQ0/ADST0-B/DSMCLK3-D
122	P66/DQM0/CS6#/MTIOC7D/GTIOC2B/CTX2	VCC
123	TRDATA0/PG2/D26/ET1_TX_CLK/ CAT1_TX_CLK	VSS
124	P65/CKE/CS5#	VCL
125	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105	PE07/PIO_047/A8-B/A20-C/TOC1/GTETRGD/ GTCPPO7/GTIOC10B/POEGD/ET1_LINKSTA-E/ CAT1_LINKSTA-D/CATRESTOUT-C/ XSPI1_CS0#-A/PIXD7-C/IRQ7

176-Pin LFQFP	RX72M	RX74M
126	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/AN104	PE06/PIO_046/A9-B/A21-C/TIC1/GTETRGC/ GTADSM1/GTIOC10A/POEGB/SSL13-A/ ET1_RX_CLK-D/RMII1_REF50CK-D/ CAT1_RX_CLK-D/CATLEDERR-B/XSPI1_DS-A/ PIXD6-C/IRQ6
127	VCC	PE05/PIO_045/A10-B/A22-C/GTOWLO-C/ GTIOC9B/SSL12-A/ET1_RXD3-D/ CAT1_ERXD3-D/CATLEDRUN-B/XSPI1_IO3-A/ PIXD5-C/IRQ5
128	P70/SDCLK/CATLINKACT0	PE04/PIO_044/A11-B/A23-C/GTOWUP-C/ GTIOC9A/CTS12#-A/SSL11-A/ET1_RXD2-D/ CAT1_ERXD2-D/CATLEDSTER-B/XSPI1_IO2-A/ XSPI1_WP0#-C/PIXD4-C/IRQ12
129	VSS	PE03/PIO_043/A12-B/TOC3/GTOVLO-C/ GTIOC8B/CTS12#-A/RTS12#-A/SS12#-A/ DE12-A/TXDB12-A/MISO1-A/ET1_RXD1-D/ RMII1_RXD1-D/CAT1_ERXD1-D/SD0DAT7-B/ XSPI1_IO1-A/PIXD3-C/IRQ11
130	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ET0_RX_CLK/ REF50CK0/CAT0_RX_CLK/LCD_DATA11-B/ IRQ5/AN103	PE02/PIO_042/A13-B/TIC3/GTOVUP-C/ GTIOC8A/RXD12-A/SMISO12-A/SSCL12-A/ MOSI1-A/ET1_RXD0-D/RMII1_RXD0-D/ CAT1_ERXD0-D/SD0DAT6-B/XSPI1_IO0-A/ PIXD2-C/IRQ7-DS
131	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/CAT0_ERXD2/LCD_DATA12-B/ AN102	CLKOUT/PE01/PIO_041/A14-B/GTOULO-C/ GTIOC7B/TXD12-A/SMOSI12-A/SSDA12-A/ TXDA12-A/RSPCK1-A/ET1_RX_DV-D/ RMII1_CRS_DV-D/CAT1_RX_DV-D/SD0DAT5-B/ XSPI1_CK-A/PIXD1-C/IRQ9
132	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/CTS12#/RTS12#/SS12#/ ET0_ERXD3/CAT0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101	ETHPHYCLK/PE00/PIO_040/A15-B/GTOUUP-C/ GTIOC7A/SCK12-A/CTS12#-A/TXDB12-A/ SSL10-A/ET1_RX_ER-D/RMII1_RX_ER-D/ CAT1_RX_ER-D/SD0DAT4-B/XSPI1_CKN#-A/ XSPI1_CS1#-B/PIXD0-C/IRQ8
133	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/PO23/ TIC3/GTIOC0B/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/MMC_D6-B/LCD_DATA14-B/ IRQ7-DS/AN100	P607/PIO_015/CS0#-B/D16-B/GTETRGB/ GTADSM0/GTIOC15B/POEGA/CTS8#-B/ CTS9#-B/RTS9#-B/SS9#-B/DE9-B/TXDB9-B/ CRX2-C/ET1_INT-B/ET_TAS_STA3/CATIRQ-B/ XSPI0_RSTO0#-A/IRQ15/DSMDAT5-A
134	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/MTIOC3B/ PO18/GTIOC1B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1	P606/PIO_014/CS1#-C/D17-B/GTETRGA/ GTCPPO4/GTIOC15A/POEGC/SCK9-B/ CTS9#-B/TXDB9-B/SSL03-D/CTX2-C/ ET1_TX_ER-B/ET_TAS_STA2/CATLINKACT1-B/ XSPI0_RESET0#-A/IRQ14/DSMCLK5-A
135	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/GTIOC2B/ SCK12/SSLB1-B/MMC_D4-B/LCD_DATA16-B/ ANEX0	P605/PIO_013/CS2#-C/D18-B/GTIOC6B/RXD9-B/ SMISO9-B/SSCL9-B/SSL02-D/ET1_TXD3-B/ ET_TAS_STA1/CAT1_ETXD3-B/XSPI0_INT0#-A/ XSPI0_ECS0#-A/IRQ13/DSMDAT4-A
136	P64/WE#/D3[A3/D3]/CS4#/ET1_ETXD0/ RMII1_TXD0/CAT1_ETXD0	P604/PIO_012/CS3#-C/D19-B/GTIOC6A/TXD9-B/ SMOSI9-B/SSDA9-B/TXDA9-B/SSL01-D/ ET1_TXD2-B/ET_TAS_STA0/CAT1_ETXD2-B/ XSPI0_CS1#-A/XSPI0_RSTO0#-B/IRQ4/ DSMCLK4-A
137	P63/CAS#/D2[A2/D2]/CS3#/ET1_ETXD1/ RMII1_TXD1/CAT1_ETXD1	P603/PIO_011/WE#-B/D20-B/GTIOC5B/ CTS8#-B/RTS8#-B/SS8#-B/DE8-B/TXDB8-B/ CTS9#-B/MISO0-D/ET1_TXD1-B/RMII1_TXD1-B/ GPTP_PTPOUT3/CAT1_ETXD1-B/CATSYNC0-B/ XSPI0_IO7-A/PCKO-B/IRQ3/DSMDAT3-A

176-Pin LFQFP	RX72M	RX74M
138	P62/RAS#/D1[A1/D1]/CS2#/ET1_ERXD0/ RMII1_RXD0/CAT1_ERXD0	P602/PIO_010/CAS#-B/D21-B/GTIOC5A/SCK8-B/ CTS8#-B/TXDB8-B/MOSI0-D/ET1_TXD0-B/ RMII1_TXD0-B/GPTP_PTPOUT2/ CAT1_ETXD0-B/CATLATCH0-B/XSPI0_IO6-A/ HSYNC-B/IRQ2/ADTRG2#/DSMCLK3-A
139	P61/SDCS#/D0[A0/D0]/CS1#/ET1_ERXD1/ RMII1_RXD1/CAT1_ERXD1	P601/PIO_009/RAS#-B/D22-B/GTIOC4B/ RXD8-B/SMISO8-B/SSCL8-B/RSPCK0-D/ ET1_TX_EN-B/RMII1_TX_EN-B/ GPTP_PTPOUT1/CAT1_TX_EN-B/ CATSYNC1-D/XSPI0_IO5-A/VSYNC-B/IRQ1/ ADTRG1#
140	VSS	P600/PIO_008/SDCS#-B/D23-B/GTIOC4A/ TXD8-B/SMOSI8-B/SSDA8-B/TXDA8-B/SSL00-D/ ET1_TX_CLK-B/GPTP_PTPOUT0/ CAT1_TX_CLK-B/CATLATCH1-D/XSPI0_IO4-A/ PIXCLK-B/IRQ0/ADTRG0#
141	P60/CS0#/ET1_TX_EN/RMII1_TXD_EN/ CAT1_TX_EN	VCC2
142	VCC	VSS
143	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ ET1_RX_ER/RMII1_RX_ER/CAT1_RX_ER/ QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/ LCD_DATA17-B/IRQ7/AN107	VCL
144	TRDATA7/PG1/D25/ET1_RX_ER/RMII1_RX_ER/ CAT1_RX_ER	PD07/PIO_039/A16-B/D24-B/GTIW-C/GTIOC3B/ POEGA/TXD3-A/SMOSI3-A/SSDA3-A/TXDA3-A/ CTX1-B/ET1_LINKSTA-B/CAT1_LINKSTA-B/ SD0CD-B/XSPI0_CS0#-A/XSPI0_RESET1#-B/ PIXD7-B/IRQ7/AN031
145	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/ET1_RX_CLK/REF50CK1/ CAT1_RX_CLK/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/IRQ6/AN106	PD06/PIO_038/A17-B/D25-B/GTIV-C/GTIOC3A/ POEGB/RXD3-A/SMISO3-A/SSCL3-A/SSL23-A/ CRX1-B/ET1_RX_ER-B/RMII1_RX_ER-B/ CAT1_RX_ER-B/CATLEDERR-D/SD0WP-B/ XSPI0_DS-A/PIXD6-B/IRQ6/AN030
146	TRDATA6/PG0/D24/ET1_RX_CLK/REF50CK1/ CAT1_RX_CLK	PD05/PIO_037/A18-B/D26-B/GTIU-C/GTIOC2B/ POEGD/SCK3-A/CTS3#-A/TXDB3-A/SSL22-A/ CTX0-B/ET1_RX_DV-B/RMII1_CRS_DV-B/ CAT1_RX_DV-B/CATLEDSTER-D/SD0DAT1-B/ XSPI0_IO3-A/PIXD5-B/IRQ5/AN029
147	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/MTCLKA/ POE10#/SSLC1-A/ET1_MDC/PMGI1_MDC/ QSPCLK-B/SDHI_CLK-B/MMC_CLK-B/ LCD_DATA19-B/IRQ5/AN113	PD04/PIO_036/A19-B/D27-B/GTETRGA/ GTIOC2A/POEGC/CTS2#-A/CTS3#-A/RTS3#-A/ SS3#-A/DE3-A/TXDB3-A/SSL21-A/CRX0-B/ ET1_RX_CLK-B/RMII1_REF50CK-B/ CAT1_RX_CLK-B/CATLEDRUN-D/SD0DAT0-B/ XSPI0_IO2-A/XSPI0_WP0#-B/PIXD4-B/IRQ4/ AN028
148	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0-A/ ET1_MDIO/PMGI1_MDIO/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112	PD03/PIO_035/A20-B/D28-B/TOC2/GTIOC1B/ POEGA/TXD2-A/SMOSI2-A/SSDA2-A/TXDA2-A/ MISO2-A/ET1_RXD3-B/CAT1_ERXD3-B/ CAT0_MDIO-D/SD0CLK-B/XSPI0_IO1-A/ PIXD3-B/IRQ3/AN027
149	TRSYNC1/P97/D23/A23/ET1_ERXD3/ CAT1_ERXD3	PD02/PIO_034/A21-B/D29-B/TIC2/GTETRGB/ GTIOC1A/POEGB/RXD2-A/SMISO2-A/SSCL2-A/ MOSI2-A/ET1_RXD2-B/CAT1_ERXD2-B/ CAT0_MDC-D/SD0CMD-B/XSPI0_IO0-A/ PIXD2-B/IRQ2/AN026

176-Pin LFQFP	RX72M	RX74M
150	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/ET1_WOL/QIO3-B/ SDHI_D3-B/MMC_D3-B/LCD_DATA21-B/IRQ3/ AN111	PD01/PIO_033/A22-B/D30-B/GTETRGC/ GTIOC0B/POEGC/SCK2-A/CTS2#-A/TXDB2-A/ RSPCK2-A/ET1_RXD1-B/RMII1_RXD1-B/ CAT1_ERXD1-B/CATSYNC0-D/SD0DAT3-B/ XSPI0_CK-A/PIXD1-B/IRQ1/AN025
151	VSS	PD00/PIO_032/A23-B/D31-B/GTETRGD/ GTIOC0A/POEGD/CTS2#-A/RTS2#-A/SS2#-A/ DE2-A/TXDB2-A/CTS3#-A/SSL20-A/ ET1_RXD0-B/RMII1_RXD0-B/CAT1_ERXD0-B/ CATLATCH0-D/SD0DAT2-B/XSPI0_CKN#-A/ XSPI0_CS1#-B/PIXD0-B/IRQ0/AN024
152	TRDATA5/P96/D22/A22/ET1_ERXD2/ CAT1_ERXD2	VCC2
153	VCC	VSS
154	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/ET1_EXOUT/QIO2-B/ SDHI_D2-B/MMC_D2-B/LCD_DATA22-B/IRQ2/ AN110	VCL
155	TRDATA4/P95/D21/A21/ET1_ERXD1/ RMII1_RXD1/CAT1_ERXD1	P903/PIO_003/GTETRGD/GTCPPO9/POEGD/ CTS6#-B/CTS1#-C/RTS1#-C/SS1#-C/DE1-C/ TXDB1-C/ET1_MDIO-B/ET_TAS_STA3/ CATIRQ-C/XSPI0_WP1#-A/IRQ11/AN035
156	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/AN109	P902/PIO_002/GTETRGC/GTCPPO8/SCK1-C/ CTS1#-C/TXDB1-C/ET1_MDC-B/ET_TAS_STA2/ CATRESTOUT-B/XSPI0_RESET1#-A/IRQ10/ AN034
157	P94/D20/A20/ET1_ERXD0/RMII1_RXD0/ CAT1_ERXD0	P901/PIO_001/GTETRGB/GTCPPO6/TXD1-C/ SMOSI1-C/SSDA1-C/TXDA1-C/ET1_CRS-B/ ET_TAS_STA1/CATLATCH1-B/ XSPI0_RSTO1#-A/XSPI0_RESET0#-B/IRQ9/ AN033
158	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108	P900/PIO_000/GTETRGA/GTCPPO5/RXD1-C/ SMISO1-C/SSCL1-C/ET1_COL-B/ ET_TAS_STA0/CATSYNC1-B/XSPI0_INT1#-A/ XSPI0_ECS1#-A/IRQ0/AN032
159	P93/D19/A19/POE0#/CTS7#/RTS7#/SS7#/ ET1_LINKSTA/CAT1_LINKSTA/AN117/ DSMDAT4	AVCC0
160	P92/D18/A18/POE4#/RXD7/SMISO7/SSCL7/ ET1_CRS/RMII1_CRS_DV/CAT1_RX_DV/AN116/ DSMCLK4	AVSS0
161	P91/D17/A17/SCK7/ET1_COL/AN115/DSMDAT5	VREFL0
162	VSS	VREFH0
163	P90/D16/A16/TXD7/SMOSI7/SSDA7/ ET1_RX_DV/CAT1_RX_DV/AN114/DSMCLK5	P407/PIO_055/IRQ15-DS/AN007
164	VCC	P406/PIO_054/IRQ14-DS/AN006
165	P47/IRQ15-DS/AN007	P405/PIO_053/IRQ13-DS/AN005
166	P46/IRQ14-DS/AN006	P404/PIO_052/IRQ12-DS/AN004
167	P45/IRQ13-DS/AN005	P403/PIO_051/IRQ11-DS/AN003
168	P44/IRQ12-DS/AN004	P402/PIO_050/IRQ10-DS/AN002
169	P43/IRQ11-DS/AN003	P401/PIO_049/IRQ9-DS/AN001
170	P42/IRQ10-DS/AN002	P400/PIO_048/IRQ8-DS/AN000
171	P41/IRQ9-DS/AN001	P415/PIO_063/IRQ31/AN015/DA1
172	VREFL0	P414/PIO_062/IRQ30/AN014/DA0

176-Pin LFQFP	RX72M	RX74M
173	P40/IRQ8-DS/AN000	P007/PIO_007/GTCPPO6/GTIOC13B/POEGA/CTS0#-B/RTS0#-B/SS0#-B/DE0-B/TXDB0-B/ET1_INT-D/CATIRQ-E/IRQ23-DS/ADTRG0#/AN023/PDMDAT0-C
174	VREFH0	P006/PIO_006/GTCPPO5/GTIOC13A/GTIOC9B/SCK0-B/CTS0#-B/TXDB0-B/ET1_LINKSTA-D/CAT1_LINKSTA-E/IRQ22-DS/ADTRG1#/AN022/PDMCLK0-C/PCOUTZ1
175	AVCC0	P005/PIO_005/GTCPPO4/GTIOC12B/GTIOC9A/RXD0-B/SMISO0-B/SSCL0-B/SSILRCK1/ET1_MDIO-D/CATLATCH0-E/IRQ21-DS/ADTRG2#/AN021/DSMDAT2-B/PCOUTB1
176	P07/IRQ15/ADTRG0#	P004/PIO_004/GTCPPO3/GTIOC12A/GTIOC8B/TXD0-B/SMOSI0-B/SSDA0-B/TXDA0-B/SSITXD1/ET1_MDC-D/CATSYNC0-E/IRQ20-DS/AN020/DSMCLK2-B/PCOUTA1

Note: 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

Table 3.6 Comparative Listing of RX72N/RX74N 176-Pin LFQFP Package Pin Functions

176-Pin LFQFP	RX72N	RX74N
1	AVSS0	P003/PIO_003/GTCPPO2/GTIOC11B/GTIOC8A/RXD7-A/SMISO7-A/SSCL7-A/SSIRXD1/ET0_MDIO-D/IRQ19-DS/AN019/PCOUTB0
2	P05/SSILRCK1/IRQ13/DA1	P002/PIO_002/TMCI1/GTCPPO1/GTIOC11A/GTIOC7B/TXD7-A/SMOSI7-A/SSDA7-A/TXDA7-A/SSIBCK1/ET0_MDC-D/IRQ18-DS/AN018/PCOUTA0
3	AVCC1	P001/PIO_001/TMCI0/GTCPPO0/GTIOC10B/GTIOC7A/SCK7-A/CTS7#-A/TXDB7-A/SSIBCK0/ET0_LINKSTA-D/IRQ17-DS/AN017/PCOUTZ0
4	P03/SSIDATA1/IRQ11/DA0	P000/PIO_000/TMRI0/GTCPPO7/GTIOC10A/POEGB/CTS0#-B/CTS7#-A/RTS7#-A/SS7#-A/DE7-A/TXDB7-A/AUDIO_CLK/ET0_INT-D/IRQ16-DS/AN016
5	AVSS1	VCC
6	P02/TMCI1/SCK6/SSIBCK1/IRQ10/AN120	VSS
7	P01/TMCI0/RXD6/SMISO6/SSCL6/SSIBCK0/IRQ9/AN119	VSS
8	P00/TMRI0/TXD6/SMOSI6/SSDA6/AUDIO_CLK/IRQ8/AN118	VCL
9	PF5/WAIT#/SSILRCK0/IRQ4	RES#
10	EMLE	MD/P315
11	PJ5/POE8#/CTS2#/RTS2#/SS2#/SSIRXD0/EPLSOUT0	P312/PIO_060/BACK#-B/RTCIC2/GTETRGD/GTCPPO15/POEGA/SSL13-B/SSILRCK0/IRQ20/ADTRG2#/TAMPI2
12	VSS	P311/PIO_059/BREQ#-B/RTCIC1/GTETRGC/GTCPPO14/POEGD/CTS7#-A/SSL12-B/SSIRXD0/ET0_WOL-C/IRQ19/ADTRG1#/TAMPI2
13	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#/SSITXD0/ET0_EXOUT	P310/PIO_058/RTCIC0/CACREF/GTETRGB/GTCPPO1/POEGC/CTS0#-C/CTS1#-B/SSL11-B/SSITXD0/IRQ18/ADTRG0#/TAMPI1
14	VCL	VBATT/VCC
15	VBATT	XCIN/EXCIN/P309

176-Pin LFQFP	RX72N	RX74N
16	NC	XCOUT/P308
17	TRST#/PF4	VSS
18	MD/FINED	XTAL/P307
19	XCIN	EXTAL/P306
20	XCOUT	VCC
21	RES#	P305/NMI/IRQ0
22	XTAL/P37	AVCC_USBHS
23	VSS	USBHS_RREF
24	EXTAL/P36	AVSS_USBHS
25	VCC	USBHS_DM
26	UPSEL/P35/NMI	USBHS_DP
27	P34/MTIOC0A/TMCI3/PO12/POE10#/SCK6/ SCK0/ET0_LINKSTA/IRQ4	VSS_USBHS
28	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/ POE4#/POE11#/RXD6/SMISO6/SSCL6/RXD0/ SMISO0/SSCL0/CRX0/PCKO/IRQ3-DS	VCC_USBHS
29	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCIC2/ RTCOUT/POE0#/POE10#/TXD6/SMOSI6/ SSDA6/TXD0/SMOSI0/SSDA0/CTX0/ USB0_VBUSEN/VSYNC/IRQ2-DS	VCC_USB
30	TMS/PF3	PF01/PIO_049/GTCPPO15/USB0_DM/IRQ1
31	TDI/PF2/RXD1/SMISO1/SSCL1	PF00/PIO_048/GTCPPO14/USB0_DP/IRQ0
32	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/ RTS1#/SS1#/SSLB0-A/ET1_MDC/ PMGI1_MDC/IRQ1-DS	VSS_USB
33	P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/MISOB-A/ET1_MDIO/ PMGI1_MDIO/IRQ0-DS	P207/PIO_023/A23-C/CS4#-C/TMRI3/ GTOWLO-D/GTIOC2B/GTIOC6B/RXD1-B/ SMISO1-B/SSCL1-B/MISO1-B/SDAHS2-B/ CRX1-A/USB0_ID/USBHS_OVRCURB-DS/ ET0_RXD3-B/PCKO-A/IRQ3-DS/ADTRG2#
34	TCK/PF1/SCK1	P206/PIO_022/A22-C/CS5#-C/TMO3/RTCOUT/ GTOWUP-D/GTIOC2A/GTIOC6A/CTS6#-A/ TXD1-B/SMOSI1-B/SSDA1-B/TXDA1-B/MOSI1-B/ SCLHS2-B/CTX1-A/USB0_EXICEN/ USBHS_OVRCURA-DS/SSITXD1/ET0_RXD2-B/ VSYNC-A/IRQ2-DS/ADTRG1#/PCOUTZ1
35	TDO/PF0/TXD1/SMOSI1/SSDA1	CLKOUT/P205/PIO_021/A21-C/CS6#-C/ GTOVLO-D/GTIOC1B/GTIOC5B/SCK1-B/ CTS1#-B/TXDB1-B/RSPCK1-B/SDAHS1-B/ CRX0-A/USB0_VBUS/USBHS_VBUSEN/ SSIRXD1/ET0_RXD1-B/RMII0_RXD1-B/ SD0CD-C/HSYNC-A/IRQ5/ADTRG0#/PCOUTB1
36	P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A/ET1_WOL	ETHPHYCLK/P204/PIO_020/A20-C/CS7#-C/ TMRI1/GTOVUP-D/GTIOC1A/GTIOC5A/ CTS1#-B/RTS1#-B/SS1#-B/DE1-B/TXDB1-B/ SSL10-B/SCLHS1-B/CTX0-A/USB0_VBUSEN/ USBHS_VBUS-DS/SSIBCK1/ET0_RXD0-B/ RMII0_RXD0-B/SD0WP-C/PIXCLK-A/ IRQ12/PCOUTA1
37	P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/ SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A/ ET1_EXOUT	VCL
38	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SSIDATA1/SDHI_CD/HSYNC/ADTRG0#	VSS
39	VCC	VCC

176-Pin LFQFP	RX72N	RX74N
40	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/SSIBCK1/SDHI_WP/PIXCLK	P203/PIO_019/CS2#-B/BACK#-A/GTOULO-D/GTIOC0B/GTIOC4B/RXD6-A/SMISO6-A/SSCL6-A/CTS3#-B/SSL00-C/SDA00-B/CRX2-B/USB0_OVRCURB/USBHS_ID/SSIBCK0/ET0_RX_CLK-B/RMII0_REF50CK-B/SD0DAT1-C/PIXD7-A/IRQ3/PDMDAT0-B
41	VSS	P202/PIO_018/CS3#-B/BREQ#-A/TMO0/GTOUUP-D/GTIOC0A/GTIOC4A/TXD6-A/SMOSI6-A/SSDA6-A/TXDA6-A/RSPCK0-C/SCL00-B/CTX2-B/USB0_OVRCURA/USBHS_EXICEN/AUDIO_CLK/ET0_RX_DV-B/RMII0_CRS_DV-B/SD0DAT0-C/PIXD6-A/IRQ15/PDMCLK0-B
42	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/SDHI_D1-C/PIXD7	ETHPHYCLK/P304/PIO_028/ALE-C/WAIT#-B/TMCI3/GTETRGD/GTCPPO0/POEGA/CTS0#-A/CTS1#-A/USB0_VBUSEN/USBHS_ID/ET0_INT-E/IRQ0-DS/ADTRG0#
43	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/GTIOC1A/SCK0/USB0_OVRCURB/AUDIO_CLK/SDHI_D0-C/PIXD6	TDI/P303/PIO_027/TMCI2/GTCPPO13/RXD0-A/SMISO0-A/SSCL0-A/RXD1-A/SMISO1-A/SSCL1-A/MISO1-C/IRQ1
44	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/USB0_EXICEN/SSILRCK0/SDHI_CLK-C/PIXD5/IRQ9	TDO/P302/PIO_026/TMRI3/GTCPPO12/TXD0-A/SMOSI0-A/SSDA0-A/TXDA0-A/TXD1-A/SMOSI1-A/SSDA1-A/TXDA1-A/MOSI1-C/IRQ4
45	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/SDHI_CMD-C/PIXD4/IRQ8	TCK/SWCLK/P301/PIO_025/TMCI3/GTCPPO11/SCK0-A/CTS0#-A/TXDB0-A/SCK1-A/CTS1#-A/TXDB1-A/RSPCK1-C/IRQ7
46	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/GTIOC0B/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/SSITXD0/EPLSOUT0/SDHI_D3-C/PIXD3/IRQ7/ADTRG1#	TMS/SWDIO/P300/PIO_024/TMO1/GTCPPO10/CTS0#-A/RTS0#-A/SS0#-A/DE0-A/TXDB0-A/CTS1#-A/RTS1#-A/SS1#-A/DE1-A/TXDB1-A/SSL10-C/ET0_WOL-D/IRQ6
47	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/SSDA10/TXD10/EPLSOUT1/SDHI_D2-C/PIXD2	P805/PIO_061/GTADSM1/GTIOC15B/SCK5-B/CTS5#-B/TXDB5-B/SSL22-B/CRX0-D/USB0_VBUSEN/USBHS_VBUSEN/ET0_TXD0-C/RMII0_TXD0-C/HSYNC-D/IRQ5/ADSYNC-C/PCINB0
48	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/USB0_VBUSEN/USB0_VBUS/USB0_OVRCURB/IRQ6/ADTRG0#	P804/PIO_060/GTADSM0/GTIOC15A/CTS5#-B/RTS5#-B/SS5#-B/DE5-B/TXDB5-B/SSL21-B/CTX0-D/USB0_OVRCURA/USBHS_OVRCURA/ET0_TX_EN-C/RMII0_TX_EN-C/PCKO-D/IRQ4/PCINA0
49	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/SSCL10/RXD10/PIXD1	P201/PIO_017/TMCI0/GTIW-D/GTIOC3B/GTIOC14B/SCK6-A/CTS6#-A/TXDB6-AMISO0-C/SCLHS1-A/USB0_EXICEN/SSILRCK0/ET0_RX_ER-B/RMII0_RX_ER-B/SD0CLK-C/PIXD5-A/IRQ9/PCINZ0
50	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/GTETRGA/RXD1/SMISO1/SSCL1/SCK3/CRX1-DS/SSILRCK1/PIXD0/IRQ5	P200/PIO_016/TMRI0/GTETRGA/GTIOC3A/GTIOC14A/CTS6#-A/RTS6#-A/SS6#-A/DE6-A/TXDB6-A/MOSI0-C/SDAHS1-A/USB0_ID/SSIRXD0/ET0_TX_EN-B/RMII0_TX_EN-B/SD0CMD-C/PIXD4-A/IRQ8/ADTRG2#/PCINZ1
51	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/GTETRGD/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/LCD_CLK-A/IRQ4	P107/PIO_015/TMO1/GTIV-D/GTIOC15B/POEGA/TXD3-B/SMOSI3-B/SSDA3-B/TXDA3-B/SDAHS2-A/SSITXD0/ET0_TXD3-B/SD0DAT3-C/PIXD3-A/IRQ31-DS/ADTRG1#/PCINB1
52	P13/WR2#/BC2#/MTIOC0B/TIOCA5/TMO3/PO13/GTADSM1/TXD2/SMOSI2/SSDA2/SDA0[FM+]/LCD_TCON0-A/IRQ3/ADTRG1#	CLKOUT/P106/PIO_014/TMO2/RTCOUT/GTIU-D/GTIOC15A/POEGB/RXD3-B/SMISO3-B/SSCL3-B/SCLHS2-A/ET0_TXD2-B/SD0DAT2-C/PIXD2-A/IRQ30-DS/ADTRG0#/PCINA1

176-Pin LFQFP	RX72N	RX74N
53	P12/WR3#/BC3#/MTIC5U/TMCI1/GTADSM0/ RXD2/SMISO2/SSCL2/SCL0[FM+]/LCD_TCON1-A/IRQ2	P105/PIO_013/TMCI2/GTIV-E/GTIOC14B/ TXD2-B/SMOSI2-B/SSDA2-B/TXDA2-B/SCK3-B/ CTS3#-B/TXDB3-B/CRX2-A/USB0_VBUS/ USBHS_OVRCURB/SSILRCK1/ET0_TXD1-B/ RMII0_TXD1-B/PIXD1-A/IRQ29-DS/ADST1-A/ PCINB0
54	VCC_USB	P104/PIO_012/TMRI2/GTIW-E/GTIOC14A/ RXD2-B/SMISO2-B/SSCL2-B/CTS3#-B/RTS3#-B/ SS3#-B/DE3-B/TXDB3-B/CTX2-A/ USB0_OVRCURA-DS/USBHS_VBUS/ ET0_TXD0-B/RMII0_TXD0-B/PIXD0-A/IRQ4/ ADST0-A/PCINA0
55	USB0_DM	VCL
56	USB0_DP	VSS
57	VSS_USB	VCC
58	CLKOUT25M/PJ2/TXD8/SMOSI8/SSDA8/ SSLC3-B/LCD_TCON2-A	P103/PIO_011/TMO3/GTADSM1/GTIOC13B/ CTS2#-B/SDA00-A/ET0_CRS-D/IRQ3
59	PJ1/MTIOC6A/RXD8/SMISO8/SSCL8/SSLC2-B/ EPLSOUT1/LCD_TCON3-A	P102/PIO_010/TMCI1/GTADSM0/GTIOC13A/ SCL00-A/ET0_COL-D/IRQ2
60	PJ0/MTIOC6B/SCK8/SSLC1-B/ EPLSOUT0/LCD_DATA0-A	P101/PIO_009/CS0#-A/ALE-B/TMCI3/GTETRGC/ GTADSM1/GTIOC12B/SCK2-B/CTS2#-B/ TXDB2-B/USB0_VBUS-DS/USBHS_EXICEN/ ET0_TX_CLK-B/IRQ1/ADTRG1#
61	P85/MTIOC6C/TIOCC0/LCD_DATA1-A	P100/PIO_008/CS1#-B/WAIT#-A/TMRI3/ CACREF/GTIU-E/GTADSM0/GTIOC12A/ CTS2#-B/RTS2#-B/SS2#-B/DE2-B/TXDB2-B/ CTS5#-B/USB0_OVRCURB-DS/USBHS_VBUS/ ET0_TX_ER-B/IRQ0/ADTRG2#
62	P84/MTIOC6D/ET1_LINKSTA/LCD_DATA2-A	VCC_DCDC
63	P57/RXD7/SMISO7/SSCL7/SSLC0-B/ LCD_DATA3-A	VCC_DCDC
64	CLKOUT25M/P56/EDACK1/MTIOC3C/TIOCA1/ SCK7/RSPCKC-B/LCD_DATA4-A	VCC_DCDC
65	P55/D0[A0/D0]/EDREQ0/WAIT#/MTIOC4D/ TMO3/TXD7/SMOSI7/SSDA7/MISOC-B/CRX1/ ET0_EXOUT/LCD_DATA5-A/IRQ10	VLO
66	P54/D1[A1/D1]/EDACK0/ALE/MTIOC4B/TMCI1/ CTS2#/RTS2#/SS2#/MOSIC-B/CTX1/ ET0_LINKSTA/LCD_DATA6-A	VLO
67	P11/MTIC5V/TMCI3/SCK2/EPLSOUT1/ LCD_DATA7-A/IRQ1	VLO
68	P10/ALE/MTIC5W/TMRI3/IRQ0	VSS_DCDC
69	P53/BCLK	VSS_DCDC
70	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A	P503/PIO_035/WR3#-A/BC3#-A/A19-C/ GTIOC3B/RXD2-C/SMISO2-C/SSCL2-C/ CRX1-C/USB0_OVRCURB/SSIRXD0/ SD0DAT7-A/IRQ3
71	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	P502/PIO_034/WR2#-A/BC2#-A/A18-C/ GTIOC3A/TXD2-C/SMOSI2-C/SSDA2-C/ TXDA2-C/SSL13-C/CTX1-C/ET0_WOL-B/ SD0DAT6-A/IRQ2/ADST2-C
72	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A	P501/PIO_033/WR1#-A/BC1#-A/A17-C/ GTIOC2B/SCK2-C/CTS2#-C/TXDB2-C/SSL12-C/ CRX0-C/ET0_INT-B/SD0DAT5-A/IRQ1/ADST1-C
73	VSS	P500/PIO_032/WR#-A/WR0#-A/A16-C/GTIOC2A/ CTS2#-C/RTS2#-C/SS2#-C/DE2-C/TXDB2-C/ CTS7#-B/SSL11-C/CTX0-C/ET0_LINKSTA-B/ SD0DAT4-A/IRQ0/ADST0-C

176-Pin LFQFP	RX72N	RX74N
74	P83/EDACK1/MTIOC4C/GTIOC0A/SCK10/ SS10#/CTS10#/ET0_CRS/RMII0_CRS_DV/ LCD_DATA8-A	P803/PIO_059/CS3#-A/WR1#-B/BC1#-B/ GTIOC1B/POEGA/CTS10#-B/RTS10#-B/ SS10#-B/DE10-B/TXDB10-B/CTX2-D/ USB0_ID/ET0_MDC-B/IRQ3/ADSYNC-B
75	VCC	P802/PIO_058/CS2#-A/WR#-B/WR0#-B/GTIW-B/ GTIOC1A/POEGB/SCK10-B/CTS10#-B/ TXDB10-B/CRX2-D/USB0_EXICEN/ ET0_MDIO-B/IRQ2/ADCNV2-B
76	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/ ET0_COL/MMC_D7-A/LCD_DATA9-A/IRQ14	VCL
77	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/MTCLKA/ TMCI2/PO30/TIC0/GTIOC3B/RXD8/SMISO8/ SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ ET0_ETXD3/MMC_D6-A/LCD_DATA10-A/IRQ13	VSS
78	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/RTS8#/ SCK10/RSPCKA-A/ET0_ETXD2/MMC_D5-A/ LCD_DATA11-A	VCC
79	P82/EDREQ1/MTIOC4A/PO28/GTIOC2A/ SMOSI10/SSDA10/TXD10/ET0_ETXD1/ RMII0_TXD1/MMC_D4-A/LCD_DATA12-A	CLKOUT/P801/PIO_057/EBCLK-A/GTIV-B/ GTIOC0B/POEGC/TXD10-B/SMOSI10-B/ SSDA10-B/TXDA10-B/ET0_CRS-B/ IRQ9/ADCNV1-B
80	P81/EDACK0/MTIOC3D/PO27/GTIOC0B/ SMISO10/SSCL10/RXD10/ET0_ETXD0/ RMII0_TXD0/QIO3-A/SDHI_CD/MMC_D3-A/ LCD_DATA13-A	P800/PIO_056/CS1#-A/DQM0-B/GTIU-B/ GTIOC0A/POEGD/RXD10-B/SMISO10-B/ SSCL10-B/ET0_COL-B/IRQ8/ADCNV0-B
81	P80/EDREQ0/MTIOC3B/PO26/SCK10/RTS10#/ ET0_TX_EN/RMII0_TXD_EN/QIO2-A/ SDHI_WP/MMC_D2-A/LCD_DATA14-A	ETHPHYCLK/PC07/PIO_031/D0-A/TMO2/TOC0/ CACREF/GTETRGD/GTADSM1/GTIOC15B/ POEGA/TXD8-A/SMOSI8-A/SSDA8-A/TXDA8-A/ MISO0-A/SSITXD0/SD0CD-A/IRQ14/ PDMDAT0-A
82	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/ POE0#/GTETRGC/SCK5/CTS8#/SS8#/SS10#/ CTS10#/RTS10#/SSLA0-A/ET0_TX_CLK/QMI-A/ QIO1-A/SDHI_D1-A/MMC_D1-A/LCD_DATA15-A	PC06/PIO_030/D1-A/TMCI2/TIC0/GTETRGC/ GTCPPO7/GTIOC15A/POEGB/RXD8-A/ SMISO8-A/SSCL8-A/MOSI0-A/SSILRCK0/ ET0_TX_ER-A/SD0WP-A/IRQ13/PDMCLK0-A
83	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/MMC_D0-A/LCD_DATA16-A	PC05/PIO_029/D2-A/TMRI2/GTOWLO-B/ GTIOC9B/SCK8-A/CTS8#-A/TXDB8-A/ RSPCK0-A/SSIBCK0/ET0_TX_EN-A/ RMII0_TX_EN-A/SD0DAT1-A/IRQ5/PCOUTZ1
84	P77/CS7#/PO23/SMOSI11/SSDA11/TXD11/ ET0_RX_ER/RMII0_RX_ER/QSPCLK-A/ SDHI_CLK-A/MMC_CLK-A/LCD_DATA17-A	PC04/PIO_028/D3-A/TMCI1/GTOWUP-B/ GTIOC9A/CTS8#-A/RTS8#-A/SS8#-A/ DE8-A/TXDB8-A/CTS11#-A/SSL00-A/AUDIO_CLK/ET0_TXD3-A/SD0DAT0-A/ IRQ12/PCOUTB1
85	P76/CS6#/PO22/SMISO11/SSCL11/RXD11/ ET0_RX_CLK/REF50CK0/QSSL-A/SDHI_CMD-A/ MMC_CMD-A/LCD_DATA18-A	PC03/PIO_027/D4-A/GTOVLO-B/GTIOC8B/ TXD11-A/SMOSI11-A/SSDA11-A/TXDA11-A/ SDAHS1-C/ET0_TXD2-A/SD0CLK-A/ IRQ11/PCOUTA1
86	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ET0_RX_DV/ SDHI_D3-A/MMC_CD-A/LCD_DATA19-A	PC02/PIO_026/D5-A/GTOVUP-B/GTIOC8A/ RXD11-A/SMISO11-A/SSCL11-A/SSL03-A/ SCLHS1-C/ET0_TXD1-A/RMII0_TXD1-A/ SD0CMD-A/IRQ10/PCOUTZ0
87	P75/CS5#/PO20/SCK11/RTS11#/ET0_ERXD0/ RMII0_RXD0/SDHI_D2-A/MMC_RES#-A/ LCD_DATA20-A	PC01/PIO_025/D6-A/GTOULO-B/GTIOC7B/ SCK11-A/CTS11#-A/TXDB11-A/SSL02-A/ SDA00-C/ET0_TXD0-A/RMII0_TXD0-A/ SD0DAT3-A/IRQ12/PCOUTB0

176-Pin LFQFP	RX72N	RX74N
88	P74/A20/CS4#/PO19/SS11#/CTS11#/ ET0_ERXD1/RMII0_RXD1/LCD_DATA21-A	PC00/PIO_024/D7-A/GTOUUP-B/GTIOC7A/ CTS11#-A/RTS11#-A/SS11#-A/DE11-A/ TXDB11-A/SSL01-A/SCL00-C/ET0_TX_CLK-A/ SD0DAT2-A/IRQ14/PCOUTA0
89	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/LCD_DATA22-A/IRQ12	PB07/PIO_023/D8-A/GTOWLO-A/GTIOC6B/ TXD9-A/SMOSI9-A/SSDA9-A/TXDA9-A/ ET0_LINKSTA-A/IRQ15
90	VCC	PB06/PIO_022/D9-A/GTOWUP-A/GTIOC6A/ RXD9-A/SMISO9-A/SSCL9-A/ET0_RX_ER-A/ RMII0_RX_ER-A/IRQ6
91	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/ SS5#/SSLA1-A/ET0_ERXD3/IRQ14	PB05/PIO_021/D10-A/TMRI1/GTOVLO-A/ GTIOC5B/SCK9-A/CTS9#-A/TXDB9-A/ ET0_RX_DV-A/RMII0_CRS_DV-A/IRQ13
92	VSS	PB04/PIO_020/D11-A/GTOVUP-A/GTIOC5A/ CTS4#-A/CTS9#-A/RTS9#-A/SS9#-A/DE9-A/ TXDB9-A/ET0_RX_CLK-A/RMII0_REF50CK-A/ IRQ4
93	P73/CS3#/PO16/ET0_WOL/LCD_EXTCLK-A	VCC
94	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV	VSS
95	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1	VCL
96	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/SCK11/ET0_ETXD0/ RMII0_TXD0/LCD_CLK-B	PB03/PIO_019/D12-A/TMO0/GTOULO-A/GTIOC4B/SCK4-A/CTS4#-A/TXDB4-A/ET0_RXD3-A/IRQ3
97	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/SS11#/ CTS11#/RTS11#/ET0_TX_EN/RMII0_TXD_EN/ LCD_TCON0-B	PB02/PIO_018/D13-A/GTOUUP-A/GTIOC4A/ CTS4#-A/RTS4#-A/SS4#-A/DE4-A/TXDB4-A/ CTS9#-A/ET0_RXD2-A/IRQ2
98	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK4/SCK6/ET0_RX_ER/ RMII0_RX_ER/LCD_TCON1-B	PB01/PIO_017/D14-A/TMCI0/GTETRGB/ GTCPPO4/GTIOC14B/POEGA/TXD4-A/ SMOSI4-A/SSDA4-A/TXDA4-A/ET0_RXD1-A/ RMII0_RXD1-A/IRQ4-DS/PCINB1
99	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/ SS4#/CTS6#/RTS6#/SS6#/ET0_RX_CLK/ REF50CK0/LCD_TCON2-B	PB00/PIO_016/D15-A/GTETRGA/GTADSM0/ GTIOC14A/POEGC/RXD4-A/SMISO4-A/ SSCL4-A/ET0_RXD0-A/RMII0_RXD0-A/ IRQ12/ADST2-A/PCINA1
100	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/ PO25/TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/ SSDA6/ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS	PG02/PIO_058/DQM3-A/WR3#-C/BC3#-C/ GTIOC11A/TXD8-C/SMOSI8-C/SSDA8-C/ TXDA8-C/IRQ10
101	P72/A19/CS2#/ET0_MDC/PMGI0_MDC/ LCD_DATA23-A	PG01/PIO_057/DQM0-A/WR#-C/WR0#-C/ GTCPPO1/RXD8-C/SMISO8-C/SSCL8-C/IRQ9
102	P71/A18/CS1#/ET0_MDIO/PMGI0_MDIO	PG00/PIO_056/DQM1-A/WR1#-C/BC1#-C/ GTCPPO0/SCK8-C/CTS8#-C/TXDB8-C/IRQ8
103	VCC	ETHPHYCLK/PA07/PIO_015/A0-A/BC0#-A/ DQM1-B/GTIOC3B/GTIOC13B/RXD10-A/ SMISO10-A/SSCL10-A/MISO0-B/IRQ7/PCINB0
104	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/ET0_ERXD1/ RMII0_RXD1/LCD_DATA0-B/IRQ12	PA06/PIO_014/A1-A/DQM2-B/TMCI3/GTIOC3A/ GTIOC13A/TXD10-A/SMOSI10-A/SSDA10-A/ TXDA10-A/MOSI0-B/IRQ14/PCINZ1
105	VSS	PA05/PIO_013/A2-A/GTIOC2B/GTIOC12B/ SCK10-A/CTS10#-A/TXDB10-A/RSPCK0-B/ IRQ5/PCINA0
106	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B	PA04/PIO_012/A3-A/TMRI0/GTIOC2A/ GTIOC12A/CTS10#-A/RTS10#-A/SS10#-A/ DE10-A/TXDB10-A/SSL00-B/IRQ5-DS/PCINZ0

176-Pin LFQFP	RX72N	RX74N
107	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/RTS5#/SS5#/ MOSIA-B/ET0_EXOUT/LCD_DATA2-B	VCC
108	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/LCD_DATA3-B	VSS
109	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/ TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC/ PMGI0_MDC/LCD_DATA4-B/IRQ5-DS	VCL
110	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/ PMGI0_MDIO/LCD_DATA5-B/IRQ6-DS	PA03/PIO_011/A4-A/GTIOC1B/GTIOC11B/ RXD5-A/SMISO5-A/SSCL5-A/IRQ6-DS/ ADSYNC-A
111	TRDATA3/PG7/D31/ET1_TX_ER	PA02/PIO_010/A5-A/GTIW-A/GTIOC1A/ GTIOC11A/TXD5-A/SMOSI5-A/SSDA5-A/ TXDA5-A/SSL03-B/IRQ10/ADCNV2-A
112	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B	PA01/PIO_009/A6-A/GTIV-A/GTIOC0B/ GTIOC10B/SCK5-A/CTS5#-A/TXDB5-A/ SSL02-B/IRQ11/ADCNV1-A
113	TRDATA2/PG6/D30/ET1_ETXD3	ETHPHYCLK/PA00/PIO_008/A7-A/CACREF/ GTIU-A/GTIOC0A/GTIOC10A/CTS10#-A/ CTS5#-A/RTS5#-A/SS5#-A/DE5-A/TXDB5-A/ SSL01-B/IRQ1-DS/ADCNV0-A
114	PA1/DQM3/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/GTIOC2A/SCK5/SSLA2-B/ ET0_WOL/LCD_DATA7-B/IRQ11	P707/PIO_055/WE#-A/CS7#-A/GTIOC13B/ TXD11-B/SMOSI11-B/SSDA11-B/TXDA11-B/ XSPI1_RESET1#-B/IRQ7
115	VCC	P706/PIO_054/CAS#-A/CS6#-A/GTIOC13A/ RXD11-B/SMISO11-B/SSCL11-B/ XSPI1_WP1#-B/IRQ14/ADCNV2-C
116	TRCLK/PG5/D29/ET1_ETXD2	P705/PIO_053/RAS#-A/CS5#-A/GTIOC12B/ SCK11-B/CTS11#-B/TXDB11-B/ XSPI1_RSTO1#-B/IRQ13/ADCNV1-C
117	VSS	P704/PIO_052/SDCS#-A/CS4#-A/GTIOC12A/ CTS4#-B/CTS11#-B/RTS11#-B/SS11#-B/DE11-B/ TXDB11-B/XSPI1_INT1#-B/XSPI1_ECS1#-B/ IRQ12/ADCNV0-C
118	PA0/DQM2/BC0#/A0/MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/LCD_DATA8-B	P703/PIO_051/ALE-A/WR2#-B/BC2#-B/CACREF/ GTETRGB/GTIOC11B/CTS4#-B/RTS4#-B/ SS4#-B/DE4-B/TXDB4-B/XSPI1_RESET0#-B/ PCKO-C/IRQ8
119	TRSYNC/PG4/D28/ET1_ETXD1/RMII1_TXD1	P702/PIO_050/RD#-A/DQM3-B/GTETRGA/ GTIOC11A/SCK4-B/CTS4#-B/TXDB4-B/ XSPI1_WP0#-B/XSPI1_RESET1#-C/ HSYNC-C/IRQ10/ADST2-B
120	P67/DQM1/CS7#/MTIOC7C/GTIOC1B/CRX2/ EPLSOUT1/IRQ15	P701/PIO_049/CKE-A/WR3#-B/BC3#-B/ GTIOC10B/RXD4-B/SMISO4-B/SSCL4-B/ XSPI1_RSTO0#-B/XSPI1_RESET0#-B/ VSYNC-C/IRQ1/ADST1-B
121	TRDATA1/PG3/D27/ET1_ETXD0/RMII1_TXD0	ETHPHYCLK/P700/PIO_048/SDCLK-A/ GTIOC10A/TXD4-B/SMOSI4-B/SSDA4-B/ TXDA4-B/XSPI1_INT0#-B/XSPI1_ECS0#-B/ PIXCLK-C/IRQ0/ADST0-B
122	P66/DQM0/CS6#/MTIOC7D/GTIOC2B/CTX2	VCC
123	TRDATA0/PG2/D26/ET1_TX_CLK	VSS
124	P65/CKE/CS5#	VCL
125	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105	PE07/PIO_047/A8-B/A20-C/TOC1/GTETRGD/ GTCPPO7/GTIOC10B/POEGD/XSPI1_CS0#-A/ PIXD7-C/IRQ7
126	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/AN104	PE06/PIO_046/A9-B/A21-C/TIC1/GTETRGC/ GTADSM1/GTIOC10A/POEGB/SSL13-A/ XSPI1_DS-A/PIXD6-C/IRQ6

176-Pin LFQFP	RX72N	RX74N
127	VCC	PE05/PIO_045/A10-B/A22-C/GTOWLO-C/ GTIOC9B/SSL12-A/XSPI1_IO3-A/PIXD5-C/IRQ5
128	P70/SDCLK	PE04/PIO_044/A11-B/A23-C/GTOWUP-C/ GTIOC9A/CTS12#-A/SSL11-A/XSPI1_IO2-A/ XSPI1_WP0#-C/PIXD4-C/IRQ12
129	VSS	PE03/PIO_043/A12-B/TOC3/GTOVLO-C/ GTIOC8B/CTS12#-A/RTS12#-A/SS12#-A/ DE12-A/TXDB12-A/MISO1-A/SD0DAT7-B/ XSPI1_IO1-A/PIXD3-C/IRQ11
130	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ET0_RX_CLK/ REF50CK0/LCD_DATA11-B/IRQ5/AN103	PE02/PIO_042/A13-B/TIC3/GTOVUP-C/ GTIOC8A/RXD12-A/SMISO12-A/SSCL12-A/ MOSI1-A/SD0DAT6-B/XSPI1_IO0-A/PIXD2-C/ IRQ7-DS
131	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/LCD_DATA12-B/AN102	CLKOUT/PE01/PIO_041/A14-B/GTOULO-C/ GTIOC7B/TXD12-A/SMOSI12-A/SSDA12-A/ TXDA12-A/RSPCK1-A/SD0DAT5-B/XSPI1_CK-A/ PIXD1-C/IRQ9
132	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/CTS12#/RTS12#/SS12#/ ET0_ERXD3/MMC_D7-B/LCD_DATA13-B/AN101	ETHPHYCLK/PE00/PIO_040/A15-B/GTOUUP-C/ GTIOC7A/SCK12-A/CTS12#-A/TXDB12-A/ SSL10-A/SD0DAT4-B/XSPI1_CKN#-A/ XSPI1_CS1#-B/PIXD0-C/IRQ8
133	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/PO23/ TIC3/GTIOC0B/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/MMC_D6-B/LCD_DATA14-B/ IRQ7-DS/AN100	P607/PIO_015/CS0#-B/D16-B/GTETRGB/ GTADSM0/GTIOC15B/POEGA/CTS8#-B/ CTS9#-B/RTS9#-B/SS9#-B/DE9-B/TXDB9-B/ CRX2-C/XSPI0_RSTO0#-A/IRQ15
134	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/MTIOC3B/ PO18/GTIOC1B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1	P606/PIO_014/CS1#-C/D17-B/GTETRGA/ GTCPPO4/GTIOC15A/POEGC/SCK9-B/ CTS9#-B/TXDB9-B/SSL03-D/CTX2-C/ XSPI0_RESET0#-A/IRQ14
135	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/GTIOC2B/ SCK12/SSLB1-B/MMC_D4-B/LCD_DATA16-B/ ANEX0	P605/PIO_013/CS2#-C/D18-B/GTIOC6B/RXD9-B/ SMISO9-B/SSCL9-B/SSL02-D/XSPI0_INT0#-A/ XSPI0_ECS0#-A/IRQ13
136	P64/WE#/D3[A3/D3]/CS4#/ET1_ETXD0/ RMII1_TXD0	P604/PIO_012/CS3#-C/D19-B/GTIOC6A/TXD9-B/ SMOSI9-B/SSDA9-B/TXDA9-B/SSL01-D/ XSPI0_CS1#-A/XSPI0_RSTO0#-B/IRQ4
137	P63/CAS#/D2[A2/D2]/CS3#/ET1_ETXD1/ RMII1_TXD1	P603/PIO_011/WE#-B/D20-B/GTIOC5B/ CTS8#-B/RTS8#-B/SS8#-B/DE8-B/TXDB8-B/ CTS9#-B/MISO0-D/XSPI0_IO7-A/PCKO-B/IRQ3
138	P62/RAS#/D1[A1/D1]/CS2#/ET1_ERXD0/ RMII1_RXD0	P602/PIO_010/CAS#-B/D21-B/GTIOC5A/SCK8-B/ CTS8#-B/TXDB8-B/MOSI0-D/XSPI0_IO6-A/ HSYNC-B/IRQ2/ADTRG2#
139	P61/SDCS#/D0[A0/D0]/CS1#/ET1_ERXD1/ RMII1_RXD1	P601/PIO_009/RAS#-B/D22-B/GTIOC4B/ RXD8-B/SMISO8-B/SSCL8-B/RSPCK0-D/ GPTP_PTPOUT1/XSPI0_IO5-A/VSYNC-B/ IRQ1/ADTRG1#
140	VSS	P600/PIO_008/SDCS#-B/D23-B/GTIOC4A/ TXD8-B/SMOSI8-B/SSDA8-B/TXDA8-B/ SSL00-D/GPTP_PTPOUT0/XSPI0_IO4-A/ PIXCLK-B/IRQ0/ADTRG0#
141	P60/CS0#/ET1_TX_EN/RMII1_TXD_EN	VCC2
142	VCC	VSS
143	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ ET1_RX_ER/RMII1_RX_ER/QMI-B/QIO1-B/ SDHI_D1-B/MMC_D1-B/LCD_DATA17-B/ IRQ7/AN107	VCL
144	TRDATA7/PG1/D25/ET1_RX_ER/RMII1_RX_ER	PD07/PIO_039/A16-B/D24-B/GTIW-C/GTIOC3B/ POEGA/TXD3-A/SMOSI3-A/SSDA3-A/TXDA3-A/ CTX1-B/SD0CD-B/XSPI0_CS0#-A/ XSPI0_RESET1#-B/PIXD7-B/IRQ7/AN031

176-Pin LFQFP	RX72N	RX74N
145	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/ET1_RX_CLK/REF50CK1/QMO-B/ QIO0-B/SDHI_D0-B/MMC_D0-B/ LCD_DATA18-B/IRQ6/AN106	PD06/PIO_038/A17-B/D25-B/GTIV-C/GTIOC3A/ POEGB/RXD3-A/SMISO3-A/SSCL3-A/SSL23-A/ CRX1-B/SD0WP-B/XSPI0_DS-A/PIXD6-B/IRQ6/ AN030
146	TRDATA6/PG0/D24/ET1_RX_CLK/REF50CK1	PD05/PIO_037/A18-B/D26-B/GTIU-C/GTIOC2B/ POEGD/SCK3-A/CTS3#-A/TXDB3-A/SSL22-A/ CTX0-B/SD0DAT1-B/XSPI0_IO3-A/PIXD5-B/ IRQ5/AN029
147	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/MTCLKA/ POE10#/SSLC1-A/ET1_MDC/PMGI1_MDC/ QSPCLK-B/SDHI_CLK-B/MMC_CLK-B/ LCD_DATA19-B/IRQ5/AN113	PD04/PIO_036/A19-B/D27-B/GTETRGA/ GTIOC2A/POEGC/CTS2#-A/CTS3#-A/RTS3#-A/ SS3#-A/DE3-A/TXDB3-A/SSL21-A/CRX0-B/ SD0DAT0-B/XSPI0_IO2-A/XSPI0_WP0#-B/ PIXD4-B/IRQ4/AN028
148	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0-A/ ET1_MDIO/PMGI1_MDIO/QSSL-B/ SDHI_CMD-B/MMC_CMD-B/ LCD_DATA20-B/IRQ4/AN112	PD03/PIO_035/A20-B/D28-B/TOC2/GTIOC1B/ POEGA/TXD2-A/SMOSI2-A/SSDA2-A/TXDA2-A/ MISO2-A/SD0CLK-B/XSPI0_IO1-A/PIXD3-B/ IRQ3/AN027
149	TRSYNC1/P97/D23/A23/ET1_ERXD3	PD02/PIO_034/A21-B/D29-B/TIC2/GTETRGB/ GTIOC1A/POEGB/RXD2-A/SMISO2-A/SSCL2-A/ MOSI2-A/SD0CMD-B/XSPI0_IO0-A/PIXD2-B/ IRQ2/AN026
150	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/ET1_WOL/QIO3-B/ SDHI_D3-B/MMC_D3-B/LCD_DATA21-B/ IRQ3/AN111	PD01/PIO_033/A22-B/D30-B/GTETRGC/ GTIOC0B/POEGC/SCK2-A/CTS2#-A/TXDB2-A/ RSPCK2-A/SD0DAT3-B/XSPI0_CK-A/PIXD1-B/ IRQ1/AN025
151	VSS	PD00/PIO_032/A23-B/D31-B/GTETRGD/ GTIOC0A/POEGD/CTS2#-A/RTS2#-A/SS2#-A/ DE2-A/TXDB2-A/CTS3#-A/SSL20-A/SD0DAT2-B/ XSPI0_CKN#-A/XSPI0_CS1#-B/PIXD0-B/ IRQ0/AN024
152	TRDATA5/P96/D22/A22/ET1_ERXD2	VCC2
153	VCC	VSS
154	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/ET1_EXOUT/QIO2-B/ SDHI_D2-B/MMC_D2-B/LCD_DATA22-B/IRQ2/ AN110	VCL
155	TRDATA4/P95/D21/A21/ET1_ERXD1/ RMII1_RXD1	P903/PIO_003/GTETRGD/GTCPPO9/POEGD/ CTS6#-B/CTS1#-C/RTS1#-C/SS1#-C/DE1-C/ TXDB1-C/XSPI0_WP1#-A/IRQ11/AN035
156	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/AN109	P902/PIO_002/GTETRGC/GTCPPO8/SCK1-C/ CTS1#-C/TXDB1-C/XSPI0_RESET1#-A/ IRQ10/AN034
157	P94/D20/A20/ET1_ERXD0/RMII1_RXD0	P901/PIO_001/GTETRGB/GTCPPO6/TXD1-C/ SMOSI1-C/SSDA1-C/TXDA1-C/ XSPI0_RSTO1#-A/XSPI0_RESET0#-B/ IRQ9/AN033
158	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108	P900/PIO_000/GTETRGA/GTCPPO5/RXD1-C/ SMISO1-C/SSCL1-C/XSPI0_INT1#-A/ XSPI0_ECS1#-A/IRQ0/AN032
159	P93/D19/A19/POE0#/CTS7#/RTS7#/SS7#/ ET1_LINKSTA/AN117	AVCC0
160	P92/D18/A18/POE4#/RXD7/SMISO7/SSCL7/ ET1_CRS/RMII1_CRS_DV/AN116	AVSS0
161	P91/D17/A17/SCK7/ET1_COL/AN115	VREFL0
162	VSS	VREFH0
163	P90/D16/A16/TXD7/SMOSI7/SSDA7/ ET1_RX_DV/AN114	P407/PIO_055/IRQ15-DS/AN007
164	VCC	P406/PIO_054/IRQ14-DS/AN006

176-Pin LFQFP	RX72N	RX74N
165	P47/IRQ15-DS/AN007	P405/PIO_053/IRQ13-DS/AN005
166	P46/IRQ14-DS/AN006	P404/PIO_052/IRQ12-DS/AN004
167	P45/IRQ13-DS/AN005	P403/PIO_051/IRQ11-DS/AN003
168	P44/IRQ12-DS/AN004	P402/PIO_050/IRQ10-DS/AN002
169	P43/IRQ11-DS/AN003	P401/PIO_049/IRQ9-DS/AN001
170	P42/IRQ10-DS/AN002	P400/PIO_048/IRQ8-DS/AN000
171	P41/IRQ9-DS/AN001	P415/PIO_063/IRQ31/AN015/DA1
172	VREFL0	P414/PIO_062/IRQ30/AN014/DA0
173	P40/IRQ8-DS/AN000	P007/PIO_007/GTCPPO6/GTIOC13B/POEGA/ CTS0#-B/RTS0#-B/SS0#-B/DE0-B/TXDB0-B/ IRQ23-DS/ADTRG0#/AN023/PDMDAT0-C
174	VREFH0	P006/PIO_006/GTCPPO5/GTIOC13A/GTIOC9B/ SCK0-B/CTS0#-B/TXDB0-B/IRQ22-DS/ ADTRG1#/AN022/PDMCLK0-C/PCOUTZ1
175	AVCC0	P005/PIO_005/GTCPPO4/GTIOC12B/GTIOC9A/ RXD0-B/SMISO0-B/SSCL0-B/SSILRCK1/ IRQ21-DS/ADTRG2#/AN021/PCOUTB1
176	P07/IRQ15/ADTRG0#	P004/PIO_004/GTCPPO3/GTIOC12A/GTIOC8B/ TXD0-B/SMOSI0-B/SSDA0-B/TXDA0-B/ SSITXD1/IRQ20-DS/AN020/PCOUTA1

3.4 144-Pin Package

Table 3.7 is Comparative Listing of RX72M/RX74M 144-Pin LFQFP Package Pin Functions, and Table 3.8 is Comparative Listing of RX72N/RX74N 144-Pin Package Pin Functions.

Table 3.7 Comparative Listing of RX72M/RX74M 144-Pin LFQFP Package Pin Functions

144-Pin LFQFP	RX72M	RX74M
1	AVSS0	P003/PIO_003/GTCPPO2/GTIOC11B/ GTIOC8A/RXD7-A/SMISO7-A/SSCL7-A/ SSIRXD1/ET0_MDIO-D/CAT0_MDIO-E/ IRQ19-DS/AN019/DSMDAT1-B/PCOUTB0
2	P05/SSILRCK1/IRQ13/DA1	P002/PIO_002/TMCI1/GTCPPO1/GTIOC11A/ GTIOC7B/TXD7-A/SMOSI7-A/SSDA7-A/ TXDA7-A/SSIBCK1/ET0_MDC-D/ CAT0_MDC-E/IRQ18-DS/AN018/DSMCLK1-B/ PCOUTA0
3	AVCC1	P001/PIO_001/TMCI0/GTCPPO0/GTIOC10B/ GTIOC7A/SCK7-A/CTS7#-A/TXDB7-A/ SSIBCK0/ET0_LINKSTA-D/CAT0_LINKSTA-E/ IRQ17-DS/AN017/DSMDAT0-B/PCOUTZ0
4	P03/SSIDATA1/IRQ11/DA0	P000/PIO_000/TMRI0/GTCPPO7/GTIOC10A/ POEGB/CTS0#-B/CTS7#-A/RTS7#-A/SS7#-A/ DE7-A/TXDB7-A/AUDIO_CLK/ET0_INT-D/ CATRESTOUT-E/IRQ16-DS/AN016/ DSMCLK0-B
5	AVSS1	VCC
6	P02/TMCI1/SCK6/SSIBCK1/CATLEDSTER/ IRQ10/AN120	VSS
7	P01/TMCI0/RXD6/SMISO6/SSCL6/SSIBCK0/ CATLEDERR/IRQ9/AN119	VCL
8	P00/TMRI0/TXD6/SMOSI6/SSDA6/ AUDIO_CLK/CATLATCH1/IRQ8/AN118	RES#
9	EMLE	MD/P315
10	VSS	P312/PIO_060/BACK#-B/RTCIC2/GTETRGD/ GTCPPO15/POEGA/SSL13-B/SSILRCK0/ ET1_WOL-C/IRQ20/ADTRG2#/DSMDAT2-C/TAMPI2
11	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/SS6#/ CTS0#/RTS0#/SS0#/SSITXD0/ET0_EXOUT/ CATRESTOUT	P311/PIO_059/BREQ#-B/RTCIC1/GTETRGC/ GTCPPO14/POEGD/CTS7#-A/SSL12-B/ SSIRXD0/ET0_WOL-C/IRQ19/ADTRG1#/ DSMCLK2-C/TAMPI1
12	VCL	P310/PIO_058/RTCIC0/CACREF/GTETRGB/ GTCPPO1/POEGC/CTS0#-C/CTS1#-B/ SSL11-B/SSITXD0/ET1_INT-E/CATIRQ-D/ IRQ18/ADTRG0#/TAMPI0
13	VBATT	VBATT/VCC
14	MD/FINED	XCIN/EXCIN/P309
15	XCIN	XCOUT/P308
16	XCOUT	VSS
17	RES#	XTAL/P307
18	XTAL/P37	EXTAL/P306
19	VSS	VCC
20	EXTAL/P36	P305/NMI/IRQ0
21	VCC	VCC_USB
22	UPSEL/P35/NMI	PF01/PIO_049/GTCPPO15/USB0_DM/IRQ1
23	TRST#/P34/MTIOC0A/TMCI3/PO12/POE10#/ SCK6/SCK0/ET0_LINKSTA/CAT0_LINKSTA/ IRQ4/DSMDAT0	PF00/PIO_048/GTCPPO14/USB0_DP/IRQ0

144-Pin LFQFP	RX72M	RX74M
24	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/SMISO6/SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/IRQ3_DS/DSMCLK0	VSS_USB
25	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCIC2/RTCOUT/POE0#/POE10#/TXD6/SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/CTX0/USB0_VBUSEN/VSYNC/IRQ2_DS	P207/PIO_023/A23-C/CS4#-C/TMRI3/GTOWLO-D/GTIOC2B/GTIOC6B/RXD1-B/SMISO1-B/SSCL1-B/MISO1-B/SDAHS2-B/CRX1-A/USB0_ID/ET0_RXD3-B/CAT0_ERXD3-B/PCKO-A/IRQ3-DS/ADTRG2#/DSMDAT5-B
26	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/ET1_MDC/PMGI1_MDC/IRQ1_DS	P206/PIO_022/A22-C/CS5#-C/TMO3/RTCOUT/GTOWUP-D/GTIOC2A/GTIOC6A/CTS6#-A/TXD1-B/SMOSI1-B/SSDA1-B/TXDA1-B/MOSI1-B/SCLHS2-B/CTX1-A/USB0_EXICEN/SSITXD1/ET0_RXD2-B/CAT0_ERXD2-B/VSYNC-A/IRQ2-DS/ADTRG1#/DSMCLK5-B/PCOUTZ1
27	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ET1_MDIO/PMGI1_MDIO/IRQ0_DS	CLKOUT/P205/PIO_021/A21-C/CS6#-C/GTOVLO-D/GTIOC1B/GTIOC5B/SCK1-B/CTS1#-B/TXDB1-B/RSPCK1-B/SDAHS1-B/CRX0-A/USB0_VBUS/SSIRXD1/ET0_RXD1-B/RMII0_RXD1-B/CAT0_ERXD1-B/SD0CD-C/HSYNC-A/IRQ5/ADTRG0#/DSMDAT4-B/PCOUTB1
28	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A/ET1_WOL/CATIRQ	ETHPHYCLK/P204/PIO_020/A20-C/CS7#-C/TMRI1/GTOVUP-D/GTIOC1A/GTIOC5A/CTS1#-B/RTS1#-B/SS1#-B/DE1-B/TXDB1-B/SSL10-B/SCLHS1-B/CTX0-A/USB0_VBUSEN/SSIBCK1/ET0_RXD0-B/RMII0_RXD0-B/CAT0_ERXD0-B/SD0WP-C/PIXCLK-A/IRQ12/DSMCLK4-B/PCOUTA1
29	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A/ET1_EXOUT/CATLINKACT1	VCL
30	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/SSIDATA1/SDHI_CD/HSYNC/ADTRG0#	VSS
31	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/SSIBCK1/SDHI_WP/PIXCLK	VCC
32	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/GTIOC0A/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/SS0#/CTX1/SSIBCK0/SDHI_D1-C/PIXD7	P203/PIO_019/CS2#-B/BACK#-A/GTOULO-D/GTIOC0B/GTIOC4B/RXD6-A/SMISO6-A/SSCL6-A/CTS3#-B/SSL00-C/SDA00-B/CRX2-B/USB0_OVRCURB/SSIBCK0/ET0_RX_CLK-B/RMII0_REF50CK-B/CAT0_RX_CLK-B/CATI2CDATA-C/SD0DAT1-C/PIXD7-A/IRQ3/DSMDAT3-B/PDMDAT0-B
33	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/GTIOC1A/SCK0/USB0_OVRCURB/AUDIO_CLK/SDHI_D0-C/PIXD6	P202/PIO_018/CS3#-B/BREQ#-A/TMO0/GTOUUP-D/GTIOC0A/GTIOC4A/TXD6-A/SMOSI6-A/SSDA6-A/TXDA6-A/RSPCK0-C/SCL00-B/CTX2-B/USB0_OVRCURA/AUDIO_CLK/ET0_RX_DV-B/RMII0_CRS_DV-B/CAT0_RX_DV-B/CATI2CCLK-C/SD0DAT0-C/PIXD6-A/IRQ15/DSMCLK3-B/PDMCLK0-B
34	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/USB0_EXICEN/SSILRCK0/SDHI_CLK-C/PIXD5/IRQ9	ETHPHYCLK/P304/PIO_028/ALE-C/WAIT#-B/TMCI3/GTETRGD/GTCPPO0/POEGA/CTS0#-A/CTS1#-A/USB0_VBUSEN/ET0_INT-E/CATRESTOUT-D/IRQ0-DS/ADTRG0#

144-Pin LFQFP	RX72M	RX74M
35	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMD-C/PIXD4/IRQ8	TDI/P303/PIO_027/TMCI2/GTCPPO13/RXD0-A/ SMISO0-A/SSCL0-A/RXD1-A/SMISO1-A/ SSCL1-A/MISO1-C/ET1_CRS-D/IRQ1
36	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/SCK1/ TXD3/SMOSI3/SSDA3/SDA2_DS/SSITXD0/ EPLSOUT0/CATSYNC0/SDHI_D3-C/PIXD3/ IRQ7/ADTRG1#	TDO/P302/PIO_026/TMRI3/GTCPPO12/TXD0-A/ SMOSI0-A/SSDA0-A/TXDA0-A/TXD1-A/ SMOSI1-A/SSDA1-A/TXDA1-A/MOSI1-C/ ET1_COL-D/IRQ4
37	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/ SSDA10/TXD10/EPLSOUT1/CATSYNC1/ SDHI_D2-C/PIXD2	TCK/SWCLK/P301/PIO_025/TMCI3/GTCPPO11/ SCK0-A/CTS0#-A/TXDB0-A/SCK1-A/CTS1#-A/ TXDB1-A/RSPCK1-C/ET1_WOL-D/IRQ7
38	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/SMOSI1/SSDA1/ RXD3/SMISO3/SSCL3/SCL2_DS/ USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#	TMS/SWDIO/P300/PIO_024/TMO1/GTCPPO10/ CTS0#-A/RTS0#-A/SS0#-A/DE0-A/TXDB0-A/ CTS1#-A/RTS1#-A/SS1#-A/DE1-A/TXDB1-A/ SSL10-C/ET0_WOL-D/IRQ6
39	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/ SSCL10/RXD10/CATLINKACT0/PIXD1	P201/PIO_017/TMCI0/GTIW-D/GTIOC3B/ GTIOC14B/SCK6-A/CTS6#-A/TXDB6-A/ MISO0-C/SCLHS1-A/USB0_EXICEN/ SSILRCK0/ET0_RX_ER-B/RMII0_RX_ER-B/ CAT0_RX_ER-B/SD0CLK-C/PIXD5-A/IRQ9/ PCINZ0
40	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/GTETRGA/RXD1/SMISO1/ SSCL1/SCK3/CRX1_DS/SSILRCK1/ CATLEDRUN/PIXD0/IRQ5	P200/PIO_016/TMRI0/GTETRGA/GTIOC3A/ GTIOC14A/CTS6#-A/RTS6#-A/SS6#-A/DE6-A/ TXDB6-A/MOSI0-C/SDAHS1-A/USB0_ID/ SSIRXD0/ET0_TX_EN-B/RMII0_TX_EN-B/ CAT0_TX_EN-B/SD0CMD-C/PIXD4-A/IRQ8/ ADTRG2#/PCINZ1
41	P13/MTIOC0B/TIOCA5/TMO3/PO13/ GTADSM1/TXD2/SMOSI2/SSDA2/SDA0[FM+]/ IRQ3/ADTRG1#	P107/PIO_015/TMO1/GTIV-D/GTIOC15B/ POEGA/TXD3-B/SMOSI3-B/SSDA3-B/TXDA3-B/ SDAHS2-A/SSITXD0/ET0_TXD3-B/ CAT0_ETXD3-B/CATI2CDATA-B/SD0DAT3-C/ PIXD3-A/IRQ31-DS/ADTRG1#/PCINB1
42	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/GTETRGD/CTS1#/RTS1#/SS1#/ CTX1/USB0_OVRCURA/IRQ4	CLKOUT/P106/PIO_014/TMO2/RTCOUT/ GTIU-D/GTIOC15A/POEGB/RXD3-B/SMISO3-B/ SSCL3-B/SCLHS2-A/ET0_TXD2-B/ CAT0_ETXD2-B/CATI2CCLK-B/SD0DAT2-C/ PIXD2-A/IRQ30-DS/ADTRG0#/PCINA1
43	P12/TMCI1/GTADSM0/RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	P105/PIO_013/TMCI2/GTIV-E/GTIOC14B/ TXD2-B/SMOSI2-B/SSDA2-B/TXDA2-B/SCK3-B/ CTS3#-B/TXDB3-B/CRX2-A/USB0_VBUS/ SSILRCK1/ET0_TXD1-B/RMII0_TXD1-B/ CAT0_ETXD1-B/CATLEDRUN-C/PIXD1-A/ IRQ29-DS/ADST1-A/DSMDAT1-C/PCINB0
44	VCC_USB	P104/PIO_012/TMRI2/GTIW-E/GTIOC14A/ RXD2-B/SMISO2-B/SSCL2-B/CTS3#-B/ RTS3#-B/SS3#-B/DE3-B/TXDB3-B/CTX2-A/ USB0_OVRCURA-DS/ET0_TXD0-B/ RMII0_TXD0-B/CAT0_ETXD0-B/ CATLEDSTER-C/PIXD0-A/IRQ4/ADST0-A/ DSMCLK1-C/PCINA0
45	USB0_DM	VCL
46	USB0_DP	VSS
47	VSS_USB	VCC
48	CLKOUT25M/PJ2/TXD8/SMOSI8/SSDA8	P103/PIO_011/TMO3/GTADSM1/GTIOC13B/ CTS2#-B/SDA00-A/ET0_CRS-D/ CATI2CDATA-A/IRQ3
49	CLKOUT25M/P56/EDACK1/MTIOC3C/TIOCA1/ SCK7/DSMDAT1	P102/PIO_010/TMCI1/GTADSM0/GTIOC13A/ SCL00-A/ET0_COL-D/CATI2CCLK-A/IRQ2

144-Pin LFQFP	RX72M	RX74M
50	TRDATA3/P55/D0[A0/D0]/WAIT#/EDREQ0/ MTIOC4D/TMO3/TXD7/SMOSI7/SSDA7/CRX1/ ET0_EXOUT/IRQ10	P101/PIO_009/CS0#-A/ALE-B/TMCI3/ GTETRGC/GTADSM1/GTIOC12B/SCK2-B/ CTS2#-B/TXDB2-B/USB0_VBUS-DS/ ET0_TX_CLK-B/CAT0_TX_CLK-B/ CAT0_LINKSTA-D/IRQ1/ADTRG1#/ DSMDAT0-C
51	TRDATA2/P54/ALE/D1[A1/D1]/EDACK0/ MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1/ ET0_LINKSTA/CAT0_LINKSTA	P100/PIO_008/CS1#-B/WAIT#-A/TMRI3/ CACREF/GTIU-E/GTADSM0/GTIOC12A/ CTS2#-B/RTS2#-B/SS2#-B/DE2-B/TXDB2-B/ CTS5#-B/USB0_OVRCURB-DS/ET0_TX_ER-B/ CATLINKACT0-B/CATLEDERR-C/IRQ0/ ADTRG2#/DSMCLK0-C
52	P53*1/BCLK	VCC_DCDC
53	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A/ CATLEDSTER	VCC_DCDC
54	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	VLO
55	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A/CATLEDERR	VLO
56	VSS	VSS_DCDC
57	TRCLK/P83/EDACK1/MTIOC4C/GTIOC0A/ SCK10/SS10#/CTS10#/ET0_CRS/ RMII0_CRS_DV/CAT0_RX_DV/DSMCLK1	VSS_DCDC
58	VCC	P803/PIO_059/CS3#-A/WR1#-B/BC1#-B/ GTIOC1B/POEGA/CTS10#-B/RTS10#-B/ SS10#-B/DE10-B/TXDB10-B/CTX2-D/USB0_ID/ ET0_MDC-B/CAT0_MDC-B/IRQ3/ADSYNC-B/ DSMDAT3-C
59	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/GTIOC3A/TXD8/ SMOSI8/SSDA8/SMOSI10/SSDA10/TXD10/ MISOA-A/ET0_COL/MMC_D7-A/IRQ14	P802/PIO_058/CS2#-A/WR#-B/WR0#-B/ GTIW-B/GTIOC1A/POEGB/SCK10-B/ CTS10#-B/TXDB10-B/CRX2-D/USB0_EXICEN/ ET0_MDIO-B/CAT0_MDIO-B/IRQ2/ADCNV2-B/ DSMCLK3-C
60	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/MTCLKA/ TMCI2/PO30/TIC0/GTIOC3B/RXD8/SMISO8/ SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ ET0_ETXD3/CAT0_ETXD3/CATLATCH1/ MMC_D6-A/IRQ13	VCL
61	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/RTS8#/ SCK10/RSPCKA-A/ET0_ETXD2/CAT0_ETXD2/ MMC_D5-A	VSS
62	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ GTIOC2A/SMOSI10/SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/CAT0_ETXD1/ CATI2CDATA/MMC_D4-A	VCC
63	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ GTIOC0B/SMISO10/SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/CAT0_ETXD0/ CATI2CCLK/QIO3-A/SDHI_CD/MMC_D3-A	CLKOUT/P801/PIO_057/EBCLK-A/GTIV-B/ GTIOC0B/POEGC/TXD10-B/SMOSI10-B/ SSDA10-B/TXDA10-B/ET0_CRS-B/ CATSYNC0-A/IRQ9/ADCNV1-B/DSMDAT4-C
64	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10/RTS10#/ET0_TX_EN/RMII0_TXD_EN/ CAT0_TX_EN/CATLATCH0/QIO2-A/SDHI_WP/ MMC_D2-A	P800/PIO_056/CS1#-A/DQM0-B/GTIU-B/ GTIOC0A/POEGD/RXD10-B/SMISO10-B/ SSCL10-B/ET0_COL-B/CATLATCH0-A/IRQ8/ ADCNV0-B/DSMCLK4-C
65	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/GTETRGC/SCK5/SS8#/CTS8#/ SS10#/CTS10#/RTS10#/SSLA0-A/ ET0_TX_CLK/CAT0_TX_CLK/CATSYNC0/ QMI-A/QIO1-A/SDHI_D1-A/MMC_D1-A	ETHPHYCLK/PC07/PIO_031/D0-A/TMO2/ TOC0/CACREF/GTETRGD/GTADSM1/ GTIOC15B/POEGA/TXD8-A/SMOSI8-A/ SSDA8-A/TXDA8-A/MISO0-A/SSITXD0/ CATRESTOUT-A/SD0CD-A/IRQ14/ DSMDAT5-C/PDMDAT0-A

144-Pin LFQFP	RX72M	RX74M
66	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/MMC_D0-A	PC06/PIO_030/D1-A/TMCI2/TIC0/GTETRGC/ GTCPPO7/GTIOC15A/POEGB/RXD8-A/ SMISO8-A/SSCL8-A/MOSI0-A/SSILRCK0/ ET0_TX_ER-A/CATLINKACT0-A/SD0WP-A/ IRQ13/DSMCLK5-C/PDMCLK0-A
67	TRDATA7/P77/CS7#/PO23/SMOSI11/SSDA11/ TXD11/ET0_RX_ER/RMII0_RX_ER/ CAT0_RX_ER/QSPCLK-A/ SDHI_CLK-A/MMC_CLK-A	PC05/PIO_029/D2-A/TMRI2/GTOWLO-B/ GTIOC9B/SCK8-A/CTS8#-A/TXDB8-A/ RSPCK0-A/SSIBCK0/ET0_TX_EN-A/ RMII0_TX_EN-A/CAT0_TX_EN-A/SD0DAT1-A/ IRQ5/PCOUTZ1
68	TRDATA6/P76/CS6#/PO22/SMISO11/SSCL11/ RXD11/ET0_RX_CLK/REF50CK0/ CAT0_RX_CLK/QSSL-A/SDHI_CMD-A/ MMC_CMD-A	PC04/PIO_028/D3-A/TMCI1/GTOWUP-B/ GTIOC9A/CTS8#-A/RTS8#-A/SS8#-A/DE8-A/ TXDB8-A/CTS11#-A/SSL00-A/AUDIO_CLK/ ET0_TXD3-A/CAT0_ETXD3-A/SD0DAT0-A/ IRQ12/PCOUTB1
69	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ET0_RX_DV/ CAT0_RX_DV/SDHI_D3-A/MMC_CD-A	PC03/PIO_027/D4-A/GTOVLO-B/GTIOC8B/ TXD11-A/SMOSI11-A/SSDA11-A/TXDA11-A/ SDAHS1-C/ET0_TXD2-A/CAT0_ETXD2-A/ SD0CLK-A/IRQ11/PCOUTA1
70	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/ ET0_ERXD0/RMII0_RXD0/CAT0_ERXD0/ SDHI_D2-A/MMC_RES#-A/DSMDAT2	PC02/PIO_026/D5-A/GTOVUP-B/GTIOC8A/ RXD11-A/SMISO11-A/SSCL11-A/SSL03-A/ SCLHS1-C/ET0_TXD1-A/RMII0_TXD1-A/ CAT0_ETXD1-A/SD0CMD-A/IRQ10/PCOUTZ0
71	TRDATA5/P74/A20/CS4#/PO19/SS11#/ CTS11#/ET0_ERXD1/RMII0_RXD1/ CAT0_ERXD1/DSMCLK2	PC01/PIO_025/D6-A/GTOULO-B/GTIOC7B/ SCK11-A/CTS11#-A/TXDB11-A/SSL02-A/ SDA00-C/ET0_TXD0-A/RMII0_TXD0-A/ CAT0_ETXD0-A/SD0DAT3-A/IRQ12/PCOUTB0
72	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/CAT0_ERXD2/IRQ12	PC00/PIO_024/D7-A/GTOUUP-B/GTIOC7A/ CTS11#-A/RTS11#-A/SS11#-A/DE11-A/ TXDB11-A/SSL01-A/SCL00-C/ET0_TX_CLK-A/ CAT0_TX_CLK-A/SD0DAT2-A/IRQ14/ PCOUTA0
73	VCC	PB07/PIO_023/D8-A/GTOWLO-A/GTIOC6B/ TXD9-A/SMOSI9-A/SSDA9-A/TXDA9-A/ ET0_LINKSTA-A/CAT0_LINKSTA-A/IRQ15
74	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/ET0_ERXD3/ CAT0_ERXD3/IRQ14	PB06/PIO_022/D9-A/GTOWUP-A/GTIOC6A/ RXD9-A/SMISO9-A/SSCL9-A/ET0_RX_ER-A/ RMII0_RX_ER-A/CAT0_RX_ER-A/IRQ6
75	VSS	PB05/PIO_021/D10-A/TMRI1/GTOVLO-A/ GTIOC5B/SCK9-A/CTS9#-A/TXDB9-A/ ET0_RX_DV-A/RMII0_CRS_DV-A/ CAT0_RX_DV-A/IRQ13
76	TRDATA4/P73/CS3#/PO16/ET0_WOL	PB04/PIO_020/D11-A/GTOVUP-A/GTIOC5A/ CTS4#-A/CTS9#-A/RTS9#-A/SS9#-A/DE9-A/ TXDB9-A/ET0_RX_CLK-A/RMII0_REF50CK-A/ CAT0_RX_CLK-A/IRQ4
77	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV/CAT0_RX_DV	VCC
78	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1/CAT0_ETXD1	VSS
79	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/SCK11/ ET0_ETXD0/RMII0_TXD0/CAT0_ETXD0/ LCD_CLK-B	VCL
80	PB4/A12/TIOCA4/PO28/SS9#/CTS9#/SS11#/ CTS11#/RTS11#/ET0_TX_EN/RMII0_TXD_EN/ CAT0_TX_EN/LCD_TCON0-B	PB03/PIO_019/D12-A/TMO0/GTOULO-A/ GTIOC4B/SCK4-A/CTS4#-A/TXDB4-A/ ET0_RXD3-A/CAT0_ERXD3-A/IRQ3

144-Pin LFQFP	RX72M	RX74M
81	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK4/SCK6/ ET0_RX_ER/RMII0_RX_ER/CAT0_RX_ER/ LCD_TCON1-B	PB02/PIO_018/D13-A/GTOUUP-A/GTIOC4A/ CTS4#-A/RTS4#-A/SS4#-A/DE4-A/TXDB4-A/ CTS9#-A/ET0_RXD2-A/CAT0_ERXD2-A/IRQ2
82	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/ SS4#/CTS6#/RTS6#/SS6#/ET0_RX_CLK/ REF50CK0/CAT0_RX_CLK/LCD_TCON2-B	PB01/PIO_017/D14-A/TMCI0/GTETRGB/ GTCPPO4/GTIOC14B/POEGA/TXD4-A/ SMOSI4-A/SSDA4-A/TXDA4-A/ET0_RXD1-A/ RMII0_RXD1-A/CAT0_ERXD1-A/IRQ4-DS/ DSMDAT2-A/PCINB1
83	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/ PO25/TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/ SSDA6/ET0_ERXD0/RMII0_RXD0/ CAT0_ERXD0/LCD_TCON3-B/IRQ4_DS	PB00/PIO_016/D15-A/GTETRGA/GTADSM0/ GTIOC14A/POEGC/RXD4-A/SMISO4-A/ SSCL4-A/ET0_RXD0-A/RMII0_RXD0-A/ CAT0_ERXD0-A/IRQ12/ADST2-A/ DSMCLK2-A/PCINA1
84	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/ET0_ERXD1/ RMII0_RXD1/CAT0_ERXD1/LCD_DATA0-B/ IRQ12	ETHPHYCLK/PA07/PIO_015/A0-A/BC0#-A/ DQM1-B/GTIOC3B/GTIOC13B/RXD10-A/ SMISO10-A/SSCL10-A/MISO0-B/ ET1_TX_ER-A/CATLINKACT1-A/IRQ7/PCINB0
85	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B	PA06/PIO_014/A1-A/TMCI3/GTIOC3A/ GTIOC13A/TXD10-A/SMOSI10-A/SSDA10-A/ TXDA10-A/MOSI0-B/ET1_TXD3-A/ CAT1_ETXD3-A/IRQ14/PCINZ1
86	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/GTETRGB/CTS5#/RTS5#/SS5#/ MOSIA-B/ET0_EXOUT/CATRESTOUT/ LCD_DATA2-B	PA05/PIO_013/A2-A/GTIOC2B/GTIOC12B/ SCK10-A/CTS10#-A/TXDB10-A/RSPCK0-B/ ET1_TXD2-A/CAT1_ETXD2-A/IRQ5/PCINA0
87	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/CAT0_LINKSTA/ LCD_DATA3-B	PA04/PIO_012/A3-A/TMRI0/GTIOC2A/ GTIOC12A/CTS10#-A/RTS10#-A/SS10#-A/ DE10-A/TXDB10-A/SSL00-B/ET1_TXD1-A/ RMII1_TXD1-A/CAT1_ETXD1-A/IRQ5-DS/ PCINZ0
88	VCC	VCC
89	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ ET0_MDC/CAT0_MDC/CATIRQ/PMGI0_MDC/ LCD_DATA4-B/IRQ5_DS	VSS
90	VSS	VCL
91	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/ CAT0_MDIO/PMGI0_MDIO/LCD_DATA5-B/ IRQ6_DS	PA03/PIO_011/A4-A/GTIOC1B/GTIOC11B/ RXD5-A/SMISO5-A/SSCL5-A/ET1_TXD0-A/ RMII1_TXD0-A/CAT1_ETXD0-A/IRQ6-DS/ ADSYNC-A/DSMDAT1-A
92	PG7/ET1_TX_ER	PA02/PIO_010/A5-A/GTIW-A/GTIOC1A/ GTIOC11A/TXD5-A/SMOSI5-A/SSDA5-A/ TXDA5-A/SSL03-B/ET1_TX_CLK-A/ CAT1_TX_CLK-A/IRQ10/ADCNV2-A/ DSMCLK1-A
93	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/CATLINKACT1/ LCD_DATA6-B	PA01/PIO_009/A6-A/GTIV-A/GTIOC0B/ GTIOC10B/SCK5-A/CTS5#-A/TXDB5-A/ SSL02-B/ET1_TX_EN-A/RMII1_TX_EN-A/ CAT1_TX_EN-A/IRQ11/ADCNV1-A/ DSMDAT0-A
94	PG6/ET1_ETXD3/CAT1_ETXD3	ETHPHYCLK/PA00/PIO_008/A7-A/CACREF/ GTIU-A/GTIOC0A/GTIOC10A/CTS10#-A/ CTS5#-A/RTS5#-A/SS5#-A/DE5-A/TXDB5-A/ SSL01-B/CATIRQ-A/IRQ1-DS/ADCNV0-A/ DSMCLK0-A

144-Pin LFQFP	RX72M	RX74M
95	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/ PO17/GTIOC2A/SCK5/SSLA2-B/ET0_WOL/ LCD_DATA7-B/IRQ11	P702/PIO_050/RD#-A/GTETRGA/GTIOC11A/ SCK4-B/CTS4#-B/TXDB4-B/ET1_CRS-E/ CATSYNC1-A/XSPI1_WP0#-B/ XSPI1_RESET1#-C/HSYNC-C/IRQ10/ ADST2-B/DSMCLK4-D
96	PG5/ET1_ETXD2/CAT1_ETXD2	P701/PIO_049/CKE-A/GTIOC10B/RXD4-B/ SMISO4-B/SSCL4-B/ET1_COL-E/ CATLATCH1-A/XSPI1_RSTO0#-B/ XSPI1_RESET0#-B/VSYNC-C/IRQ1/ ADST1-B/DSMDAT3-D
97	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/ PO16/CACREF/GTIOC0B/SSLA1-B/ ET0_TX_EN/RMII0_TXD_EN/CAT0_TX_EN/ CATLEDRUN/LCD_DATA8-B	ETHPHYCLK/P700/PIO_048/SDCLK-A/ GTIOC10A/TXD4-B/SMOSI4-B/SSDA4-B/ TXDA4-B/ET1_INT-A/CATRESTOUT-F/ XSPI1_INT0#-B/XSPI1_ECS0#-B/PIXCLK-C/ IRQ0/ADST0-B/DSMCLK3-D
98	P67/CS7#/MTIOC7C/GTIOC1B/CRX2/ EPLSOUT1/CATSYNC1/IRQ15	VCC
99	P66/CS6#/MTIOC7D/GTIOC2B/CTX2	VSS
100	PG2/ET1_TX_CLK/CAT1_TX_CLK	VCL
101	P65/CS5#	PE07/PIO_047/A8-B/A20-C/TOC1/GTETRGD/ GTCPPO7/GTIOC10B/POEGD/ ET1_LINKSTA-E/CAT1_LINKSTA-D/ CATRESTOUT-C/XSPI1_CS0#-A/PIXD7-C/ IRQ7
102	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105	PE06/PIO_046/A9-B/A21-C/TIC1/GTETRGC/ GTADSM1/GTIOC10A/POEGB/SSL13-A/ ET1_RX_CLK-D/RMII1_REF50CK-D/ CAT1_RX_CLK-D/CATLEDERR-B/ XSPI1_DS-A/PIXD6-C/IRQ6
103	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/AN104	PE05/PIO_045/A10-B/A22-C/GTOWLO-C/ GTIOC9B/SSL12-A/ET1_RXD3-D/ CAT1_ERXD3-D/CATLEDRUN-B/ XSPI1_IO3-A/PIXD5-C/IRQ5
104	VCC	PE04/PIO_044/A11-B/A23-C/GTOWUP-C/ GTIOC9A/CTS12#-A/SSL11-A/ET1_RXD2-D/ CAT1_ERXD2-D/CATLEDSTER-B/ XSPI1_IO2-A/XSPI1_WP0#-C/PIXD4-C/IRQ12
105	VSS	PE03/PIO_043/A12-B/TOC3/GTOVLO-C/ GTIOC8B/CTS12#-A/RTS12#-A/SS12#-A/ DE12-A/TXDB12-A/MISO1-A/ET1_RXD1-D/ RMII1_RXD1-D/CAT1_ERXD1-D/SD0DAT7-B/ XSPI1_IO1-A/PIXD3-C/IRQ11
106	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ET0_RX_CLK/ REF50CK0/CAT0_RX_CLK/LCD_DATA11-B/ IRQ5/AN103	PE02/PIO_042/A13-B/TIC3/GTOVUP-C/ GTIOC8A/RXD12-A/SMISO12-A/SSCL12-A/ MOSI1-A/ET1_RXD0-D/RMII1_RXD0-D/ CAT1_ERXD0-D/SD0DAT6-B/XSPI1_IO0-A/ PIXD2-C/IRQ7-DS
107	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/CAT0_ERXD2/LCD_DATA12-B/ AN102	CLKOUT/PE01/PIO_041/A14-B/GTOULO-C/ GTIOC7B/TXD12-A/SMOSI12-A/SSDA12-A/ TXDA12-A/RSPCK1-A/ET1_RX_DV-D/ RMII1_CRS_DV-D/CAT1_RX_DV-D/ SD0DAT5-B/XSPI1_CK-A/PIXD1-C/IRQ9
108	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/CTS12#/RTS12#/ SS12#/ET0_ERXD3/CAT0_ERXD3/MMC_D7-B/ LCD_DATA13-B/AN101	ETHPHYCLK/PE00/PIO_040/A15-B/ GTOUUP-C/GTIOC7A/SCK12-A/CTS12#-A/ TXDB12-A/SSL10-A/ET1_RX_ER-D/ RMII1_RX_ER-D/CAT1_RX_ER-D/SD0DAT4-B/ XSPI1_CKN#-A/XSPI1_CS1#-B/PIXD0-C/IRQ8

144-Pin LFQFP	RX72M	RX74M
109	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/PO23/TIC3/GTIOC0B/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/MMC_D6-B/LCD_DATA14-B/IRQ7_DS/AN100	P605/PIO_013/CS2#-C/GTIOC6B/RXD9-B/SMISO9-B/SSCL9-B/SSL02-D/ET1_TXD3-B/ET_TAS_STA1/CAT1_ETXD3-B/XSPI0_INT0#-A/XSPI0_ECS0#-A/IRQ13/DSMDAT4-A
110	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/MTIOC3B/PO18/GTIOC1B/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/MMC_D5-B/LCD_DATA15-B/ANEX1	P604/PIO_012/CS3#-C/GTIOC6A/TXD9-B/SMOSI9-B/SSDA9-B/TXDA9-B/SSL01-D/ET1_TXD2-B/ET_TAS_STA0/CAT1_ETXD2-B/XSPI0_CS1#-A/XSPI0_RSTO0#-B/IRQ4/DSMCLK4-A
111	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/GTIOC2B/SCK12/SSLB1-B/MMC_D4-B/LCD_DATA16-B/ANEX0	P603/PIO_011/WE#-B/GTIOC5B/CTS8#-B/RTS8#-B/SS8#-B/DE8-B/TXDB8-B/CTS9#-B/MISO0-D/ET1_TXD1-B/RMII1_TXD1-B/GPTP_PTPOUT3/CAT1_ETXD1-B/CATSYNC0-B/XSPI0_IO7-A/PCKO-B/IRQ3/DSMDAT3-A
112	P64/D3[A3/D3]/CS4#/ET1_ETXD0/RMII1_TXD0/CAT1_ETXD0	P602/PIO_010/CAS#-B/GTIOC5A/SCK8-B/CTS8#-B/TXDB8-B/MOSI0-D/ET1_TXD0-B/RMII1_TXD0-B/GPTP_PTPOUT2/CAT1_ETXD0-B/CATLATCH0-B/XSPI0_IO6-A/HSYNC-B/IRQ2/ADTRG2#/DSMCLK3-A
113	P63/D2[A2/D2]/CS3#/ET1_ETXD1/RMII1_TXD1/CAT1_ETXD1	P601/PIO_009/RAS#-B/GTIOC4B/RXD8-B/SMISO8-B/SSCL8-B/RSPCK0-D/ET1_TX_EN-B/RMII1_TX_EN-B/GPTP_PTPOUT1/CAT1_TX_EN-B/CATSYNC1-D/XSPI0_IO5-A/VSYNC-B/IRQ1/ADTRG1#
114	P62/D1[A1/D1]/CS2#/ET1_ERXD0/RMII1_RXD0/CAT1_ERXD0	P600/PIO_008/SDCS#-B/GTIOC4A/TXD8-B/SMOSI8-B/SSDA8-B/TXDA8-B/SSL00-D/ET1_TX_CLK-B/GPTP_PTPOUT0/CAT1_TX_CLK-B/CATLATCH1-D/XSPI0_IO4-A/PIXCLK-B/IRQ0/ADTRG0#
115	P61/D0[A0/D0]/CS1#/ET1_ERXD1/RMII1_RXD1/CAT1_ERXD1	VCC2
116	VSS	VSS
117	P60/CS0#/ET1_TX_EN/RMII1_TXD_EN/CAT1_TX_EN	PD07/PIO_039/A16-B/GTIW-C/GTIOC3B/POEGA/TXD3-A/SMOSI3-A/SSDA3-A/TXDA3-A/CTX1-B/ET1_LINKSTA-B/CAT1_LINKSTA-B/SD0CD-B/XSPI0_CS0#-A/XSPI0_RESET1#-B/PIXD7-B/IRQ7/AN031
118	VCC	PD06/PIO_038/A17-B/GTIV-C/GTIOC3A/POEGB/RXD3-A/SMISO3-A/SSCL3-A/SSL23-A/CRX1-B/ET1_RX_ER-B/RMII1_RX_ER-B/CAT1_RX_ER-B/CATLEDERR-D/SD0WP-B/XSPI0_DS-A/PIXD6-B/IRQ6/AN030
119	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ET1_RX_ER/RMII1_RX_ER/CAT1_RX_ER/QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/LCD_DATA17-B/IRQ7/AN107	PD05/PIO_037/A18-B/GTIU-C/GTIOC2B/POEGD/SCK3-A/CTS3#-A/TXDB3-A/SSL22-A/CTX0-B/ET1_RX_DV-B/RMII1_CRS_DV-B/CAT1_RX_DV-B/CATLEDSTER-D/SD0DAT1-B/XSPI0_IO3-A/PIXD5-B/IRQ5/AN029
120	PG1/ET1_RX_ER/RMII1_RX_ER/CAT1_RX_ER	PD04/PIO_036/A19-B/GTETRGA/GTIOC2A/POEGC/CTS2#-A/CTS3#-A/RTS3#-A/SS3#-A/DE3-A/TXDB3-A/SSL21-A/CRX0-B/ET1_RX_CLK-B/RMII1_REF50CK-B/CAT1_RX_CLK-B/CATLEDRUN-D/SD0DAT0-B/XSPI0_IO2-A/XSPI0_WP0#-B/PIXD4-B/IRQ4/AN028

144-Pin LFQFP	RX72M	RX74M
121	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/ET1_RX_CLK/REF50CK1/ CAT1_RX_CLK/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/IRQ6/AN106	PD03/PIO_035/A20-B/TOC2/GTIOC1B/POEGA/ TXD2-A/SMOSI2-A/SSDA2-A/TXDA2-A/ MISO2-A/ET1_RXD3-B/CAT1_ERXD3-B/ CAT0_MDIO-D/SD0CLK-B/XSPI0_IO1-A/ PIXD3-B/IRQ3/AN027
122	PG0/ET1_RX_CLK/REF50CK1/CAT1_RX_CLK	PD02/PIO_034/A21-B/TIC2/GTETRGB/ GTIOC1A/POEGB/RXD2-A/SMISO2-A/ SSCL2-A/MOSI2-A/ET1_RXD2-B/ CAT1_ERXD2-B/CAT0_MDC-D/SD0CMD-B/ XSPI0_IO0-A/PIXD2-B/IRQ2/AN026
123	PD5/D5[A5/D5]/MTIC5W/MTCLKA/MTIOC8C/ POE10#/SSLC1-A/ET1_MDC/PMGI1_MDC/ QSPCLK-B/SDHI_CLK-B/MMC_CLK-B/ LCD_DATA19-B/IRQ5/AN113	PD01/PIO_033/A22-B/GTETRGC/GTIOC0B/ POEGC/SCK2-A/CTS2#-A/TXDB2-A/ RSPCK2-A/ET1_RXD1-B/RMII1_RXD1-B/ CAT1_ERXD1-B/CATSYNC0-D/SD0DAT3-B/ XSPI0_CK-A/PIXD1-B/IRQ1/AN025
124	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0-A/ ET1_MDIO/PMGI1_MDIO/QSSL-B/ SDHI_CMD-B/MMC_CMD-B/ LCD_DATA20-B/IRQ4/AN112	PD00/PIO_032/A23-B/GTETRGD/GTIOC0A/ POEGD/CTS2#-A/RTS2#-A/SS2#-A/DE2-A/ TXDB2-A/CTS3#-A/SSL20-A/ET1_RXD0-B/ RMII1_RXD0-B/CAT1_ERXD0-B/ CATLATCH0-D/SD0DAT2-B/XSPI0_CKN#-A/ XSPI0_CS1#-B/PIXD0-B/IRQ0/AN024
125	P97/A23/ET1_ERXD3/CAT1_ERXD3	VSS
126	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/ET1_WOL/QIO3-B/ SDHI_D3-B/MMC_D3-B/LCD_DATA21-B/ IRQ3/AN111	VCL
127	P96/A22/ET1_ERXD2/CAT1_ERXD2	P901/PIO_001/GTETRGB/GTCPPO6/TXD1-C/ SMOSI1-C/SSDA1-C/TXDA1-C/ET1_CRS-B/ ET_TAS_STA1/CATLATCH1-B/ XSPI0_RSTO1#-A/XSPI0_RESET0#-B/IRQ9/ AN033
128	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/ET1_EXOUT/QIO2-B/ SDHI_D2-B/MMC_D2-B/LCD_DATA22-B/ IRQ2/AN110	P900/PIO_000/GTETRGA/GTCPPO5/RXD1-C/ SMISO1-C/SSCL1-C/ET1_COL-B/ ET_TAS_STA0/CATSYNC1-B/ XSPI0_INT1#-A/XSPI0_ECS1#-A/IRQ0/AN032
129	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/AN109	AVCC0
130	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108	AVSS0
131	P93/A19/POE0#/CTS7#/RTS7#/SS7#/ ET1_LINKSTA/CAT1_LINKSTA/AN117	VREFL0
132	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ ET1_CRS/RMII1_CRS_DV/CAT1_RX_DV/ AN116	VREFH0
133	P91/A17/SCK7/ET1_COL/AN115	P405/PIO_053/IRQ13-DS/AN005
134	VSS	P404/PIO_052/IRQ12-DS/AN004
135	P90/A16/TXD7/SMOSI7/SSDA7/ET1_RX_DV/ CAT1_RX_DV/AN114	P403/PIO_051/IRQ11-DS/AN003
136	VCC	P402/PIO_050/IRQ10-DS/AN002
137	P44/IRQ12_DS/AN004	P401/PIO_049/IRQ9-DS/AN001
138	P43/IRQ11_DS/AN003	P400/PIO_048/IRQ8-DS/AN000
139	P42/IRQ10_DS/AN002	P415/PIO_063/IRQ31/AN015/DA1
140	P41/IRQ9_DS/AN001	P414/PIO_062/IRQ30/AN014/DA0
141	VREFL0	P007/PIO_007/GTCPPO6/GTIOC13B/POEGA/ CTS0#-B/RTS0#-B/SS0#-B/DE0-B/TXDB0-B/ ET1_INT-D/CATIRQ-E/IRQ23-DS/ADTRG0#/ AN023/PDMDAT0-C

144-Pin LFQFP	RX72M	RX74M
142	P40/IRQ8_DS/AN000	P006/PIO_006/GTCPPO5/GTIOC13A/ GTIOC9B/SCK0-B/CTS0#-B/TXDB0-B/ ET1_LINKSTA-D/CAT1_LINKSTA-E/IRQ22-DS/ ADTRG1#/AN022/PDMCLK0-C/PCOUTZ1
143	VREFH0	P005/PIO_005/GTCPPO4/GTIOC12B/ GTIOC9A/RXD0-B/SMISO0-B/SSCL0-B/ SSILRCK1/ET1_MDIO-D/CATLATCH0-E/ IRQ21-DS/ADTRG2#/AN021/DSMDAT2-B/ PCOUTB1
144	AVCC0	P004/PIO_004/GTCPPO3/GTIOC12A/ GTIOC8B/TXD0-B/SMOSI0-B/SSDA0-B/ TXDA0-B/SSITXD1/ET1_MDC-D/CATSYNC0-E/ IRQ20-DS/AN020/DSMCLK2-B/PCOUTA1

Note: 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

Table 3.8 Comparative Listing of RX72N/RX74N 144-Pin Package Pin Functions

144-Pin	RX72N (144-Pin LFQFP)	RX74N (144-Pin LFQFP)
1	AVSS0	P003/PIO_003/GTCPPO2/GTIOC11B/GTIOC8A/ RXD7-A/SMISO7-A/SSCL7-A/SSIRXD1/ ET0_MDIO-D/IRQ19-DS/AN019/PCOUTB0
2	P05/SSILRCK1/IRQ13/DA1	P002/PIO_002/TMCI1/GTCPPO1/GTIOC11A/ GTIOC7B/TXD7-A/SMOSI7-A/SSDA7-A/ TXDA7-A/SSIBCK1/ET0_MDC-D/IRQ18-DS/ AN018/PCOUTA0
3	AVCC1	P001/PIO_001/TMCI0/GTCPPO0/GTIOC10B/ GTIOC7A/SCK7-A/CTS7#-A/TXDB7-A/SSIBCK0/ ET0_LINKSTA-D/IRQ17-DS/AN017/PCOUTZ0
4	P03/SSIDATA1/IRQ11/DA0	P000/PIO_000/TMRI0/GTCPPO7/GTIOC10A/ POEGB/CTS0#-B/CTS7#-A/RTS7#-A/SS7#-A/ DE7-A/TXDB7-A/AUDIO_CLK/ET0_INT-D/ IRQ16-DS/AN016
5	AVSS1	VCC
6	P02/TMCI1/SCK6/SSIBCK1/IRQ10/AN120	VSS
7	P01/TMCI0/RXD6/SMISO6/SSCL6/SSIBCK0/ IRQ9/AN119	VCL
8	P00/TMRI0/TXD6/SMOSI6/SSDA6/AUDIO_CLK/ IRQ8/AN118	RES#
9	PF5/WAIT#/SSILRCK0/IRQ4	MD/P315
10	EMLE	P312/PIO_060/BACK#-B/RTCIC2/GTETRGD/ GTCPPO15/POEGA/SSL13-B/SSILRCK0/IRQ20/ ADTRG2#/TAMPI2
11	PJ5/POE8#/CTS2#/RTS2#/SS2#/SSIRXD0/ EPLSOUT0	P311/PIO_059/BREQ#-B/RTCIC1/GTETRGC/ GTCPPO14/POEGD/CTS7#-A/SSL12-B/ SSIRXD0/ET0_WOL-C/IRQ19/ADTRG1#/TAMPI1
12	VSS	P310/PIO_058/RTCIC0/CACREF/GTETRGB/ GTCPPO1/POEGC/CTS0#-C/CTS1#-B/SSL11-B/ SSITXD0/IRQ18/ADTRG0#/TAMPI0

144-Pin	RX72N (144-Pin LFQFP)	RX74N (144-Pin LFQFP)
13	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/SS6#/ CTS0#/RTS0#/SS0#/SSITXD0/ET0_EXOUT	VBATT/VCC
14	VCL	XCIN/EXCIN/P309
15	VBATT	XCOUT/P308
16	MD/FINED	VSS
17	XCIN	XTAL/P307
18	XCOUT	EXTAL/P306
19	RES#	VCC
20	XTAL/P37	P305/NMI/IRQ0
21	VSS	VCC_USB
22	EXTAL/P36	PF01/PIO_049/GTCPPO15/USB0_DM/IRQ1
23	VCC	PF00/PIO_048/GTCPPO14/USB0_DP/IRQ0
24	UPSEL/P35/NMI	VSS_USB
25	TRST#/P34/MTIOC0A/TMCI3/PO12/POE10#/ SCK6/SCK0/ET0_LINKSTA/IRQ4	P207/PIO_023/A23-C/CS4#-C/TMRI3/ GTOWLO-D/GTIOC2B/GTIOC6B/RXD1-B/ SMISO1-B/SSCL1-B/MISO1-B/SDAHS2-B/ CRX1-A/USB0_ID/ET0_RXD3-B/PCKO-A/ IRQ3-DS/ADTRG2#
26	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/ POE4#/POE11#/RXD6/SMISO6/SSCL6/RXD0/ SMISO0/SSCL0/CRX0/PCKO/IRQ3-DS	P206/PIO_022/A22-C/CS5#-C/TMO3/RTCOUT/ GTOWUP-D/GTIOC2A/GTIOC6A/CTS6#-A/ TXD1-B/SMOSI1-B/SSDA1-B/TXDA1-B/MOSI1-B/ SCLHS2-B/CTX1-A/USB0_EXICEN/SSITXD1/ ET0_RXD2-B/VSYNC-A/IRQ2-DS/ADTRG1#/ PCOUTZ1
27	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCIC2/ RTCOUT/POE0#/POE10#/TXD6/SMOSI6/ SSDA6/TXD0/SMOSI0/SSDA0/CTX0/ USB0_VBUSEN/VSYNC/IRQ2-DS	CLKOUT/P205/PIO_021/A21-C/CS6#-C/ GTOVLO-D/GTIOC1B/GTIOC5B/SCK1-B/ CTS1#-B/TXDB1-B/RSPCK1-B/SDAHS1-B/ CRX0-A/USB0_VBUS/SSIRXD1/ET0_RXD1-B/ RMII0_RXD1-B/SD0CD-C/HSYNC-A/IRQ5/ ADTRG0#/PCOUTB1
28	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/ RTS1#/SS1#/SSLB0-A/ET1_MDC/PMGI1_MDC/ IRQ1-DS	ETHPHYCLK/P204/PIO_020/A20-C/CS7#-C/ TMRI1/GTOVUP-D/GTIOC1A/GTIOC5A/CTS1#-B/ RTS1#-B/SS1#-B/DE1-B/TXDB1-B/SSL10-B/ SCLHS1-B/CTX0-A/USB0_VBUSEN/SSIBCK1/ ET0_RXD0-B/RMII0_RXD0-B/SD0WP-C/ PIXCLK-A/IRQ12/PCOUTA1
29	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/MISOB-A/ET1_MDIO/ PMGI1_MDIO/IRQ0-DS	VCL
30	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A/ET1_WOL	VSS
31	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A/ ET1_EXOUT	VCC
32	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SSIDATA1/SDHI_CD/HSYNC/ADTRG0#	P203/PIO_019/CS2#-B/BACK#-A/GTOULO-D/ GTIOC0B/GTIOC4B/RXD6-A/SMISO6-A/ SSCL6-A/CTS3#-B/SSL00-C/SDA00-B/CRX2-B/ USB0_OVRCURB/SSIBCK0/ET0_RX_CLK-B/ RMII0_REF50CK-B/SD0DAT1-C/PIXD7-A/IRQ3/ PDMDAT0-B

144-Pin	RX72N (144-Pin LFQFP)	RX74N (144-Pin LFQFP)
33	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/ TMRI1/PO4/SCK3/USB0_VBUSEN/SSIBCK1/ SDHI_WP/PIXCLK	P202/PIO_018/CS3#-B/BREQ#-A/TMO0/ GTOUUP-D/GTIOC0A/GTIOC4A/TXD6-A/ SMOSI6-A/SSDA6-A/TXDA6-A/RSPCK0-C/ SCL00-B/CTX2-B/USB0_OVRCURA/ AUDIO_CLK/ET0_RX_DV-B/RMII0_CRS_DV-B/ SD0DAT0-C/PIXD6-A/IRQ15/PDMCLK0-B
34	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/ GTIOC0A/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/ SS0#/CTX1/SSIBCK0/SDHI_D1-C/PIXD7	ETHPHYCLK/P304/PIO_028/ALE-C/WAIT#-B/ TMCI3/GTETRGD/GTCPPO0/POEGA/CTS0#-A/ CTS1#-A/USB0_VBUSEN/ET0_INT-E/IRQ0-DS/ ADTRG0#
35	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/GTIOC1A/SCK0/USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/PIXD6	TDI/P303/PIO_027/TMCI2/GTCPPO13/RXD0-A/ SMISO0-A/SSCL0-A/RXD1-A/SMISO1-A/ SSCL1-A/MISO1-C/IRQ1
36	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/ GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/PIXD5/ IRQ9	TDO/P302/PIO_026/TMRI3/GTCPPO12/TXD0-A/ SMOSI0-A/SSDA0-A/TXDA0-A/TXD1-A/ SMOSI1-A/SSDA1-A/TXDA1-A/MOSI1-C/IRQ4
37	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMD-C/PIXD4/IRQ8	TCK/SWCLK/P301/PIO_025/TMCI3/GTCPPO11/ SCK0-A/CTS0#-A/TXDB0-A/SCK1-A/CTS1#-A/ TXDB1-A/RSPCK1-C/IRQ7
38	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/SCK1/ TXD3/SMOSI3/SSDA3/SDA2-DS/SSITXD0/ EPLSOUT0/SDHI_D3-C/PIXD3/IRQ7/ADTRG1#	TMS/SWDIO/P300/PIO_024/TMO1/GTCPPO10/ CTS0#-A/RTS0#-A/SS0#-A/DE0-A/TXDB0-A/ CTS1#-A/RTS1#-A/SS1#-A/DE1-A/TXDB1-A/ SSL10-C/ET0_WOL-D/IRQ6
39	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/ SSDA10/TXD10/EPLSOUT1/SDHI_D2-C/PIXD2	P201/PIO_017/TMCI0/GTIW-D/GTIOC3B/ GTIOC14B/SCK6-A/CTS6#-A/TXDB6-A/ MISO0-C/SCLHS1-A/USB0_EXICEN/SSILRCK0/ ET0_RX_ER-B/RMII0_RX_ER-B/SD0CLK-C/ PIXD5-A/IRQ9/PCINZ0
40	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/ PO14/RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/ SMISO3/SSCL3/SCL2-DS/USB0_VBUSEN/ USB0_VBUS/USB0_OVRCURB/IRQ6/ADTRG0#	P200/PIO_016/TMRI0/GTETRGA/GTIOC3A/ GTIOC14A/CTS6#-A/RTS6#-A/SS6#-A/DE6-A/ TXDB6-A/MOSI0-C/SDAHS1-A/USB0_ID/ SSIRXD0/ET0_TX_EN-B/RMII0_TX_EN-B/ SD0CMD-C/PIXD4-A/IRQ8/ADTRG2#/PCINZ1
41	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/ SSCL10/RXD10/PIXD1	P107/PIO_015/TMO1/GTIV-D/GTIOC15B/ POEGA/TXD3-B/SMOSI3-B/SSDA3-B/TXDA3-B/ SDAHS2-A/SSITXD0/ET0_TXD3-B/SD0DAT3-C/ PIXD3-A/IRQ31-DS/ADTRG1#/PCINB1
42	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/ PO13/GTETRGA/RXD1/SMISO1/SSCL1/SCK3/ CRX1-DS/SSILRCK1/PIXD0/IRQ5	CLKOUT/P106/PIO_014/TMO2/RTCOUT/ GTIU-D/GTIOC15A/POEGB/RXD3-B/SMISO3-B/ SSCL3-B/SCLHS2-A/ET0_TXD2-B/SD0DAT2-C/ PIXD2-A/IRQ30-DS/ADTRG0#/PCINA1
43	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/ PO15/GTETRGD/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4	P105/PIO_013/TMCI2/GTIV-E/GTIOC14B/ TXD2-B/SMOSI2-B/SSDA2-B/TXDA2-B/SCK3-B/ CTS3#-B/TXDB3-B/CRX2-A/USB0_VBUS/ SSILRCK1/ET0_TXD1-B/RMII0_TXD1-B/ PIXD1-A/IRQ29-DS/ADST1-A/PCINB0
44	P13/MTIOC0B/TIOCA5/TMO3/PO13/GTADSM1/ TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ ADTRG1#	P104/PIO_012/TMRI2/GTIW-E/GTIOC14A/ RXD2-B/SMISO2-B/SSCL2-B/CTS3#-B/RTS3#-B/ SS3#-B/DE3-B/TXDB3-B/CTX2-A/ USB0_OVRCURA-DS/ET0_TXD0-B/ RMII0_TXD0-B/PIXD0-A/IRQ4/ADST0-A/PCINA0

144-Pin	RX72N (144-Pin LFQFP)	RX74N (144-Pin LFQFP)
45	P12/TMCI1/GTADSM0/RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	VCL
46	VCC_USB	VSS
47	USB0_DM	VCC
48	USB0_DP	P103/PIO_011/TMO3/GTADSM1/GTIOC13B/ CTS2#-B/SDA00-A/ET0_CRS-D/IRQ3
49	VSS_USB	P102/PIO_010/TMCI1/GTADSM0/GTIOC13A/ SCL00-A/ET0_COL-D/IRQ2
50	CLKOUT25M/P56/EDACK1/MTIOC3C/TIOCA1/ SCK7	P101/PIO_009/CS0#-A/ALE-B/TMCI3/GTETRGC/ GTADSM1/GTIOC12B/SCK2-B/CTS2#-B/ TXDB2-B/USB0_VBUS-DS/ET0_TX_CLK-B/ IRQ1/ADTRG1#
51	TRDATA3/P55/D0[A0/D0]/WAIT#/EDREQ0/ MTIOC4D/TMO3/TXD7/SMOSI7/SSDA7/CRX1/ ET0_EXOUT/IRQ10	P100/PIO_008/CS1#-B/WAIT#-A/TMRI3/ CACREF/GTIU-E/GTADSM0/GTIOC12A/ CTS2#-B/RTS2#-B/SS2#-B/DE2-B/TXDB2-B/ CTS5#-B/USB0_OVRCURB-DS/ET0_TX_ER-B/ IRQ0/ADTRG2#
52	TRDATA2/P54/ALE/D1[A1/D1]/EDACK0/ MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1/ ET0_LINKSTA	VCC_DCDC
53	P53*1/BCLK	VCC_DCDC
54	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A	VLO
55	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	VLO
56	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A	VSS_DCDC
57	VSS	VSS_DCDC
58	TRCLK/P83/EDACK1/MTIOC4C/GTIOC0A/ SCK10/SS10#/CTS10#/ET0_CRS/ RMII0_CRS_DV	P803/PIO_059/CS3#-A/WR1#-B/BC1#-B/ GTIOC1B/POEGA/CTS10#-B/RTS10#-B/ SS10#-B/DE10-B/TXDB10-B/CTX2-D/USB0_ID/ ET0_MDC-B/IRQ3/ADSYNC-B
59	VCC	P802/PIO_058/CS2#-A/WR#-B/WR0#-B/GTIW-B/ GTIOC1A/POEGB/SCK10-B/CTS10#-B/ TXDB10-B/CRX2-D/USB0_EXICEN/ ET0_MDIO-B/IRQ2/ADCNV2-B
60	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/ ET0_COL/MMC_D7-A/IRQ14	VCL
61	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/MTCLKA/ TMCI2/PO30/TIC0/GTIOC3B/RXD8/SMISO8/ SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ ET0_ETXD3/MMC_D6-A/IRQ13	VSS
62	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/RTS8#/ SCK10/RSPCKA-A/ET0_ETXD2/MMC_D5-A	VCC
63	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ GTIOC2A/SMOSI10/SSDA10/TXD10/ ET0_ETXD1/RMII0_TXD1/MMC_D4-A	CLKOUT/P801/PIO_057/EBCLK-A/GTIV-B/ GTIOC0B/POEGC/TXD10-B/SMOSI10-B/ SSDA10-B/TXDA10-B/ET0_CRS-B/IRQ9/ ADCNV1-B
64	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ GTIOC0B/SMISO10/SSCL10/RXD10/ ET0_ETXD0/RMII0_TXD0/QIO3-A/SDHI_CD/ MMC_D3-A	P800/PIO_056/CS1#-A/DQM0-B/GTIU-B/ GTIOC0A/POEGD/RXD10-B/SMISO10-B/ SSCL10-B/ET0_COL-B/IRQ8/ADCNV0-B

144-Pin	RX72N (144-Pin LFQFP)	RX74N (144-Pin LFQFP)
65	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/SCK10/ RTS10#/ET0_TX_EN/RMII0_TXD_EN/QIO2-A/ SDHI_WP/MMC_D2-A	ETHPHYCLK/PC07/PIO_031/D0-A/TMO2/TOC0/ CACREF/GTETRGD/GTADSM1/GTIOC15B/ POEGA/TXD8-A/SMOSI8-A/SSDA8-A/TXDA8-A/ MISO0-A/SSITXD0/SD0CD-A/IRQ14/ PDMDAT0-A
66	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/ POE0#/GTETRGC/SCK5/CTS8#/SS8#/SS10#/ CTS10#/RTS10#/SSLA0-A/ET0_TX_CLK/QMI-A/ QIO1-A/SDHI_D1-A/MMC_D1-A	PC06/PIO_030/D1-A/TMCI2/TIC0/GTETRGC/ GTCPPO7/GTIOC15A/POEGB/RXD8-A/ SMISO8-A/SSCL8-A/MOSI0-A/SSILRCK0/ ET0_TX_ER-A/SD0WP-A/IRQ13/PDMCLK0-A
67	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER/QMO-A/ QIO0-A/SDHI_D0-A/MMC_D0-A	PC05/PIO_029/D2-A/TMRI2/GTOWLO-B/ GTIOC9B/SCK8-A/CTS8#-A/TXDB8-A/ RSPCK0-A/SSIBCK0/ET0_TX_EN-A/ RMII0_TX_EN-A/SD0DAT1-A/IRQ5/PCOUTZ1
68	TRDATA7/P77/CS7#/PO23/SMOSI11/SSDA11/ TXD11/ET0_RX_ER/RMII0_RX_ER/QSPCLK-A/ SDHI_CLK-A/MMC_CLK-A	PC04/PIO_028/D3-A/TMCI1/GTOWUP-B/ GTIOC9A/CTS8#-A/RTS8#-A/SS8#-A/DE8-A/ TXDB8-A/CTS11#-A/SSL00-A/AUDIO_CLK/ ET0_TXD3-A/SD0DAT0-A/IRQ12/PCOUTB1
69	TRDATA6/P76/CS6#/PO22/SMISO11/SSCL11/ RXD11/ET0_RX_CLK/REF50CK0/QSSL-A/ SDHI_CMD-A/MMC_CMD-A	PC03/PIO_027/D4-A/GTOVLO-B/GTIOC8B/ TXD11-A/SMOSI11-A/SSDA11-A/TXDA11-A/ SDAHS1-C/ET0_TXD2-A/SD0CLK-A/IRQ11/ PCOUTA1
70	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ET0_RX_DV/ SDHI_D3-A/MMC_CD-A	PC02/PIO_026/D5-A/GTOVUP-B/GTIOC8A/ RXD11-A/SMISO11-A/SSCL11-A/SSL03-A/ SCLHS1-C/ET0_TXD1-A/RMII0_TXD1-A/ SD0CMD-A/IRQ10/PCOUTZ0
71	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/ ET0_ERXD0/RMII0_RXD0/SDHI_D2-A/ MMC_RES#-A	PC01/PIO_025/D6-A/GTOULO-B/GTIOC7B/ SCK11-A/CTS11#-A/TXDB11-A/SSL02-A/ SDA00-C/ET0_TXD0-A/RMII0_TXD0-A/ SD0DAT3-A/IRQ12/PCOUTB0
72	TRDATA5/P74/A20/CS4#/PO19/SS11#/CTS11#/ ET0_ERXD1/RMII0_RXD1	PC00/PIO_024/D7-A/GTOUUP-B/GTIOC7A/ CTS11#-A/RTS11#-A/SS11#-A/DE11-A/ TXDB11-A/SSL01-A/SCL00-C/ET0_TX_CLK-A/ SD0DAT2-A/IRQ14/PCOUTA0
73	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/IRQ12	PB07/PIO_023/D8-A/GTOWLO-A/GTIOC6B/ TXD9-A/SMOSI9-A/SSDA9-A/TXDA9-A/ ET0_LINKSTA-A/IRQ15
74	VCC	PB06/PIO_022/D9-A/GTOWUP-A/GTIOC6A/ RXD9-A/SMISO9-A/SSCL9-A/ET0_RX_ER-A/ RMII0_RX_ER-A/IRQ6
75	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/ SS5#/SSLA1-A/ET0_ERXD3/IRQ14	PB05/PIO_021/D10-A/TMRI1/GTOVLO-A/ GTIOC5B/SCK9-A/CTS9#-A/TXDB9-A/ ET0_RX_DV-A/RMII0_CRS_DV-A/IRQ13
76	VSS	PB04/PIO_020/D11-A/GTOVUP-A/GTIOC5A/ CTS4#-A/CTS9#-A/RTS9#-A/SS9#-A/DE9-A/ TXDB9-A/ET0_RX_CLK-A/RMII0_REF50CK-A/ IRQ4
77	TRDATA4/P73/CS3#/PO16/ET0_WOL	VCC
78	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV	VSS

144-Pin	RX72N (144-Pin LFQFP)	RX74N (144-Pin LFQFP)
79	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1	VCL
80	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/SCK11/ET0_ETXD0/ RMII0_TXD0/LCD_CLK-B	PB03/PIO_019/D12-A/TMO0/GTOULO-A/ GTIOC4B/SCK4-A/CTS4#-A/TXDB4-A/ ET0_RXD3-A/IRQ3
81	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/SS11#/ CTS11#/RTS11#/ET0_TX_EN/RMII0_TXD_EN/ LCD_TCON0-B	PB02/PIO_018/D13-A/GTOUUP-A/GTIOC4A/ CTS4#-A/RTS4#-A/SS4#-A/DE4-A/TXDB4-A/ CTS9#-A/ET0_RXD2-A/IRQ2
82	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK4/SCK6/ET0_RX_ER/ RMII0_RX_ER/LCD_TCON1-B	PB01/PIO_017/D14-A/TMCI0/GTETRGB/ GTCPPO4/GTIOC14B/POEGA/TXD4-A/ SMOSI4-A/SSDA4-A/TXDA4-A/ET0_RXD1-A/ RMII0_RXD1-A/IRQ4-DS/PCINB1
83	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/ SS4#/CTS6#/RTS6#/SS6#/ET0_RX_CLK/ REF50CK0/LCD_TCON2-B	PB00/PIO_016/D15-A/GTETRGA/GTADSM0/ GTIOC14A/POEGC/RXD4-A/SMISO4-A/ SSCL4-A/ET0_RXD0-A/RMII0_RXD0-A/IRQ12/ ADST2-A/PCINA1
84	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/ PO25/TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/ SSDA6/ET0_ERXD0/RMII0_RXD0/ LCD_TCON3-B/IRQ4-DS	ETHPHYCLK/PA07/PIO_015/A0-A/BC0#-A/ DQM1-B/GTIOC3B/GTIOC13B/RXD10-A/ SMISO10-A/SSCL10-A/MISO0-B/IRQ7/PCINB0
85	P72/A19/CS2#/ET0_MDC/PMGI0_MDC	PA06/PIO_014/A1-A/TMCI3/GTIOC3A/ GTIOC13A/TXD10-A/SMOSI10-A/SSDA10-A/ TXDA10-A/MOSI0-B/IRQ14/PCINZ1
86	P71/A18/CS1#/ET0_MDIO/PMGI0_MDIO	PA05/PIO_013/A2-A/GTIOC2B/GTIOC12B/ SCK10-A/CTS10#-A/TXDB10-A/RSPCK0-B/IRQ5/ PCINA0
87	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/ET0_ERXD1/ RMII0_RXD1/LCD_DATA0-B/IRQ12	PA04/PIO_012/A3-A/TMRI0/GTIOC2A/ GTIOC12A/CTS10#-A/RTS10#-A/SS10#-A/ DE10-A/TXDB10-A/SSL00-B/IRQ5-DS/PCINZ0
88	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B	VCC
89	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/RTS5#/SS5#/ MOSIA-B/ET0_EXOUT/LCD_DATA2-B	VSS
90	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/LCD_DATA3-B	VCL
91	VCC	PA03/PIO_011/A4-A/GTIOC1B/GTIOC11B/ RXD5-A/SMISO5-A/SSCL5-A/IRQ6-DS/ ADSYNC-A
92	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/ TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC/ PMGI0_MDC/LCD_DATA4-B/IRQ5-DS	PA02/PIO_010/A5-A/GTIW-A/GTIOC1A/ GTIOC11A/TXD5-A/SMOSI5-A/SSDA5-A/ TXDA5-A/SSL03-B/IRQ10/ADCNV2-A
93	VSS	PA01/PIO_009/A6-A/GTIV-A/GTIOC0B/ GTIOC10B/SCK5-A/CTS5#-A/TXDB5-A/SSL02-B/ IRQ11/ADCNV1-A
94	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/ PMGI0_MDIO/LCD_DATA5-B/IRQ6-DS	ETHPHYCLK/PA00/PIO_008/A7-A/CACREF/ GTIU-A/GTIOC0A/GTIOC10A/CTS10#-A/ CTS5#-A/RTS5#-A/SS5#-A/DE5-A/TXDB5-A/ SSL01-B/IRQ1-DS/ADCNV0-A

144-Pin	RX72N (144-Pin LFQFP)	RX74N (144-Pin LFQFP)
95	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B	P702/PIO_050/RD#-A/GTETRGA/GTIOC11A/ SCK4-B/CTS4#-B/TXDB4-B/XSPI1_WP0#-B/ XSPI1_RESET1#-C/HSYNC-C/IRQ10/ADST2-B
96	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/ PO17/GTIOC2A/SCK5/SSLA2-B/ET0_WOL/ LCD_DATA7-B/IRQ11	P701/PIO_049/CKE-A/GTIOC10B/RXD4-B/ SMISO4-B/SSCL4-B/XSPI1_RSTO0#-B/ XSPI1_RESET0#-B/VSYNC-C/IRQ1/ADST1-B
97	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/ PO16/CACREF/GTIOC0B/SSLA1-B/ET0_TX_EN/ RMII0_TXD_EN/LCD_DATA8-B	ETHPHYCLK/P700/PIO_048/SDCLK-A/ GTIOC10A/TXD4-B/SMOSI4-B/SSDA4-B/ TXDA4-B/XSPI1_INT0#-B/XSPI1_ECS0#-B/ PIXCLK-C/IRQ0/ADST0-B
98	P67/DQM1/CS7#/MTIOC7C/GTIOC1B/CRX2/ EPLSOUT1/IRQ15	VCC
99	P66/DQM0/CS6#/MTIOC7D/GTIOC2B/CTX2	VSS
100	P65/CKE/CS5#	VCL
101	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105	PE07/PIO_047/A8-B/A20-C/TOC1/GTETRGD/ GTCPPO7/GTIOC10B/POEGD/XSPI1_CS0#-A/ PIXD7-C/IRQ7
102	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/AN104	PE06/PIO_046/A9-B/A21-C/TIC1/GTETRGC/ GTADSM1/GTIOC10A/POEGB/SSL13-A/ XSPI1_DS-A/PIXD6-C/IRQ6
103	VCC	PE05/PIO_045/A10-B/A22-C/GTOWLO-C/ GTIOC9B/SSL12-A/XSPI1_IO3-A/PIXD5-C/IRQ5
104	P70/SDCLK	PE04/PIO_044/A11-B/A23-C/GTOWUP-C/ GTIOC9A/CTS12#-A/SSL11-A/XSPI1_IO2-A/ XSPI1_WP0#-C/PIXD4-C/IRQ12
105	VSS	PE03/PIO_043/A12-B/TOC3/GTOVLO-C/ GTIOC8B/CTS12#-A/RTS12#-A/SS12#-A/ DE12-A/TXDB12-A/MISO1-A/SD0DAT7-B/ XSPI1_IO1-A/PIXD3-C/IRQ11
106	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ET0_RX_CLK/ REF50CK0/LCD_DATA11-B/IRQ5/AN103	PE02/PIO_042/A13-B/TIC3/GTOVUP-C/ GTIOC8A/RXD12-A/SMISO12-A/SSCL12-A/ MOSI1-A/SD0DAT6-B/XSPI1_IO0-A/PIXD2-C/ IRQ7-DS
107	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/LCD_DATA12-B/AN102	CLKOUT/PE01/PIO_041/A14-B/GTOULO-C/ GTIOC7B/TXD12-A/SMOSI12-A/SSDA12-A/ TXDA12-A/RSPCK1-A/SD0DAT5-B/XSPI1_CK-A/ PIXD1-C/IRQ9
108	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/CTS12#/RTS12#/SS12#/ ET0_ERXD3/MMC_D7-B/LCD_DATA13-B/AN101	ETHPHYCLK/PE00/PIO_040/A15-B/GTOUUP-C/ GTIOC7A/SCK12-A/CTS12#-A/TXDB12-A/ SSL10-A/SD0DAT4-B/XSPI1_CKN#-A/ XSPI1_CS1#-B/PIXD0-C/IRQ8
109	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/PO23/ TIC3/GTIOC0B/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/MMC_D6-B/LCD_DATA14-B/ IRQ7-DS/AN100	P605/PIO_013/CS2#-C/GTIOC6B/RXD9-B/ SMISO9-B/SSCL9-B/SSL02-D/XSPI0_INT0#-A/ XSPI0_ECS0#-A/IRQ13
110	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/MTIOC3B/ PO18/GTIOC1B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1	P604/PIO_012/CS3#-C/GTIOC6A/TXD9-B/ SMOSI9-B/SSDA9-B/TXDA9-B/SSL01-D/ XSPI0_CS1#-A/XSPI0_RSTO0#-B/IRQ4
111	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/GTIOC2B/ SCK12/SSLB1-B/MMC_D4-B/LCD_DATA16-B/ ANEX0	P603/PIO_011/WE#-B/GTIOC5B/CTS8#-B/ RTS8#-B/SS8#-B/DE8-B/TXDB8-B/CTS9#-B/ MISO0-D/XSPI0_IO7-A/PCKO-B/IRQ3

144-Pin	RX72N (144-Pin LFQFP)	RX74N (144-Pin LFQFP)
112	P64/WE#/D3[A3/D3]/CS4#/RMII1_TXD0	P602/PIO_010/CAS#-B/GTIOC5A/SCK8-B/ CTS8#-B/TXDB8-B/MOSI0-D/XSPI0_IO6-A/ HSYNC-B/IRQ2/ADTRG2#
113	P63/CAS#/D2[A2/D2]/CS3#/RMII1_TXD1	P601/PIO_009/RAS#-B/GTIOC4B/RXD8-B/ SMISO8-B/SSCL8-B/RSPCK0-D/ GPTP_PTPOUT1/XSPI0_IO5-A/VSYNC-B/IRQ1/ ADTRG1#
114	P62/RAS#/D1[A1/D1]/CS2#/RMII1_RXD0	P600/PIO_008/SDCS#-B/GTIOC4A/TXD8-B/ SMOSI8-B/SSDA8-B/TXDA8-B/SSL00-D/ GPTP_PTPOUT0/XSPI0_IO4-A/PIXCLK-B/IRQ0/ ADTRG0#
115	P61/SDCS#/D0[A0/D0]/CS1#/RMII1_RXD1	VCC2
116	VSS	VSS
117	P60/CS0#/RMII1_TXD_EN	PD07/PIO_039/A16-B/GTIW-C/GTIOC3B/ POEGA/TXD3-A/SMOSI3-A/SSDA3-A/TXDA3-A/ CTX1-B/SD0CD-B/XSPI0_CS0#-A/ XSPI0_RESET1#-B/PIXD7-B/IRQ7/AN031
118	VCC	PD06/PIO_038/A17-B/GTIV-C/GTIOC3A/POEGB/ RXD3-A/SMISO3-A/SSCL3-A/SSL23-A/CRX1-B/ SD0WP-B/XSPI0_DS-A/PIXD6-B/IRQ6/AN030
119	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ RMII1_RX_ER/QMI-B/QIO1-B/SDHI_D1-B/ MMC_D1-B/LCD_DATA17-B/IRQ7/AN107	PD05/PIO_037/A18-B/GTIU-C/GTIOC2B/POEGD/ SCK3-A/CTS3#-A/TXDB3-A/SSL22-A/CTX0-B/ SD0DAT1-B/XSPI0_IO3-A/PIXD5-B/IRQ5/AN029
120	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/REF50CK1/QMO-B/QIO0-B/ SDHI_D0-B/MMC_D0-B/LCD_DATA18-B/IRQ6/ AN106	PD04/PIO_036/A19-B/GTETRGA/GTIOC2A/ POEGC/CTS2#-A/CTS3#-A/RTS3#-A/SS3#-A/ DE3-A/TXDB3-A/SSL21-A/CRX0-B/SD0DAT0-B/ XSPI0_IO2-A/XSPI0_WP0#-B/PIXD4-B/IRQ4/ AN028
121	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/MTCLKA/ POE10#/SSLC1-A/ET1_MDC/PMGI1_MDC/ QSPCLK-B/SDHI_CLK-B/MMC_CLK-B/ LCD_DATA19-B/IRQ5/AN113	PD03/PIO_035/A20-B/TOC2/GTIOC1B/POEGA/ TXD2-A/SMOSI2-A/SSDA2-A/TXDA2-A/MISO2-A/ SD0CLK-B/XSPI0_IO1-A/PIXD3-B/IRQ3/AN027
122	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0-A/ ET1_MDIO/PMGI1_MDIO/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112	PD02/PIO_034/A21-B/TIC2/GTETRGB/GTIOC1A/ POEGB/RXD2-A/SMISO2-A/SSCL2-A/MOSI2-A/ SD0CMD-B/XSPI0_IO0-A/PIXD2-B/IRQ2/AN026
123	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/ET1_WOL/QIO3-B/ SDHI_D3-B/MMC_D3-B/LCD_DATA21-B/IRQ3/ AN111	PD01/PIO_033/A22-B/GTETRGC/GTIOC0B/ POEGC/SCK2-A/CTS2#-A/TXDB2-A/RSPCK2-A/ SD0DAT3-B/XSPI0_CK-A/PIXD1-B/IRQ1/AN025
124	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/ET1_EXOUT/QIO2-B/ SDHI_D2-B/MMC_D2-B/LCD_DATA22-B/IRQ2/ AN110	PD00/PIO_032/A23-B/GTETRGD/GTIOC0A/ POEGD/CTS2#-A/RTS2#-A/SS2#-A/DE2-A/ TXDB2-A/CTS3#-A/SSL20-A/SD0DAT2-B/ XSPI0_CKN#-A/XSPI0_CS1#-B/PIXD0-B/IRQ0/ AN024
125	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/AN109	VSS
126	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108	VCL
127	P93/A19/POE0#/CTS7#/RTS7#/SS7#/ ET1_LINKSTA/AN117	P901/PIO_001/GTETRGB/GTCPPO6/TXD1-C/ SMOSI1-C/SSDA1-C/TXDA1-C/ XSPI0_RSTO1#-A/XSPI0_RESET0#-B/IRQ9/ AN033

144-Pin	RX72N (144-Pin LFQFP)	RX74N (144-Pin LFQFP)
128	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ RMII1_CRS_DV/AN116	P900/PIO_000/GTETRGA/GTCPPO5/RXD1-C/ SMISO1-C/SSCL1-C/XSPI0_INT1#-A/ XSPI0_ECS1#-A/IRQ0/AN032
129	P91/A17/SCK7/AN115	AVCC0
130	VSS	AVSS0
131	P90/A16/TXD7/SMOSI7/SSDA7/AN114	VREFL0
132	VCC	VREFH0
133	P47/IRQ15-DS/AN007	P405/PIO_053/IRQ13-DS/AN005
134	P46/IRQ14-DS/AN006	P404/PIO_052/IRQ12-DS/AN004
135	P45/IRQ13-DS/AN005	P403/PIO_051/IRQ11-DS/AN003
136	P44/IRQ12-DS/AN004	P402/PIO_050/IRQ10-DS/AN002
137	P43/IRQ11-DS/AN003	P401/PIO_049/IRQ9-DS/AN001
138	P42/IRQ10-DS/AN002	P400/PIO_048/IRQ8-DS/AN000
139	P41/IRQ9-DS/AN001	P415/PIO_063/IRQ31/AN015/DA1
140	VREFL0	P414/PIO_062/IRQ30/AN014/DA0
141	P40/IRQ8-DS/AN000	P007/PIO_007/GTCPPO6/GTIOC13B/POEGA/ CTS0#-B/RTS0#-B/SS0#-B/DE0-B/TXDB0-B/ IRQ23-DS/ADTRG0#/AN023/PDMDAT0-C
142	VREFH0	P006/PIO_006/GTCPPO5/GTIOC13A/GTIOC9B/ SCK0-B/CTS0#-B/TXDB0-B/IRQ22-DS/ ADTRG1#/AN022/PDMCLK0-C/PCOUTZ1
143	AVCC0	P005/PIO_005/GTCPPO4/GTIOC12B/GTIOC9A/ RXD0-B/SMISO0-B/SSCL0-B/SSILRCK1/ IRQ21-DS/ADTRG2#/AN021/PCOUTB1
144	P07/IRQ15/ADTRG0#	P004/PIO_004/GTCPPO3/GTIOC12A/GTIOC8B/ TXD0-B/SMOSI0-B/SSDA0-B/TXDA0-B/ SSITXD1/IRQ20-DS/AN020/PCOUTA1

3.5 100-Pin Package

Table 3.9 is Comparative Listing of RX72M/RX74M 100-Pin Package Pin Functions, and Table 3.10 is Comparative Listing of RX72N/RX74N 100-Pin Package Pin Functions.

Table 3.9 Comparative Listing of RX72M/RX74M 100-Pin Package Pin Functions

100-Pin LFQFP	RX72M	RX74M
1	AVSS0	P003/PIO_003/GTCPPO2/GTIOC11B/ GTIOC8A/RXD7-A/SMISO7-A/SSCL7-A/ SSIRXD1/ET0_MDIO-D/CAT0_MDIO-E/ IRQ19-DS/AN019/DSMDAT1-B/PCOUTB0
2	AVCC1	P002/PIO_002/TMCI1/GTCPPO1/GTIOC11A/ GTIOC7B/TXD7-A/SMOSI7-A/SSDA7-A/ TXDA7-A/SSIBCK1/ET0_MDC-D/ CAT0_MDC-E/IRQ18-DS/AN018/DSMCLK1-B/ PCOUTA0
3	AVSS1	P001/PIO_001/TMCI0/GTCPPO0/GTIOC10B/ GTIOC7A/SCK7-A/CTS7#-A/TXDB7-A/ SSIBCK0/ET0_LINKSTA-D/CAT0_LINKSTA-E/ IRQ17-DS/AN017/DSMDAT0-B/PCOUTZ0
4	P00/TMRI0/TXD6/SMOSI6/SSDA6/ AUDIO_CLK/CATLATCH1/IRQ8/AN118	VSS
5	EMLE	VCL
6	VCL	RES#
7	VBATT	MD/P315
8	MD/FINED	P312/PIO_060/RTCIC2/GTETRGD/GTCPPO15/ POEGA/SSL13-B/SSILRCK0/ET1_WOL-C/ IRQ20/ADTRG2#/DSMDAT2-C/TAMPI2
9	XCIN	P311/PIO_059/RTCIC1/GTETRGC/GTCPPO14/ POEGD/CTS7#-A/SSL12-B/SSIRXD0/ ET0_WOL-C/IRQ19/ADTRG1#/DSMCLK2-C/TAMPI1
10	XCOUT	P310/PIO_058/RTCIC0/CACREF/GTETRGB/ GTCPPO1/POEGC/CTS0#-C/CTS1#-B/ SSL11-B/SSITXD0/ET1_INT-E/CATIRQ-D/ IRQ18/ADTRG0#/TAMPI0
11	RES#	VBATT/VCC
12	XTAL/P37	XCIN/EXCIN/P309
13	VSS	XCOUT/P308
14	EXTAL/P36	VSS
15	VCC	XTAL/P307
16	UPSEL/P35/NMI	EXTAL/P306
17	TRST#/P34/MTIOC0A/TMCI3/PO12/POE10#/ SCK6/SCK0/ET0_LINKSTA/CAT0_LINKSTA/ IRQ4	VCC
18	P33/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/ POE11#/RXD6/SMISO6/SSCL6/RXD0/SMISO0/ SSCL0/CRX0/IRQ3_DS	P305/NMI/IRQ0
19	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCIC2/ RTCOUT/POE0#/POE10#/TXD6/SMOSI6/ SSDA6/TXD0/SMOSI0/SSDA0/CTX0/ USB0_VBUSEN/IRQ2_DS	VCC_USB
20	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0A/ET1_MDC/ PMGI1_MDC/IRQ1_DS	PF01/PIO_049/GTCPPO15/USB0_DM/IRQ1
21	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/MISOB-A/ ET1_MDIO/PMGI1_MDIO/IRQ0_DS	PF00/PIO_048/GTCPPO14/USB0_DP/IRQ0

100-Pin LFQFP	RX72M	RX74M
22	TCK/P27/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A/ET1_WOL/CATIRQ	VSS_USB
23	TDO/P26/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/ SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A/ ET1_EXOUT/CATLINKACT1	ETHPHYCLK/P304/PIO_028/TMCI3/GTETRGD/ GTCPPO0/POEGA/CTS0#-A/CTS1#-A/ USB0_VBUSEN/ET0_INT-E/CATRESTOUT-D/ IRQ0-DS/ADTRG0#
24	CLKOUT/P25/MTIOC4C/MTCLKB/TIOCA4/ PO5/RXD3/SMISO3/SSCL3/SSIDATA1/ ADTRG0#	TDI/P303/PIO_027/TMCI2/GTCPPO13/RXD0-A/ SMISO0-A/SSCL0-A/RXD1-A/SMISO1-A/ SSCL1-A/MISO1-C/ET1_CRS-D/IRQ1
25	P24/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/ SCK3/USB0_VBUSEN/SSIBCK1	TDO/P302/PIO_026/TMRI3/GTCPPO12/ TXD0-A/SMOSI0-A/SSDA0-A/TXDA0-A/ TXD1-A/SMOSI1-A/SSDA1-A/TXDA1-A/ MOSI1-C/ET1_COL-D/IRQ4
26	P23/MTIOC3D/MTCLKD/TIOCD3/PO3/ GTIOC0A/TXD3/SMOSI3/SSDA3/CTS0#/ RTS0#/SS0#/CTX1/SSIBCK0	TCK/SWCLK/P301/PIO_025/TMCI3/ GTCPPO11/SCK0-A/CTS0#-A/TXDB0-A/ SCK1-A/CTS1#-A/TXDB1-A/RSPCK1-C/ ET1_WOL-D/IRQ7
27	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/ GTIOC2A/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/IRQ9	TMS/SWDIO/P300/PIO_024/TMO1/GTCPPO10/ CTS0#-A/RTS0#-A/SS0#-A/DE0-A/TXDB0-A/ CTS1#-A/RTS1#-A/SS1#-A/DE1-A/TXDB1-A/ SSL10-C/ET0_WOL-D/IRQ6
28	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ IRQ8	P201/PIO_017/TMCI0/GTIW-D/GTIOC3B/ GTIOC14B/MISO0-C/SCLHS1-A/ USB0_EXICEN/SSILRCK0/ET0_RX_ER-B/ RMII0_RX_ER-B/CAT0_RX_ER-B/SD0CLK-C/ IRQ9/PCINZ0
29	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/SCK1/ TXD3/SMOSI3/SSDA3/SDA2_DS/SSITXD0/ EPLSOUT0/CATSYNC0/IRQ7/ADTRG1#	P200/PIO_016/TMRI0/GTETRGA/GTIOC3A/ GTIOC14A/MOSI0-C/SDAHS1-A/USB0_ID/ SSIRXD0/ET0_TX_EN-B/RMII0_TX_EN-B/ CAT0_TX_EN-B/SD0CMD-C/IRQ8/ADTRG2#/ PCINZ1
30	P87/MTIOC4C/TIOCA2/GTIOC1B/SMOSI10/ SSDA10/TXD10/EPLSOUT1/CATSYNC1	P107/PIO_015/TMO1/GTIV-D/GTIOC15B/ POEGA/TXD3-B/SMOSI3-B/SSDA3-B/ TXDA3-B/SDAHS2-A/SSITXD0/ET0_TXD3-B/ CAT0_ETXD3-B/CATI2CDATA-B/SD0DAT3-C/ IRQ31-DS/ADTRG1#/PCINB1
31	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/SMOSI1/SSDA1/ RXD3/SMISO3/SSCL3/SCL2_DS/ USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#	CLKOUT/P106/PIO_014/TMO2/RTCOUT/ GTIU-D/GTIOC15A/POEGB/RXD3-B/ SMISO3-B/SSCL3-B/SCLHS2-A/ET0_TXD2-B/ CAT0_ETXD2-B/CATI2CCLK-B/SD0DAT2-C/ IRQ30-DS/ADTRG0#/PCINA1
32	P86/MTIOC4D/TIOCA0/GTIOC2B/SMISO10/ SSCL10/RXD10/CATLINKACT0	P105/PIO_013/TMCI2/GTIV-E/GTIOC14B/ TXD2-B/SMOSI2-B/SSDA2-B/TXDA2-B/SCK3-B/ CTS3#-B/TXDB3-B/CRX2-A/USB0_VBUS/ SSILRCK1/ET0_TXD1-B/RMII0_TXD1-B/ CAT0_ETXD1-B/CATLEDRUN-C/IRQ29-DS/ ADST1-A/DSMDAT1-C/PCINB0
33	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/GTETRGA/RXD1/SMISO1/ SSCL1/SCK3/CRX1_DS/SSILRCK1/ CATLEDRUN/IRQ5	P104/PIO_012/TMRI2/GTIW-E/GTIOC14A/ RXD2-B/SMISO2-B/SSCL2-B/CTS3#-B/ RTS3#-B/SS3#-B/DE3-B/TXDB3-B/CTX2-A/ USB0_OVRCURA-DS/ET0_TXD0-B/ RMII0_TXD0-B/CAT0_ETXD0-B/ CATLEDSTER-C/IRQ4/ADST0-A/DSMCLK1-C/ PCINA0
34	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/GTETRGD/CTS1#/RTS1#/SS1#/ CTX1/USB0_OVRCURA/IRQ4	VCL
35	VCC_USB	VSS
36	USB0_DM	VCC

100-Pin LFQFP	RX72M	RX74M
37	USB0_DP	P103/PIO_011/TMO3/GTADSM1/GTIOC13B/CTS2#-B/SDA00-A/ET0_CRS-D/CATI2CDATA-A/IRQ3
38	VSS_USB	P102/PIO_010/TMCI1/GTADSM0/GTIOC13A/SCL00-A/ET0_COL-D/CATI2CCLK-A/IRQ2
39	CLKOUT25M/P56/MTIOC3C/TIOCA1/SCK7	P101/PIO_009/TMCI3/GTETRGC/GTADSM1/GTIOC12B/SCK2-B/CTS2#-B/TXDB2-B/USB0_VBUS-DS/ET0_TX_CLK-B/CAT0_TX_CLK-B/CAT0_LINKSTA-D/IRQ1/ADTRG1#/DSMDAT0-C
40	P51/SCK2/SSLB2-A	VCC_DCDC
41	P52/RXD2/SMISO2/SSCL2/SSLB3-A/CATLEDSTER	VLO
42	P50/TXD2/SMOSI2/SSDA2/SSLB1-A/CATLEDERR	VSS_DCDC
43	VSS	VSS
44	VCC	PC06/PIO_030/TMCI2/GTETRGC/GTCPPO7/GTIOC15A/POEGB/RXD8-A/SMISO8-A/SSCL8-A/MOSI0-A/SSILRCK0/ET0_TX_ER-A/CATLINKACT0-A/SD0WP-A/IRQ13/PDMCLK0-A
45	UB/PC7/MTIOC3A/MTCLKB/TMO2/PO31/CACREF/GTIOC3A/TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/TXD10/ET0_COL/IRQ14	PC05/PIO_029/TMRI2/GTOWLO-B/GTIOC9B/SCK8-A/CTS8#-A/TXDB8-A/RSPCK0-A/SSIBCK0/ET0_TX_EN-A/RMII0_TX_EN-A/CAT0_TX_EN-A/SD0DAT1-A/IRQ5/PCOUTZ1
46	PC6/MTIOC3C/MTCLKA/TMCI2/PO30/GTIOC3B/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/ET0_ETXD3/CAT0_ETXD3/CATLATCH1/IRQ13	PC04/PIO_028/TMCI1/GTOWUP-B/GTIOC9A/CTS8#-A/RTS8#-A/SS8#-A/DE8-A/TXDB8-A/CTS11#-A/SSL00-A/AUDIO_CLK/ET0_TXD3-A/CAT0_ETXD3-A/SD0DAT0-A/IRQ12/PCOUTB1
47	PC5/MTIOC3B/MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/RTS8#/SCK10/ET0_ETXD2/CAT0_ETXD2	PC03/PIO_027/GTOVLO-B/GTIOC8B/TXD11-A/SMOSI11-A/SSDA11-A/TXDA11-A/SDAHS1-C/ET0_TXD2-A/CAT0_ETXD2-A/SD0CLK-A/IRQ11/PCOUTA1
48	P82/MTIOC4A/PO28/GTIOC2A/SMOSI10/SSDA10/TXD10/ET0_ETXD1/RMII0_TXD1/CAT0_ETXD1/CATI2CDATA	PC02/PIO_026/GTOVUP-B/GTIOC8A/RXD11-A/SMISO11-A/SSCL11-A/SSL03-A/SCLHS1-C/ET0_TXD1-A/RMII0_TXD1-A/CAT0_ETXD1-A/SD0CMD-A/IRQ10/PCOUTZ0
49	P81/MTIOC3D/PO27/GTIOC0B/SMISO10/SSCL10/RXD10/ET0_ETXD0/RMII0_TXD0/CAT0_ETXD0/CATI2CCLK	PC01/PIO_025/GTOULO-B/GTIOC7B/SCK11-A/CTS11#-A/TXDB11-A/SSL02-A/SDA00-C/ET0_TXD0-A/RMII0_TXD0-A/CAT0_ETXD0-A/SD0DAT3-A/IRQ12/PCOUTB0
50	P80/MTIOC3B/PO26/SCK10/RTS10#/ET0_TX_EN/RMII0_TXD_EN/CAT0_TX_EN/CATLATCH0	PC00/PIO_024/GTOUUP-B/GTIOC7A/CTS11#-A/RTS11#-A/SS11#-A/DE11-A/TXDB11-A/SSL01-A/SCL00-C/ET0_TX_CLK-A/CAT0_TX_CLK-A/SD0DAT2-A/IRQ14/PCOUTA0
51	PC4/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/GTETRGC/SCK5/SS8#/CTS8#/SS10#/CTS10#/RTS10#/ET0_TX_CLK/CAT0_TX_CLK/CATSYNC0	PB06/PIO_022/GTOWUP-A/GTIOC6A/ET0_RX_ER-A/RMII0_RX_ER-A/CAT0_RX_ER-A/IRQ6
52	PC2/MTIOC4B/TCLKA/PO21/GTIOC2B/RXD5/SMISO5/SSCL5/ET0_RX_DV/CAT0_RX_DV	PB05/PIO_021/TMRI1/GTOVLO-A/GTIOC5B/ET0_RX_DV-A/RMII0_CRS_DV-A/CAT0_RX_DV-A/IRQ13
53	PB7/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ET0_CRS/RMII0_CRS_DV/CAT0_RX_DV	PB04/PIO_020/GTOVUP-A/GTIOC5A/CTS4#-A/ET0_RX_CLK-A/RMII0_REF50CK-A/CAT0_RX_CLK-A/IRQ4

100-Pin LFQFP	RX72M	RX74M
54	PB6/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/ SSCL9/SMISO11/SSCL11/RXD11/ET0_ETXD1/ RMII0_TXD1/CAT0_ETXD1	PB03/PIO_019/TMO0/GTOULO-A/ GTIOC4B/SCK4-A/CTS4#-A/TXDB4-A/ ET0_RXD3-A/CAT0_ERXD3-A/IRQ3
55	PB5/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/ POE4#/SCK9/RTS9#/SCK11/ET0_ETXD0/ RMII0_TXD0/CAT0_ETXD0	PB02/PIO_018/GTOUUP-A/GTIOC4A/CTS4#-A/ RTS4#-A/SS4#-A/DE4-A/TXDB4-A/ ET0_RXD2-A/CAT0_ERXD2-A/IRQ2
56	PB4/TIOCA4/PO28/SS9#/CTS9#/SS11#/ CTS11#/RTS11#/ET0_TX_EN/RMII0_TXD_EN/ CAT0_TX_EN	PB01/PIO_017/TMCI0/GTETRGB/GTCPPO4/ GTIOC14B/POEGA/TXD4-A/SMOSI4-A/ SSDA4-A/TXDA4-A/ET0_RXD1-A/ RMII0_RXD1-A/CAT0_ERXD1-A/IRQ4-DS/ DSMDAT2-A/PCINB1
57	PB3/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK4/SCK6/ ET0_RX_ER/RMII0_RX_ER/CAT0_RX_ER	PB00/PIO_016/GTETRGA/GTADSM0/ GTIOC14A/POEGC/RXD4-A/SMISO4-A/ SSCL4-A/ET0_RXD0-A/RMII0_RXD0-A/ CAT0_ERXD0-A/IRQ12/ADST2-A/DSMCLK2-A/ PCINA1
58	PB1/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/ PO25/TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/ SSDA6/ET0_ERXD0/RMII0_RXD0/ CAT0_ERXD0/IRQ4_DS	ETHPHYCLK/PA07/PIO_015/GTIOC3B/ GTIOC13B/RXD10-A/SMISO10-A/SSCL10-A/ MISO0-B/ET1_TX_ER-A/CATLINKACT1-A/ IRQ7/PCINB0
59	PB0/MTIC5W/TIOCA3/PO24/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/ET0_ERXD1/ RMII0_RXD1/CAT0_ERXD1/IRQ12	PA06/PIO_014/TMCI3/GTIOC3A/GTIOC13A/ TXD10-A/SMOSI10-A/SSDA10-A/TXDA10-A/ MOSI0-B/ET1_TXD3-A/CAT1_ETXD3-A/IRQ14/ PCINZ1
60	PA6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/RTS5#/SS5#/ ET0_EXOUT/CATRESTOUT	PA05/PIO_013/GTIOC2B/GTIOC12B/SCK10-A/ CTS10#-A/TXDB10-A/RSPCK0-B/ET1_TXD2-A/ CAT1_ETXD2-A/IRQ5/PCINA0
61	VCC	PA04/PIO_012/TMRI0/GTIOC2A/GTIOC12A/ CTS10#-A/RTS10#-A/SS10#-A/DE10-A/ TXDB10-A/SSL00-B/ET1_TXD1-A/ RMII1_TXD1-A/CAT1_ETXD1-A/IRQ5-DS/ PCINZ0
62	PA4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/ TXD5/SMOSI5/SSDA5/ET0_MDC/CAT0_MDC/ CATIRQ/PMGI0_MDC/IRQ5_DS	VCC
63	VSS	VSS
64	PA3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/ RXD5/SMISO5/SSCL5/ET0_MDIO/ CAT0_MDIO/PMGI0_MDIO/IRQ6_DS	VCL
65	PA2/MTIOC7A/PO18/GTIOC1A/RXD5/SMISO5/ SSCL5/CATLINKACT1	PA03/PIO_011/GTIOC1B/GTIOC11B/ RXD5-A/SMISO5-A/SSCL5-A/ET1_TXD0-A/ RMII1_TXD0-A/CAT1_ETXD0-A/IRQ6-DS/ ADSYNC-A/DSMDAT1-A
66	PG6/ET1_ETXD3/CAT1_ETXD3	PA02/PIO_010/GTIW-A/GTIOC1A/GTIOC11A/ TXD5-A/SMOSI5-A/SSDA5-A/TXDA5-A/ SSL03-B/ET1_TX_CLK-A/CAT1_TX_CLK-A/ IRQ10/ADCNV2-A/DSMCLK1-A
67	PA1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/ PO17/GTIOC2A/SCK5/ET0_WOL/IRQ11	PA01/PIO_009/GTIV-A/ GTIOC0B/GTIOC10B/SCK5-A/CTS5#-A/ TXDB5-A/SSL02-B/ET1_TX_EN-A/ RMII1_TX_EN-A/CAT1_TX_EN-A/IRQ11/ ADCNV1-A/DSMDAT0-A
68	PG5/ET1_ETXD2/CAT1_ETXD2	ETHPHYCLK/PA00/PIO_008/CACREF/ GTIU-A/GTIOC0A/GTIOC10A/CTS10#-A/ CTS5#-A/RTS5#-A/SS5#-A/DE5-A/TXDB5-A/ SSL01-B/CATIRQ-A/IRQ1-DS/ADCNV0-A/ DSMCLK0-A

100-Pin LFQFP	RX72M	RX74M
69	PA0/MTIOC4A/MTIOC6D/TIOCA0/PO16/ CACREF/GTIOC0B/ET0_TX_EN/ RMII0_TXD_EN/CAT0_TX_EN/CATLEDRUN	PE06/PIO_046/GTETRGC/GTADSM1/ GTIOC10A/POEGB/SSL13-A/ET1_RX_CLK-D/ RMII1_REF50CK-D/CAT1_RX_CLK-D/ CATLEDERR-B/XSPI1_DS-A/IRQ6
70	P67/MTIOC7C/GTIOC1B/CRX2/EPLSOUT1/ CATSYNC1/IRQ15	PE05/PIO_045/GTOWLO-C/GTIOC9B/ SSL12-A/ET1_RXD3-D/CAT1_ERXD3-D/ CATLEDRUN-B/XSPI1_IO3-A/IRQ5
71	P66/MTIOC7D/GTIOC2B/CTX2	PE04/PIO_044/GTOWUP-C/GTIOC9A/ CTS12#-A/SSL11-A/ET1_RXD2-D/ CAT1_ERXD2-D/CATLEDSTER-B/ XSPI1_IO2-A/XSPI1_WP0#-C/IRQ12
72	PG2/ET1_TX_CLK/CAT1_TX_CLK	PE03/PIO_043/TOC3/GTOVLO-C/GTIOC8B/ CTS12#-A/RTS12#-A/SS12#-A/DE12-A/ TXDB12-A/MISO1-A/ET1_RXD1-D/ RMII1_RXD1-D/CAT1_ERXD1-D/SD0DAT7-B/ XSPI1_IO1-A/IRQ11
73	PE5/MTIOC4C/MTIOC2B/GTIOC0A/ ET0_RX_CLK/REF50CK0/CAT0_RX_CLK/ IRQ5/AN103	PE02/PIO_042/TIC3/GTOVUP-C/GTIOC8A/ RXD12-A/SMISO12-A/SSCL12-A/MOSI1-A/ ET1_RXD0-D/RMII1_RXD0-D/CAT1_ERXD0-D/ SD0DAT6-B/XSPI1_IO0-A/IRQ7-DS
74	PE4/MTIOC4D/MTIOC1A/PO28/GTIOC1A/ ET0_ERXD2/CAT0_ERXD2/AN102	CLKOUT/PE01/PIO_041/GTOULO-C/GTIOC7B/ TXD12-A/SMOSI12-A/SSDA12-A/TXDA12-A/ RSPCK1-A/ET1_RX_DV-D/RMII1_CRS_DV-D/ CAT1_RX_DV-D/SD0DAT5-B/XSPI1_CK-A/ IRQ9
75	PE3/MTIOC4B/PO26/POE8#/GTIOC2A/ ET0_ERXD3/CAT0_ERXD3/AN101	ETHPHYCLK/PE00/PIO_040/GTOUUP-C/ GTIOC7A/SCK12-A/CTS12#-A/TXDB12-A/ SSL10-A/ET1_RX_ER-D/RMII1_RX_ER-D/ CAT1_RX_ER-D/SD0DAT4-B/XSPI1_CKN#-A/ XSPI1_CS1#-B/IRQ8
76	P64/ET1_ETXD0/RMII1_TXD0/CAT1_ETXD0	P601/PIO_009/GTIOC4B/RXD8-B/SMISO8-B/ SSCL8-B/RSPCK0-D/ET1_TX_EN-B/ RMII1_TX_EN-B/GPTP_PTPOUT1/ CAT1_TX_EN-B/CATSYNC1-D/IRQ1/ADTRG1#
77	P63/ET1_ETXD1/RMII1_TXD1/CAT1_ETXD1	P600/PIO_008/GTIOC4A/TXD8-B/SMOSI8-B/ SSDA8-B/TXDA8-B/SSL00-D/ET1_TX_CLK-B/ GPTP_PTPOUT0/CAT1_TX_CLK-B/ CATLATCH1-D/IRQ0/ADTRG0#
78	P62/ET1_ERXD0/RMII1_RXD0/CAT1_ERXD0	PD07/PIO_039/GTIW-C/GTIOC3B/POEGA/ TXD3-A/SMOSI3-A/SSDA3-A/TXDA3-A/ CTX1-B/ET1_LINKSTA-B/CAT1_LINKSTA-B/ SD0CD-B/XSPI0_CS0#-A/XSPI0_RESET1#-B/ IRQ7/AN031
79	P61/ET1_ERXD1/RMII1_RXD1/CAT1_ERXD1	PD06/PIO_038/GTIV-C/GTIOC3A/POEGB/ RXD3-A/SMISO3-A/SSCL3-A/SSL23-A/ CRX1-B/ET1_RX_ER-B/RMII1_RX_ER-B/ CAT1_RX_ER-B/CATLEDERR-D/SD0WP-B/ XSPI0_DS-A/IRQ6/AN030
80	VSS	PD05/PIO_037/GTIU-C/GTIOC2B/POEGD/ SCK3-A/CTS3#-A/TXDB3-A/SSL22-A/CTX0-B/ ET1_RX_DV-B/RMII1_CRS_DV-B/ CAT1_RX_DV-B/CATLEDSTER-D/SD0DAT1-B/ XSPI0_IO3-A/IRQ5/AN029
81	P60/ET1_TX_EN/RMII1_TXD_EN/ CAT1_TX_EN	PD04/PIO_036/GTETRGA/GTIOC2A/POEGC/ CTS2#-A/CTS3#-A/RTS3#-A/SS3#-A/DE3-A/ TXDB3-A/SSL21-A/CRX0-B/ET1_RX_CLK-B/ RMII1_REF50CK-B/CAT1_RX_CLK-B/ CATLEDRUN-D/SD0DAT0-B/XSPI0_IO2-A/ XSPI0_WP0#-B/IRQ4/AN028

100-Pin LFQFP	RX72M	RX74M
82	VCC	PD03/PIO_035/TOC2/GTIOC1B/POEGA/ TXD2-A/SMOSI2-A/SSDA2-A/TXDA2-A/ MISO2-A/ET1_RXD3-B/CAT1_ERXD3-B/ CAT0_MDIO-D/SD0CLK-B/XSPI0_IO1-A/IRQ3/ AN027
83	PD7/MTIC5U/POE0#/ET1_RX_ER/ RMII1_RX_ER/CAT1_RX_ER/IRQ7/AN107	PD02/PIO_034/TIC2/GTETRGB/GTIOC1A/ POEGB/RXD2-A/SMISO2-A/SSCL2-A/ MOSI2-A/ET1_RXD2-B/CAT1_ERXD2-B/ CAT0_MDC-D/SD0CMD-B/XSPI0_IO0-A/IRQ2/ AN026
84	PD6/MTIC5V/MTIOC8A/POE4#/ET1_RX_CLK/ REF50CK1/CAT1_RX_CLK/IRQ6/AN106	PD01/PIO_033/GTETRGC/GTIOC0B/POEGC/ SCK2-A/CTS2#-A/TXDB2-A/RSPCK2-A/ ET1_RXD1-B/RMII1_RXD1-B/CAT1_ERXD1-B/ CATSYNC0-D/SD0DAT3-B/XSPI0_CK-A/IRQ1/ AN025
85	P97/ET1_ERXD3/CAT1_ERXD3	PD00/PIO_032/GTETRGD/GTIOC0A/POEGD/ CTS2#-A/RTS2#-A/SS2#-A/DE2-A/TXDB2-A/ CTS3#-A/SSL20-A/ET1_RXD0-B/ RMII1_RXD0-B/CAT1_ERXD0-B/ CATLATCH0-D/SD0DAT2-B/XSPI0_CKN#-A/ XSPI0_CS1#-B/IRQ0/AN024
86	P96/ET1_ERXD2/CAT1_ERXD2	VCC2
87	PD2/MTIOC4D/GTIOC0B/CRX0/ET1_EXOUT/ IRQ2/AN110	VSS
88	PD1/MTIOC4B/POE0#/GTIOC1A/CTX0/IRQ1/ AN109	VCL
89	P93/POE0#/CTS7#/RTS7#/SS7#/ ET1_LINKSTA/CAT1_LINKSTA/AN117	AVCC0
90	P92/POE4#/RXD7/SMISO7/SSCL7/ET1_CRS/ RMII1_CRS_DV/CAT1_RX_DV/AN116	AVSS0
91	P91/SCK7/ET1_COL/AN115	VREFL0
92	VSS	VREFH0
93	P90/TXD7/SMOSI7/SSDA7/ET1_RX_DV/ CAT1_RX_DV/AN114	P404/PIO_052/IRQ12-DS/AN004
94	VCC	P402/PIO_050/IRQ10-DS/AN002
95	P42/IRQ10_DS/AN002	P400/PIO_048/IRQ8-DS/AN000
96	P41/IRQ9_DS/AN001	P414/PIO_062/IRQ30/AN014/DA0
97	VREFL0	P007/PIO_007/GTCPPO6/GTIOC13B/POEGA/ CTS0#-B/RTS0#-B/SS0#-B/DE0-B/TXDB0-B/ ET1_INT-D/CATIRQ-E/IRQ23-DS/ADTRG0#/ AN023/PDMDAT0-C
98	P40/IRQ8_DS/AN000	P006/PIO_006/GTCPPO5/GTIOC13A/ GTIOC9B/SCK0-B/CTS0#-B/TXDB0-B/ ET1_LINKSTA-D/CAT1_LINKSTA-E/IRQ22-DS/ ADTRG1#/AN022/PDMCLK0-C/PCOUTZ1
99	VREFH0	P005/PIO_005/GTCPPO4/GTIOC12B/ GTIOC9A/RXD0-B/SMISO0-B/SSCL0-B/ SSILRCK1/ET1_MDIO-D/CATLATCH0-E/ IRQ21-DS/ADTRG2#/AN021/DSMDAT2-B/ PCOUTB1
100	AVCC0	P004/PIO_004/GTCPPO3/GTIOC12A/ GTIOC8B/TXD0-B/SMOSI0-B/SSDA0-B/ TXDA0-B/SSITXD1/ET1_MDC-D/CATSYNC0-E/ IRQ20-DS/AN020/DSMCLK2-B/PCOUTA1

Note: 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

Table 3.10 Comparative Listing of RX72N/RX74N 100-Pin Package Pin Functions

100-Pin	RX72N (100-Pin LFQFP)	RX74N (100-Pin LFQFP)
1	AVCC1	P003/PIO_003/GTCPPO2/GTIOC11B/GTIOC8A/ RXD7-A/SMISO7-A/SSCL7-A/SSIRXD1/ ET0_MDIO-D/IRQ19-DS/AN019/PCOUTB0
2	EMLE	P002/PIO_002/TMCI1/GTCPPO1/GTIOC11A/ GTIOC7B/TXD7-A/SMOSI7-A/SSDA7-A/ TXDA7-A/SSIBCK1/ET0_MDC-D/IRQ18-DS/ AN018/PCOUTA0
3	AVSS1	P001/PIO_001/TMCI0/GTCPPO0/GTIOC10B/ GTIOC7A/SCK7-A/CTS7#-A/TXDB7-A/SSIBCK0/ ET0_LINKSTA-D/IRQ17-DS/AN017/PCOUTZ0
4	PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/SS6#/ CTS0#/RTS0#/SS0#/SSITXD0/ET0_EXOUT	VSS
5	VCL	VCL
6	VBATT	RES#
7	MD/FINED	MD/P315
8	XCIN	P312/PIO_060/RTCIC2/GTETRGD/GTCPPO15/ POEGA/SSL13-B/SSILRCK0/IRQ20/ADTRG2#/TAMPI2
9	XCOUT	P311/PIO_059/RTCIC1/GTETRGC/GTCPPO14 /POEGD/CTS7#-A/SSL12-B/SSIRXD0/ ET0_WOL-C/IRQ19/ADTRG1#/TAMPI1
10	RES#	P310/PIO_058/RTCIC0/CACREF/GTETRGB/ GTCPPO1/POEGC/CTS0#-C/CTS1#-B/SSL11-B/ SSITXD0/IRQ18/ADTRG0#/TAMPI0
11	XTAL/P37	VBATT/VCC
12	VSS	XCIN/EXCIN/P309
13	EXTAL/P36	XCOUT/P308
14	VCC	VSS
15	UPSEL/P35/NMI	XTAL/P307
16	TRST#/P34/MTIOC0A/TMCI3/PO12/POE10#/ SCK6/SCK0/ET0_LINKSTA/IRQ4	EXTAL/P306
17	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/ POE4#/POE11#/RXD6/SMISO6/SSCL6/RXD0/ SMISO0/SSCL0/CRX0/IRQ3-DS	VCC
18	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCIC2/ RTCOUT/POE0#/POE10#/TXD6/SMOSI6/ SSDA6/TXD0/SMOSI0/SSDA0/CTX0/ USB0_VBUSEN/IRQ2-DS	P305/NMI/IRQ0
19	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/ RTS1#/SS1#/SSLB0-A/IRQ1-DS	VCC_USB
20	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS	PF01/PIO_049/GTCPPO15/USB0_DM/IRQ1
21	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A	PF00/PIO_048/GTCPPO14/USB0_DP/IRQ0
22	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A	VSS_USB
23	CLKOUT/P25/CS5#/EDACK1/MTIOC4C/ MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SSIDATA1/ADTRG0#	ETHPHYCLK/P304/PIO_028/TMCI3/GTETRGD/ GTCPPO0/POEGA/CTS0#-A/CTS1#-A/ USB0_VBUSEN/ET0_INT-E/IRQ0-DS/ADTRG0#

100-Pin	RX72N (100-Pin LFQFP)	RX74N (100-Pin LFQFP)
24	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/ TMRI1/PO4/SCK3/USB0_VBUSEN/SSIBCK1	TDI/P303/PIO_027/TMCI2/GTCPPO13/RXD0-A/ SMISO0-A/SSCL0-A/RXD1-A/SMISO1-A/ SSCL1-A/MISO1-C/IRQ1
25	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/ GTIOC0A/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/ SS0#/CTX1/SSIBCK0	TDO/P302/PIO_026/TMRI3/GTCPPO12/TXD0-A/ SMOSI0-A/SSDA0-A/TXDA0-A/TXD1-A/ SMOSI1-A/SSDA1-A/TXDA1-A/MOSI1-C/IRQ4
26	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/GTIOC1A/SCK0/USB0_OVRCURB/ AUDIO_CLK	TCK/SWCLK/P301/PIO_025/TMCI3/GTCPPO11/ SCK0-A/CTS0#-A/TXDB0-A/SCK1-A/CTS1#-A/ TXDB1-A/RSPCK1-C/IRQ7
27	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/ GTIOC2A/RXD0/SMISO0/SSCL0/USB0_EXICEN/ SSILRCK0/SCL1/IRQ9	TMS/SWDIO/P300/PIO_024/TMO1/GTCPPO10/ CTS0#-A/RTS0#-A/SS0#-A/DE0-A/TXDB0-A/ CTS1#-A/RTS1#-A/SS1#-A/DE1-A/TXDB1-A/ SSL10-C/ET0_WOL-D/IRQ6
28	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/USB0_ID/SSIRXD0/SDA1/ IRQ8	P201/PIO_017/TMCI0/GTIW-D/GTIOC3B/ GTIOC14B/MISO0-C/SCLHS1-A/USB0_EXICEN/ SSILRCK0/ET0_RX_ER-B/RMII0_RX_ER-B/ SD0CLK-C/IRQ9/PCINZ0
29	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/GTIOC0B/SCK1/ TXD3/SMOSI3/SSDA3/SDA2-DS/SSITXD0/ EPLSOUT0/IRQ7/ADTRG1#	P200/PIO_016/TMRI0/GTETRGA/GTIOC3A/ GTIOC14A/MOSI0-C/SDAHS1-A/USB0_ID/ SSIRXD0/ET0_TX_EN-B/RMII0_TX_EN-B/ SD0CMD-C/IRQ8/ADTRG2#/PCINZ1
30	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/ PO14/RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/ SMISO3/SSCL3/SCL2-DS/USB0_VBUSEN/ USB0_VBUS/USB0_OVRCURB/IRQ6/ADTRG0#	P107/PIO_015/TMO1/GTIV-D/GTIOC15B/ POEGA/TXD3-B/SMOSI3-B/SSDA3-B/TXDA3-B/ SDAHS2-A/SSITXD0/ET0_TXD3-B/SD0DAT3-C/ IRQ31-DS/ADTRG1#/PCINB1
31	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/ PO13/GTETRGA/RXD1/SMISO1/SSCL1/SCK3/ CRX1-DS/SSILRCK1/IRQ5	CLKOUT/P106/PIO_014/TMO2/RTCOUT/ GTIU-D/GTIOC15A/POEGB/RXD3-B/SMISO3-B/ SSCL3-B/SCLHS2-A/ET0_TXD2-B/SD0DAT2-C/ IRQ30-DS/ADTRG0#/PCINA1
32	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/ PO15/GTETRGD/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4	P105/PIO_013/TMCI2/GTIV-E/GTIOC14B/ TXD2-B/SMOSI2-B/SSDA2-B/TXDA2-B/SCK3-B/ CTS3#-B/TXDB3-B/CRX2-A/USB0_VBUS/ SSILRCK1/ET0_TXD1-B/RMII0_TXD1-B/ IRQ29-DS/ADST1-A/PCINB0
33	P13/MTIOC0B/TIOCA5/TMO3/PO13/GTADSM1/ TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ ADTRG1#	P104/PIO_012/TMRI2/GTIW-E/GTIOC14A/ RXD2-B/SMISO2-B/SSCL2-B/CTS3#-B/RTS3#-B/ SS3#-B/DE3-B/TXDB3-B/CTX2-A/ USB0_OVRCURA-DS/ET0_TXD0-B/ RMII0_TXD0-B/IRQ4/ADST0-A/PCINA0
34	P12/TMCI1/GTADSM0/RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	VCL
35	VCC_USB	VSS
36	USB0_DM	VCC
37	USB0_DP	P103/PIO_011/TMO3/GTADSM1/GTIOC13B/ CTS2#-B/SDA00-A/ET0_CRS-D/IRQ3
38	VSS_USB	P102/PIO_010/TMCI1/GTADSM0/GTIOC13A/ SCL00-A/ET0_COL-D/IRQ2
39	P55/D0[A0/D0]/WAIT#/EDREQ0/MTIOC4D/ TMO3/CRX1/ET0_EXOUT/IRQ10	P101/PIO_009/TMCI3/GTETRGC/GTADSM1/ GTIOC12B/SCK2-B/CTS2#-B/TXDB2-B/ USB0_VBUS-DS/ET0_TX_CLK-B/IRQ1/ ADTRG1#

100-Pin	RX72N (100-Pin LFQFP)	RX74N (100-Pin LFQFP)
40	P54/ALE/D1[A1/D1]/EDACK0/MTIOC4B/TMCI1/ CTS2#/RTS2#/SS2#/CTX1/ET0_LINKSTA	VCC_DCDC
41	P53*1/BCLK	VLO
42	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A	VSS_DCDC
43	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	VSS
44	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A	PC06/PIO_030/TMCI2/GTETRGC/GTCPPO7/ GTIOC15A/POEGB/RXD8-A/SMISO8-A/ SSCL8-A/MOSI0-A/SSILRCK0/ET0_TX_ER-A/ SD0WP-A/IRQ13/PDMCLK0-A
45	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/ PO31/TOC0/CACREF/GTIOC3A/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/ ET0_COL/IRQ14	PC05/PIO_029/TMRI2/GTOWLO-B/GTIOC9B/ SCK8-A/CTS8#-A/TXDB8-A/RSPCK0-A/ SSIBCK0/ET0_TX_EN-A/RMII0_TX_EN-A/ SD0DAT1-A/IRQ5/PCOUTZ1
46	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/MTCLKA/ TMCI2/PO30/TIC0/GTIOC3B/RXD8/SMISO8/ SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ ET0_ETXD3/IRQ13	PC04/PIO_028/TMCI1/GTOWUP-B/GTIOC9A/ CTS8#-A/RTS8#-A/SS8#-A/DE8-A/TXDB8-A/ CTS11#-A/SSL00-A/AUDIO_CLK/ET0_TXD3-A/ SD0DAT0-A/IRQ12/PCOUTB1
47	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/GTIOC1A/SCK8/RTS8#/ SCK10/RSPCKA-A/ET0_ETXD2	PC03/PIO_027/GTOVLO-B/GTIOC8B/TXD11-A/ SMOSI11-A/SSDA11-A/TXDA11-A/SDAHS1-C/ ET0_TXD2-A/SD0CLK-A/IRQ11/PCOUTA1
48	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/ POE0#/GTETRGC/SCK5/CTS8#/SS8#/SS10#/ CTS10#/RTS10#/SSLA0-A/ET0_TX_CLK	PC02/PIO_026/GTOVUP-B/GTIOC8A/RXD11-A/ SMISO11-A/SSCL11-A/SSL03-A/SCLHS1-C/ ET0_TXD1-A/RMII0_TXD1-A/SD0CMD-A/IRQ10/ PCOUTZ0
49	PC3/A19/MTIOC4D/TCLKB/PO24/GTIOC1B/ TXD5/SMOSI5/SSDA5/ET0_TX_ER	PC01/PIO_025/GTOULO-B/GTIOC7B/SCK11-A/ CTS11#-A/TXDB11-A/SSL02-A/SDA00-C/ ET0_TXD0-A/RMII0_TXD0-A/SD0DAT3-A/IRQ12/ PCOUTB0
50	PC2/A18/MTIOC4B/TCLKA/PO21/GTIOC2B/ RXD5/SMISO5/SSCL5/SSLA3-A/ET0_RX_DV	PC00/PIO_024/GTOUUP-B/GTIOC7A/CTS11#-A/ RTS11#-A/SS11#-A/DE11-A/TXDB11-A/SSL01-A/ SCL00-C/ET0_TX_CLK-A/SD0DAT2-A/IRQ14/ PCOUTA0
51	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/ET0_ERXD2/IRQ12	PB06/PIO_022/GTOWUP-A/GTIOC6A/ ET0_RX_ER-A/RMII0_RX_ER-A/IRQ6
52	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/ SS5#/SSLA1-A/ET0_ERXD3/IRQ14	PB05/PIO_021/TMRI1/GTOVLO-A/GTIOC5B/ ET0_RX_DV-A/RMII0_CRS_DV-A/IRQ13
53	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ ET0_CRS/RMII0_CRS_DV	PB04/PIO_020/GTOVUP-A/GTIOC5A/CTS4#-A/ ET0_RX_CLK-A/RMII0_REF50CK-A/IRQ4
54	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ ET0_ETXD1/RMII0_TXD1	PB03/PIO_019/TMO0/GTOULO-A/GTIOC4B/ SCK4-A/CTS4#-A/TXDB4-A/ET0_RXD3-A/IRQ3
55	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/ PO29/POE4#/SCK9/RTS9#/SCK11/ET0_ETXD0/ RMII0_TXD0/LCD_CLK-B	PB02/PIO_018/GTOUUP-A/GTIOC4A/CTS4#-A/ RTS4#-A/SS4#-A/DE4-A/TXDB4-A/ET0_RXD2-A/ IRQ2
56	PB4/A12/TIOCA4/PO28/CTS9#/SS9#/SS11#/ CTS11#/RTS11#/ET0_TX_EN/RMII0_TXD_EN/ LCD_TCON0-B	PB01/PIO_017/TMCI0/GTETRGB/GTCPPO4/ GTIOC14B/POEGA/TXD4-A/SMOSI4-A/ SSDA4-A/TXDA4-A/ET0_RXD1-A/ RMII0_RXD1-A/IRQ4-DS/PCINB1

100-Pin	RX72N (100-Pin LFQFP)	RX74N (100-Pin LFQFP)
57	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE11#/SCK6/ET0_RX_ER/ RMII0_RX_ER/LCD_TCON1-B	PB00/PIO_016/GTETRGA/GTADSM0/ GTIOC14A/POEGC/RXD4-A/SMISO4-A/ SSCL4-A/ET0_RXD0-A/RMII0_RXD0-A/IRQ12/ ADST2-A/PCINA1
58	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/RTS6#/ SS6#/ET0_RX_CLK/REF50CK0/LCD_TCON2-B	ETHPHYCLK/PA07/PIO_015/GTIOC3B/ GTIOC13B/RXD10-A/SMISO10-A/SSCL10-A/ MISO0-B/IRQ7/PCINB0
59	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/ PO25/TXD6/SMOSI6/SSDA6/ET0_ERXD0/ RMII0_RXD0/LCD_TCON3-B/IRQ4-DS	PA06/PIO_014/TMCI3/GTIOC3A/GTIOC13A/ TXD10-A/SMOSI10-A/SSDA10-A/TXDA10-A/ MOSI0-B/IRQ14/PCINZ1
60	VCC	PA05/PIO_013/GTIOC2B/GTIOC12B/SCK10-A/ CTS10#-A/TXDB10-A/RSPCK0-B/IRQ5/PCINA0
61	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/SMISO6/ SSCL6/ET0_ERXD1/RMII0_RXD1/ LCD_DATA0-B/IRQ12	PA04/PIO_012/TMRI0/GTIOC2A/GTIOC12A/ CTS10#-A/RTS10#-A/SS10#-A/DE10-A/ TXDB10-A/SSL00-B/IRQ5-DS/PCINZ0
62	VSS	VCC
63	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/ LCD_DATA1-B	VSS
64	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/ POE10#/GTETRGB/CTS5#/RTS5#/SS5#/ MOSIA-B/ET0_EXOUT/LCD_DATA2-B	VCL
65	PA5/A5/MTIOC6B/TIOCB1/PO21/GTIOC0A/ RSPCKA-B/ET0_LINKSTA/LCD_DATA3-B	PA03/PIO_011/GTIOC1B/GTIOC11B/RXD5-A/ SMISO5-A/SSCL5-A/IRQ6-DS/ADSYNC-A
66	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/ TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC/ PMGI0_MDC/LCD_DATA4-B/IRQ5-DS	PA02/PIO_010/GTIW-A/GTIOC1A/GTIOC11A/ TXD5-A/SMOSI5-A/SSDA5-A/TXDA5-A/SSL03-B/ IRQ10/ADCNV2-A
67	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/ PMGI0_MDIO/LCD_DATA5-B/IRQ6-DS	PA01/PIO_009/GTIV-A/GTIOC0B/GTIOC10B/ SCK5-A/CTS5#-A/TXDB5-A/SSL02-B/IRQ11/ ADCNV1-A
68	PA2/A2/MTIOC7A/PO18/GTIOC1A/RXD5/ SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B	ETHPHYCLK/PA00/PIO_008/CACREF/GTIU-A/ GTIOC0A/GTIOC10A/CTS10#-A/CTS5#-A/ RTS5#-A/SS5#-A/DE5-A/TXDB5-A/SSL01-B/ IRQ1-DS/ADCNV0-A
69	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/ PO17/GTIOC2A/SCK5/SSLA2-B/ET0_WOL/ LCD_DATA7-B/IRQ11	PE06/PIO_046/GTETRGC/GTADSM1/ GTIOC10A/POEGB/SSL13-A/XSPI1_DS-A/ IRQ6
70	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/ PO16/CACREF/GTIOC0B/SSLA1-B/ET0_TX_EN/ RMII0_TXD_EN/LCD_DATA8-B	PE05/PIO_045/GTOWLO-C/GTIOC9B/SSL12-A/ XSPI1_IO3-A/IRQ5
71	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/TOC1/ GTIOC3A/MISOB-B/SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105	PE04/PIO_044/GTOWUP-C/GTIOC9A/ CTS12#-A/SSL11-A/XSPI1_IO2-A/ XSPI1_WP0#-C/IRQ12
72	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/TIC1/ GTIOC3B/MOSIB-B/SDHI_CD/MMC_CD-B/ LCD_DATA10-B/IRQ6/AN104	PE03/PIO_043/TOC3/GTOVLO-C/GTIOC8B/ CTS12#-A/RTS12#-A/SS12#-A/DE12-A/ TXDB12-A/MISO1-A/SD0DAT7-B/XSPI1_IO1-A/ IRQ11
73	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/GTIOC0A/RSPCKB-B/ET0_RX_CLK/ REF50CK0/LCD_DATA11-B/IRQ5/AN103	PE02/PIO_042/TIC3/GTOVUP-C/GTIOC8A/ RXD12-A/SMISO12-A/SSCL12-A/MOSI1-A/ SD0DAT6-B/XSPI1_IO0-A/IRQ7-DS
74	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/GTIOC1A/SSLB0-B/ ET0_ERXD2/LCD_DATA12-B/AN102	CLKOUT/PE01/PIO_041/GTOULO-C/GTIOC7B/ TXD12-A/SMOSI12-A/SSDA12-A/TXDA12-A/ RSPCK1-A/SD0DAT5-B/XSPI1_CK-A/IRQ9

100-Pin	RX72N (100-Pin LFQFP)	RX74N (100-Pin LFQFP)
75	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/PO26/ TOC3/POE8#/GTIOC2A/CTS12#/RTS12#/SS12#/ ET0_ERXD3/MMC_D7-B/LCD_DATA13-B/AN101	ETHPHYCLK/PE00/PIO_040/GTOUUP-C/ GTIOC7A/SCK12-A/CTS12#-A/TXDB12-A/ SSL10-A/SD0DAT4-B/XSPI1_CKN#-A/ XSPI1_CS1#-B/IRQ8
76	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/PO23/ TIC3/GTIOC0B/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/MMC_D6-B/LCD_DATA14-B/ IRQ7-DS/AN100	P601/PIO_009/GTIOC4B/RXD8-B/SMISO8-B/ SSCL8-B/RSPCK0-D/GPTP_PTPOUT1/IRQ1/ ADTRG1#
77	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/MTIOC3B/ PO18/GTIOC1B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ LCD_DATA15-B/ANEX1	P600/PIO_008/GTIOC4A/TXD8-B/SMOSI8-B/ SSDA8-B/TXDA8-B/SSL00-D/GPTP_PTPOUT0/ IRQ0/ADTRG0#
78	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/GTIOC2B/ SCK12/SSLB1-B/MMC_D4-B/LCD_DATA16-B/ ANEX0	PD07/PIO_039/GTIW-C/GTIOC3B/POEGA/ TXD3-A/SMOSI3-A/SSDA3-A/TXDA3-A/CTX1-B/ SD0CD-B/XSPI0_CS0#-A/XSPI0_RESET1#-B/ IRQ7/AN031
79	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/QMI-B/ QIO1-B/SDHI_D1-B/MMC_D1-B/LCD_DATA17-B/ IRQ7/AN107	PD06/PIO_038/GTIV-C/GTIOC3A/POEGB/ RXD3-A/SMISO3-A/SSCL3-A/SSL23-A/CRX1-B/ SD0WP-B/XSPI0_DS-A/IRQ6/AN030
80	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B/IRQ6/AN106	PD05/PIO_037/GTIU-C/GTIOC2B/POEGD/ SCK3-A/CTS3#-A/TXDB3-A/SSL22-A/CTX0-B/ SD0DAT1-B/XSPI0_IO3-A/IRQ5/AN029
81	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/MTCLKA/ POE10#/SSLC1-A/QSPCLK-B/SDHI_CLK-B/ MMC_CLK-B/LCD_DATA19-B/IRQ5/AN113	PD04/PIO_036/GTETRGA/GTIOC2A/POEGC/ CTS2#-A/CTS3#-A/RTS3#-A/SS3#-A/DE3-A/ TXDB3-A/SSL21-A/CRX0-B/SD0DAT0-B/ XSPI0_IO2-A/XSPI0_WP0#-B/IRQ4/AN028
82	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0-A/ QSSL-B/SDHI_CMD-B/MMC_CMD-B/ LCD_DATA20-B/IRQ4/AN112	PD03/PIO_035/TOC2/GTIOC1B/POEGA/TXD2-A/ SMOSI2-A/SSDA2-A/TXDA2-A/MISO2-A/ SD0CLK-B/XSPI0_IO1-A/IRQ3/AN027
83	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ GTIOC0A/RSPCKC-A/QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B/IRQ3/AN111	PD02/PIO_034/TIC2/GTETRGB/GTIOC1A/ POEGB/RXD2-A/SMISO2-A/SSCL2-A/MOSI2-A/ SD0CMD-B/XSPI0_IO0-A/IRQ2/AN026
84	PD2/D2[A2/D2]/MTIOC4D/TIC2/GTIOC0B/ MISOC-A/CRX0/QIO2-B/SDHI_D2-B/MMC_D2-B/ LCD_DATA22-B/IRQ2/AN110	PD01/PIO_033/GTETRGC/GTIOC0B/POEGC/ SCK2-A/CTS2#-A/TXDB2-A/RSPCK2-A/ SD0DAT3-B/XSPI0_CK-A/IRQ1/AN025
85	PD1/D1[A1/D1]/MTIOC4B/POE0#/GTIOC1A/ MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/AN109	PD00/PIO_032/GTETRGD/GTIOC0A/POEGD/ CTS2#-A/RTS2#-A/SS2#-A/DE2-A/TXDB2-A/ CTS3#-A/SSL20-A/SD0DAT2-B/XSPI0_CKN#-A/ XSPI0_CS1#-B/IRQ0/AN024
86	PD0/D0[A0/D0]/POE4#/GTIOC1B/ LCD_EXTCLK-B/IRQ0/AN108	VCC2
87	P47/IRQ15-DS/AN007	VSS
88	P46/IRQ14-DS/AN006	VCL
89	P45/IRQ13-DS/AN005	AVCC0
90	P44/IRQ12-DS/AN004	AVSS0
91	P43/IRQ11-DS/AN003	VREFL0
92	P42/IRQ10-DS/AN002	VREFH0
93	P41/IRQ9-DS/AN001	P404/PIO_052/IRQ12-DS/AN004
94	VREFL0	P402/PIO_050/IRQ10-DS/AN002
95	P40/IRQ8-DS/AN000	P400/PIO_048/IRQ8-DS/AN000
96	VREFH0	P414/PIO_062/IRQ30/AN014/DA0

100-Pin	RX72N (100-Pin LFQFP)	RX74N (100-Pin LFQFP)
97	AVCC0	P007/PIO_007/GTCPPO6/GTIOC13B/POEGA/ CTS0#-B/RTS0#-B/SS0#-B/DE0-B/TXDB0-B/ IRQ23-DS/ADTRG0#/AN023/PDMDAT0-C
98	P07/IRQ15/ADTRG0#	P006/PIO_006/GTCPPO5/GTIOC13A/GTIOC9B/ SCK0-B/CTS0#-B/TXDB0-B/IRQ22-DS/ ADTRG1#/AN022/PDMCLK0-C/PCOUTZ1
99	AVSS0	P005/PIO_005/GTCPPO4/GTIOC12B/GTIOC9A/ RXD0-B/SMISO0-B/SSCL0-B/SSILRCK1/ IRQ21-DS/ADTRG2#/AN021/PCOUTB1
100	P05/SSILRCK1/IRQ13/DA1	P004/PIO_004/GTCPPO3/GTIOC12A/GTIOC8B/ TXD0-B/SMOSI0-B/SSDA0-B/TXDA0-B/ SSITXD1/IRQ20-DS/AN020/PCOUTA1

Note: 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

4. Points to Note when Replacing MCUs

This section presents important information on differences between the RX72M/RX72N Group and the RX74M/RX74N Group.

4.1, Notes on Pin Design presents notes related to hardware. 4.2, Notes on Functional Design presents notes related to software.

4.1 Notes on Pin Design

4.1.1 Selection of the Operating Mode by the Mode-Setting Pins at the Time of Release from the Reset State

The mode setting pins at the time of release from the reset state are the MD and UB pins in the RX72M/RX72N Group, but only the MD pin is used for this purpose in the RX74M/RX74N Group.

4.2 Notes on Functional Design

The following describes points to note related to software regarding function settings that differ between the RX72M/RX72N Group and the RX74M/RX74N Group.

For differences between modules and functions, see section 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware of each MCU group, listed in section 5, Reference Documents.

4.2.1 Performing RAM Self-Diagnostics on Save Register Banks

On the RX74M/RX74N Group, save register banks are configured in the RAM. The save register banks are provided with a buffer. Therefore, if a SAVE instruction is used to write data to a register and then a RSTR instruction is used to read data from the same register, the data is actually read from the buffer and not from the RAM memory cells. When performing self-diagnostics on the RAM in a save register bank, use the following sequence of steps for checking the written data in order to prevent the data from being read from the buffer:

(1) Use the SAVE instruction to write data to the bank that is the target of the diagnostic test.

(2) Use the SAVE instruction to write data to a bank other than that written to in step 1.

(3) Use the RSTR instruction to read data from the bank written to in step 1.

4.2.2 Using Flash Memory and Extra MRAM Commands

On the RX72M/RX72N Group, programming and erasing of the flash memory is accomplished by setting FACI commands in the FACI command-issuing area to control the FCU. On the RX74M/RX74N Group, the security, safety, and system configuration settings to be saved in the extra MRAM and OPT areas are saved by setting MACI commands in the MACI command-issuing area. Note that the function for erasure and blank checking of the MRAM is not present.

Table 4.1 is Comparison of Specifications of FACI Commands and MACI Commands.

Table 4.1 Comparison of Specifications of FACI Commands and MACI Commands

Item	FACI Command (RX72M/RX72N)	MACI Command (RX74M/RX74N)
Usable commands	• Programming • Block erase • Multi-block erase • P/E suspend • P/E resume • Status clear • Forced stop • Blank check • Configuration setting	• Programming • Status clear • Forced stop • Configuration setting • Increment counter • Counter reading

4.2.3 Clock Frequency Settings

The restrictions on clock frequency settings differ between the RX72M/RX72N Group and the RX74M/RX74N Group. For details, see Table 4.2.

Table 4.2 Comparison of Restrictions on Clock Frequency Settings

Item	RX72M/RX72N	RX74M/RX74N
Restrictions on clock frequency settings	• ICLK ≥ BCLK • PCLKA ≥ PCLKB • PCLKB ≥ PCLKC • PCLKB ≥ PCLKD	• ICLK ≥ BCLK • PCLKD ≥ PCLKA ≥ PCLKB • CPUCLK0 ≥ ICLK • MRICLK ≥ ICLK • CPUCLK0 ≥ MRICLK • ICLK ≥ MRPCLK
Restrictions on the clock frequency ratio	• ICLK:FCLK = N:1 or 1:N • ICLK:PCLKA = N:1 or 1:N • ICLK:PCLKB = N:1 or 1:N • ICLK:PCLKC = N:1 or 1:N • ICLK:PCLKD = N:1 or 1:N • ICLK:BCLK = N:1	• ICLK:FCLK = N:1 or 1:N • ICLK:PCLKA = N:1 or 1 N • ICLK:PCLKB = N:1 or 1:N • ICLK:PCLKC = N:1 or 1:N • ICLK:PCLKD = N:1 or 1:N • ICLK:BCLK = N:1 • CPUCLK0: ICLK = N:1 • MRICLK:ICLK = N:1 • CPUCLK0: MRICLK = N:1 • ICLK:MRPCLK = N:1

4.2.4 Battery Backup Function

On the RX74M/RX74N Group, when the voltage level at the VBATT is lower than the guaranteed operation range, operation of the sub-clock oscillator and RTC is not guaranteed. If the VBATT pin falls below the guaranteed operating voltage, initialize the RTC, and then supply the power again.

4.2.5 All-Module Clock Stop Mode

The RX74M/RX74N Group does not have all-module clock stop mode.

4.2.6 Priority Order of Buses

On the RX72M/RX72N Group, the priority order of buses is set by using the bus priority control register (BUSPRI). On the RX74M/RX74N Group, “fixed-priority” or “round-robin” is selected by using the ARBS bit in bus slave arbitration control register 0.

4.2.7 Pin Assignment Function

On the RX72M/RX72N Group, the pin function control register described in the Multi-Function Pin Controller section is used to assign a function from among multiple modules to each pin corresponding to the register. On the RX74M/RX74N Group, it is necessary to set pin assignment to a module function corresponding to the register by using the port function register described in the I/O Ports section.

4.2.8 Operation of Main Clock Oscillation Stop Detection Function

The oscillation stop detection function detects stopping of the main clock oscillator and switches the clock source of the system clock. On the RX72M/RX72N Group, a clock source that can be switched while the clock is stopped is the LOCO (240 kHz). On the RX74M/RX74N Group, it is switched to the MOCO (8 MHz).

In addition, if the main clock is stopped when it is used as the clock source of the PLL, the clock source of the system clock is switched to the LOCO on the RX72M/RX72N Group. On the RX74M/RX74N Group, the system clock is not switched and the PLL operates in free-running mode.

4.2.9 Scan Conversion Time of 12-Bit A/D Converter and 16-Bit A/D Converter

The scan conversion time differs between the RX72M/RX72N Group and the RX74M/RX74N Group. For details, refer to the User’s Manual: Hardware for the RX72M/RX72N Group and the RX74M/RX74N Group, listed in section 5, Reference Documents, to check the analog input sampling time and scan conversion time of the corresponding module.

4.2.10 Initialization of Port Direction Register (PDR)

The method of initializing the PDR register differs between the RX72M/RX72N Group and the RX74M/RX74N Group, even on products with the same pin count.

5. Reference Documents

User's manuals: Hardware

RX72M Group User's Manual: Hardware Rev.1.20 (R01UH0804EJ0120)
(The latest version can be downloaded from the Renesas Electronics website.)

RX72N Group User's Manual: Hardware Rev.1.20 (R01UH0824EJ0120)
(The latest version can be downloaded from the Renesas Electronics website.)

RX74M Group User's Manual: Hardware Rev.1.10 (R01UH1055EJ0110)
(The latest version can be downloaded from the Renesas Electronics website.)

RX74N Group User's Manual: Hardware Rev.1.10 (R01UH1056EJ0110)
(The latest version can be downloaded from the Renesas Electronics website.)

Application note

Design Guide for Migration between RX Family: Differences in Package External form (R01AN4591EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical updates and technical news
(The latest version can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This application note reflects the content of the following technical updates:

- TN-RX*-A0147B/E
- TN-RX*-A187A/E
- TN-RX*-A192A/E
- TN-RX*-A193A/E
- TN-RX*-A195A/E
- TN-RX*-A203A/E
- TN-RX*-A207A/E
- TN-RX*-A208A/E
- TN-RX*-A209A/E
- TN-RX*-A210A/E
- TN-RX*-A212A/E
- TN-RX*-A0215A/E
- TN-RX*-A0227A/E
- TN-RX*-A0232A/E
- TN-RX*-A0233A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.10	Oct.2.26	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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