Purpose and Agreement

- This DRAM list for RZ MPUs would **help RZ customers to choose an appropriate DRAM among many products.** In addition to "Recommendation" that fully verified with real boards, we newly **defined "Option" that briefly verified with simulation to provide wider selection to save cost/TAT for memory selection.**
- Please use this information for your reference and confirm if it works with SI/PI verification with your design under your responsibility. Please understand that Renesas will not guarantee that those DRAMs can work with custom boards.

Definition of recommendation level

Table 1 Definition of recommendation level

Recommendation level	Recommendation level	Deliverables	Notes
Recommendation	Verified functions with EVK Verified all verification items satisfying the criteria defined in the Renesas' DDR verification guide with simulation	PCB reference design data PCB design guide	-
Option1	Verified eye mask satisfying the criteria defined in the Renesas' DDR design guide with simulation	None	Simulation was done with PCB data of EVK by Aurora systems. For details, please contact Aurora systems.
Option2	Verified functions with Renesas internal device board. Verified all verification items satisfying the criteria defined in the Renesas' DDR verification guide with simulation	None	Deliverables cannot be shared because Renesas internal device board is not released.

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1. DRAM recommendation list

1.1 RZ/G2 Group

The table describes DRAM information of RZ/G2 group.
You can also refer to RZ/G series website for more information included products and related Evaluation Kit (EVK).

Table 1.1 RZ/G2 Group

Product(Device)	Memory Type[Capacity]	DRAM memory P/N	Recommendation level
RZ/G2L 15x15mm, 0.5mm pitch, PBGA	DDR4[1GByte]	Micron: MT40A1G16KD-062E:E	Recommendation(EVK)
	DDR4[1GByte]	Nanya: NT5AD512M16C4-JRI	Option1
	DDR4[2GByte]	Samsung: K4AAG165WA-BCTD	Option1
	DDR4[2GByte]	Alliance: AS4C1G16D4	Option1
RZ/G2LC 13x13mm, 0.5mm pitch, PBGA	DDR4 [1GByte]	Micron: MT40A512M16LY-062EIT:E	Recommendation(EVK)
	DDR3L[512KByte]	Micron: MT41K256M16TW-107 XIT:P	Option2
RZ/G2UL (Type-1) 13x13mm, 0.5mm pitch, PBGA	DDR4 [1GByte]	Micron: MT40A512M16LY-062EIT:E	Recommendation(EVK)
	DDR3L [512KByte]	Micron: MT41K256M16TW-107 IT	Option2

1.2 RZ/Five Group

The table describes DRAM information of RZ/Five group.
You can also refer to RZ/G series website for more information included products and related Evaluation Kit (EVK).

Table 1.2 RZ/Five Group

Product(Device)	Memory Type[Capacity]	DRAM memory P/N	Recommendation level
RZ/Five 13x13mm, 0.5mm pitch, PBGA	DDR4[1GByte]	Micron: MT40A512M16LY-062EIT:E	Recommendation(EVK)
	DDR3L[512KByte]	Micron: MT41K256M16TW-107 IT	Option
RZ/Five 11x11mm, 0.5mm pitch, PBGA	DDR4[1GByte]	Micron: MT40A512M16TB-062E IT:R	Option

1.3 RZ/G3 Group

The table describes DRAM information of RZ/G3 group.
You can also refer to RZ/G series website for more information included products and related Evaluation Kit (EVK).

Table 1.3 RZ/G3 Group

Product(Device)	Memory Type[Capacity]	DRAM memory P/N	Recommendation level
RZ/G3S 14x14mm, 0.5mm pitch, PBGA	LPDDR4 [1GByte]	Micron: MT53E512M16D1FW-046WT	Recommendation(EVK)
	DDR4 [4GByte]	Micron: MT40A2G16TBB-062E:F	Option2
	LPDDR4 [1GByte]	Nanya NT6AN512M16AV-J1I	Option1
RZ/G3S 13x13mm, 0.5mm pitch, PBGA	LPDDR4 [1GByte]	Micron: MT53D512M16D1DS-046 IT:D	Option2
	DDR4 [4GByte]	Micron: MT40A2G16TBB-062E:F	Option2
RZ/G3E 15x15mm, 0.5mm pitch. FCBGA	LPDDR4X*1 [4GByte]	Micron: MT53E1G32D2FW-046 WT:C	Recommendation (EVK)
	LPDDR4X [8GByte]	Micron: MT53E2G32D4DE-046 AIT:C	Option2
	LPDDR4 [4GByte]	Micron: MT53E1G32D2FW	Option2
	LPDDR4X [4GByte]	Nanya: NT6AP1024F32BV-J1	Option1
	LPDDR4X [4GByte]	Alliance: AS4C1G32MD4V-046BIN	Option1

1.4 RZ/V2 Group

The table describes DRAM information of RZ/V2 group.
You can also refer to RZ/V series website for more information included products and related Evaluation Kit (EVK).

Table 1.4 RZ/V2 Group

Product(Device)	Memory Type[Capacity]	DRAM memory P/N	Recommendation level
RZ/V2L 15x15mm, 0.5mm pitch, PBGA	DDR4 [2GByte] [1GByte]	Micron: MT40A1G16KD-062E:E MT53D512M16D1DS-046	Recommendation(EVK)
	DDR4 [2GByte]	Samsung: K4AAG165WA-BCTD	Option1
	DDR4 [2GByte]	Alliance: AS4C1G16D4	Option1
RZ/V2M/MA 13x13mm, 0.5mm pitch, PBGA	LPDDR4 [8GByte]	Micron: MT53D1024M32D4DT-053 AIT:D MT53E1G32D2NP-046 WT:B	Recommendation(EVK)
RZ/V2H 19x19mm, 0.5mm pitch, FCBGA	LPDDR4X [8GByte]	Micron: MT53E2G32D4DE-046 AIT:C MT53E2G32D4DE-046 WT:C	Recommendation (EVK)
	LPDDR4X [4GByte]	Micron: MT53E1G32D2FW-046	Option1
	LPDDR4X [4GByte]	Nanya: NT6AP1024F32BV-J1	Option1
	LPDDR4X [4GByte]	Alliance: AS4C1G32MD4V-046BIN	Option1
RZ/V2N 15x15mm, 0.5mm pitch. FCBGA	LPDDR4X [8GByte]	Micron: MT53E2G32D4DE-046 AIT:C MT53E2G32D4DE-046 WT:C	Recommendation (EVK)

1.5 RZ/T2 Group

The table describes DRAM information of RZ/T2 group.
You can also refer to RZ/T series website for more information included products and related Evaluation Kit (EVK).

Table 1.5 RZ/T2 Group

Product(Device)	Memory Type[Capacity]	DRAM memory P/N	Recommendation level
RZ/T2H 23x23mm, 0.8mm pitch, FCBGA	LPDDR4 [8GByte]	Micron: MT53E2G32D4DE-046 WT:C	Recommendation(EVK)

1.6 RZ/N2 Group

The table describes DRAM information of RZ/N2 group.
You can also refer to RZ/N series website for more information included products and related Evaluation Kit (EVK).

Table 1.6 RZ/N2 Group

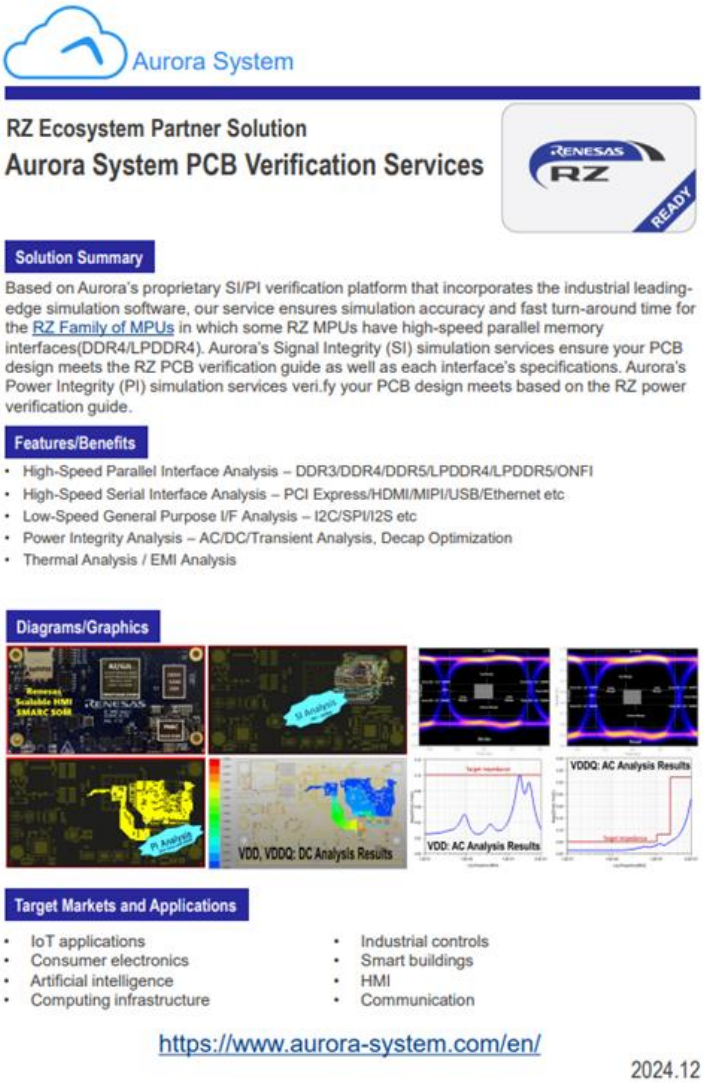
Product(Device)	Memory Type[Capacity]	DRAM memory P/N	Recommendation level
RZ/N2H 21x21mm, 0.8mm pitch, FCBGA	LPDDR4 [8GByte]	Micron: MT53E2G32D4DE-046 WT:C	Recommendation(EVK)

2. SI/PI simulation partner

Renesas recommends you to rely on PCB verification service vendor through SI/PI simulation if you have no experience in SI/PI or when you face any trouble in SI/PI simulation etc.

❖ [Aurora System PCB Verification Services | Renesas]

- Is a partner of Renesas Ready Partner Network
- Executed SI/PI simulation of the combination of RZ and DDR memory devices defined as “Option” at recommendation level
- Can provide the simulation report
- **This experience helps to smoothly offer SI/PI simulation service for RZ family at shorter TAT**



REVISION HISTORY	RZ Family DRAM list

Rev.	Date	Description	
		Page	Summary
1.00	Aug 1, 2025	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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