

## RZ/N2H Group

### HIPERFACE DSL Safety sample program

---

#### Introduction

This application note explains a sample program for acquiring and indicating information including safety data from an encoder in conformance with the HIPERFACE DSL<sup>®</sup> communications protocol specification by using the encoder Interface of the RZ/N2H.

The features of the program:

- Acquiring angle information, etc. from an encoder (EDM35-2KF0A020A) compliant with the HIPERFACE DSL<sup>®</sup> communications protocol specification

#### Target Device

RZ/N2H

---

**Table of Contents**

1. Specifications .....	4
2. Operating Environment.....	5
3. Peripheral Functions.....	6
3.1 Pins.....	6
4. Software .....	8
4.1 HFDSL Driver Function .....	8
4.2 File Structure .....	8
4.3 Functions .....	8
4.4 Specifications of API Functions.....	9
4.4.1 R_HFDSL_Open .....	9
4.4.2 R_HFDSL_Close .....	9
4.4.3 R_HFDSL_GetVersion .....	10
4.4.4 R_HFDSL_Control .....	10
4.5 Specifications of User-defined Functions .....	15
4.5.1 hfdsl_int_nml_callback .....	15
4.5.2 hfdsl_int_err_callback.....	15
4.5.3 hfdsl_int_safety_callback .....	16
4.5.4 hfdsl_int_mrcv_callback .....	16
4.5.5 hfdsl_int_smrcv_callback .....	17
4.6 Interrupt Handler.....	17
4.6.1 hfdsl_int_isr_chn (n=0 to 15).....	17
4.6.2 hfdsl_ints_isr_chn (n=0 to 15).....	17
4.6.3 hfdsl_fpr_isr_chn (n=0 to 15) .....	18
4.6.4 hfdsl_sp_isr_chn (n=0 to 15).....	18
4.6.5 hfdsl_err_isr.....	18
4.7 Interrupts .....	19
4.8 Constants and Error Codes.....	21
4.9 Fixed-width Integers .....	21
4.10 Structures, Unions, and Enumerated Types .....	22
4.10.1 Structures .....	22
4.10.2 Unions .....	23
4.10.3 Enumerated Types .....	23
4.11 Description of the Sample Program .....	24
4.11.1 Outline of Operations .....	24
4.11.2 Variables for the Sample Program .....	26
4.11.3 Constants for the Sample Program .....	27
4.11.4 Flowchart of Main Processing .....	28
4.11.5 Operation Sequence .....	37

4.11.6 Console Commands ..... 42

5. Sample Code.....45

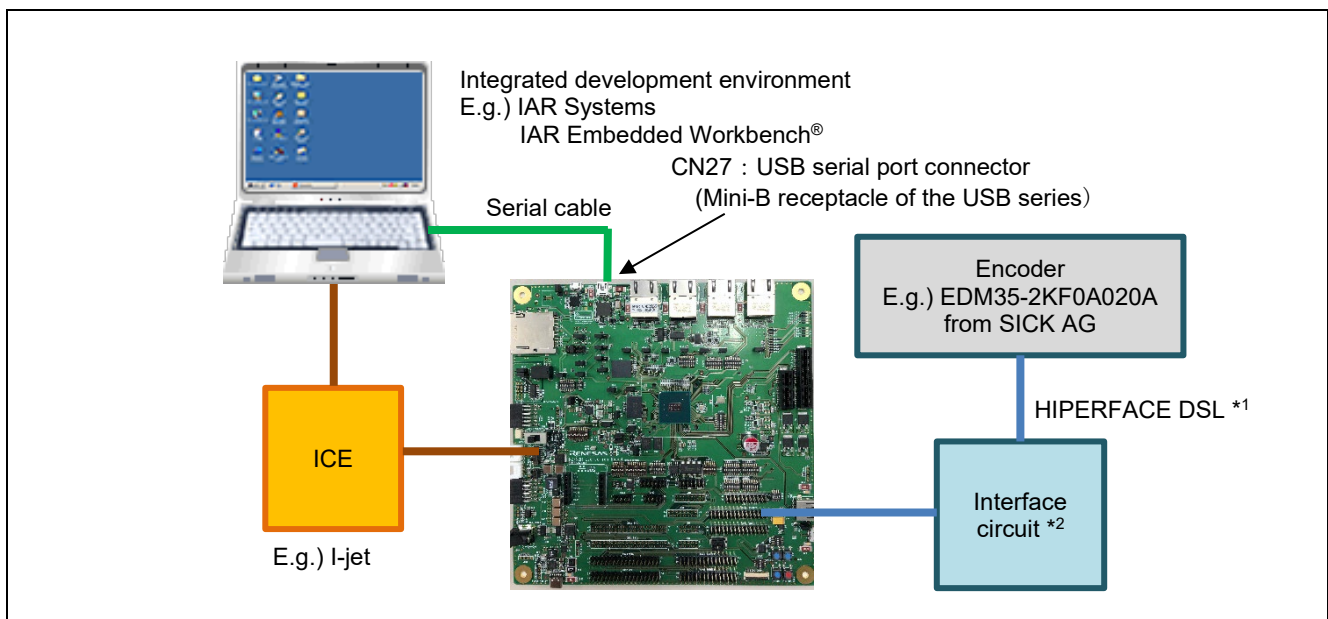
Revision History .....46

## 1. Specifications

Table 1.1 lists the peripheral functions to be used and their applications. Figure 1.1 shows the operating environment when the sample code is being executed.

**Table 1.1 Peripheral Functions and Applications**

Peripheral Module	Application
HIPERFACE DSL controller (HDSL)	Handling transfer to and from an absolute encoder incorporating a facility for handling the HIPERFACE DSL communications protocol
Interrupt controller (ICU)	Controlling interrupts from the HDSL controller
General PWM timer (GPT) unit 0 channel 0	Generating event cycles for input to the ELC
Event link controller (ELC)	Makes the link between events output from unit 0 channel 0 of the GPT and the HDSL module.
Serial Communication Interface (SCI) UART	Asynchronous communications of the SCI are used for COM port communications by using USB interface. It is used for console interface of the sample program.



**Figure 1.1 Operating Environment**

- Note: 1. For allowable cable length, refer to the encoder manuals.  
 2. Refer to the “HIPERFACE DSL® MASTER Safety Integration Manual”.

## 2. Operating Environment

The sample code covered in this application note is for the environment below.

**Table 2.1 Operating Environment**

Item		Description
MCU		RZ/N2H Group
Operating frequency *1	CR52 ver.	CPUCLK = 1000 MHz (Cortex®-R52 CPU0)
	CA55 ver.	CPUCLK = 1200 MHz (Cortex®-A55 Core0)
Operating voltage		0.8 V (Core) / 1.1 V (DDR) / 1.8 V (PLL, etc.) / 3.3 V (I/O)
Integrated development environment *2		IAR Systems: IAR Embedded Workbench® for Arm® RENESAS: e <sup>2</sup> studio
Board		RZ/N2H Evaluation Board (RTK9RZN2Hxxxxxxxx)
Devices (function to be used on the board)		None

- Note
1. This sample program has a CR52 version that runs on the CPU core Cortex®-R52 and a CA55 version that runs on the CPU core Cortex®-A55. CR52 ver. and CA55 ver. are descriptions of the respective version.
  2. Refer to the RZ/N2H Group Encoder I/F HIPERFACE DSL Safety sample program Release Note to check the version number of the integrated development environment.

### 3. Peripheral Functions

The basics of the peripheral modules, operating modes, and registers are described in the “RZ/N2H Group User’s Manual: Hardware”

#### 3.1 Pins

The pins used and their functions are listed in the table below. Channels HFDSL8, HFDSL12, and HFDSL15 out of HFDSL0 to HFDSL15 have no assigned I/O ports. The remaining 13 channels are available to use.

**Table 3.1 Pins Used and Their Functions**

Channel	Pin Name	I/O Port	Input /Output	Voltage Domain	Description
HFDSL0	ENCIFDI00 (dsl_in)	P14_5	Input	VDD33	Data input
	ENCIFDO00 (dsl_out)	P14_4	Output	VDD33	Data output
	ENCIFOE00 (dsl_en)	P14_3	Output	VDD33	Drive/receive control
HFDSL1	ENCIFDI01 (dsl_in)	P27_0	Input	VDD33	Data input
	ENCIFDO01 (dsl_out)	P26_7	Output	VDD33	Data output
	ENCIFOE01 (dsl_en)	P02_1	Output	VDD1833_5	Drive/receive control
HFDSL2	ENCIFDI02 (dsl_in)	P03_2	Input	VDD33	Data input
	ENCIFDO02 (dsl_out)	P03_1	Output	VDD33	Data output
	ENCIFOE02 (dsl_en)	P03_4	Output	VDD33	Drive/receive control
HFDSL3	ENCIFDI03 (dsl_in)	P13_3	Input	VDD1833_6	Data input
	ENCIFDO03 (dsl_out)	P13_2	Output	VDD1833_6	Data output
	ENCIFOE03 (dsl_en)	P13_1	Output	VDD1833_6	Drive/receive control
HFDSL4	ENCIFDI04(dsl_in)	P10_5	Input	VDD33	Data input
	ENCIFDO04 (dsl_out)	P10_4	Output	VDD33	Data output
	ENCIFOE04 (dsl_en)	P10_3	Output	VDD33	Drive/receive control
HFDSL5	ENCIFDI05 (dsl_in)	P12_7	Input	VDD1833_6	Data input
	ENCIFDO05 (dsl_out)	P12_6	Output	VDD1833_6	Data output
	ENCIFOE05 (dsl_en)	P12_5	Output	VDD1833_6	Drive/receive control
HFDSL6	ENCIFDI06 (dsl_in)	P34_1	Input	VDD1833_3	Data input
	ENCIFDO06 (dsl_out)	P34_0	Output	VDD1833_3	Data output
	ENCIFOE06 (dsl_en)	P33_7	Output	VDD1833_3	Drive/receive control
HFDSL7	ENCIFDI07 (dsl_in)	P34_5	Input	VDD1833_3	Data input
	ENCIFDO07 (dsl_out)	P34_4	Output	VDD1833_3	Data output
	ENCIFOE07 (dsl_en)	P34_3	Output	VDD1833_3	Drive/receive control
HFDSL8	ENCIFDI08 (dsl_in)	-	-	-	N.A.
	ENCIFDO08 (dsl_out)	-	-	-	N.A.
	ENCIFOE08 (dsl_en)	-	-	-	N.A.
HFDSL9	ENCIFDI09 (dsl_in)	P29_4	Input	VDD1833_2	Data input
	ENCIFDO09 (dsl_out)	P29_3	Output	VDD1833_2	Data output
	ENCIFOE09 (dsl_en)	P29_2	Output	VDD1833_2	Drive/receive control
HFDSL10	ENCIFDI10 (dsl_in)	P30_0	Input	VDD1833_2	Data input
	ENCIFDO10 (dsl_out)	P29_7	Output	VDD1833_2	Data output
	ENCIFOE10 (dsl_en)	P29_6	Output	VDD1833_2	Drive/receive control
HFDSL11	ENCIFDI11 (dsl_in)	P30_4	Input	VDD1833_2	Data input
	ENCIFDO11 (dsl_out)	P30_3	Output	VDD1833_2	Data output
	ENCIFOE11 (dsl_en)	P30_2	Output	VDD1833_2	Drive/receive control

Channel	Pin Name	I/O Port	Input /Output	Voltage Domain	Description
HFDSL12	ENCIFDI12 (dsl_in)	-	-	-	N.A.
	ENCIFDO12 (dsl_out)	-	-	-	N.A.
	ENCIFOE12 (dsl_en)	-	-	-	N.A.
HFDSL13	ENCIFDI13 (dsl_in)	P13_7	Input	VDD1833_6	Data input
	ENCIFDO13 (dsl_out)	P13_6	Output	VDD1833_6	Data output
	ENCIFOE13 (dsl_en)	P13_5	Output	VDD1833_6	Drive/receive control
HFDSL14	ENCIFDI14 (dsl_in)	P18_7	Input	VDD33	Data input
	ENCIFDO14 (dsl_out)	P18_6	Output	VDD33	Data output
	ENCIFOE14 (dsl_en)	P18_5	Output	VDD33	Drive/receive control
HFDSL15	ENCIFDI15 (dsl_in)	-	-	-	N.A.
	ENCIFDO15 (dsl_out)	-	-	-	N.A.
	ENCIFOE15 (dsl_en)	-	-	-	N.A.

## 4. Software

### 4.1 HFDSL Driver Function

The functions of the HFDSL driver are listed below.

1. Initial settings
2. Acquiring positional data
3. Transmitting and receiving messages

### 4.2 File Structure

For the file structure, refer to the release note for the RZ/N2H Group Encoder I/F HIPERFACE DSL Safety sample program.

### 4.3 Functions

The functions to be used are listed in the table below.

**Table 4.1 Functions**

Category	Function Name	Page Number
HFDSL driver API functions	R_HFDSL_Open	9
	R_HFDSL_Close	9
	R_HFDSL_GetVersion	10
	R_HFDSL_Control	10
User-defined functions	hfdsl_int_nml_callback	15
	hfdsl_int_err_callback	15
	hfdsl_int_safety_callback	16
	hfdsl_int_mrcv_callback	16
	hfdsl_int_smrcv_callback	17
Interrupt handlers	hfdsl_int_isr_chn (n=0 to 15)	17
	hfdsl_ints_isr_chn (n=0 to 15)	17
	hfdsl_fpr_isr_chn (n=0 to 15)	18
	hfdsl_sp_isr_chn (n=0 to 15)	18
	hfdsl_err_isr	18

## 4.4 Specifications of API Functions

### 4.4.1 R\_HFDSL\_Open

---

<b>R_HFDSL_Open</b>	
Synopsis	Starts controlling operation of the encoder.
Header	r_hfdsl_rzt2_if.h
Declaration	int32_t R_HFDSL_Open(const int32_t id, r_hfdsl_info_t* p_info);
Description	Call this function before using the HFDSL driver. It initializes the driver. <ul style="list-style-type: none"> <li>• Setting the interrupts</li> <li>• Setting the callback functions</li> </ul>
Argument	id : Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.) R_HFDSL0_ID : Specifies channel 0. R_HFDSL1_ID : Specifies channel 1. : : R_HFDSL15_ID : Specifies channel 15. Others : Setting is not allowed. p_info : Holder for the initial settings of the driver Set the pointer to the r_hfdsl_info_t structure which holds the information on the initial settings of the driver.
Return value	R_HFDSL_SUCCESS: Normal termination R_HFDSL_ERR_INVALID_ARG: Abnormal termination (The id or the r_hfdsl_info_t structure member pointed by p_info is not available or not specified.) R_HFDSL_ERR_ACCESS: Abnormal termination (This function is already executed.)
Note	The channels 8, 12, and 15 are not available in this sample program. Calling this API function from within a callback function is prohibited.

### 4.4.2 R\_HFDSL\_Close

---

<b>R_HFDSL_Close</b>	
Synopsis	Ending control of the encoder
Header	r_hfdsl_rzt2_if.h
Declaration	int32_t R_HFDSL_Close(const int32_t id);
Description	This function stops controlling operation of the encoder on the designated channel.
Argument	id : Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.) R_HFDSL0_ID : Specifies channel 0. R_HFDSL1_ID : Specifies channel 1. : : R_HFDSL15_ID : Specifies channel 15. Others : Setting is not allowed.
Return Value	R_HFDSL_SUCCESS: Normal termination R_HFDSL_ERR_INVALID_ARG: Abnormal termination (The id is not available or not specified.)
Note	Before calling this function, be sure to call R_HFDSL_Open. The channels 8, 12, and 15 are not available in this sample program. Calling this API function from within a callback function is prohibited.

### 4.4.3 R\_HFDSL\_GetVersion

---

#### R\_HFDSL\_GetVersion

---

Synopsis	Acquire the version number of the encoder interface driver.
Header	r_hfdsl_rzt2_if.h
Declaration	uint32_t R_HFDSL_GetVersion(void);
Description	This function acquires the version number of the HFDSL driver.
Argument	None
Return value	The major part of the version number is stored in the sixteen MSBs and the minor part of the version number is stored in the sixteen LSBs. Ex.) For ver.1.2, the value returned is 0x00010002.

### 4.4.4 R\_HFDSL\_Control

---

#### R\_HFDSL\_Control

---

Synopsis	Controlling operation of the encoder.																		
Header	r_hfdsl_rzt2_if.h																		
Declaration	int32_t R_HFDSL_Control(const int32_t id, const r_hfdsl_cmd_t cmd, void *const p_buf);																		
Description	This function controls operations of the encoder by using the cmd argument. See section “4.4.4(1), Protocol Initialization Commands” and section “4.4.4(2), Control Commands” for the operation.																		
Argument	<table> <tr> <td>id</td> <td>: Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.)</td> </tr> <tr> <td>R_HFDSL0_ID</td> <td>: Specifies channel 0.</td> </tr> <tr> <td>R_HFDSL1_ID</td> <td>: Specifies channel 1.</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>R_HFDSL15_ID</td> <td>: Specifies channel 15.</td> </tr> <tr> <td>Others</td> <td>: Setting is not allowed.</td> </tr> <tr> <td>cmd</td> <td>: Command</td> </tr> <tr> <td></td> <td>For details, see section “4.4.4(1), Protocol Initialization Commands” and section “4.4.4(2), Control Commands”.</td> </tr> <tr> <td>p_buf</td> <td>: Arguments corresponding to each cmd.</td> </tr> </table>	id	: Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.)	R_HFDSL0_ID	: Specifies channel 0.	R_HFDSL1_ID	: Specifies channel 1.	:	:	R_HFDSL15_ID	: Specifies channel 15.	Others	: Setting is not allowed.	cmd	: Command		For details, see section “4.4.4(1), Protocol Initialization Commands” and section “4.4.4(2), Control Commands”.	p_buf	: Arguments corresponding to each cmd.
id	: Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.)																		
R_HFDSL0_ID	: Specifies channel 0.																		
R_HFDSL1_ID	: Specifies channel 1.																		
:	:																		
R_HFDSL15_ID	: Specifies channel 15.																		
Others	: Setting is not allowed.																		
cmd	: Command																		
	For details, see section “4.4.4(1), Protocol Initialization Commands” and section “4.4.4(2), Control Commands”.																		
p_buf	: Arguments corresponding to each cmd.																		
Return value	R_HFDSL_SUCCESS: Normal termination R_HFDSL_ERR_INVALID_ARG: Abnormal termination (The id or cmd is not available or not specified.) See section “4.4.4(1), Protocol Initialization Commands” and section “4.4.4(2), Control Commands” for other returned values.																		
Note	The channels 8, 12, and 15 are not available in this sample program.																		

**(1) Protocol Initialization Commands****(a) R\_HFDSL\_CMD\_INIT**


---

<b>R_HFDSL_CMD_INIT</b>	
Synopsis	Protocol initialization
Header	r_hfdsl_rzt2_if.h
Declaration	int32_t R_HFDSL_Control(const int32_t id, const r_hfdsl_cmd_t cmd, void *const p_buf);
Description	Call this function after executing function R_HFDSL_Open or after a protocol reset. For how to detect a protocol reset, see section "4.5.2 hfdsl_int_err_callback".
Argument	id : Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.) R_HFDSL0_ID : Specifies channel 0. R_HFDSL1_ID : Specifies channel 1. : : R_HFDSL15_ID : Specifies channel 15. Others : Setting is not allowed. cmd : Specify R_HFDSL_CMD_INIT. p_buf : Specify NULL.
Return value	R_HFDSL_SUCCESS: Normal termination R_HFDSL_ERR_INVALID_ARG: Abnormal termination (The id or p_buf is invalid.) R_HFDSL_ERR_ACCESS: Abnormal termination (R_HFDSL_Open has not been executed.) R_HFDSL_ERR_INIT: Abnormal termination (Link check timed out.)
Note	The channels 8, 12, and 15 are not available in this sample program. Calling this API function from within a callback function is prohibited.

**(b) R\_HFDSL\_CMD\_ENCID**


---

<b>R_HFDSL_CMD_ENCID</b>	
Synopsis	Check encoder ID
Header	r_hfdsl_rzt2_if.h
Declaration	int32_t R_HFDSL_Control(const int32_t id, const r_hfdsl_cmd_t cmd, void *const p_buf);
Description	Call this function after the R_HFDSL_CMD_INIT protocol initialization command. If the value returned is R_HFDSL_ERR_INIT and the protocol is to be initialized again, start over again from the protocol initialization command R_HFDSL_CMD_INIT after executing the control command R_HFDSL_CMD_RST.
Argument	id : Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.) R_HFDSL0_ID : Specifies channel 0. R_HFDSL1_ID : Specifies channel 1. : : R_HFDSL15_ID : Specifies channel 15. Others : Setting is not allowed. cmd : Specify R_HFDSL_CMD_ENCID. p_buf : Encoder ID Specify the unit32_t pointer which holds the encoder ID.
Return value	R_HFDSL_SUCCESS: Normal termination R_HFDSL_ERR_INVALID_ARG: Abnormal termination (The id is invalid or p_buf is null.) R_HFDSL_ERR_ACCESS: Abnormal termination (R_HFDSL_CMD_INIT has not been executed.) R_HFDSL_ERR_INIT: Abnormal termination (The connected encoder ID does not match the specified ID.)
Note	The channels 8, 12, and 15 are not available in this sample program. Calling this API function from within a callback function is prohibited.

**(2) Control Commands****(a) R\_HFDSL\_CMD\_POS**


---

<b>R_HFDSL_CMD_POS</b>	
Synopsis	Acquiring the fast position
Header	r_hfdsl_rzt2_if.h
Declaration	int32_t R_HFDSL_Control(const int32_t id, const r_hfdsl_cmd_t cmd, void *const p_buf);
Description	This function acquires the fast position by reading the fast position registers (POS4 to POS0).
Argument	id : Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.) R_HFDSL0_ID : Specifies channel 0. R_HFDSL1_ID : Specifies channel 1. : : R_HFDSL15_ID : Specifies channel 15. Others : Setting is not allowed. cmd : Specify R_HFDSL_CMD_POS. p_buf : Fast position Specifies the pointer to the r_hfdsl_pos_t structure which holds the fast position value. For details, see section "4.10.1(2) r_hfdsl_pos_t".
Return value	R_HFDSL_SUCCESS: Normal termination R_HFDSL_ERR_INVALID_ARG: Abnormal termination (The id is invalid or p_buf is null.)
Note	The channels 8, 12, and 15 are not available in this sample program.

**(b) R\_HFDSL\_CMD\_VPOS**


---

<b>R_HFDSL_CMD_VPOS</b>	
Synopsis	Acquiring the safe position
Header	r_hfdsl_rzt2_if.h
Declaration	int32_t R_HFDSL_Control(const int32_t id, const r_hfdsl_cmd_t cmd, void *const p_buf);
Description	This function acquires the safe position by reading the safe position registers (VPOS4 to VPOS0), and safe position CRC registers (VPOSCRC_H, VPOSCRC_L). If the safety channel 1 interface register access is disabled, this function returns access error.
Argument	id : Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.) R_HFDSL0_ID : Specifies channel 0. R_HFDSL1_ID : Specifies channel 1. : : R_HFDSL15_ID : Specifies channel 15. Others : Setting is not allowed. cmd : Specify R_HFDSL_CMD_VPOS. p_buf : Safe position Specifies the pointer to the r_hfdsl_vpos_t structure which holds the safe position value. For details, see section "4.10.1(3) r_hfdsl_vpos_t".
Return value	R_HFDSL_SUCCESS: Normal termination R_HFDSL_ERR_INVALID_ARG: Abnormal termination (The id is invalid or p_buf is null.) R_HFDSL_ERR_ACCESS: Abnormal termination (Access to the safety channel 1 interface registers is disabled.)
Note	The channels 8, 12, and 15 are not available in this sample program.

**(c) R\_HFDSL\_CMD\_VEL**


---

<b>R_HFDSL_CMD_VEL</b>	
Synopsis	Acquiring the rotational velocity of the motor.
Header	r_hfdsl_rzt2_if.h
Declaration	int32_t R_HFDSL_Control(const int32_t id, const r_hfdsl_cmd_t cmd, void *const p_buf);
Description	This function acquires the rotational velocity of the motor by reading the velocity registers (VEL2 to VEL0).
Argument	id : Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.) R_HFDSL0_ID : Specifies channel 0. R_HFDSL1_ID : Specifies channel 1. : : R_HFDSL15_ID : Specifies channel 15. Others : Setting is not allowed. cmd : Specify R_HFDSL_CMD_VEL. p_buf : Rotational velocity of the motor Specifies the pointer to uint32_t which holds the rotational velocity of the motor.
Return value	R_HFDSL_SUCCESS: Normal termination R_HFDSL_ERR_INVALID_ARG: Abnormal termination (The id is invalid or p_buf is null.)
Note	The channels 8, 12, and 15 are not available in this sample program.

**(d) R\_HFDSL\_CMD\_MSG**


---

<b>R_HFDSL_CMD_MSG</b>	
Synopsis	Transmitting messages
Header	r_hfdsl_rzt2_if.h
Declaration	int32_t R_HFDSL_Control(const int32_t id, const r_hfdsl_cmd_t cmd, void *const p_buf);
Description	This function transmits messages. The data received is indicated by function hfdsl_int_mrcv_callback. For details of the function, see section "4.5.4 hfdsl_int_mrcv_callback".
Argument	id : Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.) R_HFDSL0_ID : Specifies channel 0. R_HFDSL1_ID : Specifies channel 1. : : R_HFDSL15_ID : Specifies channel 15. Others : Setting is not allowed. cmd : Specify R_HFDSL_CMD_MSG. p_buf : Message data for transmission Specifies the pointer to the r_hfdsl_send_msg_t structure which holds message data for transmission. For details, see section "4.10.1(4) r_hfdsl_send_msg_t".
Return value	R_HFDSL_SUCCESS: Normal termination R_HFDSL_ERR_INVALID_ARG: Abnormal termination (The id is invalid or p_buf is null.) R_HFDSL_ERR_ACCESS: Abnormal termination (The protocol initialization function described in section "4.4.4(1) Protocol Initialization Commands", has not been executed.)
Note	The channels 8, 12, and 15 are not available in this sample program. Calling this API function from within a callback function is prohibited. To proceed with the next transmission, execute this function following the hfdsl_int_mrcv_callback function.

**(e) R\_HFDSL\_CMD\_RST**


---

<b>R_HFDSL_CMD_RST</b>	
Synopsis	Protocol reset
Header	r_hfdsl_rzt2_if.h
Declaration	int32_t R_HFDSL_Control(const int32_t id, const r_hfdsl_cmd_t cmd, void *const p_buf);
Description	This function resets the protocol. After this function is called, an HDSL <sub>n</sub> _INT interrupt is generated in response to the PRST bit in the EVENT_H being set to 1. To resume communications, call the functions described in section “4.4.4(1), Protocol Initialization Commands”.
Argument	id : Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.) R_HFDSL0_ID : Specifies channel 0. R_HFDSL1_ID : Specifies channel 1. : : R_HFDSL15_ID : Specifies channel 15. Others : Setting is not allowed. cmd : Specify  R_HFDSL_CMD_RST. p_buf : Specify NULL.
Return value	R_HFDSL_SUCCESS: Normal termination R_HFDSL_ERR_INVALID_ARG: Abnormal termination (The id or p_buf is invalid.)
Note	The channels 8, 12, and 15 are not available in this sample program.

**(f) R\_HFDSL\_CMD\_SMSG**


---

<b>R_HFDSL_CMD_SMSG</b>	
Synopsis	Transmitting short message
Header	r_hfdsl_rzt2_if.h
Declaration	int32_t R_HFDSL_Control(const int32_t id, const r_hfdsl_cmd_t cmd, void *const p_buf);
Description	This function transmits messages. The data received is indicated by function hfdsl_int_smrcv_callback. For details of the function, see section “4.5.5. hfdsl_int_smrcv_callback”.
Argument	id : Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.) R_HFDSL0_ID : Specifies channel 0. R_HFDSL1_ID : Specifies channel 1. : : R_HFDSL15_ID : Specifies channel 15. Others : Setting is not allowed. cmd : Specify R_HFDSL_CMD_SMSG. p_buf : Message data for transmission Specifies the pointer to the r_hfdsl_send_msg_t structure which holds message data for transmission. For details, see section “4.10.1(4) r_hfdsl_send_msg_t”.
Return value	R_HFDSL_SUCCESS: Normal termination R_HFDSL_ERR_INVALID_ARG: Abnormal termination (The id is invalid or p_buf is null.) R_HFDSL_ERR_ACCESS: Abnormal termination (The protocol initialization function described in section “4.4.4(1) Protocol Initialization Commands”, has not been executed.)
Note	The channels 8, 12, and the 15 are not available in this sample program. Calling this API function from within a callback function is prohibited. To proceed with a next transmission, execute this function following the hfdsl_int_smrcv_callback function.

## 4.5 Specifications of User-defined Functions

### 4.5.1 hfdsl\_int\_nml\_callback

---

<b>hfdsl_int_nml_callback</b>	
Synopsis	Indicating the generation of HDSL <sub>n</sub> _FPR interrupt
Header	-
Declaration	void hfdsl_int_nml_callback(uint8_t event);
Description	This callback function is registered with the member variable p_cb_nml of the argument r_hfdsl_info_t structure of the R_HFDSL_Open function. It is called when an HDSL <sub>n</sub> _FPR interrupt is generated. This interrupt shows that the fast position registers (POS4 to POS0) have been updated. The fast position can be acquired by executing the function R_HFDSL_Control (R_HFDSL_CMD_POS) from within this function. This function is the context of the interrupt handler. To ensure interrupt responsiveness, return immediately. The function name is an example and can be set freely.
Argument	event : Source of the interrupt Holds the value POS_RDY_BIT. The value of this argument is only valid within this function.
Return value	None

### 4.5.2 hfdsl\_int\_err\_callback

---

<b>hfdsl_int_err_callback</b>	
Synopsis	Indicating the generation of HDSL <sub>n</sub> _INT interrupt
Header	-
Declaration	void hfdsl_int_err_callback(uint32_t event_err);
Description	This callback function is registered with the member variable p_cb_err of the argument r_hfdsl_info_t structure of the R_HFDSL_Open function. It is called when an HDSL <sub>n</sub> _INT interrupt is generated in response to the SUM, POS, DTE or PRST bits in the EVENT_H register, or the MIN, ANS or QMLW bits in the EVENT_L register being set to 1. This function is the context of the interrupt handler. To ensure interrupt responsiveness, return immediately. The function name is an example and can be set freely.
Argument	event_err : Source of the HDSL <sub>n</sub> _INT interrupt Holds the value of the EVENT_H, EVENT_L registers. The value of this argument is only valid within this function.
Return value	None
Note	This function is not called when an HDSL <sub>n</sub> _INT is generated in response to the FREL bit in the EVENT_L register being set to 1.

### 4.5.3 hfdsI\_int\_safety\_callback

---

<b>hfdsI_int_safety_callback</b>	
Synopsis	Indicating the generation of HDSL <sub>n</sub> _SP interrupt
Header	-
Declaration	void hfdsI_int_safety_callback(uint8_t *p_safety1, uint8_t *p_safety2);
Description	<p>This callback function is registered with the member variable p_cb_safety of the argument r_hfdsI_info_t structure of the R_HFDSL_Open function. It is called when an HDSL<sub>n</sub>_SP interrupt is generated. This interrupt shows that the safety position registers have been updated.</p> <p>This function is the context of the interrupt handler. To ensure interrupt responsiveness, return immediately. The function name is an example and can be set freely.</p>
Argument	<p>p_safety1[] : Safety channel 1 status, position, and CRC            If the safety channel 1 interface register access is enabled. the array pointed by p_safety1 holds safety channel 1 status (SAFE_SUM) register data, safe position (VPOS4 to VPOS0) register data, and safe position CRC (VPOSCRC_H, VPOSCRC_L) register data.            If the safety channel 1 interface register access is disabled, p_safety1 holds NULL pointer.            The value of this argument is only valid within this function.</p> <p>p_safety2[] : Safety channel 2 status, position, and CRC            If the safety channel 2 interface register access is enabled. the array pointed by p_safety2 holds safety channel 2 status (STATUS2) register data, safe position (VPOS24 to VPOS20) register data, and safe position CRC2 (VPOSCRC2_H, VPOSCRC2_L) register data.            If the safety channel 2 interface register access is disabled, p_safety2 holds NULL pointer.            The value of this argument is only valid within this function.</p>
Return value	None

### 4.5.4 hfdsI\_int\_mrcv\_callback

---

<b>hfdsI_int_mrcv_callback</b>	
Synopsis	Indicating that the HDSL <sub>n</sub> _INT interrupt by the FREL bit in the EVENT_L register has occurred.
Header	-
Declaration	void hfdsI_int_mrcv_callback(uint8_t* msg_data);
Description	<p>This callback function is registered with the R_HFDSL_Control (R_HFDSL_CMD_MSG) function. It is called when the HDSL<sub>n</sub>_INT interrupt by the FREL bit in the EVENT_L register occurs, and data storage of the received message is completed.</p> <p>This function is the context of the interrupt handler. To ensure interrupt responsiveness, return immediately. The function name is an example and can be set freely.</p>
Argument	<p>msg_data[] : Message address and PC_BUFF register values (long messages)            Two bytes of the message address (PC_ADD_H, PC_ADD_L) and the values of the PC_BUF0 to PC_BUF7 registers (long messages) are stored.            The fifth bit LOFF of the message address PC_ADD_H holds the message reception error flag.            The value of this argument remains valid until the next HDSL<sub>n</sub>_INT interrupt caused by the FREL bit is generated.</p>
Return value	None

### 4.5.5 hfdsI\_int\_smrcv\_callback

---

#### hfdsI\_int\_smrcv\_callback

---

<b>Synopsis</b>	Indicating that the HDSL $n$ _INTS interrupt by the FRES bit in the EVENT_S register has occurred.
<b>Header</b>	-
<b>Declaration</b>	void hfdsI_int_smrcv_callback(uint8_t* msg_data);
<b>Description</b>	This callback function is registered with the R_HFDSL_Control (R_HFDSL_CMD_MSG) function. It is called when the HDSL $n$ _INTS interrupt by the FRES bit in the EVENT_S register occurs, and data storage of the received message is completed. This function is the context of the interrupt handler. To ensure interrupt responsiveness, return immediately. The function name is an example and can be set freely.
<b>Argument</b>	msg_data[] : PC_DATA register value PC_DATA register value (as short messages) is stored. The value of this argument remains valid until the next HDSL $n$ _INTS interrupt caused by the FRES bit is generated.
<b>Return value</b>	None

## 4.6 Interrupt Handler

### 4.6.1 hfdsI\_int\_isr\_chn (n=0 to 15)

---

#### hfdsI\_int\_isr\_chn

---

<b>Synopsis</b>	Interrupt handler for the HDSL $n$ _INT
<b>Header</b>	-
<b>Declaration</b>	static void hfdsI_int_isr_chn(void);
<b>Description</b>	An interrupt handler for the HDSL $n$ _INT interrupt. If the source of an interrupt is the FREL bit of the EVENT_L register, function hfdsI_int_mrcv_callback is called as a callback function. If the source of an interrupt is other bits of the EVENT_H register and the EVENT_L register, function hfdsI_int_err_callback is called as a callback function.
<b>Argument</b>	None
<b>Return value</b>	None
<b>Note</b>	The channels 8, 12, and 15 are not available in this sample program. There are no interrupt handlers for unavailable channels.

### 4.6.2 hfdsI\_ints\_isr\_chn (n=0 to 15)

---

#### hfdsI\_ints\_isr\_chn

---

<b>Synopsis</b>	Interrupt handler for the HDSL $n$ _INTS
<b>Header</b>	-
<b>Declaration</b>	static void hfdsI_ints_isr_chn(void);
<b>Description</b>	An interrupt handler for the HDSL $n$ _INTS interrupt. If the source of an interrupt is the FRES bit of the EVENT_S register, function hfdsI_int_smrcv_callback is called as a callback function.
<b>Argument</b>	None
<b>Return value</b>	None
<b>Note</b>	The channel 8, 12, and 15 are not available in this sample program. There are no interrupt handlers for unavailable channels.

### 4.6.3 hfdsI\_fpr\_isr\_chn (n=0 to 15)

---

#### hfdsI\_fpr\_isr\_chn

---

<b>Synopsis</b>	Interrupt handler for the HDSL $n$ _FPR
<b>Header</b>	-
<b>Declaration</b>	static void hfdsI_fpr_isr_chn(void);
<b>Description</b>	An interrupt handler for the HDSL $n$ _FPR interrupt. If the interrupt is generated, function hfdsI_int_nml_callback is called as a callback function.
<b>Argument</b>	None
<b>Return value</b>	None
<b>Note</b>	The channels 8, 12, and 15 are not available in this sample program. There are no interrupt handlers for unavailable channels.

### 4.6.4 hfdsI\_sp\_isr\_chn (n=0 to 15)

---

#### hfdsI\_sp\_isr\_chn

---

<b>Synopsis</b>	Interrupt handler for the HDSL $n$ _SP
<b>Header</b>	-
<b>Declaration</b>	static void hfdsI_sp_isr_chn(void);
<b>Description</b>	An interrupt handler for the HDSL $n$ _SP interrupt. If the interrupt is generated, function hfdsI_int_safety_callback is called as a callback function.
<b>Argument</b>	None
<b>Return value</b>	None
<b>Note</b>	The channels 8, 12, and 15 are not available in this sample program. There are no interrupt handlers for unavailable channels.

### 4.6.5 hfdsI\_err\_isr

---

#### hfdsI\_err\_isr

---

<b>Synopsis</b>	Interrupt handler for the PERI_ERR0
<b>Header</b>	-
<b>Declaration</b>	static void hfdsI_err_isr(void);
<b>Description</b>	An interrupt handler for the PERI_ERR0 interrupt. If the interrupt is generated, this function reads error events from ENCIFERR_STAT $n$ (n=1 to 4) register and clear interrupt.
<b>Argument</b>	None
<b>Return value</b>	None

## 4.7 Interrupts

Table 4.2 lists the interrupts for the HFDSL driver.

**Table 4.2 Interrupts for the HFDSL Driver**

Interrupts	ID *1		Description
	CR52 ver.	CA55 ver.	
HDSL0_INT	388	716	Generated when the value of any bit in the ch0 EVENT_L, EVENT_H registers is updated to 1.
HDSL0_INTS	389	717	Generated when the short message of the ch0 is received.
HDSL0_FPR	390	718	Generated when the fast position value of the ch0 is ready to read.
HDSL0_SP	391	719	Generated when the safety position value of the ch0 is ready to read.
HDSL1_INT	392	720	Generated when the value of any bit in the ch1 EVENT_L, EVENT_H registers is updated to 1.
HDSL1_INTS	393	721	Generated when the short message of the ch1 is received.
HDSL1_FPR	394	722	Generated when the fast position value of the ch1 is ready to read.
HDSL1_SP	395	723	Generated when the safety position value of the ch1 is ready to read.
HDSL2_INT	396	724	Generated when the value of any bit in the ch2 EVENT_L, EVENT_H registers is updated to 1.
HDSL2_INTS	397	725	Generated when the short message of the ch2 is received.
HDSL2_FPR	398	726	Generated when the fast position value of the ch2 is ready to read.
HDSL2_SP	399	727	Generated when the safety position value of the ch2 is ready to read.
HDSL3_INT	400	728	Generated when the value of any bit in the ch3 EVENT_L, EVENT_H registers is updated to 1.
HDSL3_INTS	401	729	Generated when the short message of the ch3 is received.
HDSL3_FPR	402	730	Generated when the fast position value of the ch3 is ready to read.
HDSL3_SP	403	731	Generated when the safety position value of the ch3 is ready to read.
HDSL4_INT	404	732	Generated when the value of any bit in the ch4 EVENT_L, EVENT_H registers is updated to 1.
HDSL4_INTS	405	733	Generated when the short message of the ch4 is received.
HDSL4_FPR	406	734	Generated when the fast position value of the ch4 is ready to read.
HDSL4_SP	407	735	Generated when the safety position value of the ch4 is ready to read.
HDSL5_INT	408	736	Generated when the value of any bit in the ch5 EVENT_L, EVENT_H registers is updated to 1.
HDSL5_INTS	409	737	Generated when the short message of the ch5 is received.
HDSL5_FPR	410	738	Generated when the fast position value of the ch5 is ready to read.
HDSL5_SP	411	739	Generated when the safety position value of the ch5 is ready to read.
HDSL6_INT	412	740	Generated when the value of any bit in the ch6 EVENT_L, EVENT_H registers is updated to 1.
HDSL6_INTS	413	741	Generated when the short message of the ch6 is received.
HDSL6_FPR	414	742	Generated when the fast position value of the ch6 is ready to read.
HDSL6_SP	415	743	Generated when the safety position value of the ch6 is ready to read.
HDSL7_INT	416	744	Generated when the value of any bit in the ch7 EVENT_L, EVENT_H registers is updated to 1.
HDSL7_INTS	417	745	Generated when the short message of the ch7 is received.
HDSL7_FPR	418	746	Generated when the fast position value of the ch7 is ready to read.
HDSL7_SP	419	747	Generated when the safety position value of the ch7 is ready to read.
HDSL8_INT	-	-	This interrupt request is not used. *2
HDSL8_INTS	-	-	This interrupt request is not used. *2
HDSL8_FPR	-	-	This interrupt request is not used. *2
HDSL8_SP	-	-	This interrupt request is not used. *2

Interrupts	ID *1		Description
	CR52 ver.	CA55 ver.	
HDSL9_INT	420	752	Generated when the value of any bit in the ch9 EVENT_L, EVENT_H registers is updated to 1.
HDSL9_INTS	421	753	Generated when the short message of the ch9 is received.
HDSL9_FPR	422	754	Generated when the fast position value of the ch9 is ready to read.
HDSL9_SP	423	755	Generated when the safety position value of the ch9 is ready to read.
HDSL10_INT	424	756	Generated when the value of any bit in the ch10 EVENT_L, EVENT_H registers is updated to 1.
HDSL10_INTS	425	757	Generated when the short message of the ch10 is received.
HDSL10_FPR	426	758	Generated when the fast position value of the ch10 is ready to read.
HDSL10_SP	427	759	Generated when the safety position value of the ch10 is ready to read.
HDSL11_INT	428	760	Generated when the value of any bit in the ch11 EVENT_L, EVENT_H registers is updated to 1.
HDSL11_INTS	429	761	Generated when the short message of the ch11 is received.
HDSL11_FPR	430	762	Generated when the fast position value of the ch11 is ready to read.
HDSL11_SP	431	763	Generated when the safety position value of the ch11 is ready to read.
HDSL12_INT	-	-	This interrupt request is not used. *2
HDSL12_INTS	-	-	This interrupt request is not used. *2
HDSL12_FPR	-	-	This interrupt request is not used. *2
HDSL12_SP	-	-	This interrupt request is not used. *2
HDSL13_INT	432	768	Generated when the value of any bit in the ch13 EVENT_L, EVENT_H registers is updated to 1.
HDSL13_INTS	433	769	Generated when the short message of the ch13 is received.
HDSL13_FPR	434	770	Generated when the fast position value of the ch13 is ready to read.
HDSL13_SP	435	771	Generated when the safety position value of the ch13 is ready to read.
HDSL14_INT	436	772	Generated when the value of any bit in the ch14 EVENT_L, EVENT_H registers is updated to 1.
HDSL14_INTS	437	773	Generated when the short message of the ch14 is received.
HDSL14_FPR	438	774	Generated when the fast position value of the ch14 is ready to read.
HDSL14_SP	439	775	Generated when the safety position value of the ch14 is ready to read.
HDSL15_INT	-	-	This interrupt request is not used. *2
HDSL15_INTS	-	-	This interrupt request is not used. *2
HDSL15_FPR	-	-	This interrupt request is not used. *2
HDSL15_SP	-	-	This interrupt request is not used. *2
PERI_ERR0	440	417	Generated when the value of any bit indicating HDSL ch0 to ch15 error in the ENCIFERR_STATn (n=1 to 4) register is updated to 1.

- Note: 1. This sample program has a CR52 version that runs on the CPU core Cortex-R52 and a CA55 version that runs on the CPU core Cortex-A55. CR52 ver. and CA55 ver. are descriptions of the respective version.
2. The channel 8, the channel 12, and the channel 15 are not available in this sample program. The interrupt requests HDSL8\_INT, HDSL8\_INTS, HDSL8\_FPR, HDSL8\_SP, HDSL12\_INT, HDSL12\_INTS, HDSL12\_FPR, HDSL12\_SP, HDSL15\_INT, HDSL15\_INTS, HDSL15\_FPR and HDSL15\_SP are not generated.

## 4.8 Constants and Error Codes

The tables below list the constants and error codes. For the definitions, see the respective tables.

**Table 4.3 User-defined Constants for the HFDSL Driver (r\_hfdsl\_rzt2\_config.h)**

Constant Name	Setting	Description
R_HFDSL_SYNC_CTRL	3	Setting of the SYNC_CTRL register
R_HFDSL_ACC_ERR	31	Setting of the ACC_ERR register
R_HFDSL_MASK_H	4Bh	Setting of the MASK_H register *1
R_HFDSL_MASK_L	36h	Setting of the MASK_L register *1
R_HFDSL_MASK_S	01h	Setting of the MASK_S register

Note: 1. To change R\_HFDSL\_MASK\_H and R\_HFDSL\_MASK\_L, change processing of the hfdsl\_int\_isr\_chn (n=0 to 15) function in accord with the settings in the R\_HFDSL\_MASK\_H and R\_HFDSL\_MASK\_L.

**Table 4.4 Error Codes**

Constant Name	Setting	Description
R_HFDSL_SUCCESS	0	Normal termination
R_HFDSL_ERR_INVALID_ARG	-1	Argument error
R_HFDSL_ERR_ACCESS	-2	API execution order error, register access error
R_HFDSL_ERR_INIT	-3	Failure in initialization of the HFDSL controller and encoder

**Table 4.5 Interface Mode Codes for the Safe Interface**

Constant Name	Setting	Description
R_HFDSL_SP_INTERNAL_BUS_MODE	0	Internal bus mode
R_HFDSL_SP_SPI_MODE	1	SPI mode

## 4.9 Fixed-width Integers

Table 4.6 lists the fixed-width integers for the sample code. The fixed-width integers used in the sample code are defined in the standard library.

**Table 4.6 Fixed-width Integers for the Sample Code**

Symbols	Description
int8_t	8-bit signed integer
int16_t	16-bit signed integer
int32_t	32-bit signed integer
int64_t	64-bit signed integer
uint8_t	8-bit unsigned integer
uint16_t	16-bit unsigned integer
uint32_t	32-bit unsigned integer
uint64_t	64-bit unsigned integer

## 4.10 Structures, Unions, and Enumerated Types

The major structures, unions, and enumerated types are listed below.

### 4.10.1 Structures

#### (1) r\_hfdsl\_info\_t

Information on initialization of the HFDSL driver

```
typedef struct
{
    uint8_t          safe1_if_mode;  Select the interface mode for safety channel 1 interface.
                                (0: Internal bus mode, 1: SPI mode) *1
    uint8_t          safe2_if_mode;  Select the interface mode for safety channel 2 interface.
                                (0: Internal bus mode, 1: SPI mode) *1
    r_hfdsl_int_nml_cb_t  p_cb_nml;  Pointer to the callback function to be called when an
                                HDSLn_FPR interrupt is generated.
                                For details, see section "4.5.1, hfdsl_int_nml_callback". *2
                                *3
    r_hfdsl_int_err_cb_t  p_cb_err;  Pointer to the callback function to be called when an
                                HDSLn_INT interrupt is generated.
                                For details, see section "4.5.2, hfdsl_int_err_callback". *2
    r_hfdsl_int_safety_cb_t  p_cb_safety;  Pointer to the callback function to be called when an
                                HDSLn_SP interrupt is generated.
                                For details, see section "4.5.3, hfdsl_int_safety_callback".
                                *2
} r_hfdsl_info_t
```

- Note:
1. If the SPI mode is selected for safety channel interface, access to the safety channel interface registers from sample program is disabled. SPI mode is used to access the safety channel registers by external CPU via SPI interface.
  2. This function is not called if NULL is specified.
  3. This function is not called when an HDSLn\_INT interrupt is generated in response to the FREL bit in the EVENT\_L register being set to 1.

#### (2) r\_hfdsl\_pos\_t

For storing fast position

```
typedef struct
{
    bool            all;            Enables the member variable posh.
                                (true: The member variable posh is enabled,
                                false: The member variable is disabled)
    uint8_t        posh;           Holds bits [39:32] of the fast position.
                                The value is updated when the member variable all is true.
    uint32_t       pos;           Holds bits [31:0] of the fast position.
} r_hfdsl_pos_t
```

**(3) r\_hfdsl\_vpos\_t**

For storing the safe position

```
typedef struct
{
    uint8_t          vposh;    Holds bits [39:32] of the safe position.
    uint32_t         vpos;    Holds bits [31:0] of the safe position.
    uint16_t         crc;     Holds the CRC of the vertical channel
} r_hfdsl_vpos_t
```

**(4) r\_hfdsl\_send\_msg\_t**

For storing message data for transmission.

```
typedef struct
{
    uint8_t          *p_data;  Pointer to the array which holds message data for transmission
                                In the case of using with R_HFDSL_CMD_MSG control
                                command, set the pointer to the array which holds message data
                                for transmission.
                                In reading case with R_HFDSL_CMD_SMSG command, set the
                                pointer to the array which holds R_HFDSL_SMSG_READ and
                                address to read. In writing case with R_HFDSL_CMD_SMSG
                                command, set the pointer to the array which holds
                                R_HFDSL_SMSG_WRITE, address, and data to write.
    r_hfdsl_msg_cb_t p_cb_msg; Pointer to the callback function to be called when a message is
                                received.
                                For details, see sections "4.5.4, hfdsl_int_mrcv_callback" and
                                "4.5.5 hfdsl_int_smrcv_callback".
                                Be sure to set the address of hfdsl_int_mrcv_callback in case of
                                using with R_HFDSL_CMD_MSG control command. Set the
                                address of hfdsl_int_smrcv_callback in reading case with
                                R_HFDSL_CMD_SMSG control command.
                                In writing case with R_HFDSL_CMD_SMSG control commad, no
                                callback operation is generated. Set NULL for p_cb_msg.
} r_hfdsl_send_msg_t
```

**4.10.2 Unions**

Not used.

**4.10.3 Enumerated Types**

Not used.

## 4.11 Description of the Sample Program

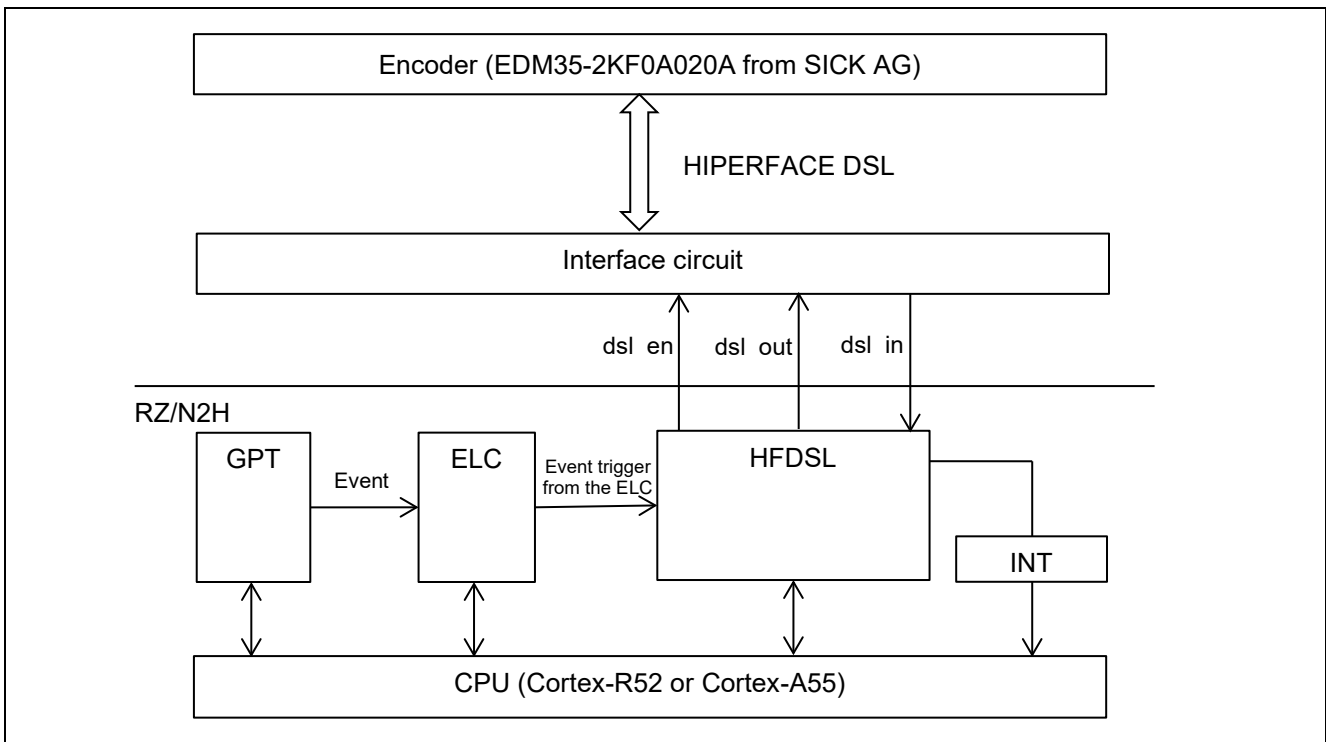
### 4.11.1 Outline of Operations

This sample program supports the encoder (EDM35-2KF0A020A from SICK AG) compliant with the HIPERFACE DSL communications protocols specification. It handles the following processing.

- 1) Indicates the following information by using a command input from the console.
  - A) Fast and safe positions
  - B) Rotational velocity of the motor
  - C) Results of transmission and reception of long messages (the type of encoder from resources)
  - D) Vertical channel data
  - E) Received status (ENC\_ST0) by short message
- 2) Runs in SYNC mode.
- 3) This sample program ends by detecting a protocol reset.

#### (1) System Block Diagram

Figure 4.1 shows a block diagram of the system.



**Figure 4.1 System Block Diagram**

## (2) Software Configuration

Figure 4.2 is a block diagram of the software.

The HFDSL driver has six sections: the opening process part configured of function R\_HFDSL\_Open, the closing process part configured of function R\_HFDSL\_Close, the protocol initialization, positional value acquisition, and message transmission parts configured of function R\_HFDSL\_Control, and the data reception part (interrupt handler) configured of the callback function.

The HFDSL driver controller section of the sample program controls the HFDSL driver, acquires the positional value, and sends messages. The results indication section (callback) displays the results of data reception.

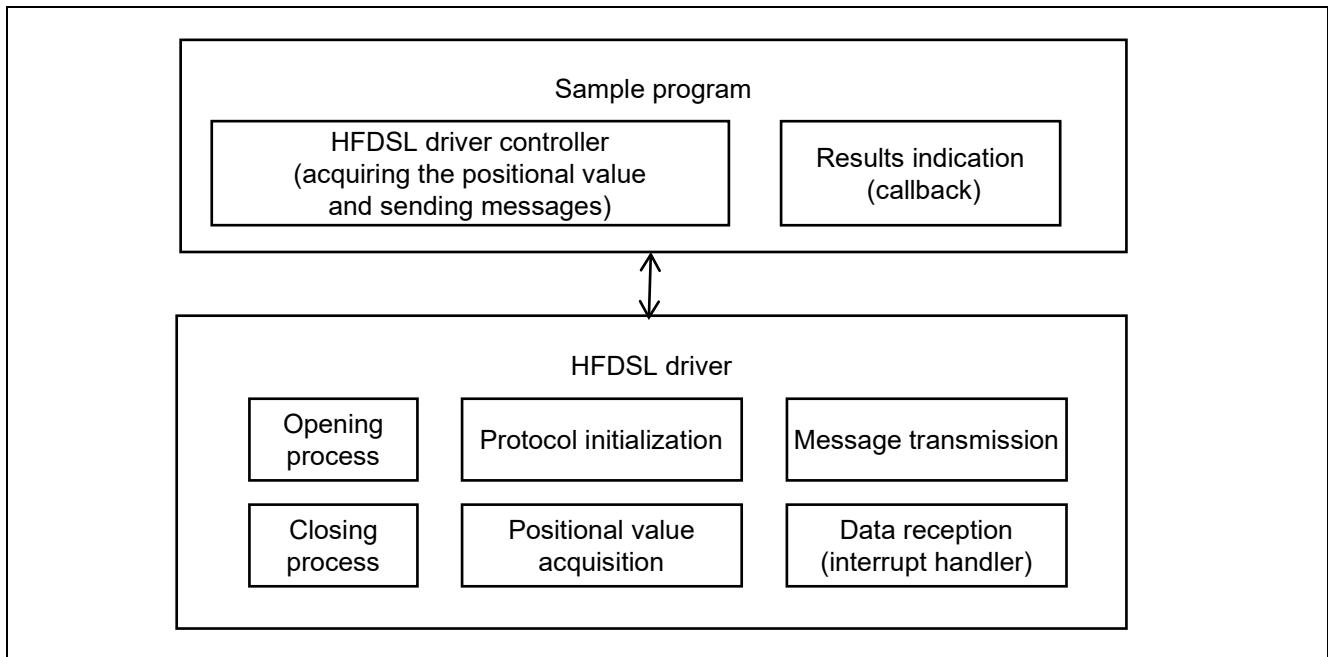


Figure 4.2 Software Configuration

### 4.11.2 Variables for the Sample Program

Table 4.7 lists the major static variables.

**Table 4.7 Major Static Variables**

Type	Variable Name	Description
bool	mrcv_flg	Message transfer completed flag (true: Transfer of messages has been completed false: Transfer of messages is in progress)
bool	prst_found	Protocol reset warning detection flag (true: Protocol reset warning is detected false: Protocol reset warning is not detected)
uint32_t	err_info	Holds the HDSLn_INT interrupt source.
uint32_t	pos_rot	Holds the number of rotations with the fast position.
uint32_t	pos_res	Holds the angle of the fast position.
bool	vpos_valid	Holds result of the safe position is valid or not.
uint32_t	vpos_rot	Holds the number of rotations with the safe positions.
uint32_t	vpos_res	Holds the angle of the safe position.
uint32_t	vel	Holds the rotational velocity of the motor.
uint8_t	lmsg_rcv[LMSG_REC_SIZE]	Holds received data in long messages.
uint8_t	smsg_rcv	Holds received short message data.
bool	safety1_valid	Holds result of the safety channel 1 data is valid or not.
bool	safety2_valid	Holds result of the safety channel 2 data is valid or not.
uint8_t	safety1[SAFETY_CNT_MAX]	Holds the received safety channel 1 data.
uint8_t	safety2[SAFETY_CNT_MAX]	Holds the received safety channel 2 data.

### 4.11.3 Constants for the Sample Program

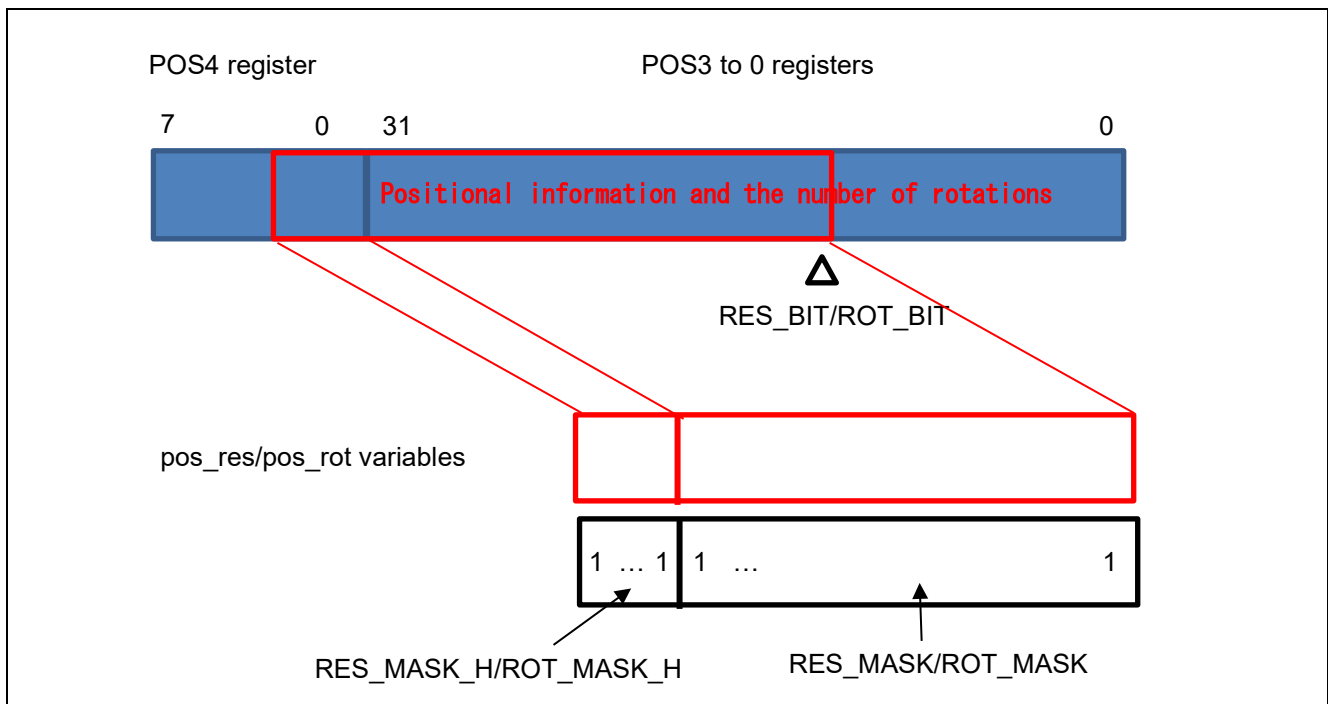
Table 4.8 lists the major constants for the sample program.

**Table 4.8 Major Constants**

Constant Name	Setting	Description
ENC_ID	00000153h	Encoder ID of EDM35-2KF0A020A *1 *2
RES_BIT	0	Position of the least significant bit of the positional information in the POS4 to 0 registers *1
RES_MASK	000FFFFFh	Masking of the positional information in the POS3 to 0 registers *1
RES_MASK_H	00000000h	Masking of the positional information in the POS4 register *1
ROT_BIT	20	Position of the least significant bit of the rotational information in the POS4 to 0 registers *1
ROT_MASK	00000FFFh	Masking of the number of rotations in the POS3 to 0 registers *1
ROT_MASK_H	00000000h	Masking of the number of rotations in the POS4 register *1
LMSG_RECV_SIZE	10	Maximum size of received data in long messages
SAFETY_CNT_MAX	8	Storing data size of the safety channels
TIMEOUT_UNIT	1000	Setting of timeout unit (1 ms)
TIMEOUT_COUNT	1000	Setting of timeout (1 ms x 1000)
INIT_RETRY_COUNT	10	Retry times of initialization error

- Note: 1. To run the sample program with an encoder other than an EDM35-2KF0A020A, change the settings to suit the specifications of the connected encoder.  
 2. Refer to the “HIPERFACE DSL® MASTER Safety Integration Manual” for details.

The figure below shows the mechanism for storing the positional and rotational information.



**Figure 4.3 Mechanism for Storing the Positional and Rotational Information**

#### 4.11.4 Flowchart of Main Processing

The flowchart below shows processing by the main function.

Processing marked with \* in the figure is shown separately in a subsequent flowchart.

##### (1) Flowchart of enc\_main

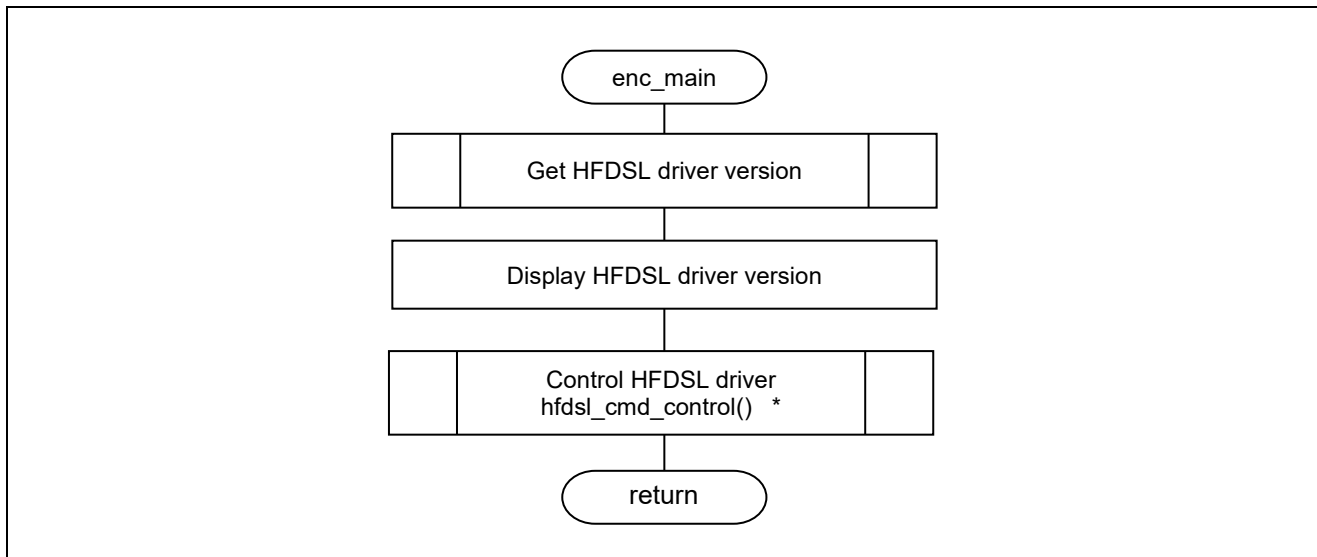


Figure 4.4 Flowchart of the `enc_main` Function

(2) Flowchart of hfdsI\_cmd\_control

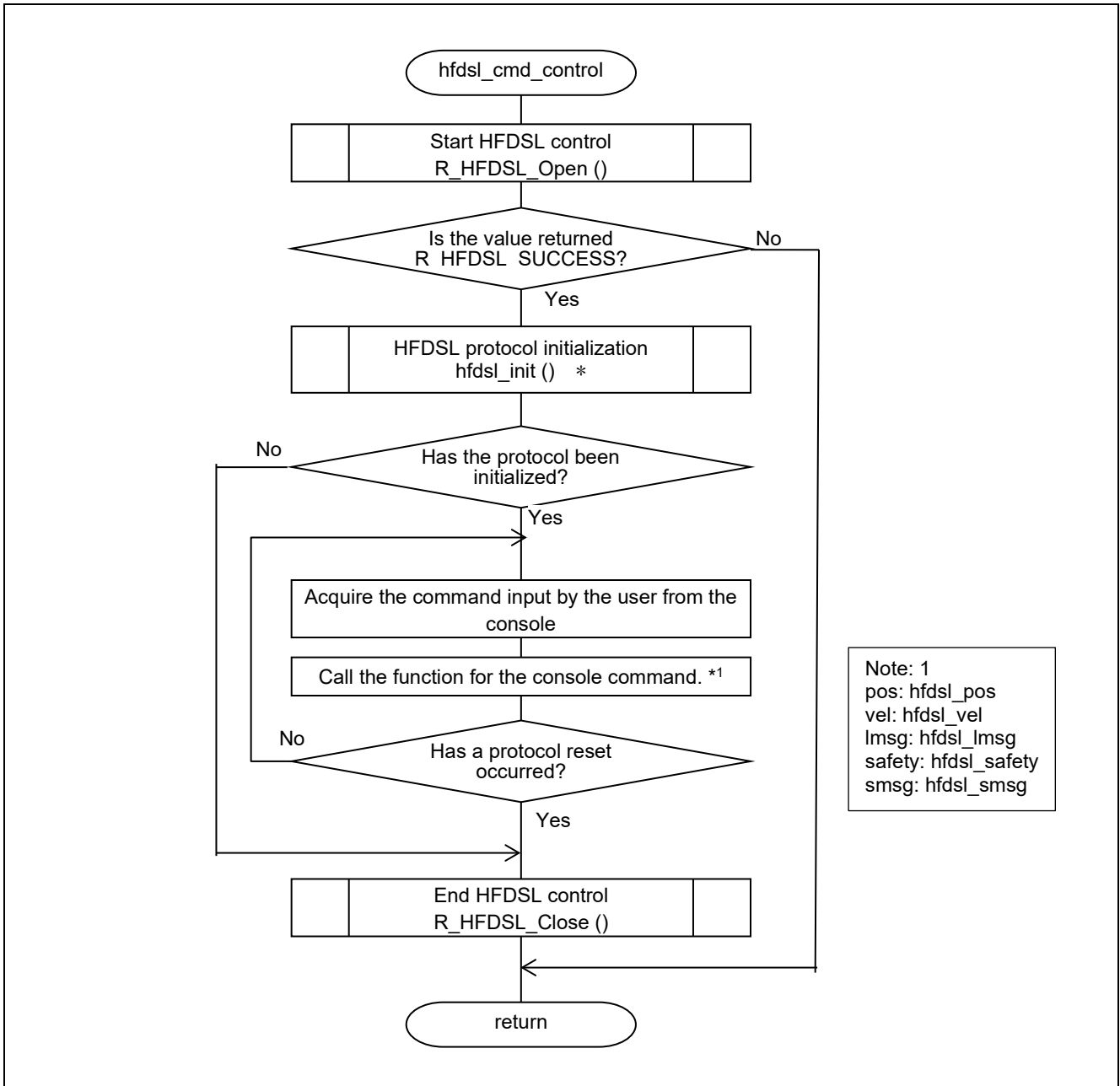


Figure 4.5 Flowchart of the hfdsI\_cmd\_control

(3) Flowchart of hfdsl\_init

This function initializes the protocol.

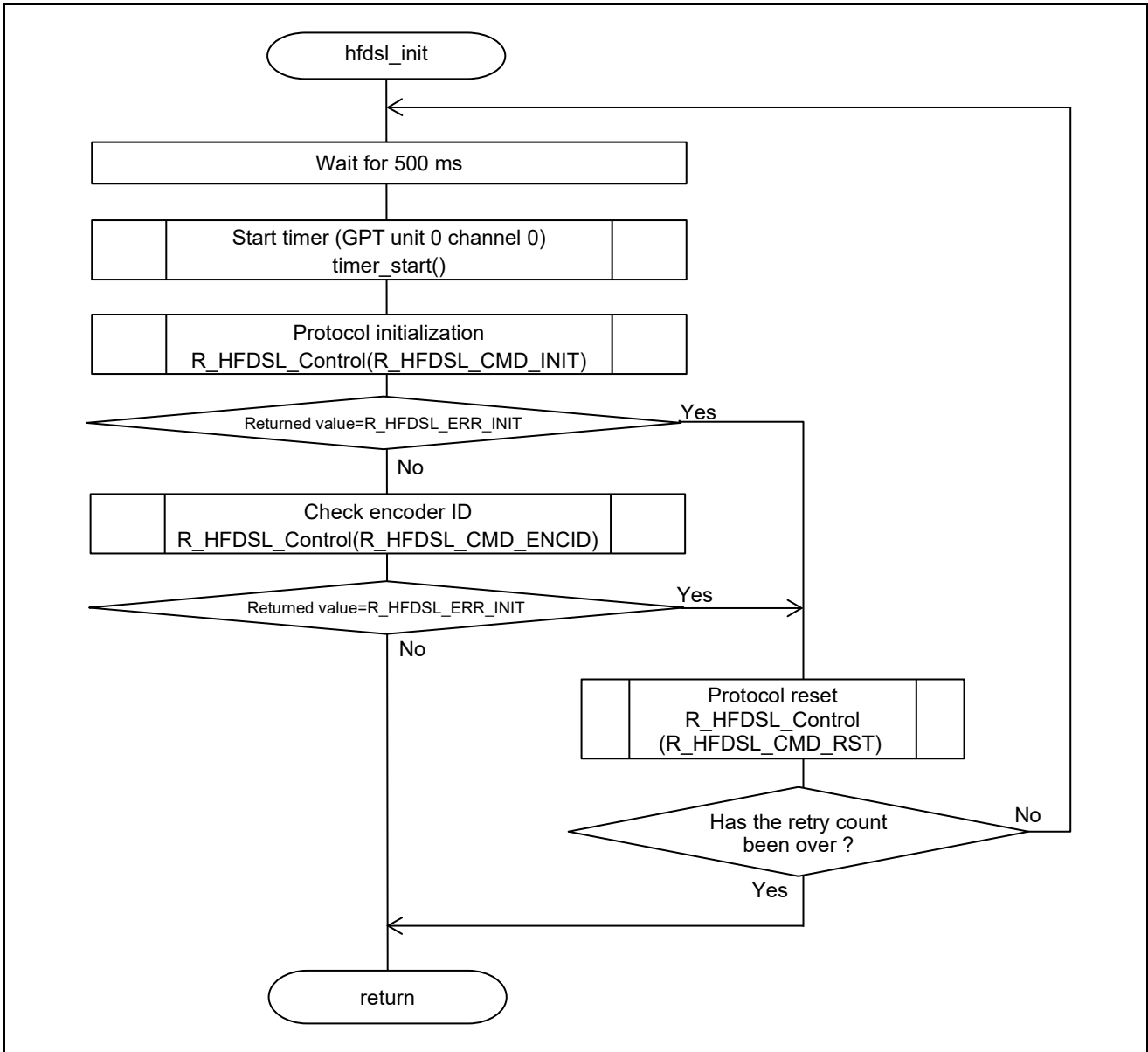


Figure 4.6 Flowchart of the hfdsl\_init

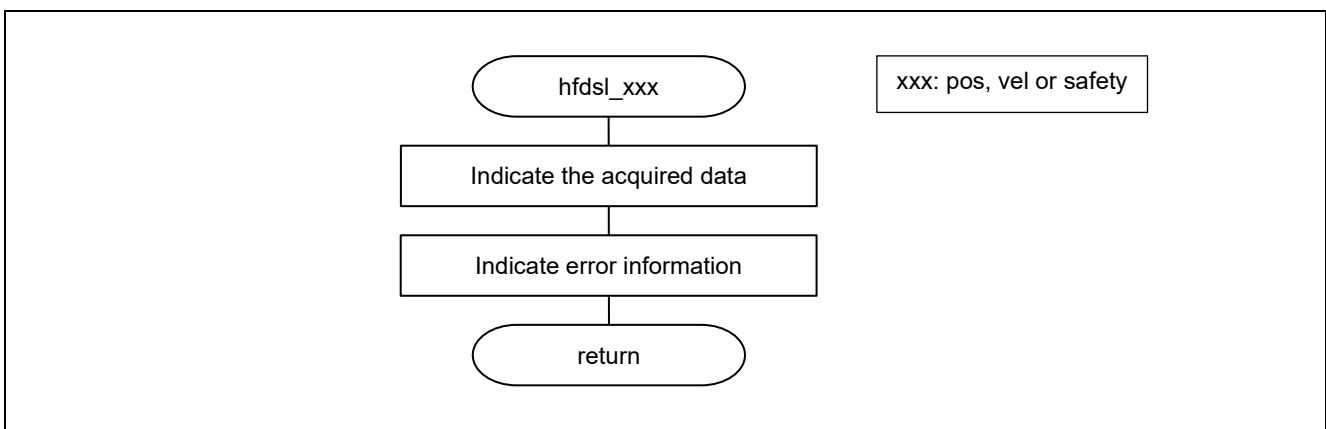
**(4) Flowchart of hfdsI\_pos, hfdsI\_vel, hfdsI\_safety**

These functions are executed in response to input of the console commands “pos”, “vel” and “safety”, and indicate the acquired data. The functions corresponding to the respective console commands and details of the items displayed are below.

**Table 4.9 Functions Corresponding to the Console Commands “pos”, “vel”, “safety”**

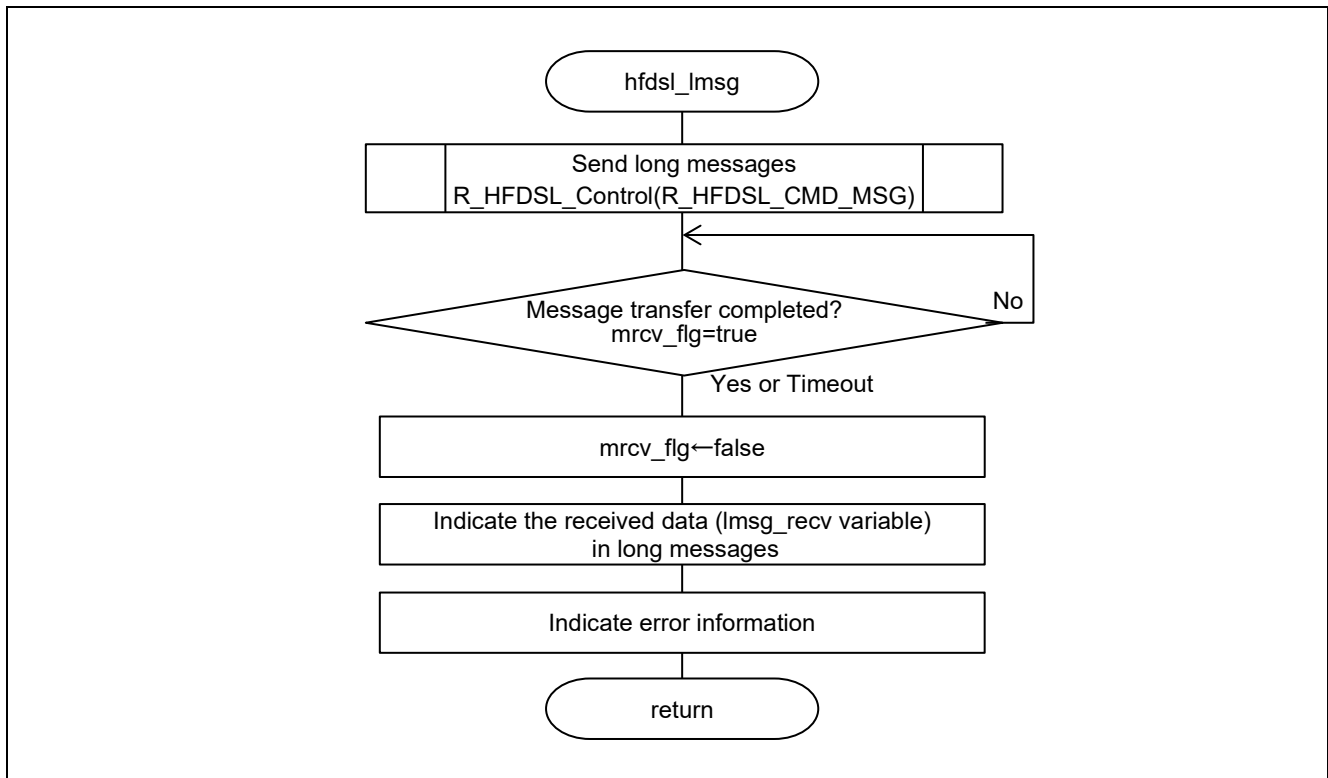
Console Command	Corresponding Function	Items Displayed
pos	hfdsI_pos	pos_rot, pos_res vpos_rot, vpos_res err_info
vel	hfdsI_vel	vel, err_info
safety	hfdsI_safety	safety1, safety2

Since the procedures for processing of the hfdsI\_pos, hfdsI\_vel and hfdsI\_safety functions are similar, they are shown in the same flowchart.

**Figure 4.7 Flowchart of the hfdsI\_pos, hfdsI\_vel, hfdsI\_safety**

**(5) Flowchart of hfdsl\_lmsg**

This function is executed in response to input of the console command "lmsg".



**Figure 4.8** Flowchart of the hfdsl\_lmsg

(6) Flowchart of hfdsl\_smsg

This function is executed in response to input of the console command “smsg”.

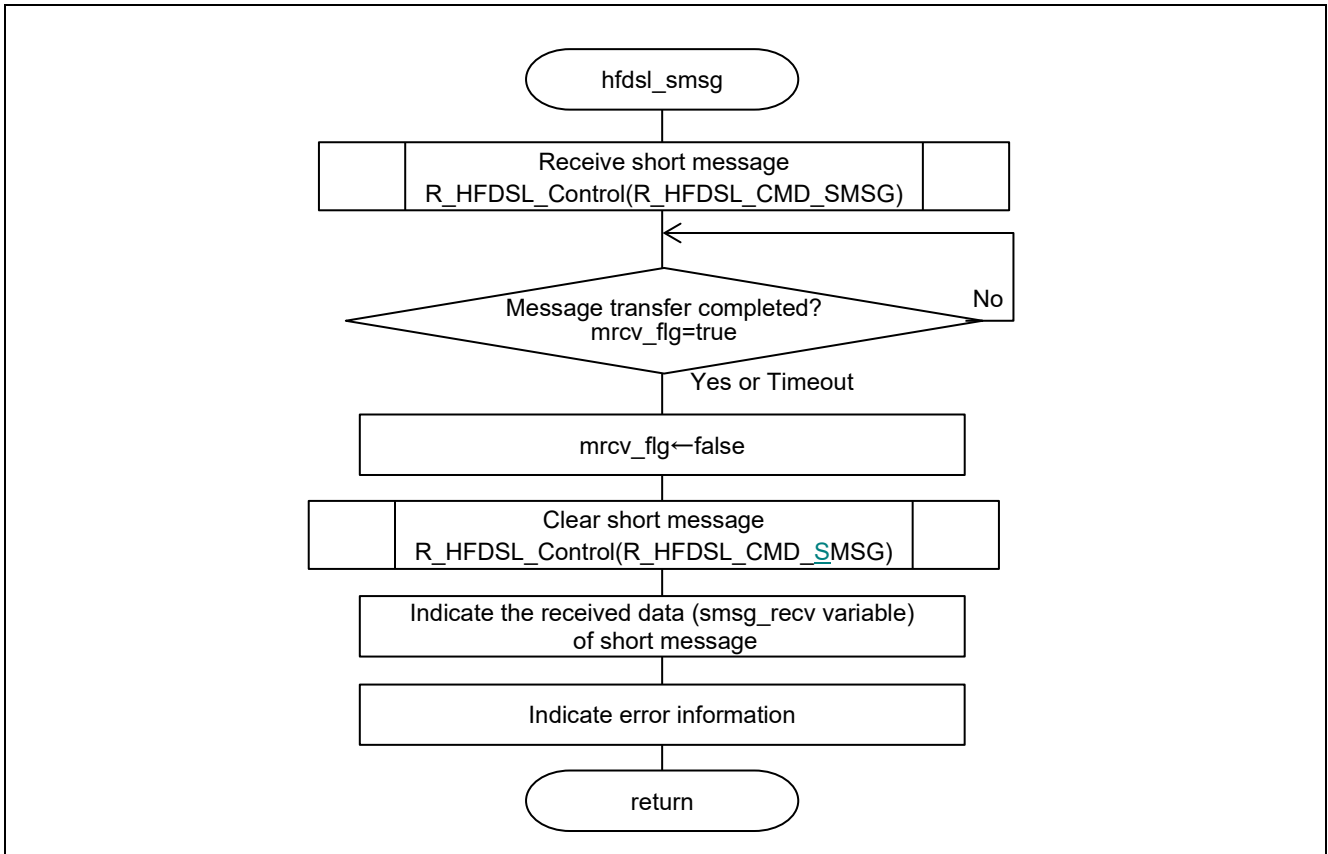


Figure 4.9 Flowchart of the hfdsl\_smsg

(7) Flowchart of hfdsl\_int\_nml\_callback

This callback function is called in response to generation of an HDSL<sub>n</sub>\_FPR interrupt.

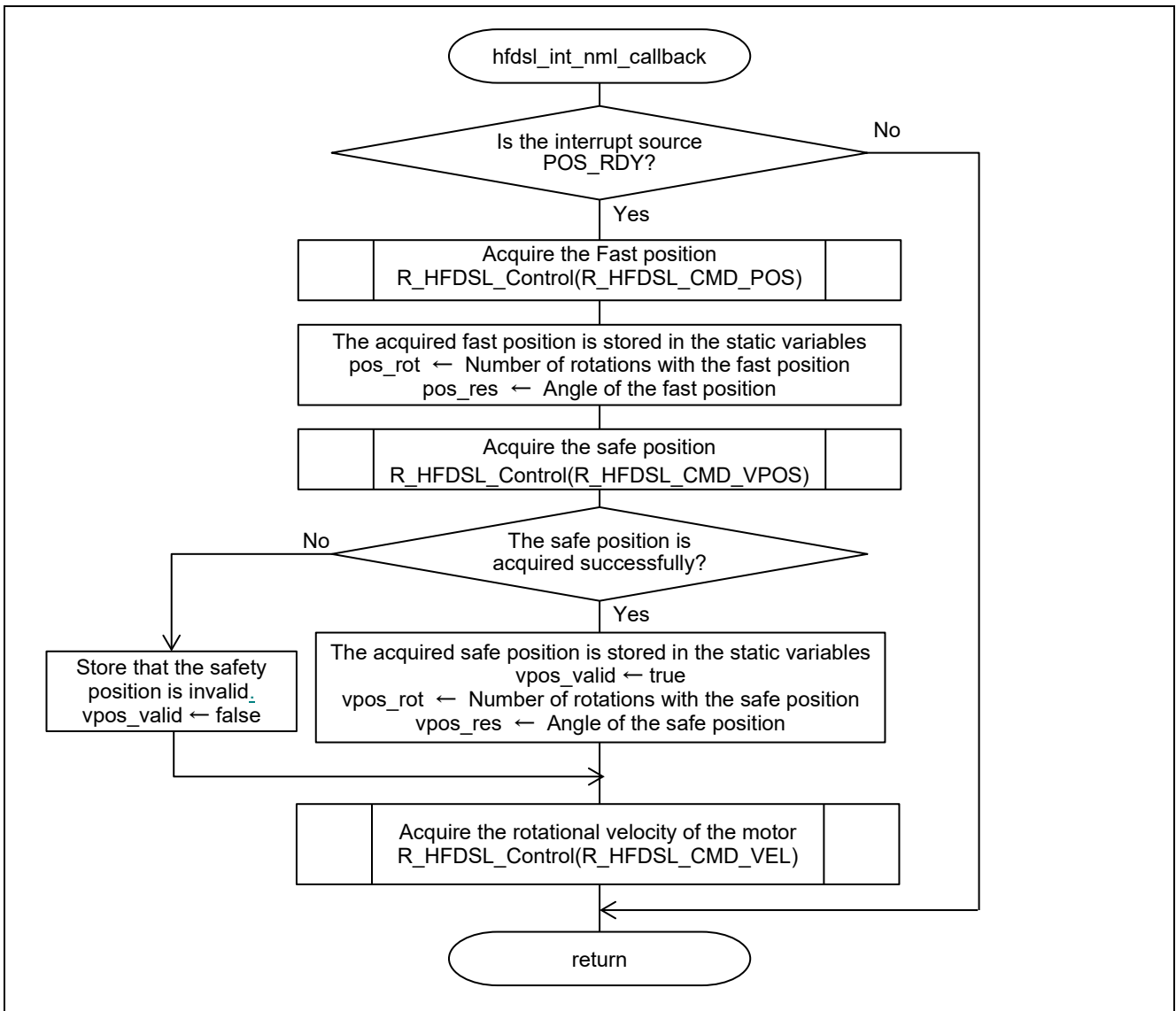
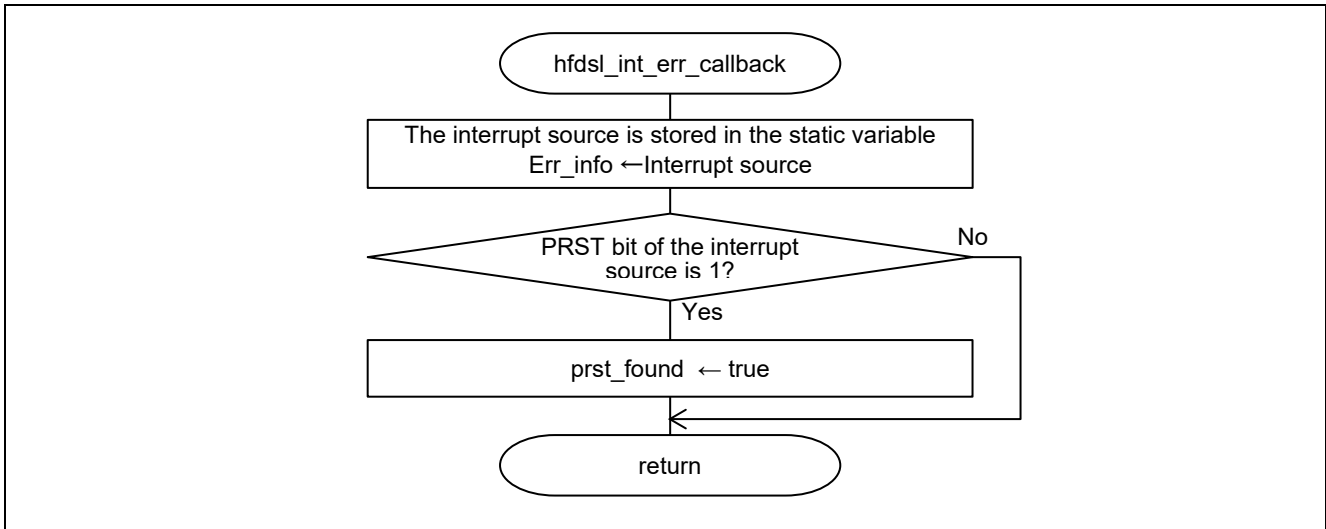


Figure 4.10 Flowchart of the hfdsl\_int\_nml\_callback

**(8) Flowchart of hfdsl\_int\_err\_callback**

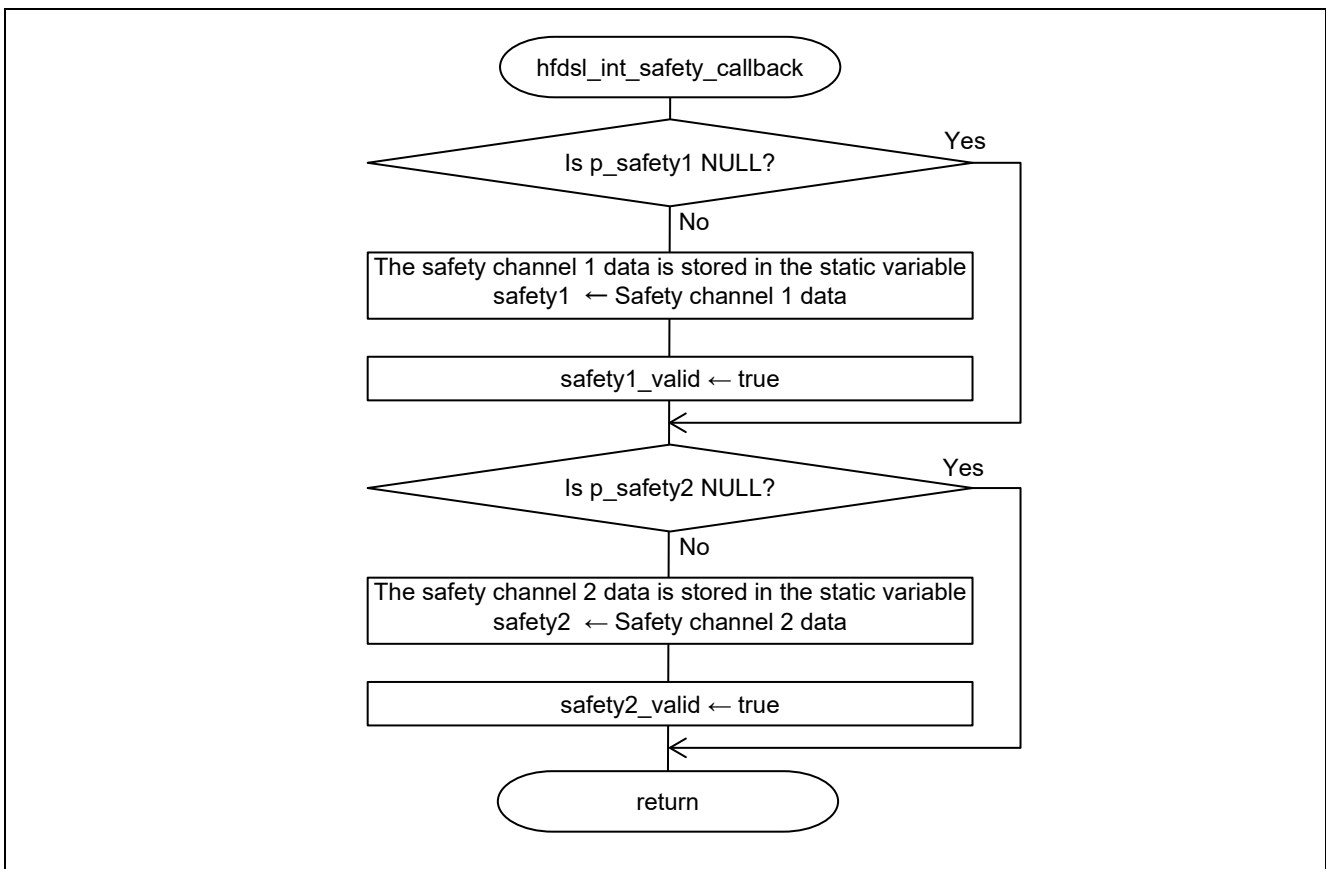
This callback function is called in response to generation of an HDSL<sub>n</sub>\_INT interrupt.



**Figure 4.11 Flowchart of the hfdsl\_int\_err\_callback**

**(9) Flowchart of hfdsl\_int\_safety\_callback**

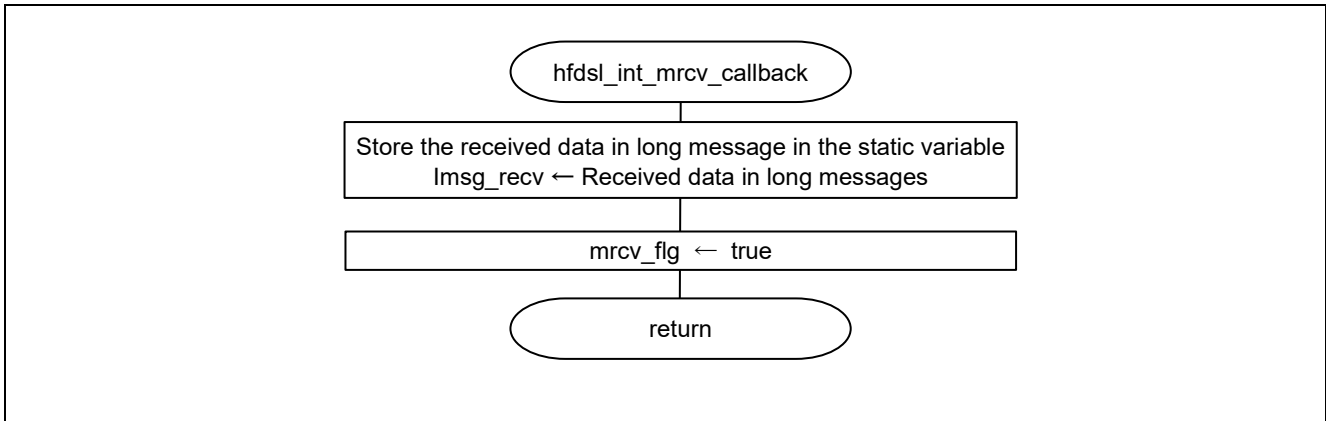
This callback function is called in response to generation of an HDSL<sub>n</sub>\_SP interrupt.



**Figure 4.12 Flowchart of the hfdsl\_int\_safety\_callback**

**(10) Flowchart of hfdsl\_int\_mrcv\_callback**

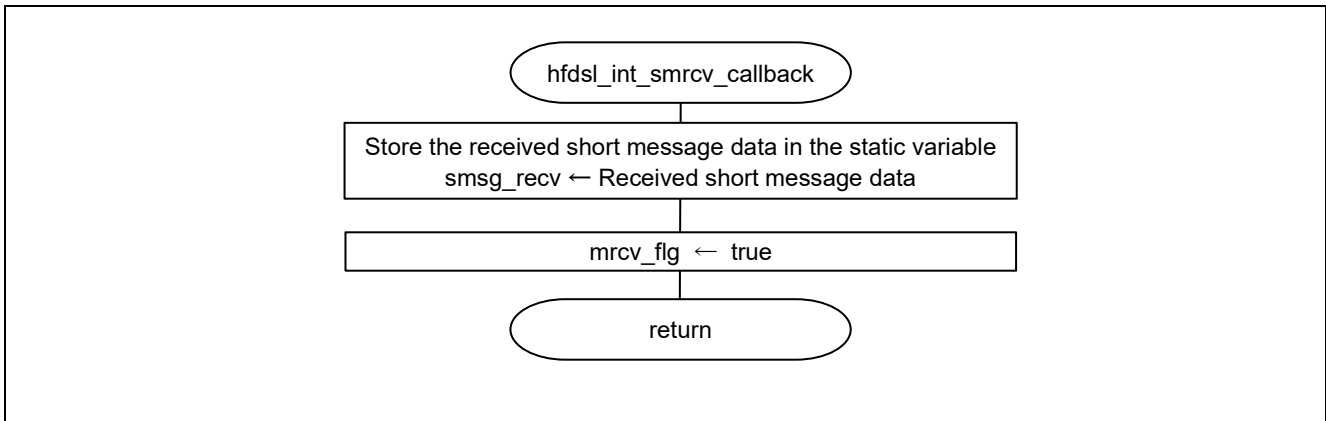
This callback function is called when the HDSL<sub>n</sub>\_INT interrupt by the EVENT\_L register FREL bit occurs and data storage of the received message is completed.



**Figure 4.13** Flowchart of the `hfdsl_int_mrcv_callback`

**(11) Flowchart of hfdsl\_int\_smrcv\_callback**

This callback function is called when the HDSL<sub>n</sub>\_INTS interrupt by the EVENT\_S register FRES bit occurs and data storage of the received message is completed.



**Figure 4.14** Flowchart of the `hfdsl_int_smrcv_callback`

4.11.5 Operation Sequence

(1) Startup Sequence

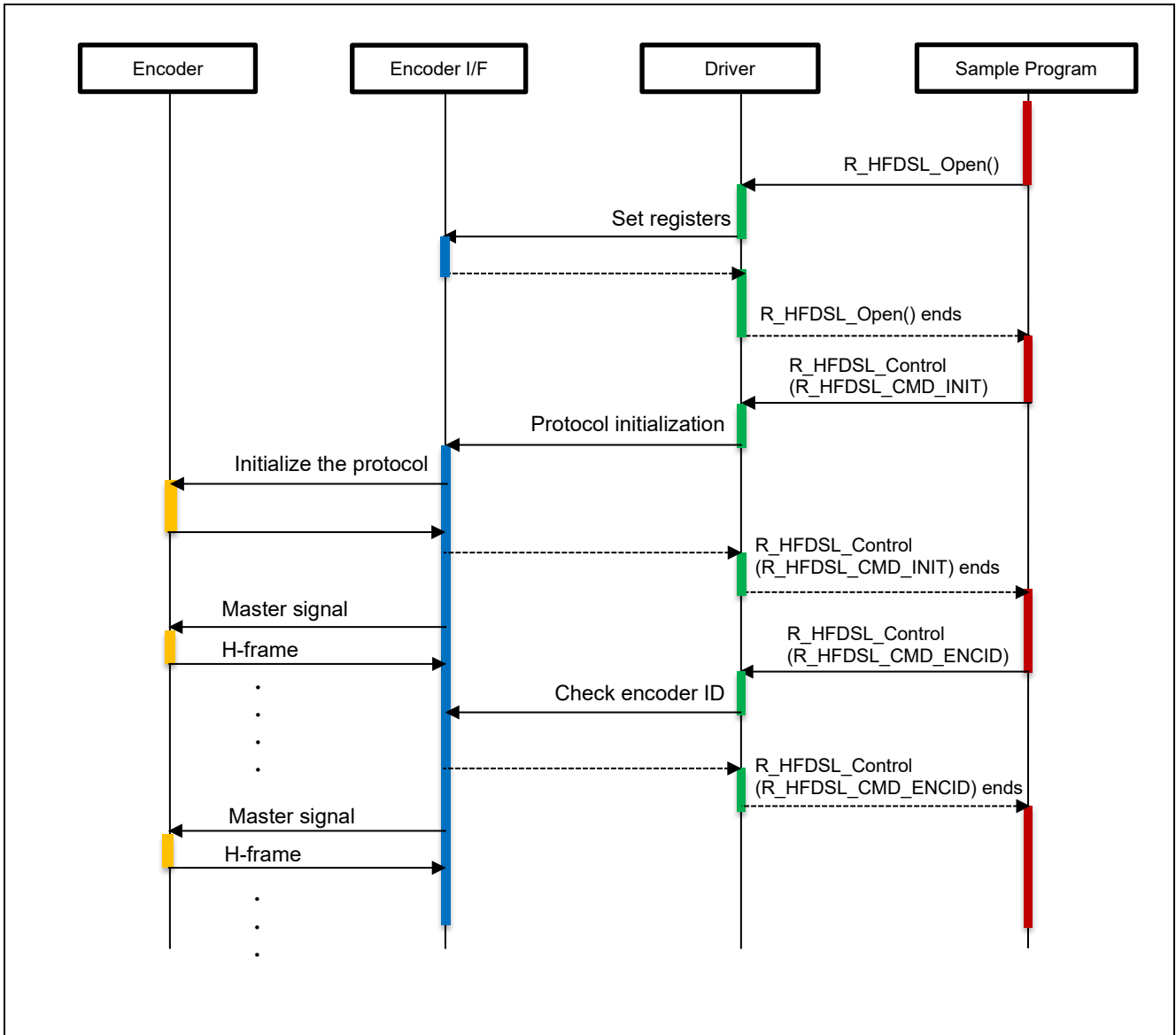


Figure 4.15 Startup Sequence Diagram

(2) Fast Position in SYNC Mode Acquisition Sequence

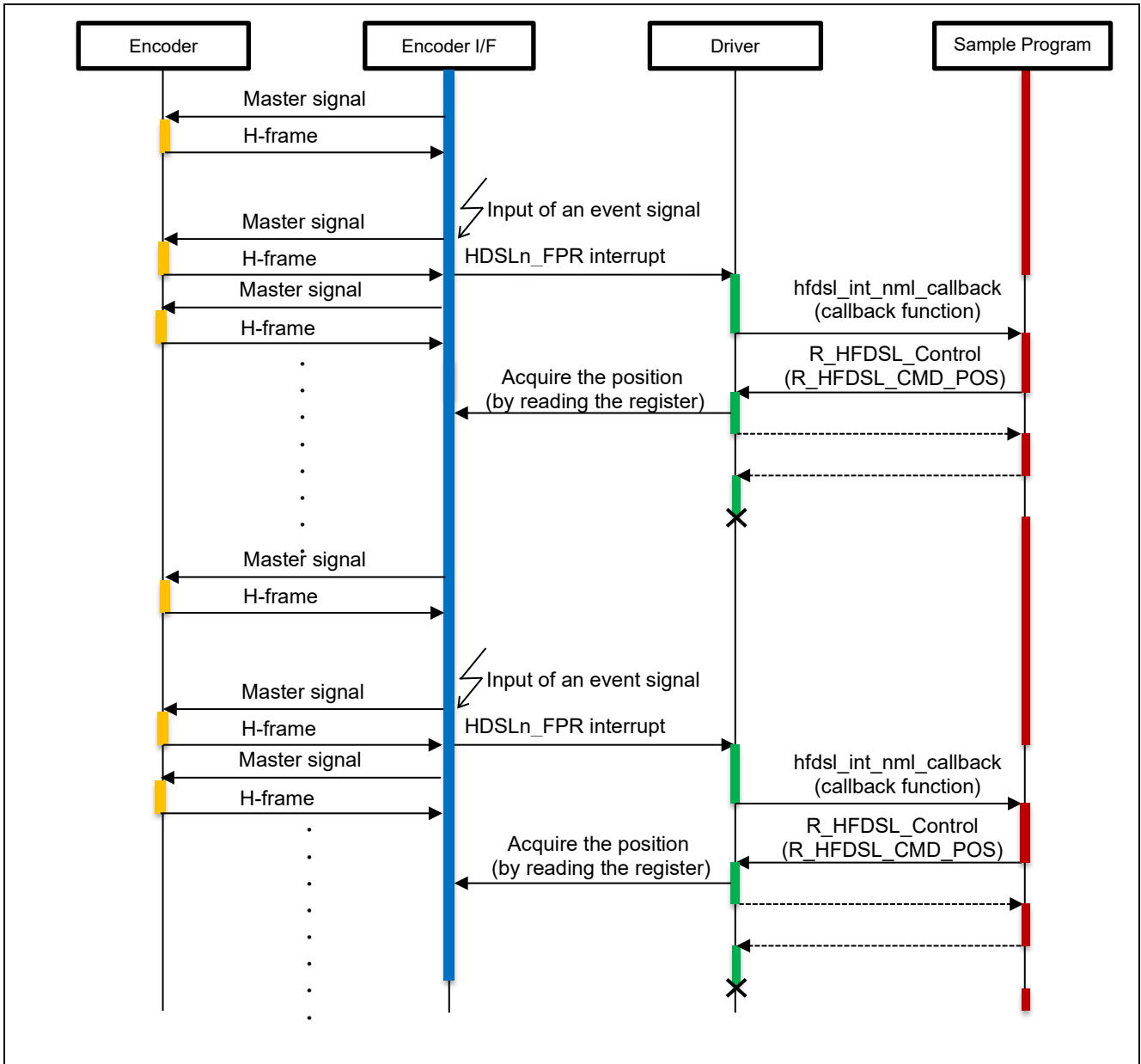


Figure 4.16 Fast Position in SYNC Mode Acquisition Sequence Diagram



(4) Message Transfer Sequence

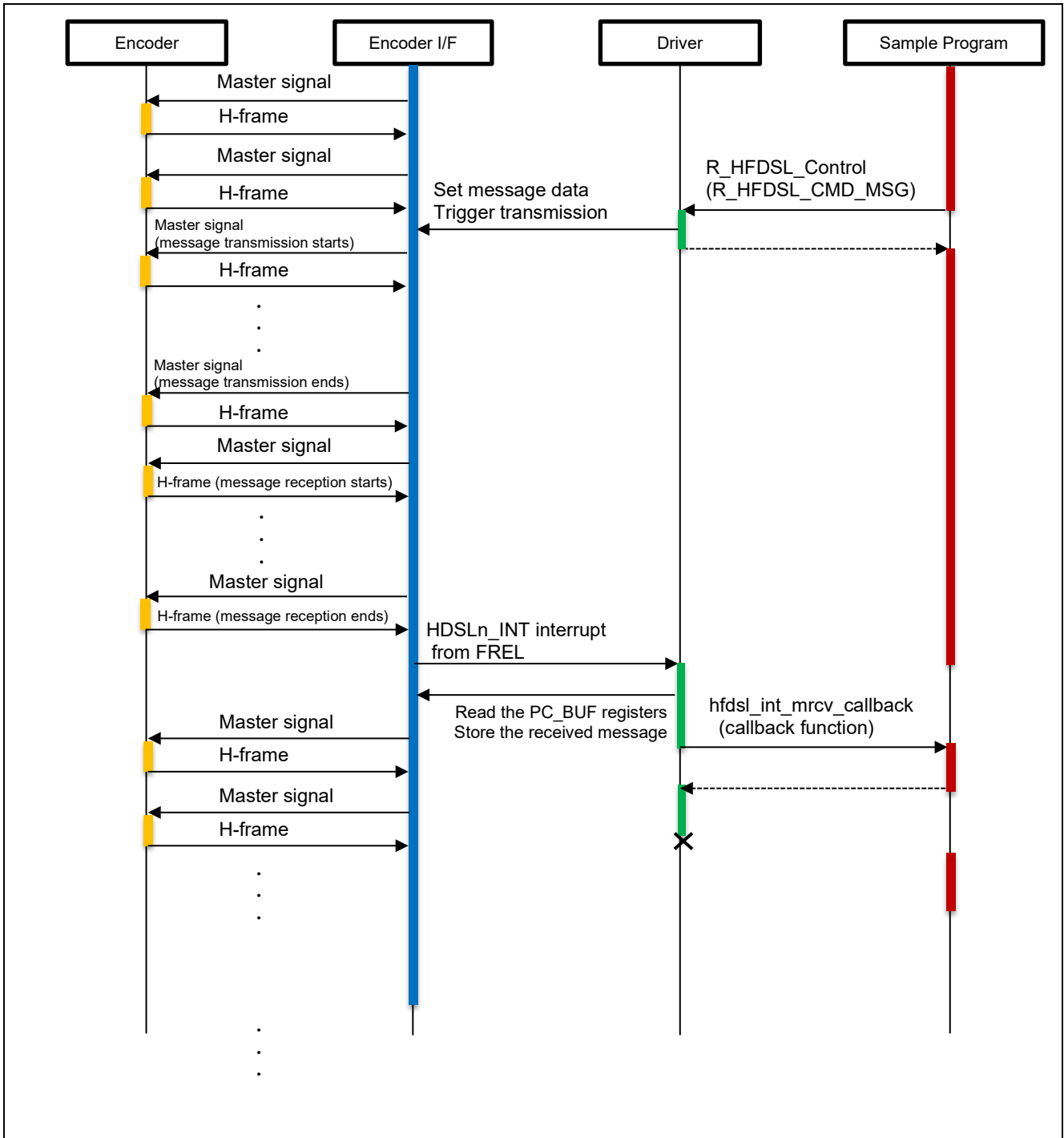


Figure 4.18 Message Transfer Sequence Diagram

(5) Stop Sequence

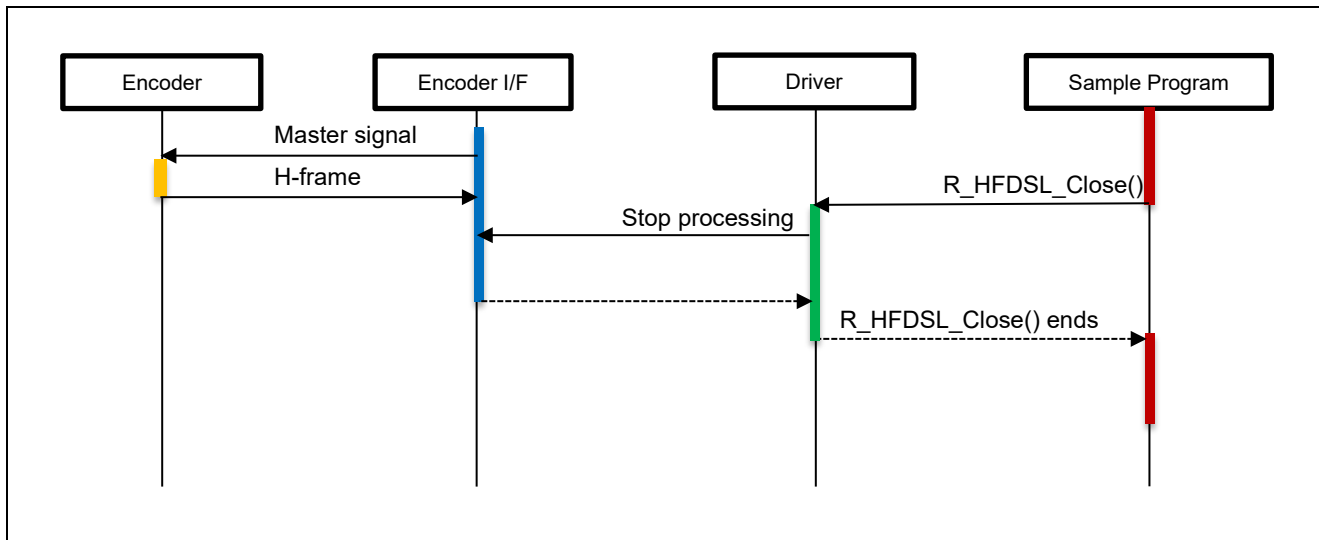


Figure 4.19 Stop Sequence Diagram

### 4.11.6 Console Commands

The commands available for input from the console are listed below.

**Table 4.10 Console Commands**

Command	Description
pos	Indicates the fast and safe positions
vel	Indicates the rotational velocity of the motor.
lmsg	Among the encoder resources, acquire the type of encoder as a long message.
safety	Displays received data of safety channel 1 and 2.
smsg	Acquire encoder status ENC_ST0 by short message and clear the status.

#### (1) Result of Running

After running, it will display the command prompt following the version. Enter the command after "hfDSL >".

```
HFDSL Safety sample program start
R_HFDSL_GetVersion = 4.0

hfDSL >
```

#### (2) pos Command

Fast position: The result of R\_HFDSL\_CMD\_POS in the hfDSL\_int\_nml\_callback function is displayed.

Safe position: The result of R\_HFDSL\_CMD\_VPOS in the hfDSL\_int\_nml\_callback function is displayed. \*

Error information: The result of the hfDSL\_int\_err\_callback function is displayed.

```
hfDSL >pos
Fast position
  Rotations   : 0x00000F76
  Angle       : 0x00067938
Safe position
  Rotations   : 0x00000F76
  Angle       : 0x000679EA
Error information
  EVENT_ERR   : 0x00000000
```

**Note:** If the SPI mode is selected for safety channel 1 interface mode by the argument p\_info of the R\_HFDSL\_Open function, access to the safety channel 1 interface registers is disabled. Values for the safe position are shown as "-".

**(3) vel Command**

Motor rotation speed: The result of R\_HFDSL\_CMD\_VEL in the hfdsl\_int\_nml\_callback function is displayed.

Error information: The result of the hfdsl\_int\_err\_callback function is displayed.

```

hfdsl >vel
Motor rotation speed
  Speed      : 0x00000026
Error information
  EVENT_ERR  : 0x00000000

```

**(4) lmsg Command**

Message address: The message address of the long message is displayed.

Motor rotation speed: The result of the hfdsl\_int\_mrcv\_callback function is displayed.

Error information: The result of the hfdsl\_int\_err\_callback function is displayed.

```

hfdsl >lmsg
Message address
  PC_ADD_H  : 0x54
  PC_ADD_L  : 0x80
Received data
  PCBUF[0]  : 0x00
  PCBUF[1]  : 0x02
Error information
  EVENT_ERR  : 0x00000000

```

**(5) safety Command**

SAFETY POSITION 1 data: Safety position 1, result of the hfdsl\_int\_safety\_callback function, is displayed. \*

SAFETY POSITION 2 data: Safety position 2, result of the hfdsl\_int\_safety\_callback function, is displayed. \*

The "data" are register data, "Rotations" and "Angle" are the values after conversion.

```

hfdsl >safety
SAFETY POSITION 1 data
  Rotations  : 0x00000F76
  Angle      : 0x00078902
  data      : 0x05 0x00 0xF7 0x67 0x89 0x02 0x42 0x12
SAFETY POSITION 2 data
  Rotations  : 0x00000F76
  Angle      : 0x000788C0
  data      : 0x9C 0xFF 0x08 0x98 0x77 0x3F 0x3D 0x9E

```

Note: If the SPI mode is selected for the safety channel 1 and the safety channel 2 interface mode by the argument p\_info of the R\_HFDSL\_Open function, access to the safety channel interface registers are disabled. Values for the SAFETY POSITION 1 and SAFETY POSITOPN 2 are shown as "-".

**(6) smsg Command**

Message address: The message address and the received data of the short message are displayed.

Error information: The result of the hfdsl\_int\_err\_callback function is displayed.

```
hfdsl > smsg
Message address
  ENC_STn      : 0x40
  S_PC_DATA    : 0x01
Error information
  EVENT_ERR    : 0x00000000
```

## 5. Sample Code

The sample code can be downloaded from the Renesas Electronics website.

**Revision History**

Rev.	Date	Description	
		Page	Summary
2.00	Dec.23.24	-	First Edition issued.
3.00	Nov 14.25	1, 4, 5 4, 27  9 to 18	Change description for trademarks. Update notes of HIPERFACE DSL MASTER Safety Integration Manual. Revise to unify description for functions.
4.00	May 08.26	5 9 to 16, 22, 23 15 to 17  27	Change frequency of the Cortex-A55 Core0 to 1200MHz. Change prefix of pointer variables to "p_". Revise header column of the specifications of user-defined functions. Correct variable name of position in fig. 4.3.

## General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

### 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

### 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

### 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

### 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

### 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

### 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

### 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

### 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

- HIPERFACE DSL is a registered trademark of SICK AG.
- IAR Embedded Workbench is a registered trademark of IAR Systems.
- Arm and Cortex are registered trademarks of Arm Limited (or its subsidiaries) in the EU and/or elsewhere. All rights reserved.
- Additionally all product names and service names in this document are a trademark or a registered trademark which belongs to the respective owners.

## Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
  - "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
  - "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION ("Vulnerability Issues"). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

## Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

## Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

## Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/).