

# **RZ/N2L Group**

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RZ/N2L Industrial Network SOM Kit Application Note: EtherNet/IP OpENer Sample Program

## Introduction

This document describes the setup procedure of the sample program for RZ/N2L port of EtherNet/IP™ "OpENer".

## **Target Device**

RZ/N2L Group

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## 1. Overview

This document describes the setup procedure of the sample program for RZ/N2L port of EtherNet/IP "OpENer" and explains the procedure for connecting the CODESYS software programmable logic controller (PLC).

In this sample program, these open-source software are used.

- EtherNet/IP OpENer
- FreeRTOS
- IwIP

For demonstration, the application of this sample program has an Exclusive Connection and an Input Only Connection. This document also explains how to connect to the CODESYS software prepared in package.

# 1.1 Abbreviations / Definitions

#### Table 1-1 Abbreviations/Definitions

Index	Abbreviations /Definitions	Description	
1	IP	Internet Protocol	
2	TCP	Transmission Control Protocol	
3	USB	Universal Serial Bus	
4	PC	Personal Computer	
5	SW	Switch	
6	EWARM	Embedded Workbench® for ARM	
7	lwIP	lightweight IP	
8	CIP	Common Industrial Protocol	
9	OSS	Open-Source Software	

## 1.2 Reference

Technical information about RZ/N2L is available via Renesas.

#### Table 1-2 Technical Inputs for RZ/N2L

Index	Technical Inputs
1	r01uh0955ejxxxx-rzn2l.pdf (RZ/N2L User's Manual: Hardware)
2	r01an6434ejxxxx-rzt2-rzn2-fsp-getting-started.pdf (Getting started with Flexible Software
	Package)
3	r12ut0020edxxxx-rzn2l-som-kit-hw.pdf (RZ/N2L Industrial Network SOM Kit Use's Manual)

## 1.3 Limitation / Known Issue

None



## 2. Features

The "OpENer" is an open-source software for I/O communication adapters of EtherNet/IP. It supports multiple I/O and explicit connections and includes objects and services for making EtherNet/IP-compliant products as defined in the ODVA specification.

This package is the RZ/N2L port of OpENer and includes OpENer source codes. Regarding the open-source license of OpENer, please see the following file.

common\oss\OpENer\license.txt

The Class Objects implemented in this sample software are as follows. For details, please see Chapter 7 Appendix C Table 7-3 ~ Table 7-9.

Table 2-1 CIP Object Classes supported on this sample software	Table 2-1 CIP Ob	oject Classes s	supported on this	s sample software
--	------------------	-----------------	-------------------	-------------------

Object Class #	Object Class Name
0x01	Identity
0x02	Massage Router
0x04	Assembly
0x06	Connection Manager
0xF5	TCP/IP Interface
0xF6	Ethernet Link
0x48	QoS



## 3. Project Setup

## 3.1 Requirements

This RZ/N2L IwIP protocol stack project has been developed and tested on these environments using the following boards and tools.

Item	Vender	Description
Board	Renesas Electronics	RZ/N2L Industrial Network SOM Kit
IDE	IAR Systems	• Embedded Workbench® for ARM Version 9.30.1
		Please apply patch
		(EWARM_Patch_for_RZN2L)
		which is available in http://www.renesas.com/rzn2l.
		Regarding how to apply the patch, please read the
		readme file in patch file.
	Renesas Electronics	• e <sup>2</sup> studio 2023-04
		<ul> <li>FSP Smart Configurator 2023-04</li> </ul>
		• RZ/N2L Flexible Software Package (FSP) v1.2.0
		Please download from the link below.
		https://github.com/renesas/rzn-fsp/releases/tag/v1.2.0
Emulator	IAR Systems	I-jet
	SEGGER	Hardware: J-Link
		Software: J-Link Commander V7.82f *1
Evaluation	CODESYS GmbH	CODESYS v3.5.15.10 32-bit *2
Software		

#### Table 3-1 RZ/N2L Requirements

 Software

 \*1:
 J-Link Commander is used for erasing flash memory.

J-Link Commander is included in "J-Link Software and Documentation Pack" on the following site. https://www.segger.com/downloads/jlink/

\*2: Please use 32bit version, the 3.5.15.10 64-bit version and other versions may not work.



# 3.2 Hardware Settings

This document describes the major hardware. Refer to RZ/N2L Industrial Network SOM Kit user's manual and schematic for more board details.



Figure 3-1 RZ/N2L Industrial Network SOM Kit

# 3.3 Note about Ethernet PHY driver using FSP

This SOM Kit has VSC8531 that is not compatible with FSP as PHY chip. Therefore, we have modified the PHY driver for VSC8531. For details, see "Appendix D: FSP Configuration for VSC8531".



## 3.4 Setup the Board

Setting the board for running sample program is shown below.

1. Connect the I-jet to J2 or the USB cable to J5 for J-link OB on Carrier board.



Figure 3-2 Setup the SOM Kit

- 2. Power is supplied by connecting USB Micro-B cable to the USB connector "J5) of the Carrier board.
- 3. Connect Ethernet Cable to the Ethernet Connector "ETH0".



## 4. Setup the Host Device

## 4.1 Configuration the Host IP Address

Set an IP address that can communicate with the device in the Ethernet adapter settings on the PC side.

This sample software sets the IP address 192.168.1.170 and subnet mask 255.255.255.0 for the device by default. Therefore, for example, set as follows on the PC side.

- IP address: 192.168.1.100
- Subnet mask: 255.255.255.0

## 4.2 Setup the CODESYS Software

This chapter describes the setup of the CODESYS software.

## 4.2.1 How to get CODESYS

CODESYS Development system is available from the following web sites. Please get version 3.5.15.10 32-bit\*.

\*: Please note that the 3.5.15.10 64-bit version or other versions may not work.

- CODESYS Store
  - > To create your account and login is required to download the CODESYS tools.
    - When you create the account as a business customer, you need:
      - VAT Number if you are European VAT registered Customers.
      - Certificate of Registration as Taxpayer (entrepreneur) if you are non-EU customers.
  - Clicks "All versions" tab to get the specified version.
- CODESYS Store North America
  - > To create your account and login is required to download the CODESYS tools.
    - United States, Canada and Mexico only can be registered in the "Country" form of the "Address Information".
  - > Clicks "Versions" tab to get the specified version.
- LINX (Distributer in Japan)

 $\triangleright$ 

- > To create your account and login is required to download the CODESYS tools.
  - ♦ Only Japanese companies can create the account.
- The latest version only is available.
  - ♦ If you use the latest version, please try updating the CODESYS project included in this package by referring the section Appendix A: How to update CODESYS project.



## 4.2.2 Startup CODESYS Tools

After install the CODESYS, please launch the CODESYS tools shown below.

#### Table 4-1 CODESYS tools

Name	Description	Note
CODESYS V3	IDE	-
CODESYS Gateway V3	Software Gateway	This may be already started by Windows Start Up Process.
CODESYS Control Win V3	Software PLC	This may be already started by Windows Start Up Process.

If the CODESYS is launched properly, the following window is shown.

CODESYS			- 🗆 X
File Edit View Project Build Online Debug To			Υ
🎦 📽 🗐   香   い つ ぶ ங 砲 🗙   西 🍕 巻 🏭	l î î î î î î î î	■ 🖋   🗊 🖆 🖆 🌾   🛣   🛱	a√
POUs - 4 X			Properties
			Property Value
POUS 😒 Devices			
Messages - Total 0 error(s), 0 warning(s), 0 message(s)	0 error(s) 🕚 0 warning(s) 🚯 0 message(s) 🗙 👌		×
Description	Project	Object Position	
			Description
			Properties Votifications
		Last build: 😋 0 🕐 0 🛛 Precompile 🗸	Project user: (nobody)

Figure 4-1 CODESYS Initial Window



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If the CODESYS Gateway and Control Win SysTray is launched properly, the following icons are shown in notification area of Windows Tool Bar. (The left icon is of the CODESYS Gateway, and the right one is of the CODESYS Control Win SysTray)

m
Figure 4-2 CODESYS Icons

Please click each icon and click "Start Gateway" and "Start PLC".

¢	<b>m</b> 😌 💈
	Start Gateway
	Stop Gateway
	Allow Edge Gateway configuration
	Exit Gateway Control
	About
ø	11 😌 🚯
	Start Gateway
	Stop Gateway
	Allow Edge Gateway configuration
	Exit Gateway Control

Figure 4-3 Start Gateway and PLC

If the Gateway and PLC is started properly, the icons pigment like the following image.



Figure 4-4 Icons with A and B successfully started



# 4.2.3 Install EDS File into CODESYS

In the CODESYS, please open "tools" > "Device Repository" in tool bar.

CODESYS		– 🗆 X
File Edit View Project Build Online	Debug Tools Window Help	<b>T</b>
🎦 🖆 🗐 🗐 🗠 🔍 🖄 🛍 🗶 🖊 🌿		
	ibrary Repository	
Devices 🗸 🗸 🛪 🗙		Properties - 🕂 🗙
		¥ Filter ▼ Sort by ▼
	🖓 Visualization Style Repository	ੈ Sort order ▼
	License Repository	Property Value
	📙 License Manager	
	Scripting	
	Customize	
	Options	
	Import and Export Options	
	Device Reader	
< >		
POUs 😪 Devices		
Messages - Total 0 error(s), 0 warning(s), 0 message(s)	- ∓ X	
	🝷 🔇 0 error(s) 🕐 0 warning(s) 🔮 0 message(s) 🔀 💥	
Description	Project Object Position	1
		Description
		e estimatori
		Properties V Notifications
	Last build: 👩 0 😗 0 Precompile 🧹	Project user: (nobody)

Figure 4-5 Device Repository in CODESYS



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Please click the "Install" to open dialog to select EDS file, and select the EDS file "renesas\_opener\_sample\_app.eds" in "scanner" directory.

Device Re	epository				>
cation	System Repository			~	Edit Locations
	(C:\ProgramData\COD	ESYS\Devices)			
	evice descriptions				
String for a	a fulltext search	Vend	or: <all vendors=""></all>	~	Install
Name	Ver	ndor Version	Description		Uninstall
🖲 🔟 Fie	eldbuses				Explort
🗄 - 🚍 нм	4I devices Cs				Laport.
🗉 🗊 PL(	Cs				
🗄 - 🔗 So	ftMotion drives				
					Details
					Class
					Close

Figure 4-6 Click "Install" in Device Repository Window



If the Renesas OpENer Device is shown in the blue line as EtherNet/IP Remote Adapter, please click "close" to close this window.

cation	System Repository				~	Edit Locations
	(C:\ProgramData\CODESYS\De	vices)				
stalled d	evice descriptions					
tring for	a fulltext search	Vendor:	<all vendors=""></all>		~	Install
Name		Ven	dor	Version	Description ^	Uninstall
<u>⊨</u>	🗕 EtherNet/IP					Export
G	🗄 🎟 Ethernet Adapter					
G	EtherNet/IP Local Adapter					
	EtherNet/IP Module					
E	EtherNet/IP Remote Adapte					
	Generic EtherNet/IP de		Smart Software Solutions GmbH	3.5.15.0	EtherNet/IP Target fo	
	Renesas OpENer Device	e Rene	esas Electronics	Major Revision=16#2, Minor Revision = 16#3	EtherNet/IP Target in	
	🗄 👄 EtherNet/IP Scanner					
	Home&Building Automation				~	
	CO Link Douison				>	
						Details
	:¥git¥dls¥OpENer_development¥O Device "Renesas OpENer Device		itions¥scanner¥renesas_opener_sa device repository.	ample_app.eds		
						Close

Figure 4-7 EtherNet/IP Remote Adapter

Preparation for using CODESYS is now complete. Continue with the program operation in Chapter 5 and then operate CODESYS again in Chapter 6.



## 5. Running the Sample Application

Before following this chapter, please look at Section 3.2 and 3.4 for board setup.

The setup differs depending on the IDE.

- When using e<sup>2</sup> studio, refer to section 5.1.
- When using EWARM, refer to section 5.2.

## 5.1 Setup sample project for e<sup>2</sup> studio

Replace the project name in the figure with the project name of this sample project.

## 5.1.1 Startup e<sup>2</sup> studio

- 1. Open the e<sup>2</sup> studio and select a directory as workspace.
- 2. Click "Open Projects from File System..." in File tab.

<b>e</b> v	workspace - e <sup>2</sup>	studio			
File	Edit Source	Refactor	Navigate	Search F	Project Re
	New			Alt+S	ihift+N >
	Open File			_	
	Open Project	s from File	e System		
	Recent Files			-	>
	Close Editor				Ctrl+W
	Close All Edit	ors		Ctrl+S	hift+W
	Save				Ctrl+S
	Save As				
R	Save All			Ctrl+S	Shift+S
	Revert				
	Move				
	Rename				F2
8	Refresh				F5
	Convert Line	Delimiters	То		>
Ð	Print				Ctrl+P
2	Import				
4	Export				
	Properties			Alt	+Enter
	Switch Works	space			>
	Restart				
	Exit				

Figure 5-1 e<sup>2</sup> studio File tab



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3. Import the project folder.

Import "\project\rzn2l\_som\opener\_single\e2studio".

Import Projects from	File System or Archive			– 🗆 X
	ile System or Archive content of your folder or archive file to	find projects and import then	n in the IDE.	
Import source:	Extracted zip folder path	\project\rzn2l_rs	k\opener_single\e2studio	V Directory Archive
type filter text				Select All
Folder			Import as Eclipse project	Deselect All
Close newly imported Use installed project con	l projects upon completion figurators to:		<u> </u>	1 of 1 selected
Search for nested pro			$\mathbf{X}$	
Detect and configure	project natures		$\mathbf{X}$	
Working sets				
Add project to wor	king sets			New
Working sets:				<ul> <li>✓ Select</li> </ul>
				Show other specialized import wizards
?			< Back Next >	Finish Cancel

Figure 5-2 Import project on e<sup>2</sup> studio



## 5.1.2 Board IP Address Setting

The IP address is set in src/renesas/application/opener\_port\_instance.c.

The following addresses are used in the example:

IP address	: 192.168.1.170
Subnet mask	: 255.255.255.0
Default gateway	: 192.168.1.1
Host Name	: OPENER_NETIF0



Figure 5-3 Static IP address



## 5.1.3 How to generate source code and how to build

1. Click the Configuration.xml.



Figure 5-4 Configuration

2. Click 'Generate Project Content' button then generate rzn, rzn\_gen, rzn\_cfg folder.



Figure 5-5 Generate Project Content





Figure 5-6 Generate project folder

3. Click the Build button in tool bar to build the project and confirm that there is no error message in build message log.

	worksp	ace - RZN	I2L_RSK_Op	ENer_single	⊧/configu	ration.xm	I - e <sup>2</sup> studio								
File	Edit	Source	Refactor	Navigate	Search	Project	Renesas Views	Run	Window	Help					
3	*		🎄 Debu	ıg	~	c≊ RZN2	L_RSK_OpENer_s	ingle D	ebug 🗸 🕴	1	- 8 6	. ھ	5	🗟 : 敗 : 🗞 : 🤅	\$\$ i 🗞

#### Figure 5-7 Build button

🔐 Problems 📃 Console 🗙 🏟 Smart Browser 👒 Smart Manual 🛛 🗱 🐥 🏠 🙀 🚮 😑 🗟 🗐 🥣 🖢 🕶 😭	-  -
CDT Build Console [RZN2L_RSK_OpENer_single]	
	~
<pre>Building target: RZN2L_RSK_OpENer_single.elf arm-none-eabi-objcopy -0 ihex "RZN2L_RSK_OpENer_single.elf" "RZN2L_RSK_OpENer_single.hex" arm-none-eabi-sizeformat=berkeley "RZN2L_RSK_OpENer_single.elf"     text data bss dec hex filename 137678 392 360212 498282 79a6a RZN2L_RSK_OpENer_single.elf 17:57:54 Build Finished. 0 errors, 378 warnings. (took 24s.193ms)</pre>	l
	~
s	>

Figure 5-8 Build message



#### 5.1.4 Download application and run debugger

1. First, erase the flash memory by following the steps below. This step can be skipped after erasing the flash memory.

#### Open the J-Link Commander.



Figure 5-9 Open J-Link Commander



First, type "connect" to establish a target connection and press enter.

Next, specify the connection conditions as follows.

- Device> (Default = press enter)
- TIF>S
- Speed> (Default = press enter)

After that, confirm the message "Cortex-R52 identified." Is displayed.

	J-Link Commander V7.82f	_	×
	SEGGER J-Link Commander V7.82f (Compiled Dec 8 2022 09:40:05) DLL version V7.82f, compiled Dec 8 2022 09:38:33		^
	Connecting to J-Link via USBO.K. Firmware: J-Link OB-S124 compiled Sep 1 2022 15:38:25 Hardware version: V1.00 J-Link uptime (since boot): Od OOh O6m O5s S/N: 831650215 VTref=3.300V		
$ \stackrel{\wedge}{\rightarrow} \stackrel{\rightarrow}{\rightarrow} \rightarrow$	Type "connect" to establish a target connection, '?' for help J-Link>connect Please specify device / core. <default>: R9A07G084M08 Type '?' for selection dialog Device&gt; Please specify target interface: J) JTAG (Default) S) SWD T) cJTAG TIF&gt;S Specify target interface speed [kHz]. <default>: 4000 kHz Speed&gt;</default></default>		
			~

Figure 5-10 Connection conditions (1/2)



Figure 5-11 Connection conditions (2/2)



Use the commands below to enable flash erase and erase the flash memory.

- >exec EnableEraseAllFlashBanks

- >Erase 0x6000000, 0x60100000

After that, confirm the message "Erasing done." Is displayed.

#### Enter "q" to exit J-Link Commander.



#### Figure 5-12 Erase flash memory (1/2)



Figure 5-13 Erase flash memory (2/2)



2. Return to e2 studio. Click the Debug button in tool bar to download the built application program and launch the debugger.



Figure 5-14 Debug button

3. Click to "Switch" button.

📴 Conf	irm Perspective Switch X
2	This kind of launch is configured to open the Debug perspective when it suspends.
	This Debug perspective supports application debugging by providing views for displaying the debug stack, variables and breakpoints.
	Switch to this perspective?
<u>R</u> em	ember my decision
	<u>S</u> witch <u>N</u> o

Figure 5-15 Confirm Perspective Switch



4. The program will break at "system\_init" for startup.



Figure 5-16 Break point 1



- 5. Before running the loaded program, please change the CPSR register of CR52 general register on Registers tabs.
- Change the "T" register bit (bit 5 in CPSR register), which is Thumb execution state bit, from "1" to "0" to switch the instruction mode from "Thumb" to "Arm".
  - When the register value is "0x000001fa", set it to "0x000001da".

If the value of "T" bit in CPSR register is not changed, please note that the program does not work properly when running.

Name	Value
👻 🛗 General Registers	
1010 rO	0x1
<sup>1010</sup> r1	0x80281a10
1010 r2	0xa500
<sup>888</sup> r3	0x80281300
<sup>1010</sup> r4	0xbb92caf
<sup>1010</sup> r5	0x1e58a574
<sup>1010</sup> r6	0x0
<sup>1010</sup> r <b>7</b>	0x0
<sup>1010</sup> r8	0x0
<sup>1010</sup> r9	0x0
<sup>1010</sup> r10	0x0
<sup>1010</sup> r11	0x0
<sup>1010</sup> r12	0xe51ff004
<sup>1010</sup> sp	0x101fe8
1010 <b> r</b>	0x10006d
<sup>0101</sup> pc	0x102000
<sup>1010</sup> cpsr	0x200001fa 0x200001da

Figure 5-17 CPSR register of CR52 generic register on Registers tab

6. Click the Resume button. The program will break at the first of main function.

workspace - RZN2L_RSK_OpENer_sing	e/rzn/fsp/src/bsp/cmsis/Device/RENESAS/Source/startup.c - e² studio
	Search Project Renesas Views Run Window Help
🐔 🗱 🔳 🔅 Debug	$\checkmark$ ] $\square$ RZN2L_RSK_OpENer_single Debug. $\checkmark$ $\Rightarrow$ $\square$ $\square$ $\square$ $\square$ $\square$ $\Rightarrow$ $\square$ $\Rightarrow$ $\square$ $\Rightarrow$ $\square$ $\Rightarrow$ $\square$ $\Rightarrow$ $\square$

Figure 5-18 Resume button



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Figure 5-19 Break point 2

7. Click the Resume button again to execute the program.



# 5.2 Setup sample project for EWARM

Replace the project name in the figure with the project name of this sample project.

## 5.2.1 Startup EWARM

- 1. Open the EWARM.
- 2. Click "Open Workspace..." in the File tab.

File Edit View Project Tools Window He
<b>*</b>
New File Ctrl+ N
1 New Workspace
Dpen File Ctrl+ O
🛅 Open Workspace
Open Header/Source File Ctrl+ Shift+ H
Close Ctrl+F4
Save Workspace
Save Workspace As
Close Workspace

Figure 5-20 EWARM file tab

3. Select the Workspace File(.eww) and click the Open button.

"\project\rzn2l\_som\opener\_single\ewarm\RZN2L\_SOM\_EIP\_OpENer.eww"

$\rightarrow$ $\checkmark$ $\uparrow$	_ ≪ project → rzn2l_rsk → opener_single	ewarm ·	✓ Ö 🔎 Sear	ch ewarm	
rganize 🔻 🛛 🛚	New folder				
A Vuick acc	Name	Date modified	Туре	Size	
	settings	9/8/2022 11:39 AM	File folder		
📃 Desk 🖈	Debug	9/13/2022 2:37 PM	File folder		
🖊 Dow 🖈	rzn	9/8/2022 11:39 AM	File folder		
pD_c 🖈	rzn_cfg	9/8/2022 11:39 AM	File folder		
OneDrive	rzn_gen	9/8/2022 11:46 AM	File folder		
	📊 script	9/8/2022 11:39 AM	File folder		
📃 My PC: R	settings	9/8/2022 4:01 PM	File folder		
🧊 3D Obje	src	9/8/2022 3:08 PM	File folder		
📃 Desktop	RZN2L_RSK_OpENer_single.eww	9/8/2022 11:39 AM	IAR IDE Workspace	1 KB	
🔮 Docum					
	File name: RZN2L_RSK_OpENer_single.evv	v	~ Workspac	e Files (*.eww)	

Figure 5-21 Open project file



## 5.2.2 Board IP Address Setting

The IP address is set in \common\renesas\application\opener\_port\_instance.c.

The following addresses are used in the example:

IP address	: 192.168.1.170
Subnet mask	: 255.255.255.0
Default gateway	: 192.168.1.1
Host Name	: OPENER_NETIF0



Figure 5-22 Static IP address



## 5.2.3 How to generate source code and how to build

 Click the "Tool" -> "FSP Smart Configurator" on tool bar. If you have not set up FSP Smart Configurator yet on EWARM, refer to r01an6434ejxxxx-rzt2-rzn2-fsp-getting-started.pdf in which section 5.4 describes how to set up it.



Figure 5-23 Tools tab

2. Click 'Generate Project Content' button then will be generate rzn, rzn\_gen, rzn\_cfg folder.

File Help Run						
FSP_Project] FS	SP Configuration $\times$		FSP Visualization	n 👩 Package	-	
Summary		Generate Project Content	<b>E</b> <u>&gt;</u>			;
Project Sum	imary	RENESAS			· · ·	
Board: Device:	RSK+RZN2L (RAM execution without flash n R9A07G084M08GBG	nemory)				
FSP Version: Project Type:						
Location:	Irz	zn2l_rsk/opener_single/ewarm 😓				
Selected softw	vare components	~				
D Sup	port					
DED CL	ocks Pins Interrupts Event Links Stacks Compon		▶ Legend			

Figure 5-24 FSP SC Smart Configurator



3. Click the Make button on tool bar to build. Once the build is completed, the build message is displayed in the Build Console window that displays compilation target files and the number of error/warnings.



Figure 5-25 Make button 1

luild		<b>▲</b> 1
Messages lwip_port_instance.c RZN2L_RSK_OpENer_single.out	File	Line
Post-build command		
50% Generating Smart Bundle100% Generating Smart Bundle		
Total number of warnings: 238		
Build succeeded		

Figure 5-26 Make button 2 and Build console



#### 5.2.4 Download application and run debugger

1. Click the Debug button in tool bar to download the built application program and launch the debugger. The program will break at the first code in main function.



Figure 5-27 Debug button



#### Figure 5-28 Break point

#### 2. Click the Go button.



#### Figure 5-29 Go button



# 6. Demonstration of the application with the CODESYS

## 6.1 Application Behavior

For demonstration, the application of OpENer RZ/N2L port has an Exclusive Connection and an Input Only Connection. The connections between the RZ/N2L application and the CODESYS project application is shown below.



The PLC program of CODESYS project is shown below. The PLC program is described by ST(Structured Text) language.

```
CycleCounter := CycleCounter+Board_SW_Input;
IF CycleCounter > CyclePerTick THEN
CycleCounter := CycleCounter-CyclePerTick;
IF 0 < Board_LED_Input AND Board_LED_Input < 8 THEN
Board_LED_Output := Board_LED_Input * 2;
ELSE
Board_LED_Output := 1;
END_IF
END_IF
```

> The Exclusive Owner Connection is bound to LED of RZ/N2L Industrial Network SOM Kit.

- The PLC program make the LEDs light by shifting every CyclePerTick .
- The Input Only Connection is bound to J6-1 ~ J6-4 of RZ/N2L Industrial Network SOM Kit.
   The PLC program read the SW values and change the incrementation value of CycleCounter for controlling the frequency of LED light shifting.

 $\triangleright$ 



CODESYS application can be shown page.

Devices – A X	Device Ethernet Re	esas OpENer Device	PLC_PRG	×		•
opener_sample_app		PROG	RAM PLC_PRG			
	Scope     Name       1     Image: Var Board_SW_Input       2     Var Board_LED_Input       3     Image: Var Board_LED_Output       4     Var CycleCounter       5     Var CyclePerTick	Address Data type BYTE BYTE BYTE INT INT		Comment Switch Input LED Input OLD Output 1 Cycle = 20ms 1 Tick = 1s	Attributes Variables	Properties <b>V</b> Notifications
Second Seco	<					
EtherNet_IP_Scanner (EtherNet/IP Scanner)	5 Board LED Output :=	AND Board_LED_Inpu Board_LED_Input *				
Renesas_OpENer_Device (Renesas OpENer De	5 Board LED Output :=	Board_LED_Input *		_	Programs	
Renesas_OpENer_Device (Renesas OpENer Device)	5         Board_LED_Output :=           6         ELSE           7         Board_LED_Output :=           8         END_IF	Board_LED_Input *			Programs	R
POUs	5         Board_LED_Output :=           6         ELSE           7         Board_LED_Output :=           8         END_IF	Board_LED_Input *				
POUs Services Devices Devices (Renesas OpENer Device) POUs Services (Renesas OpENer Devices (Renesas O	5         Board_LED_Output :=           6         ELSE           7         Board_LED_Output :=           8         END_IF	Board_LED_Input *			100	
POUs Services Devices	Derror(s)  Derror(s) Derro	Board_LED_Input *	2;	Object	100	

Figure 6-1 CODESYS Project included in this sample program

## 6.2 IP and MAC Address Configuration

#### 6.2.1 IP Configuration

This program sets own IP and related parameters to the following values defined statically by "g\_lwip\_port0\_netif\_cfg" variable in "common\renesas\opener\_port\_instance.c".

If changing the IP configuration, please change the following parameters.

Item	Value	Variable
IP Address	192.168.1.170	g_lwip_port0_netif_cfg.ip_address
Net Mask	255.255.255.0	g_lwip_port0_netif_cfg.subnet_mask
Gateway	192.168.1.1	g_lwip_port0_netif_cfg.gateway_address
Address		
Host Name	OPENER_NETIF0	g_lwip_port0_netif_cfg.p_host_name
DHCP	LWIP_PORT_DHCP_DISABLE	g_lwip_port0_netif_cfg.dhcp

If using DHCP, please set "g\_lwip\_port0\_netif\_cfg.dhcp" to "LWIP\_PORT\_DHCP\_ENABLE". After the program starts, DHCP process is executed to get an IP address dynamically. If the program gets an IP address, EtherNet/IP communication starts.



## 6.2.2 MAC Address Configuration

The MAC address is set to the following values defined statically by FSP Configurator.

#### Table 6-2 MAC Address Configuration

Item	Value (Decimal)
MAC Address	00:11:22:33:44:55

If changing the MAC address, please change the value on FSP configuration.

Regarding FSP configuration, please see the "RZ/T2M, RZ/N2L Getting Started with Flexible Software Package" (r01an6434ejxxxx-rzt2-rzn2-fsp-getting-started.pdf) document.

## 6.3 Startup Software PLC

#### 6.3.1 Open CODESYS project

Please select "File" > "Open project..." in CODESYS tool bar and open "opener\_sample\_app.project" in "scanner/codesys".

If the project is opened properly, the opened project is shown in "Device" section located at left in the following window.



Figure 6-2 Open a CODESYS Project



## 6.3.2 Network Configuration

Please double-click "Device (CODESYS Control Win V3)" to open "Communication Settings" at center section, and please click "Scan Network..." to open "Select Device" window.

opener_sample_app.project - CODESYS							- o x
File Edit View Project Build Online Debug Tool	ls Window Help						۲
🔁 🚅 📓 🗠 여 🖇 🖻 🛍 🗙 👪 🌿 🗍	에 에 에 🛍 🛅 - 🕤 🕮 🖡	Application [Device: PLC Logic] 🔹 👒 👒	> = 🔏   C= 🕫	= 4= 3   ¢   <b>∭</b>	<b>≓</b>   ∜/		
Devices 🗸 🗸 🗸 🗸	M Device X					-	Properties 👻 🗭 🗙
opener_sample_app	Communication Settings	Scan Network Gateway + Device +					🏹 Filter 🔹 🔀 Sort by 🔹
Oevice (CODESYS Control Win V3)     Oevice (CODESYS Control Win V3)	Communication Secongs						ੈ \$ Sort order ▼
Application	Applications						Property Value
1 Library Manager	Backup and Restore		•				
PLC_PRG (PRG)			And the set of				
Task Configuration     Source State S	Files				•		
EtherNet_IP_Scanner.IOCycle	Log		Gateway			-	
ENIPScannerServiceTask (IEC-Tasks)	PLC Settings	Gateway-1		~		~	
EtherNet_IP_Scanner.ServiceCycle	PLC Settings	IP-Address localhost		Press ENT	TER to set active path.		
PLC_PRG	PLC Shell	Port:					
Ethernet (Ethernet)	Users and Groups	1217					
	· · · · · · · · · · · · · · · · · · ·						
	Access Rights						
	Symbol Rights						
	IEC Objects						
	Task Deployment						
	Status						
	Status						
	Information						
		Your device can be secured. Learn more					
	<					>	
POUs 🔮 Devices	<b>`</b>						
Messages - Total 0 error(s), 0 warning(s), 0 message(s)						<b>-</b> ₽ X	
	rror(s) 😗 0 warning(s) 🚯 0 message	e(s) X X					
Description			Project	Object	Position		
							Description
							Description
							Properties Votifications
				Last build: 😋 0 😗 0	Precompile 🧹	6	Project user: (nobody)

Figure 6-3 Communication Settings



If the software PLC is found after scanning network, the device name (here, PC name) is shown under Gateway tree. Please double-click this device name (in blue portion).

Gateway-1	Device Name:  Scan Network
	Wink Device Address: 0000.8F53
	Block driver: UDP
	Encrypted Communication:
	TLS supported Number of
	channels: 4
	Serial number: 🗸

Figure 6-4 Select Device

If the network is configured properly, its configuration is shown in "Communication Settings" tab, and there are the green marks at gateway and device portions.

Device X					
Communication Settings	Scan Network Gate	eway 👻 Device 👻			_ ^
Applications			_		
Backup and Restore					
Files				•	
Log		Gateway-1	vay	[0000.BF53] (active)	
PLC Settings		IP-Address:		Device Name:	
PLC Shell		lo calhost Port:		Device Address:	
Users and Groups		1217		0000.BF53	
Access Rights				Target ID: 0000 0001	
Symbol Rights				Target Type: 4096	
IEC Objects				Target Vendor: 3S - Smart Software Solutions GmbH	
Task Deployment	-			Target Version: 3.5.15.10	
Status					

Figure 6-5 Green Marks at Gateway and Device Portions



## RZ/N2L Group RZ/N2L Industrial Network SOM Kit Application Note: EtherNet/IP OpENer Sample Program

## 6.3.3 Interface and IP address configuration

Please click "Ethernet (Ethernet)" in left section to open "Ethernet" tab in center section.

After that, please select "..." button to select network interface ethernet which is connected withRZ/N2L Industrial Network SOM Kit, and please configure the IP address and related address values of the ethernet network interface.

evices 👻 🕂 🗙	Device <b>Ethernet</b> X				-	Properties 🗸 🖡
opener_sample_app         image: app image: a	General Log Status Ethernet Device I/O Mapping Ethernet Device IEC Objects Information	Interface イーサネ IP address Subnet mask Default gateway Adjust operatine	192       . 168       . 1       . 150         255       . 255       . 255       . 0         192       . 168       . 1       . 1			Properties ♥ ₩ ♥ Filter ▼   *\$ Sort by ▼ ≜↓ Sort order ▼ Property   Value
POUs 😤 Devices	<				>	
essages - Total 0 error(s), 0 warning(s), 0 message(s)					<b>→</b> 쿠 X	
	🕈 0 warning(s) 🚯 0 message(s) 🗙					ĺ
escription		Project	Object	Position		
						Description

Figure 6-6 Open Ethernet tab


Next, please double-click "Renesas\_OpENer\_Device (Renesas OpENer Device)" in the left section to open "Renesas\_OpENer\_Device" tab in center section.

Finally, please set IP address form to the RZ/N2L Industrial Network SOM Kit device IP address.

opener_sample_app.project - CODESYS				- 🗆 X
File Edit View Project Build Online Debug Tools	Window Help			T
'iii 🛩 🖬 🚙 🗠 🖂 🌡 🛍 🛍 🗙 🛤 🎎 💑 🏂 💷 🤋		ition [Device: PLC Logic] 👻 🥨 📦 👞 👋	[19] 41 42   ¢   🛒	글'   맛
Devices 👻 👎 🕇	C Device Ethernet	Renesas_OpENer_Device 🗙	-	Properties 👻 🕂 🗙
opener_sample_app     Gener_sample_app     Device (CODESYS Control Win V3)	General	Address Settings		Y Filter ▼ Sort by ▼
🖶 🗐 PLC Logic 🖻 🕜 Application	Connections	IP address 192 . 168 . 1 . 170	EtherNet/	Property Value
Library Manager     Interformer (PRG)	Assemblies			
☐ I Task Configuration ☐ W ENIPScannerIOTask (IEC-Tasks)	User-Defined Parameters	Electronic Keying Keying Options		
European Performance (Constant)     European Performance (Con	Log	Compatibility check		
EnterStatiliterServiceTasks(LEC-Tasks)      EtherNet_IP_Scanner.ServiceCyde      Statistics	EtherNet/IP I/O Mapping	Strict identity check     Check device type     12		
PLC_PRG	EtherNet/IP IEC Objects	Check vendor ID 1105		
Ethernet (Ethernet)     EtherNet_IP_Scanner (EtherNet/IP Scanner)	Status	Check product code 65001  Check major revision 2		
Renesas_OpENer_Device (Renesas OpENer Device)	Information	Check minor revision 3		
		Restore Default Values		
POUs 🐲 Devices	<		>	
Messages - Total 0 error(s), 0 warning(s), 0 message(s)			<b>-</b> ∓ X	
- O error	s) 🕐 0 warning(s) 🚯 0 message(s) 🚺	< 😿		
Description	· · · · · · · · · · · · · · · · · · ·	Project Object	Position	
				Description
				Descritica V Mattheations
		Last build: 😋 0 🕐 0 🛛 F	Precompile 🗸 🛛 🔐	Properties Votifications Project user: (nobody)
			Precompile 🧹 🖓	Project user: (nobody) 🛛 🕅 🤅

Figure 6-7 Renesas\_OpENer\_Device (Renesas OpENer Device)



## 6.4 Operation Check

#### 6.4.1 Build Project and Start Application

Follow the following steps and figure to build the project and start the application.

- 1. Click "Build" button in the tool bar to build the CODESYS project.
- 2. Click "Login" button in the tool bar to login the network.
- 3. Click "Start" button in the tool bar to run network and application.

🎦 📽 🖳 🕘 🗠 🗠 🖄 🎭 🕼 🗙 構 🍇 🍓 🍐 🗍 🗮 🧌 🏦 🎢 🝓 🕍 🗗 🎬 Application [Device: PLC Logic] 🔹 🧐 🤴 🕨 🔚 💐 [第 15] 🔤 🖆 🎘 👘   第 1 👘   💎
🖆 😰 🖩 🚇 🗠 🗢 🐁 🛍 🏝 🗙 🚔 🍇 🕌 🐛 🧌 🧌 🧌 🎁 🎁 🏙 🔓 🖆 🛗 Application (Device: PLC Logic) 🔹 🧐 🎯 🖒 🖌 💐 🗐 🖆 🏥 🍣 (中) 🛒 🛒 👘
🎦 🚰 🖩 🚳 🗠 🖂 🕸 🎕 🗙 🕌 🍇 🍓 🍇 📕 🧌 🧌 🧌 🎲 🦄 🍓 🏰 🍙 🎦 🕮   Application [Device: PLC Logic] 🔹 🧐 🍑 💼 📽   江戸 🕾 💷 🖇   江戸 🖅 🗮 🖇   本

Figure 6-8 Build Project and Start Application

## 6.4.2 Check Network Connection

If the CODESYS application on PC connects with OpENer application on RZ/N2L properly, "Device", "Ethernet", "EtherNet\_IP\_Scanner", and "Renesas\_OpENer\_Device" in left section are marked with green cycle mark.

	_
opener_sample_app	•
🖹 🤣 折 Device [connected] (CODESYS Control Win V3)	
PLC Logic	
🖹 💮 Application [run]	
🔤 🎁 Library Manager	
PLC_PRG (PRG)	
Task Configuration	
🗐 🍪 ENIPScannerIOTask (IEC-Tasks)	
EtherNet_IP_Scanner.IOCycle	
💷 🍪 ENIPScannerServiceTask (IEC-Tasks)	
EtherNet_IP_Scanner.ServiceCycle	
🖹 🍪 MainTask (IEC-Tasks)	
PLC_PRG	
🖹 😏 🚮 Ethernet (Ethernet)	
🖹 🧐 🚹 EtherNet_IP_Scanner (EtherNet/IP Scanner)	
😔 近 Renesas_OpENer_Device (Renesas OpENer Device)	

Figure 6-9 Check Network Connection



#### 6.4.3 Check Application Behavior

Please open "EtherNet/IP I/O Mapping" page in "Renesas\_OpENer\_Device" tab.

This page shows the Exclusive Owner Connection and Input Only Connection mapping which indicates the connections between the CODESYS PLC application and the Assembly objects on RZ/N2L OpENer application. The "Current Value" column indicates the LED and SW3 values.

- > The Exclusive Owner Connection is bound to LED of RZ/N2L Industrial Network SOM Kit.
  - The LEDs lights by shifting with [SW Value] Hz.
- The Input Only Connection is bound to J6-1 ~ J6-4 of RZ/N2L Industrial Network SOM Kit.
   The SW values indicates the frequency of LED light shifting.

General	Find	Filter Show all		- 🕂 Ada	FB for IO Ch	annel →	Go to Instance
Connections	Variable		Mapping	Channel	Address	Туре	Current Value
connections	🖃 🚞 Board LED Exclusiv	e Owner					
Assemblies	😑 👋 Application.PLC	PRG.Board_LED_Input	°\$	Board LED Input Data	<del>%IB0</del>	BYTE	2
	· · · · · · · · · · · · · · · · ·			Bit0	%IX0.0	BOOL	FALSE
User-Defined Parameters	🍫			Bit1	%IX0.1	BOOL	TRUE
	🍫			Bit2	%IX0.2	BOOL	FALSE
Log	🍫			Bit3	%IX0.3	BOOL	FALSE
				Bit4	%IX0.4	BOOL	FALSE
EtherNet/IP I/O Mapping	🍫			Bit5	%IX0.5	BOOL	FALSE
				Bit6	%IX0.6	BOOL	FALSE
EtherNet/IP IEC Objects	🍫			Bit7	%IX0.7	BOOL	FALSE
Status	😑 🍢 Application.PLC		~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	Board LED Output Data	%QB0	BYTE	4
Status	*>			Bit0	%QX0.0	BOOL	FALSE
Information	*>			Bit1	%QX0.1	BOOL	FALSE
	*>			Bit2	%QX0.2	BOOL	TRUE
	*>			Bit3	%QX0.3	BOOL	FALSE
	- *			Bit4	%QX0.4	BOOL	FALSE
	<b>*</b> ø			Bit5	%QX0.5	BOOL	FALSE
	<b>*</b> ø			Bit6	%QX0.6	BOOL	FALSE
	L			Bit7	%QX0.7	BOOL	FALSE
	🖮 🚞 Board SW Input Or	ily					
	🖹 👋 Application.PLC	C_PRG.Board_SW_Input	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	Board SE Input Data	%IB1	BYTE	5
	🍫			Bit0	%IX1.0	BOOL	TRUE
	🍫			Bit1	%IX1.1	BOOL	FALSE
	🍫			Bit2	%IX1.2	BOOL	TRUE
	<b>*</b> >			Bit3	%IX1.3	BOOL	FALSE
	<b>*</b> >			Bit4	%IX1.4	BOOL	FALSE
	*>			Bit5	%IX1.5	BOOL	FALSE
	<b>*</b> >			Bit6	%IX1.6	BOOL	FALSE
	L. No			Bit7	%IX1.7	BOOL	FALSE
	<						
	Reset Mapping Always updatevariables Use parent device setting			ng			

Figure 6-10 Check Application Behavior



# 7. Appendix

## Appendix A: OSS implemented in the sample code

The following three OSS are used in the sample code.

#### OpENer

The "OpENer" is an open-source software for I/O communication adapters of EtherNet/IP. Please refer the following link for the detail.

https://github.com/EIPStackGroup/OpENer

Git comment ID used in this sample software: 05cdd03

This package is the RZ/N2L port of OpENer and includes OpENer source codes. Regarding the open-source license of OpENer, please see the following file.

common\oss\OpENer\license.txt

# FreeRTOS

The FreeRTOS is an open-source software for real-time operating system (RTOS) for microcontrollers. Please refer the following link for the details.

https://aws.amazon.com/freertos/

https://github.com/aws/amazon-freertos

Git comment ID used in this sample software: a038063

The RZ/N2L port of OpENer includes FreeRTOS source codes as a RTOS kernel. Regarding the opensource license of OpENer, please see the following file.

common\oss\amazon-freertos\LICENSE

## lwIP

The lwIP is an open-source software for a small independent implementation of the TCP/IP protocol suite. Please refer the following link for the details.

https://savannah.nongnu.org/projects/lwip/

https://github.com/lwip-tcpip/lwip

Git comment ID used in this sample software: 79cd89f

The RZ/N2L port of OpENer includes IwIP source codes as a TCP/IP stack. Regarding the open-source license of IwIP, please see the following file.

common\oss\lwip\COPYING



# Appendix B: Assembly Objects and I/O Connections

This sample application has the 7 instances of Assembly object. 5 of these instances are bound to the following array variables.

Instance No.	Туре	Description	Bound variables
100 (0x64)	Static Input	Input of Exclusive Owner I/O Connection bound to LED	g_assembly_data_led_input[1]
101 (0x65)	Static Input	Input of Input Only I/O Connection bound to SW3	g_assembly_data_sw_input[1]
150 (0x96)	Static Output	Input of Exclusive Owner I/O Connection bound to LED	g_assembly_data_led_output[1]
151 (0x97)	Static Configuration	Configuration of I/O Connections	g_assembly_data_config[4]
154 (0x9A)	Static I/O	Accessing by explicit message connection only	g_assembly_data_explicit[4]
238 (0xEE)	Static Output	Heartbeat output of Input only I/O Connection bound to SW3	-
237 (0xED)	Static Output	Heartbeat output of listen only I/O Connection.	-

#### Table 7-1 Assembly Objects and I/O Connections



# Appendix C: Support CIP Object Classes

The CIP object classes on OpENer RZ/N2L port are shown below.

#### Table 7-2 CIP Object Class on OpENer RZ/N2L port

Object Class #	Object Class Name
0x01	Identity
0x02	Massage Router
0x04	Assembly
0x06	Connection Manager
0xF5	TCP/IP Interface
0xF6	Ethernet Link
0x48	QoS

#### Table 7-3 0x01: Identity

Class	Attributes		
#	Attribute Name	Get	Set
1	Revision	0	-
2	Max Instance	0	-
3	Number of Instance	0	-
4	Optional Attribute List	-	-
5	Optional Service List	-	-
6	Max Number Class Attributes	0	-
7	Max Number Instance Attributes	0	-
Class	Services		·
#	Service Name		
0x01	Get_Attributes_All		
0x0E	Get_Attribute_Single		
Instar	nce Attributes*		
#	Attribute Name	Get	Set
1	Vendor ID	0	-
2	Device Type	0	-
3	Product Code	0	-
4	Revision	0	-
5	Status	0	-
6	Serial Number	0	-
7	Product Name	0	-
Instar	nce Service		
#	Service Name		
0x01	Get_Attributes_All		
0x05	Reset		
0x0E	Get_Attribute_Single		

\*: The values of instance attributes #1~#4, #6, and #7 are configured by macros in "deveicedata.h" in "common\renesas\oss\_deps\opener" directory.



#### Table 7-4 0x02: Massage Router

Class	Class Attributes					
#	Attribute Name	Get	Set			
1	Revision	0	-			
2	Max Instance	0	-			
3	Number of Instance	0	-			
4	Optional Attribute List	-	-			
5	Optional Service List	-	-			
6	Max Number Class Attributes	0	-			
7	Max Number Instance Attributes	0	-			
Class	Services					
#	Service Name					
0x01	Get_Attributes_All					
0x0E	Get_Attribute_Single					
Instan	ce Attributes*					
#	Attribute Name	Get	Set			
No instance attributes are implemented.						
Instance Service						
#	Service Name					
0x0E	Get_Attribute_Single					

#### Table 7-5 0x04: Assembly

Class	Attributes		
#	Attribute Name	Get	Set
1	Revision	0	-
2	Max Instance	0	-
3	Number of Instance	0	-
4	Optional Attribute List	-	-
5	Optional Service List	-	-
6	Max Number Class Attributes	0	-
7	Max Number Instance Attributes	0	-
Class	Services		
#	Service Name		
0x0E	Get_Attribute_Single		
Instan	ice Attributes*		
#	Attribute Name	Get	Set
3	Data	0	0
4	Size	0	-
Instan	ice Service		
#	Service Name		
0x0E	Get_Attribute_Single		
0x10	Set_Attribute_Single		



## Table 7-6 0x06: Connection Manager

Class	Attributes		
#	Attribute Name	Get	Set
1	Revision	0	-
2	Max Instance	0	-
3	Number of Instance	0	-
4	Optional Attribute List	-	-
5	Optional Service List	-	-
6	Max Number Class Attributes	0	-
7	Max Number Instance Attributes	0	-
Class	Services		
#	Service Name		
0x01	Get_Attributes_All		
0x0E	Get_Attribute_Single		
Instar	nce Attributes*		
#	Attribute Name	Get	Set
No ins	stance attributes are implemented.	·	·
Instar	nce Service		
#	Service Name		
0x0E	Get_Attribute_Single		
0x4E	Forward_Close		
0x54	Forward_Open		
0x5a	Get_Connection_Owner		
0x5b	Large_Forward_Open		



## Table 7-7 0xF5: TCP/IP Interface

Class	Attributes				
#	Attribute Name	Get	Set		
1	Revision	0	-		
2	Max Instance	0	-		
3	Number of Instance	0	-		
4	Optional Attribute List	-	-		
5	Optional Service List	-	-		
6	Max Number Class Attributes	0	-		
7	Max Number Instance Attributes	0	-		
Class	Services				
#	Service Name				
0x01	Get_Attributes_All				
0x0E	0E Get_Attribute_Single				
Instan	ce Attributes*				
#	Attribute Name	Get	Set		
1	Status	0	-		
2	Configuration Capacity	0	-		
3	Configuration Control	0	0		
4	Physical Link Object	0	-		
5	Interface Configuration	0	-		
6	Host name	0	-		
8	TTL Value	0	-		
9	Mcast Config	0	-		
13	Encapsulation Inactivity Timeout	0	0		
Instan	Instance Service				
#	Service Name				
0x01	Get_Attributes_All				
0x0E	Get_Attribute_Single				
0x10	Set_Attribute_Single				



#### Table 7-8 0xF6: Ethernet Link

Class	Attributes			
#	Attribute Name	Get	Set	
1	Revision	0	-	
2	Max Instance	0	-	
3	Number of Instance	0	-	
4	Optional Attribute List	-	-	
5	Optional Service List	-	-	
6	Max Number Class Attributes	0	-	
7	Max Number Instance Attributes	0	-	
Class	Services			
#	Service Name			
0x01	Get_Attributes_All			
0x0E	Get_Attribute_Single			
Instan	ce Attributes*			
#	Attribute Name	Get	Set	
1	Interface Speed	0	-	
2	Interface Flag	0	-	
3	Physical Address	0	-	
7	Interface Type	0	-	
11	Interface Capability	0	-	
Instan	ce Service			
#	Service Name			
0x01	Get_Attributes_All			
0x0E	Get_Attribute_Single			



#### Table 7-9 0x48: QoS

Class Attributes					
#	Attribute Name	Get	Set		
1	Revision	0	-		
2	Max Instance	0	-		
3	Number of Instance	0	-		
4	Optional Attribute List	-	-		
5	Optional Service List	-	-		
6	Max Number Class Attributes	0	-		
7	Max Number Instance Attributes	0	-		
Class	Services				
#	Service Name				
0x01	Get_Attributes_All				
0x0E	Get_Attribute_Single				
Instance Attributes*					
#	Attribute Name	Get	Set		
1	802.1Q Tag Enable	0	-		
2	DSCP PTP Event	0	-		
3	DSCP PTP General	0	-		
4	DSCP Urgent	0	0		
5	DSCP Scheduled	0	0		
6	DSCP High	0	0		
7	DSCP Low	0	0		
8	DSCP Explicit	0	0		
Instan	ce Service				
#	Service Name				
0x01	Get_Attributes_All				
0x0E	Get_Attribute_Single				



# Appendix D: FSP Configuration for VSC8531

RZ/N2L Industrial Network SOM Kit has VSC8531 as PHY chip. If reconfiguring by latest FSP, FSP configuration and source code needs to change from default.

(1) Regenerate source files by lates FSP

Remove the following four folders. After that, open the project according to section 5.

- When using e2studio, \project\rzn2l\_som\opener\_single\e2studio
- When using EWARM, \project\rzn2l\_som\opener\_single\ewarm



Figure 7-1 Remove folder generated by FSP

(2) Change ethernet driver configuration for VSC8531

Configure g\_ether\_phy0 Ethernet Driver on r\_ether\_phy for VSC8531 as shown in Figure 7-2. Configuration value for VSC8531 shows in Table 7-10.



Figure 7-2 Ethernet Driver Configuration for VSC8531 (e.g. ETH0)

#### Table 7-10 FSP Configuration Value for VSC8531

Items	Default value	Config value for VSC8531	
		ETH0	ETH1
PHY-LSI Address	0	0	1
Select PHY	Default	VSC8541	VSC8541



(3) Add initialization code for VSC8531

The following code for VSC8531 initialization should be added to "ether\_phy\_targets\_initialize\_vsc8541" function in rzn/fsp/src/r\_ether\_phy/r\_ether\_phy.c.

The inclusion of "board\_som.h" is also required for code activation.

#include "board\_som.h" ~~ Omission ~~ void ether\_phy\_targets\_initialize\_vsc8541 (ether\_phy\_instance\_ctrl\_t \* p\_instance\_ctrl) { ~~ Omission ~~ /\* LED Behavior \*/ reg = ether\_phy\_read(p\_instance\_ctrl, ETHER\_PHY\_REG\_LED\_BEHAVIOR); reg &= ~(1U << ETHER\_PHY\_REG\_LED0\_FEATURE\_DISABLE\_OFFSET);</pre> reg |= 1U << ETHER\_PHY\_REG\_LED1\_FEATURE\_DISABLE\_OFFSET;</pre> ether\_phy\_write(p\_instance\_ctrl, ETHER\_PHY\_REG\_LED\_BEHAVIOR, reg); #if defined(BOARD\_RZN2L\_SOM\_KIT) /\* for VSC8531 \* /\* select extended page 2 register \*/ ether\_phy\_write(p\_instance\_ctrl, ETHER\_PHY\_REG\_EXTEND\_GPI0\_PAGE, 0x02); /\* read WoL and MAC Interface Control \*/ reg = ether\_phy\_read(p\_instance\_ctrl, 0x1b); /\* set control to slow \*/ reg &= 0xFF9F; ether\_phy\_write(p\_instance\_ctrl, 0x1b, reg); /\* Configure RX\_CLK delay and TX\_CLK delay to 2.0ns \*/ ether\_phy\_write(p\_instance\_ctrl, ETHER\_PHY\_REG\_EXPAGE2\_RGMII\_CTRL, 0x0044); /\* select extended page 0 register \*/ ether\_phy\_write(p\_instance\_ctrl, ETHER\_PHY\_REG\_EXTEND\_GPI0\_PAGE, 0x00); #endif } /\* End of function ether\_phy\_targets\_initialize() \*/



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# RZ/N2L Group RZ/N2L Industrial Network SOM Kit Application Note: EtherNet/IP OpENer Sample Program

# **Revision History**

		Description	
Rev.	Date	Page	Summary
1.00	Feb. 7, 2023	-	First issued
1.10	Aug. 7, 2023	-	Support RZ/N2L FSP v1.2.0



# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

#### 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power is supplied until the power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

#### 6. Voltage application waveform at input pin Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V<sub>IL</sub> (Max.) and V<sub>IH</sub> (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V<sub>IL</sub> (Max.) and V<sub>IH</sub> (Min.).

7. Prohibition of access to reserved addresses

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8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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