RZ/T1 Group

EtherCAT Sample Program Implementation Guide for Devices with a Built-in R-IN Engine

R01AN3071EJ0110
Rev.1.10
Aug. 31, 2018

Outline

This application note describes the sample programs for enabling RZ/T1 group devices that are equipped with a built-in engine to serve as EtherCAT® slaves that are used to control industrial AC servo motors or other devices with EtherCAT communication via PLC.

The features of the sample programs are as follows:

- The sample programs run with the Cortex®-R4 and Cortex®-M3 cores. The Cortex-M3 core handles EtherCAT communication, and the Cortex-R4 core handles generation of data to be sent to the EtherCAT master and display of received data with LEDs. A shared memory driver is used for communication between the CPUs.
- An EtherCAT communication program is created by using the Beckhoff SSC Tool (EtherCAT slave sample code generation tool). The SSC Tool project file and ESI file, and patch file that corrects the sample program coding (such as the sections that depend on the RZ/T1 hardware) are provided.
- The following two sample programs are provided:
  (1) Simple I/O controller sample program for 32-bit I/O processing (hereafter, I/O controller sample program)
  (2) Sample program for verifying the CiA402 drive profile (hereafter, CiA402 sample program)

Target Devices

RZ/T1 group devices with a built-in R-IN engine.

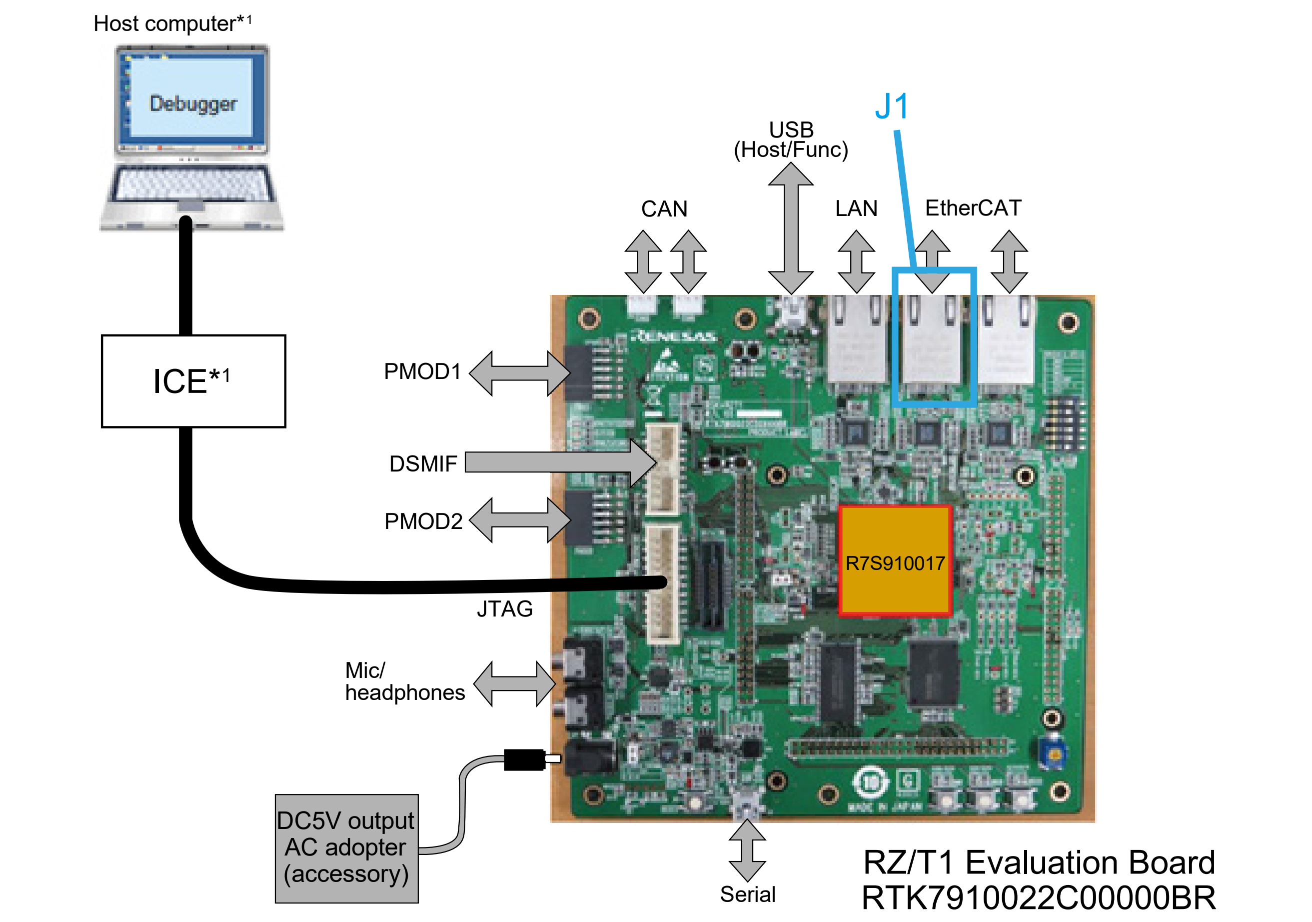
Table of Contents

1. Specifications

Table 1.1 lists the peripheral modules to be used and their applications. Figure 1.1 shows the operating environment.

Table 1.1 Peripheral Modules and Applications

Peripheral Module	Application
Clock generator	Supplying the CPU clock and low-speed on-chip oscillator clock
EtherCAT slave controller	Handling EtherCAT communication
Ethernet MAC (ETHERC)	Handling EtherCAT communication
Interrupt controller (ICUA)	Handling EtherCATSlave interrupts (EtherCAT and EtherCAT Sync0) and compare match interrupts (CMI0 and CMI1)
Compare match timer (CMT)	Handling the cycle counting of the compare match timer
Extended internal RAM	Shared memory area (Data RAM) and memory area for the program of the Cortex-M3 (Instruction RAM)
Error control module (ECM)	Initializing the ERROROUT# pin
General-purpose input/output ports	Pins which control LED display and key entry



Note 1. Indicates the device that the user needs to prepare

Figure 1.1 Operation Environment

Note: For connection with the EtherCAT master, use the LAN interface J1 (EtherCAT1 port).

2. Operation Environment

The sample programs described in this application note assume the environment below.

Table 2.1 Operation Environment

Item	Description
Board	RZ/T1 Evaluation Board RTK7910022C00000BR
CPU	RZ/T1 (with a built-in R-IN engine) R7S910017
Operating frequency	CPU clock (CPUCLK): 450 MHz (Cortex-R4) System clock (ICLK): 150 MHz (Cortex-M3)
Operating voltage	3.3 V
Operating mode	16-bit-bus boot mode SPI boot mode
Devices	• NOR flash memory Macronix MX29GL512FLT2I-10Q • Serial flash memory Macronix MX25L51245GMI-10G • EEPROM Renesas R1EX24016ASAS0 • Ethernet PHY Micrel KSZ8041TL
Communication protocol	EtherCAT®
Integrated development environment	IAR Systems Embedded Workbench® for ARM Version 8.20.2
Emulator	IAR Systems I-jet
SSC Tool	Slave Stack Code (SSC) Tool Version 5.12 provided by EtherCAT Technology Group (ETG)
Software PLC	Beckhoff Automation TwinCAT® 3

3. Peripheral Modules

For the basics of the following items, see the "*RZ/T1 Group User's Manual: Hardware*":

Clock generator, EtherCAT slave controller, Ethernet MAC (ETHERC), Interrupt controller (ICUA), Compare match timer (CMT), Error control module (ECM), Extended internal RAM, and general-purpose input/output ports

4. Hardware

4.1 Hardware Structure Example

Figure 4.1 shows an example of the hardware structure for the I/O controller sample program. Figure 4.2 shows an example of the hardware structure for the CiA402 sample program.

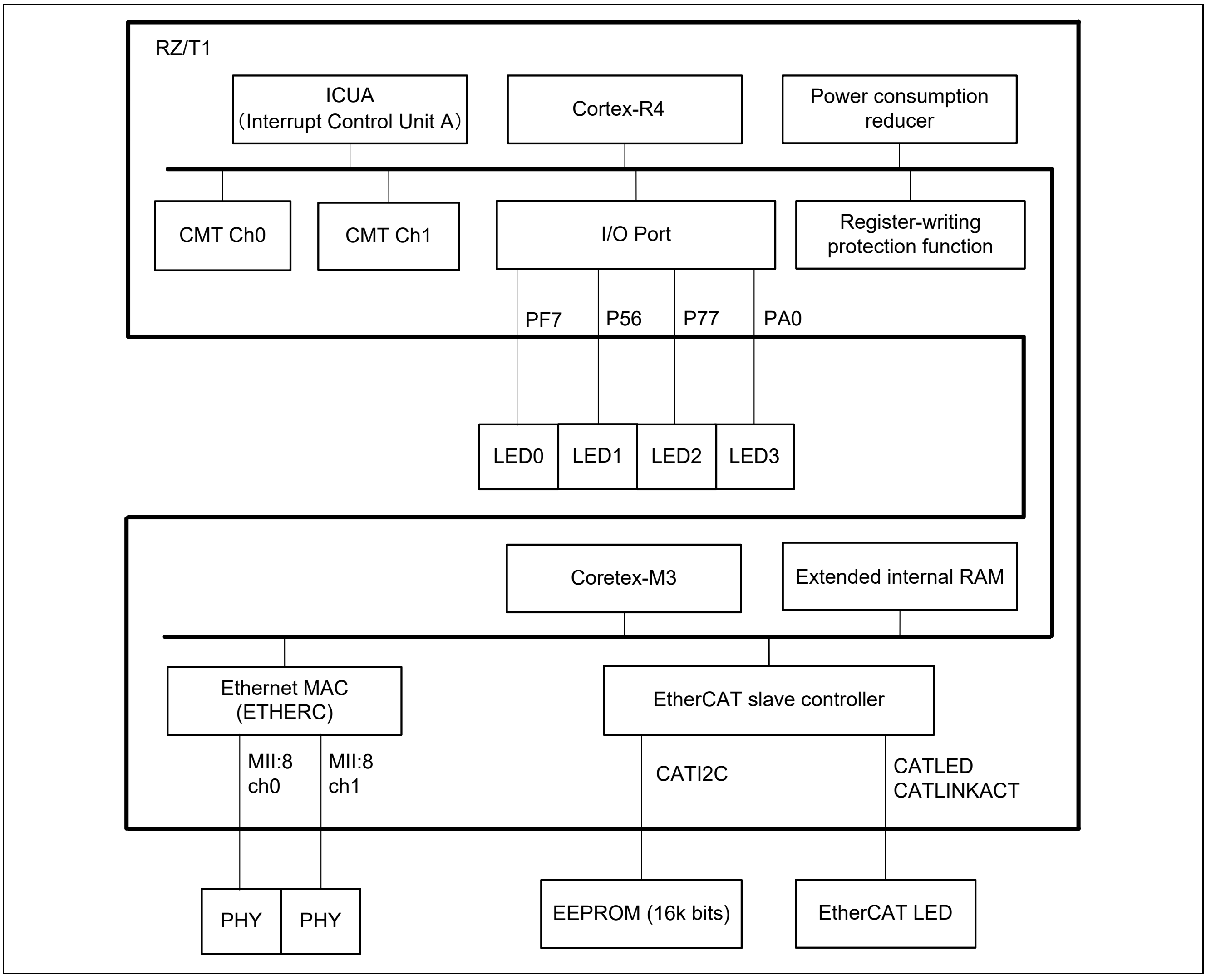


Figure 4.1 Example of the Hardware Structure for the I/O Controller Sample Program

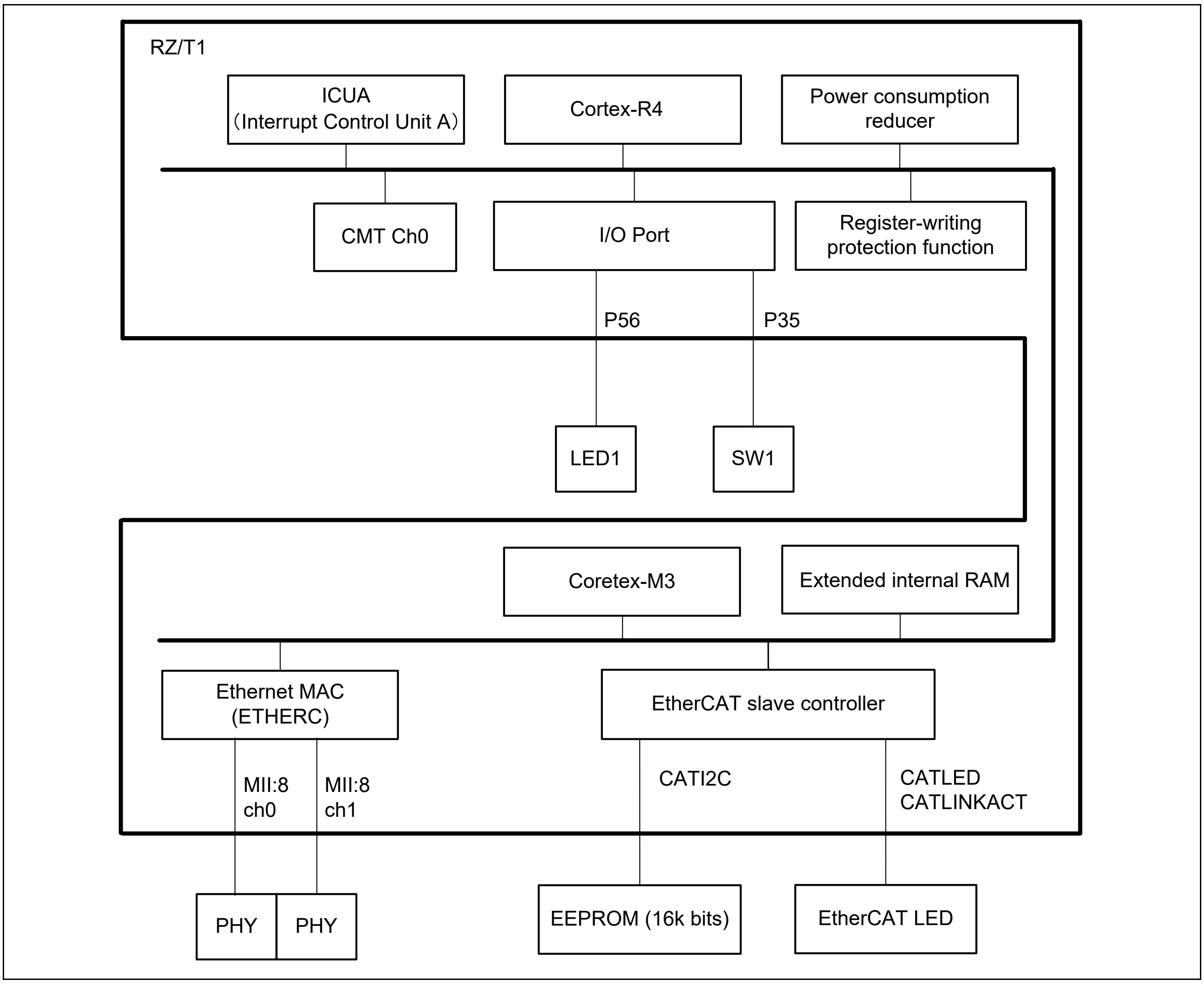


Figure 4.2 Example of the Hardware Structure for the CiA402 Sample Program

4.2 Pins Used

Table 4.1 Pins and Functions lists the pins to be used and their functions.

Table 4.1 Pins and Functions

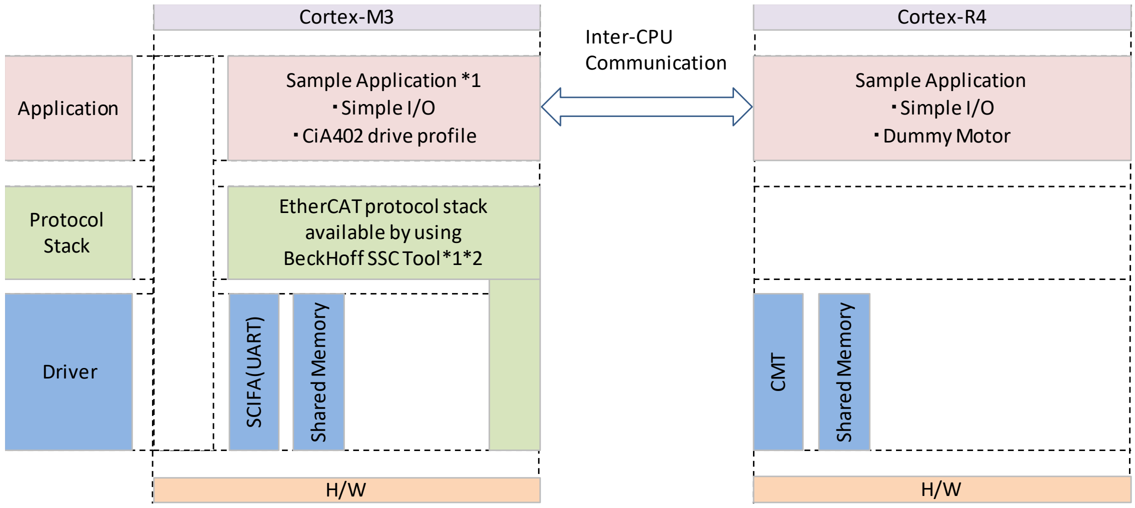
Pin Name	Input/Output	Description
MD0	Input	Select the operating mode: MD0 = L, MD1 = L, and MD2 = L: SPI boot mode MD0 = L, MD1 = H, and MD2 = L: 16-bit-bus boot mode
MD1	Input	
MD2	Input	
ETH_MDIO	Input/output	Management data signal input/output
ETH_MDC	Output	Management interface clock input/output
ETH0_RXC	Input/output	Receive clock I/O pins
ETH1_RXC		
ETH0_RXER	Input	Receive-data-error signal input
ETH1_RXER		
ETH0_RXDV	Input	Receive-data-enable signal input
ETH1_RXDV		
ETH0_RXD0-3	Input	Receive-data signal input
ETH1_RXD0-3		
ETH0_TXC	Input	10 M/100 M transmission clock (2.5/25 MHz)
ETH1_TXC		
ETH0_TXER	Output	Send-error signal output
ETH1_TXER		
ETH0_TXEN	Output	Send-enable signal output
ETH1_TXEN		
ETH0_TXD0-3	Output	Send-data signal output
ETH1_TXD0-3		
ETH0_COL	Input	Collision-detection signal input
ETH1_COL		
ETH0_CRS	Input	Carrier-sense signal input
ETH1_CRS		
CLKOUT25M0	Output	External clock output for Ethernet PHY
CLKOUT25M1		
PHYRESETOUT#	Output	PHY RESETOUT output
PHYLINK0	Input	PHY Link signal input (for Ether Switch)
PHYLINK1		
ETHSWSECOUT	Output	Per-second Ether Switch event output
ETH0_INT	Input	Ethernet PHY interrupt-request signal input
ETH1_INT		
CATI2CCLK	Output	EtherCAT EEPROM I2C clock signal output
CATI2CDATA	Input/output	EtherCAT EEPROM I2C data signal input/output
CATLINKACT1	Output	EtherCAT Link / Activity LED signal output
CATLINKACT0		
CATLEDRUN	Output	EtherCAT RUN LED signal output
CATLEDSTER	Output	EtherCAT Dual-color state LED signal
CATLEDERR	Output	EtherCAT Error LED signal output
PF7	Output	Switches LED 0 on and off.
P56	Output	Switches LED 1 on and off.

Pin Name	Input/Output	Description
P77	Output	Switches LED 2 on and off.
PA0	Output	Switches LED 3 on and off.
P35	Input	SW1 input

5. Software

5.1 Software Configuration

Figure 5.1 shows the software configuration for the sample programs.



Note 1. Renesas provides the EtherCAT SSC projects that has reflected the hardware-dependent processing and necessary modifications.

Note 2. SSC Tool: EtherCAT control program generation tool provided by Beckhoff

Figure 5.1 Software Structure Example

5.2 Directory Configuration

5.2.1 Directory Configuration of the Sample Programs for Cortex-M3

The *¥workspace¥iccarm¥Cortex-M3* directory is the base directory of the sample programs for Cortex-M3.

Table 6.1 Directory Configuration of the Sample Programs for Cortex-M3

Directory	Description
../CMSIS	Directory storing the definitions related to Cortex-M3 (CMSIS is used as is.)
../Device/Renesas/RIN_Engine/Include	Directory storing include files
../Device/Renesas/RIN_Engine/Library	Directory storing libraries
../Device/Renesas/RIN_Engine/Source/Board	Directory storing board-dependent source files
../Device/Renesas/RIN_Engine/Source/Driver	Directory storing peripheral driver source files
../Device/Renesas/RIN_Engine/Source/Project_Dual/EtherCAT_SSC_DC+hwos	Directory storing the projects for the I/O controller sample program
../Device/Renesas/RIN_Engine/Source/Project_Dual/EtherCAT_SSC_CiA402+hwos	Directory storing the projects for the CiA402 sample program
../Device/Renesas/RIN_Engine/Source/Templates	Directory storing startup files

5.2.2 Directory Configuration of the Sample Programs for Cortex-R4

The *¥workspace¥iccarm¥Cortex-R4* directory is the base directory of the sample programs for Cortex-R4.

Table 5.2 Directory Structure of the Sample Programs for Cortex-R4

Directory	Description
../ EtherCAT_SSC_DC	Directory storing the projects for the I/O controller sample program
../ EtherCAT_SSC_CiA402	Directory storing the projects for the CiA402 sample program

5.3 Operation Overview

5.3.1 I/O Controller Sample Program

Figure 5.2 shows a simple flowchart of the processing sequence from the start of the I/O controller sample program to the start of EtherCAT communication.

The program for the Cortex-R4 core makes initial settings after power is supplied to the core. First, the program copies the program code of the Cortex-M3 core, from the external flash memory to the extended internal RAM, to release the Cortex-M3 core from the reset state. Then, the program sets the LED-controlling port pins, initializes CMT0 and CMT1, and specifies the periodic event and interrupt settings.

The program for the Cortex-M3 core makes initial settings after the core is released from the reset state. After tasks are generated by HW-RTOS setup, the program starts main_task, which performs initial setup and other processing for the EtherCAT protocol stack, and then starts sub_task.

Figure 5.3 shows a simple flowchart of the processing sequence after starting EtherCAT communication.

The program for the Cortex-R4 core reads the output counter in the shared memory by using CMT0 periodic events, and then outputs the values of the low-order four bits to LED3 to LED0. The program also increments the input counter by using CMT1 periodic events, and copies the value to the shared memory.

The program for the Cortex-M3 core uses sub_task to execute the main process of the EtherCAT protocol stack. The handler for EtherCAT interrupts and EtherCAT Sync0 interrupts copies the 32-bit output values from the EtherCAT master to the output counter in the shared memory. The handler also reads the value of the input counter in the shared memory, and sends the value to the EtherCAT master as 32-bit input.

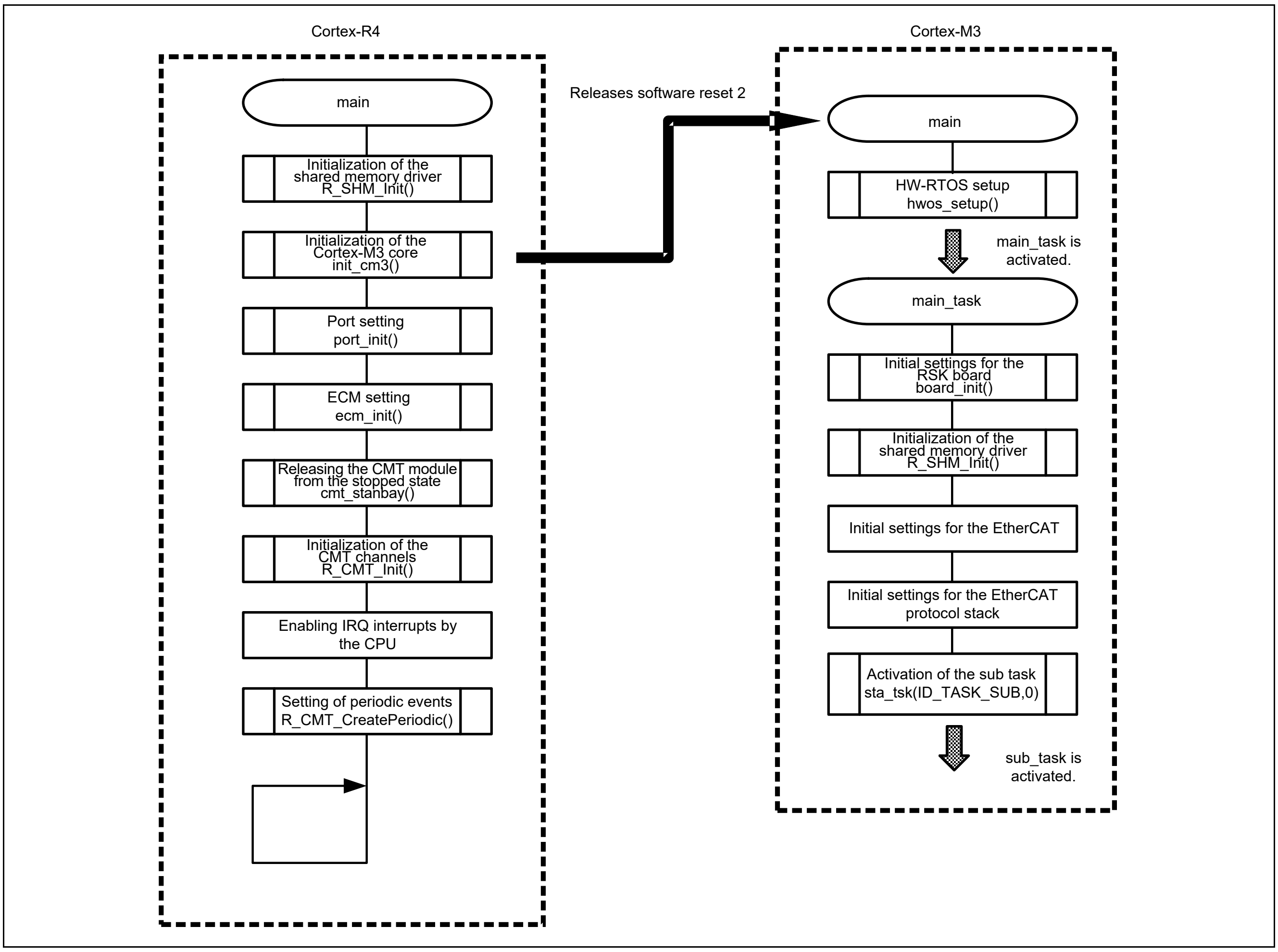


Figure 5.2 Simple Flowchart of the I/O Controller Sample Program (1)

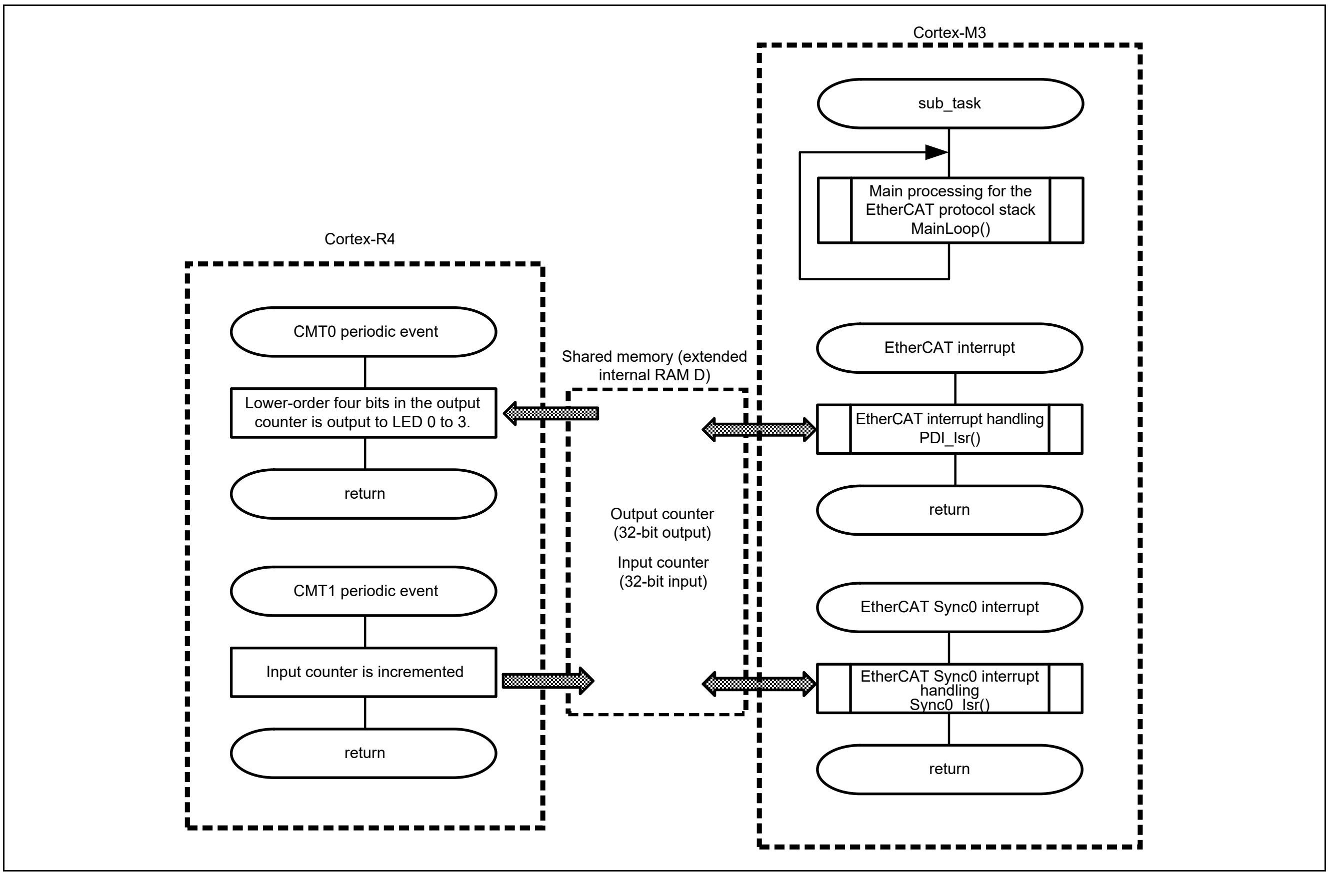


Figure 5.3 Simple Flowchart of the I/O Controller Sample Program (2)

5.3.2 CiA402 Sample Program

Figure 5.4 shows a simple flowchart of the processing sequence for the CiA402 sample program.

The program for the Cortex-R4 core makes initial settings after power is supplied to the core. First, the program copies the program code of the Cortex-M3 core, from the external flash memory to the extended internal RAM, to release the Cortex-M3 core from the reset state. Then, the program sets the LED-controlling port pins, initializes CMT0, and specifies the periodic event and interrupt settings.

In the main loop, the program checks whether an inter-CPU interrupt from the Cortex-M3 core has occurred. If an inter-CPU interrupt has occurred, the program accesses the shared memory to read the TargetPosition value and copy the ActualPosition value. The program also performs input for SW1 and output for LED1.

As pseudo motor control processing, CMT0 periodic events are used to increment the ActualPosition value until it becomes equal to the TargetPosition value while SW1 is pressed.

The program for the Cortex-M3 core makes initial settings after the core is released from the reset state. After tasks are generated by HW-RTOS setup, the program starts main_task, which performs initial setup and other processing for the EtherCAT protocol stack and CiA402 drive profile, and then executes the EtherCAT protocol stack.

The handler for EtherCAT interrupts and EtherCAT Sync0 interrupts changes the status of CiA402, reads the ActualPosition value from the shared memory, and then writes the TargetPosition value. The handler also generates an inter-CPU interrupt for the Cortex-R4 core.

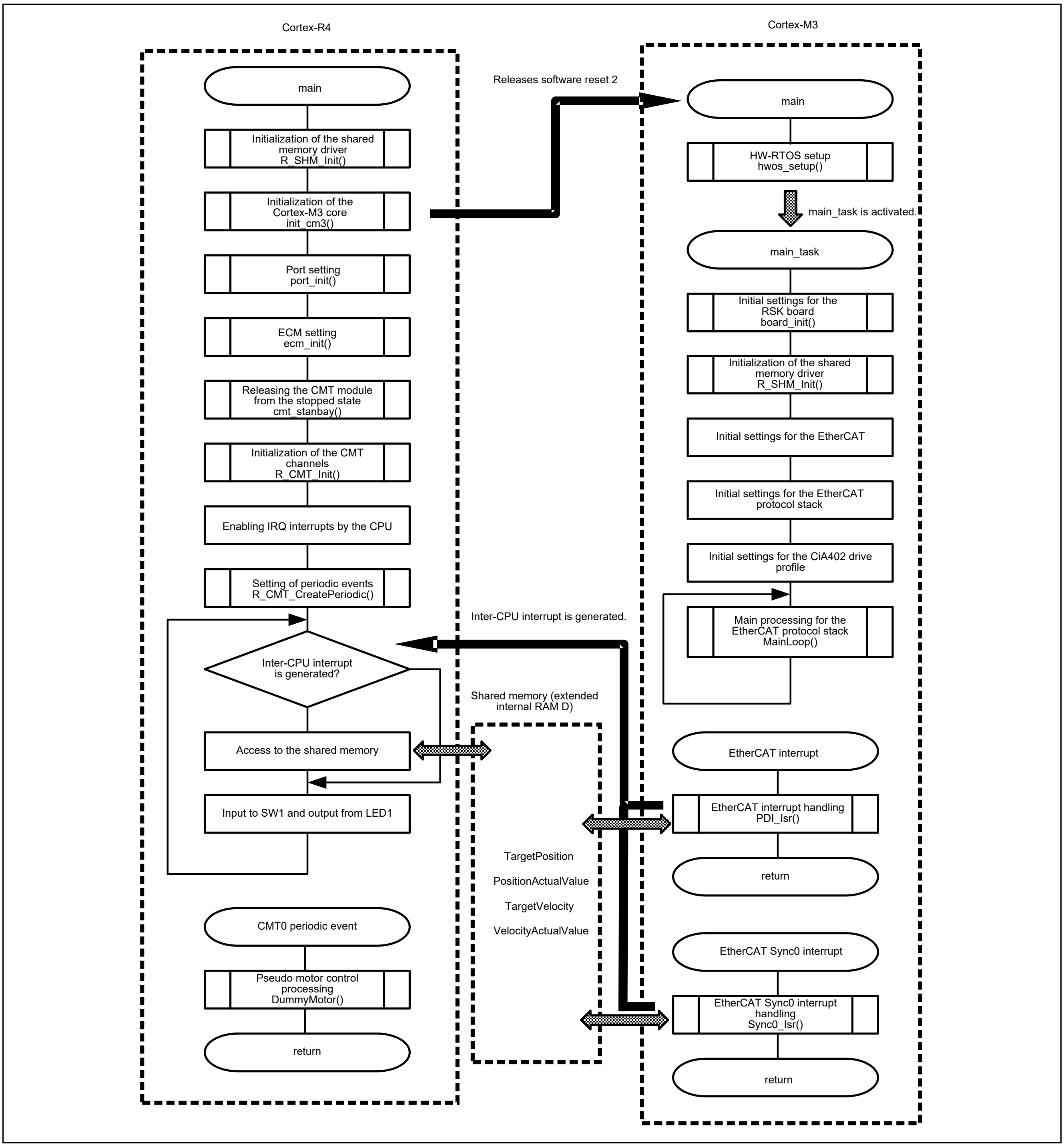


Figure 5.4 Simple Flowchart of the CiA402 Sample Program

6. Procedure for Generating Sample Programs

This chapter describes the procedure for generating sample programs. You need to prepare the EtherCAT Slave Stack Code Tool (SSC Tool) version 5.12 for this procedure.

6.1 I/O Controller Sample Program

(1) Start the SSC tool from the Windows start menu.
[EtherCAT Salve Stack Tool] > [SSC Tool]

(2) Create a new project.
[File] > [New]

(3) Press [Import], then select the SSC Tool configuration file for the I/O controller sample program.
\workspace\iccarm\Cortex-M3\Device\Renesas\RIN_Engine\Source\Project_Dual\EtherCAT_SSC_DC+hwos\RenesasSDK\CONFIG\Renesase_RZT1 config.xml

The screenshot below shows that the configuration file has been imported.

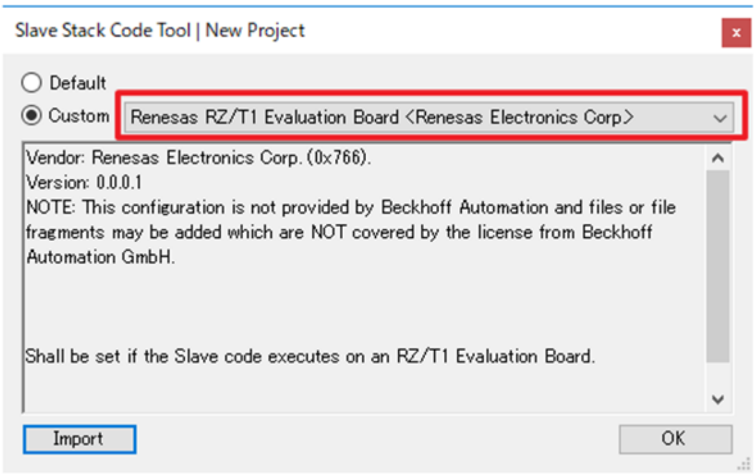


Figure 6.1 Importing SSC Tool Configuration File

Imported files are registered in the custom list and will be selectable from the drop-down list from the next time.

(1) Click [OK]. Follow the dialog and import the hardware processing file (renesashw.c).
\workspace\iccarm\Cortex-M3\Device\Renesas\RIN_Engine\Source\Project_Dual\EtherCAT_SSC_DC+hwos\RenesasSDK\renesashw.c

(2) Select [Project] > [Create new Slave Files].

(3) Press [Start] for generation of EtherCAT Salve Stack Code.

(4) [New files created successfully] will appear on the screen for a successful generation.
\workspace\iccarm\Cortex-M3\Device\Renesas\RIN_Engine\Source\Project_Dual\EtherCAT_SSC_DC+hwos\RenesasSDK\Src

6.2 CiA402 Sample Program

(1) Start the SSC Tool by double-clicking on the SSC project for the target sample program.
\workspace\iccarm\Cortex-M3\Device\Renesas\RIN_Engine\Source\Project_Dual\EtherCAT_SSC_CiA402+hwos\RenesasSDK\ssc_project\RZT1-R EtherCAT demo CiA402.esp

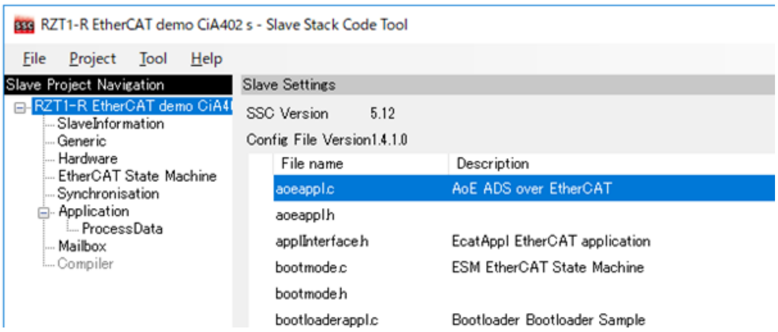


Figure 6.2 Example of Executing the Batch Command (for the I/O Controller Sample Program)

(2) Select [Project] > [Create new Slave Files].

(3) Press [Start] for generation of the EtherCAT Slave Stack Code.

(4) [New files created successfully] will appear on the screen for a successful generation.
\workspace\iccarm\Cortex-M3\Device\Renesas\RIN_Engine\Source\Project_Dual\EtherCAT_SSC_CiA402+hwos\RenesasSDK\ssc_project\Src

(5) Prepare the patch command if you don't have one yet.

Prepare You need GNU Patch 2.5.9 or later.
Download the patch command (version: 2.5.9) from the following web site, and then store the patch.exe file in a folder in a search path:
http://gnuwin32.sourceforge.net/packages/patch.htm

(6) Apply the patch.

Right-click on the apply_patch.bat file and select [Run as administrator] > [OK].

The patch file includes the RZ/T1-related corrections for the SSC source files.

Batch file:

\workspace\iccarm\Cortex-M3\Device\Renesas\RIN_Engine\Source\Project_Dual

\EtherCAT_SSC_CiA402+hwos\RenesasSDK\apply_patch.bat

Patch file:

\workspace\iccarm\Cortex-M3\Device\Renesas\RIN_Engine\Source\Project_Dual

\EtherCAT_SSC_CiA402+hwos\RenesasSDK\SSC_CiA402_yyyymmdd.patch

Note; yyyymmdd is the date of creation of the patch file.

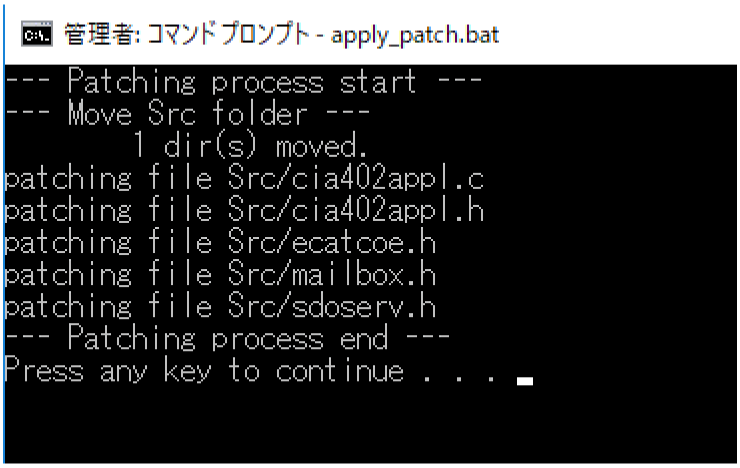


Figure 6.3 Example of Executing the Patch Command

After patching, the corrected source files are stored in the folder on the address shown below.

\workspace\iccarm\Cortex-M3\Device\Renesas\RIN_Engine\Source\Project_Dual\EtherCAT_SSC_CiA402+hwos\RenesasSDK\Src

7. Setup Needed for Connection with TwinCAT

This chapter describes how to operate the sample programs by using TwinCAT3.

Before you can start the sample programs that you created, build their source codes.

7.1 Copying the ESI Files

Before starting TwinCAT, copy the ESI files that are included in the sample programs to TwinCAT. The copy destination is *\TwinCAT\3.x\Config\IO\EtherCAT*.

- For the I/O controller sample program
  \workspace\iccarm\Cortex-M3\Device\Renesas\RIN_Engine\Source\Project_Dual
  \EtherCAT_SSC_DC+hwos\RenesasSDK\ESI_File\RZT1-R EtherCATdemo[DC].xml
- For the CiA402 sample program
  \workspace\iccarm\Cortex-M3\Device\Renesas\RIN_Engine\Source\Project_Dual
  \EtherCAT_SSC_CiA402+hwos\RenesasSDK\ESI_File\RZT1-R EtherCAT CiA402.xml

7.2 Connecting to TwinCAT

Start TwinCAT3 by using the procedure described below.

From the [Start] menu, select [Beckhoff] > [TwinCAT3] > [TwinCAT XAE (VS20XX)].

After the program is started, by selecting [File] > [New] > [Project], create a new project of the TwinCAT XAE Project type. The subsequent procedure is described below.

7.2.1 Setup for Reloading ESI Files

Load the ESI files of the sample program that you added from the TwinCAT side.

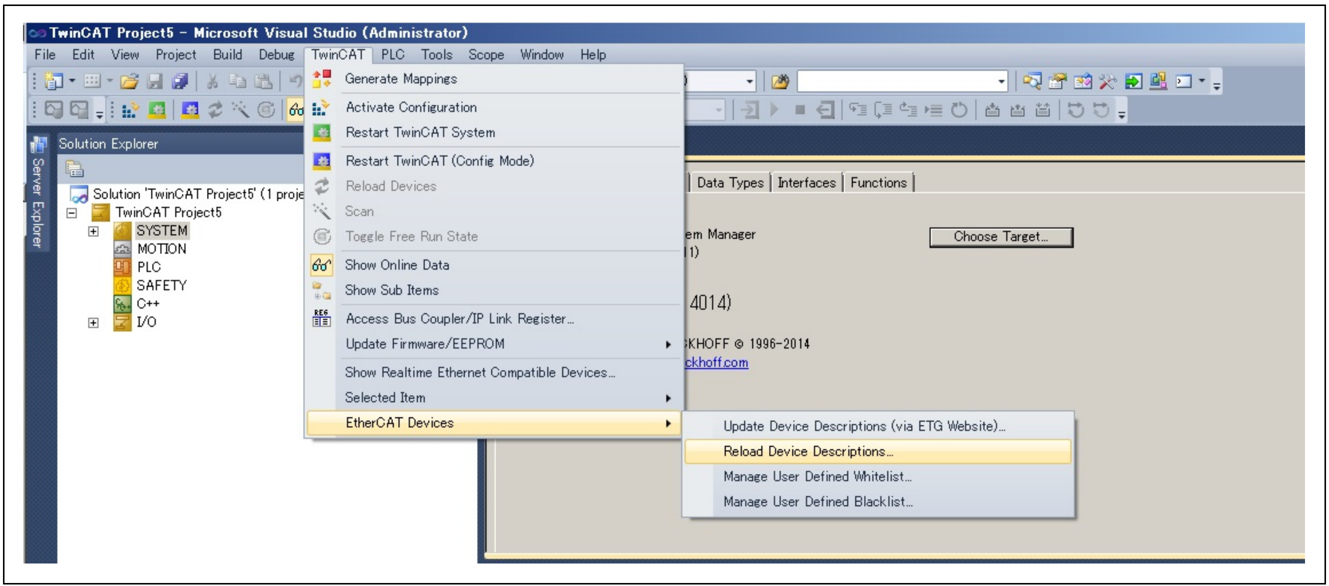


Figure 8.1 Reloading ESI Files

Select [Reload Device Descriptions] as in the above figure.

7.2.2 Scanning I/O Devices

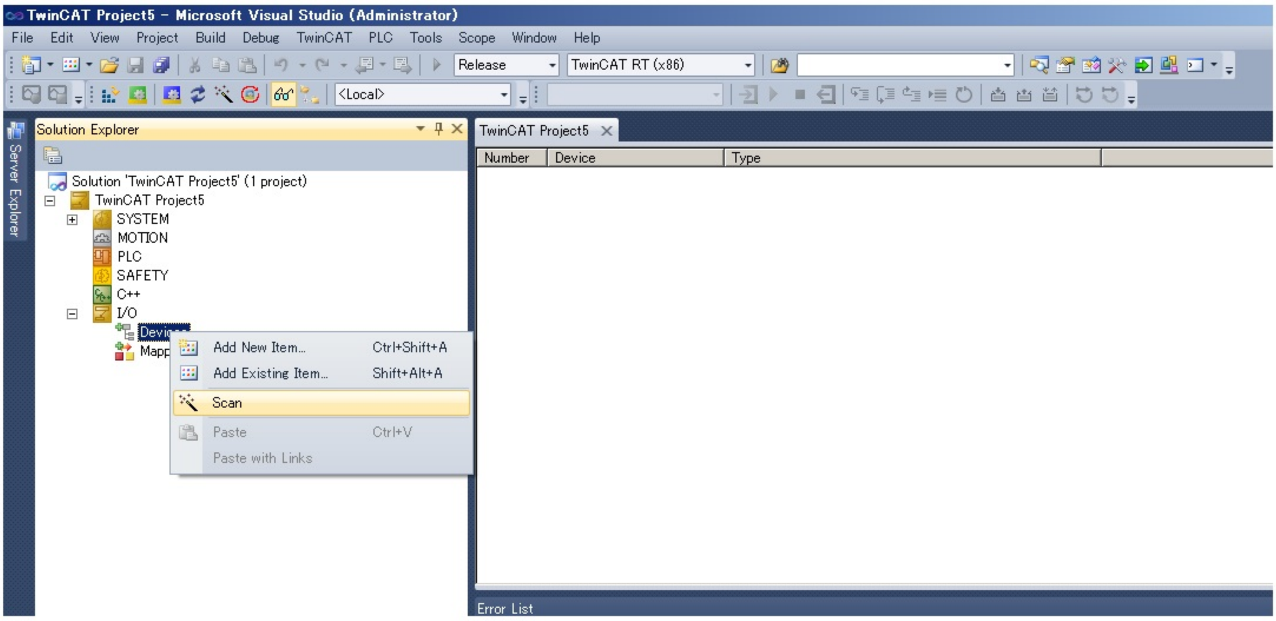


Figure 8.2 Scanning I/O Devices

As shown in the above figure, right-click [I/O Device] and select [Scan] from the menu to open a window. Execute scan in the window. After execution, perform operations as shown in Figure 8.3 and Figure 8.4.

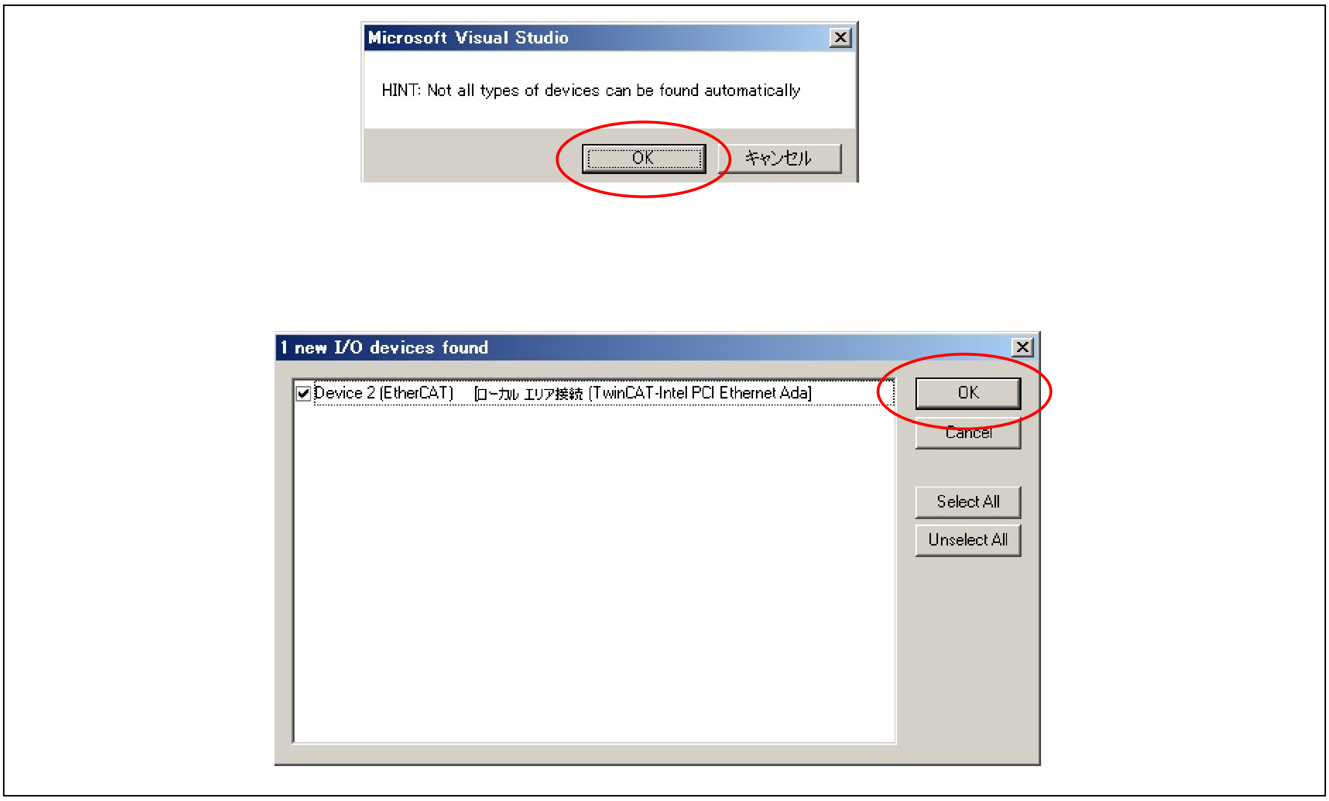


Figure 8.3 Settings for Scanning I/O Devices (1)

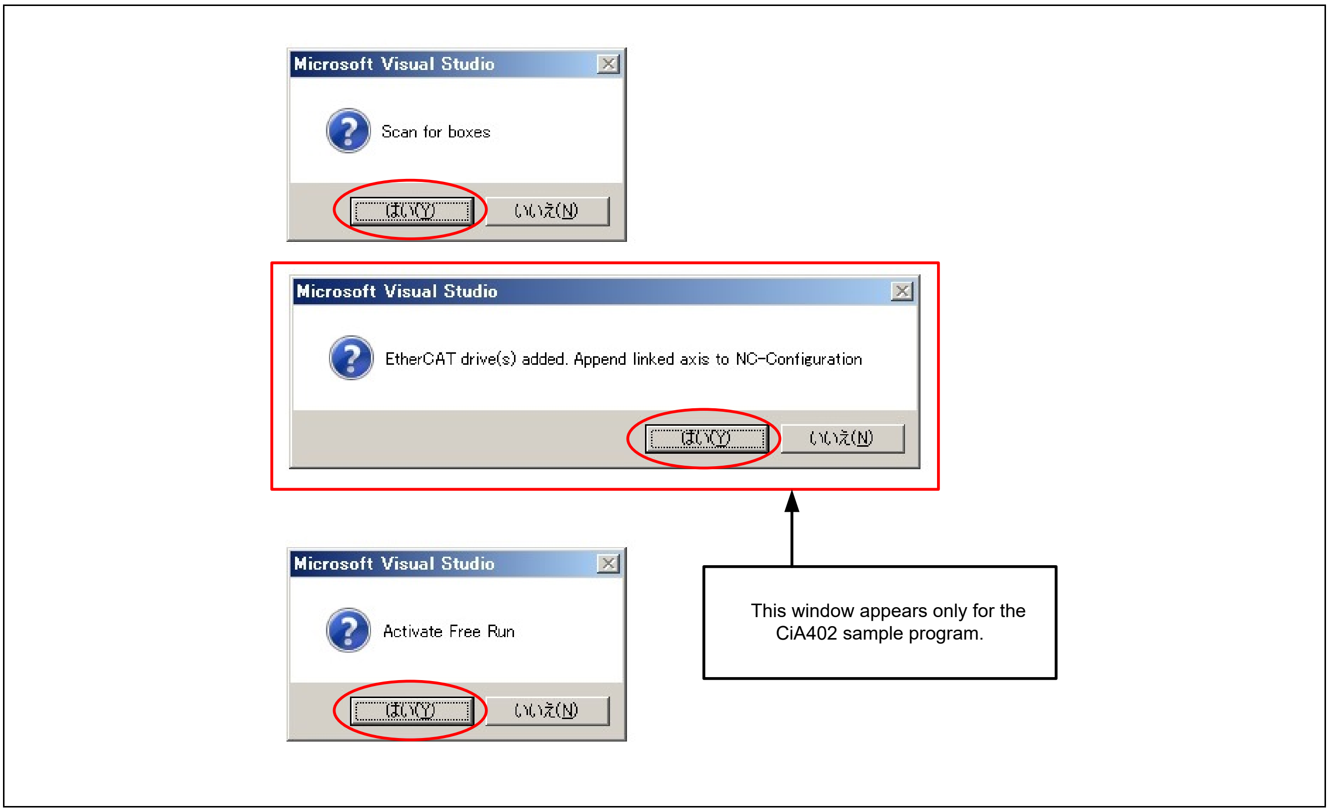


Figure 8.4 Settings for Scanning I/O Devices (2)

7.2.3 Updating EEPROM Data

If the data of another application has already been written to the EEPROM, replace the data.

The following shows the procedure for replacing the data on the EEPROM:

(1) Double-click [Box 1] to display a panel on the right side of the window as in Figure 8.5.
(2) Select the [EtherCAT] tab.
(3) Click the [Advanced Setting] button.
(4) Select [ESC Access] > [EEPROM] > [Hex Editor].
(5) Select [Download from list].
(6) Select [Available EEPROM Description].

- For the I/O controller sample program
  Select [Renesas Electronics Corp.] > [RZ/T1-R Slaves] > [RZ/T1-R EtherCAT Demo[DC]]
- For the CiA402 sample program
  Select [Renesas Electronics Corp.] > [RZ/T1-R Slaves] > [RZ/T1-R EtherCAT CiA402]

(7) Click the [OK] button.
After the data is replaced, restart RZ/T1 (by turning it off and on, or resetting it) so that the new data is applied to the microcomputer.
(8) Execute [Restart TwinCAT System].

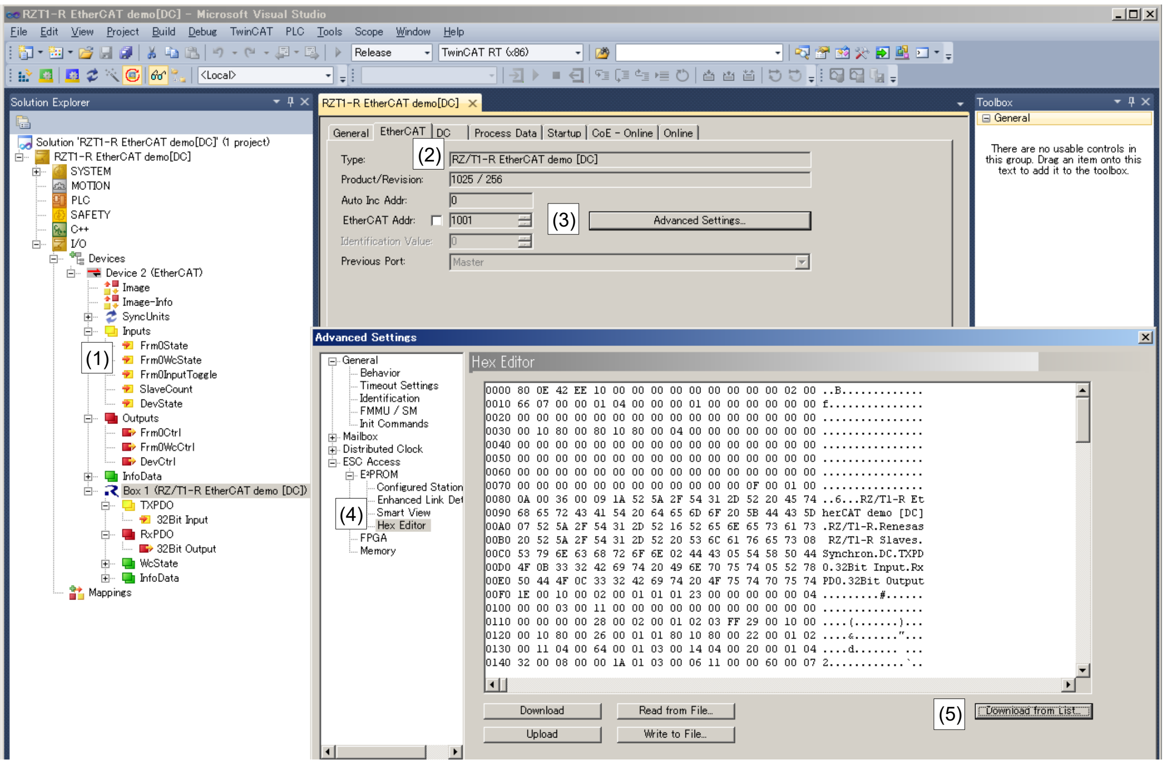


Figure 8.5 Procedure for Replacing the Data on the EEPROM (1)

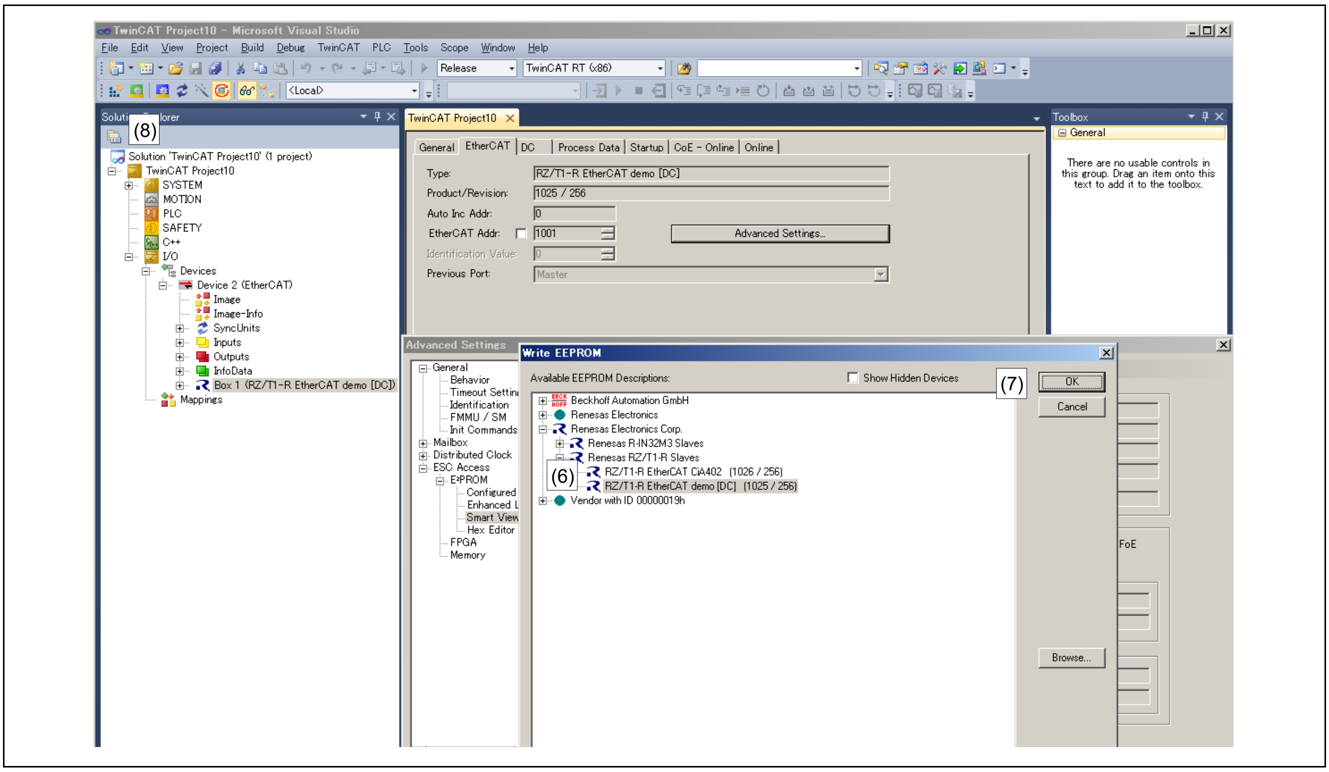


Figure 8.6 Procedure for Replacing the Data on the EEPROM (2)

7.2.4 Confirming the Communication Status

Select the [Online] tab, and then confirm that the status has been changed to OP.

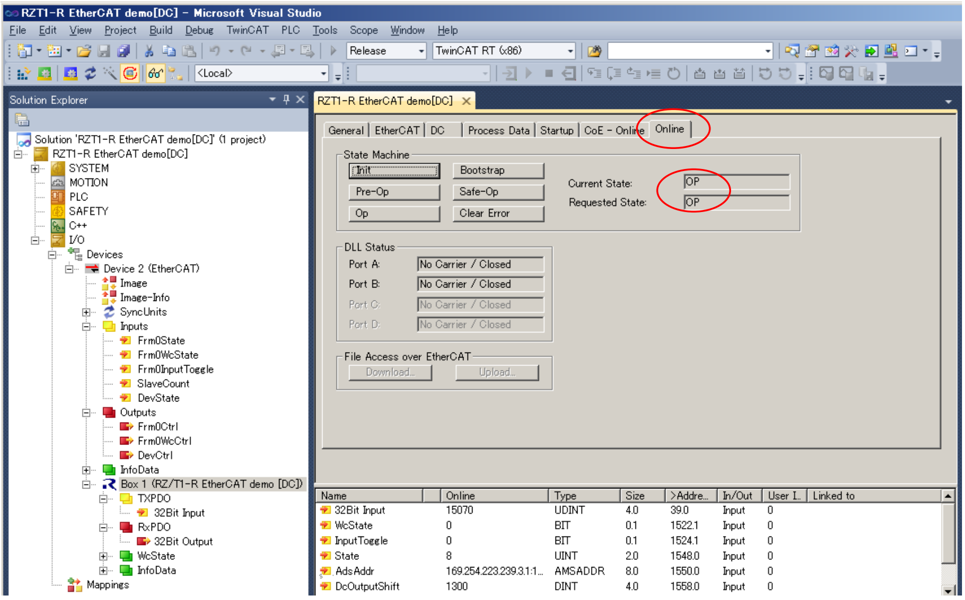


Figure 8.7 Confirming the Communication Status

Note: If the status has not been changed to OP, try [Activate Configuration], [Restart TwinCAT(Config Mode)], or another operation.

7.3 Sending/Receiving Data

7.3.1 For the I/O Controller Sample Program

(1) Checking 32-bit input

Select [32Bit Input] > [Online].
You can confirm that the value is updated (incremented).

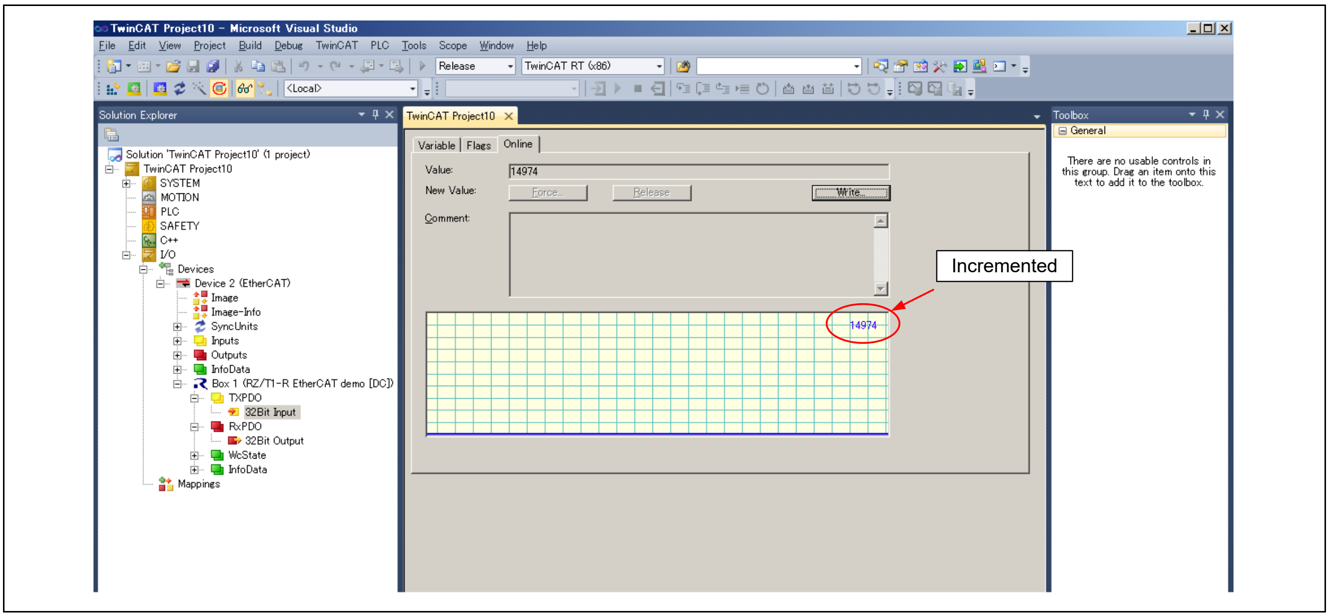


Figure 8.8 Checking 32-bit Input Values

(2) Specifying the 32-bit output settings

Select [32Bit Output] > [Online] > [Write].
Set a value for [Set Value Dialog], and then click the [OK] button.
The low-order four bits of the value are applied to LED3 to LED0. (LEDs are lit when the corresponding bits are 1.)

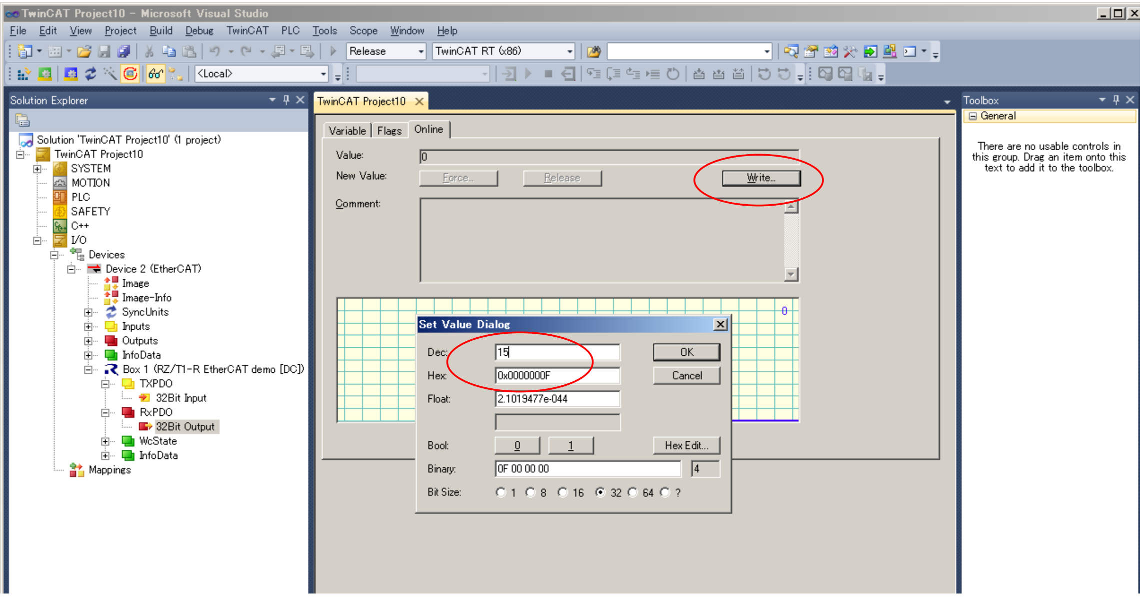


Figure 8.9 Specifying the 32-bit Output Settings

7.3.2 For the CiA402 Sample Program

(1) Checking CiA402 status transition

Select [Control Word], set the value to 7, and then change the value to 15. Then, select [Status Word], and confirm that the value is 0x1237, which means "Operation Enabled".

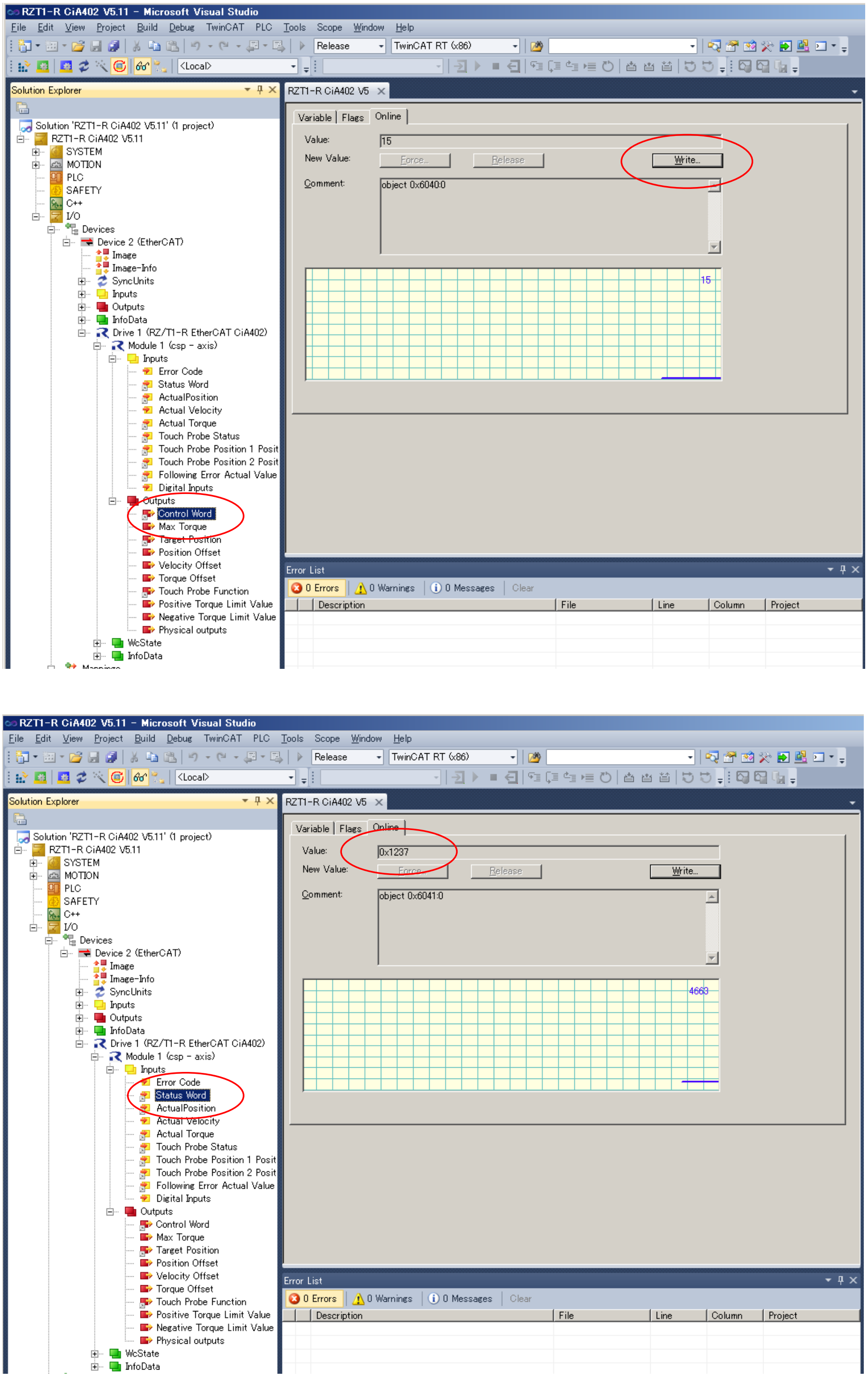


Figure 8.10 CiA402 Status Transition

Note: For details about the status transition of CiA402, refer to the "CiA402 Standards".

(2) Pseudo motor operation

For [Target Position], set any value as the target value.
Then, press SW1 to change the value of [Actual Position]. While SW1 is pressed, the value of [Actual Position] is incremented until reaching the value set for [Target Position]. When SW1 is turned off, the value of [Actual Position] is reset to 0.
Note that while SW1 is pressed, LED1 is lit.

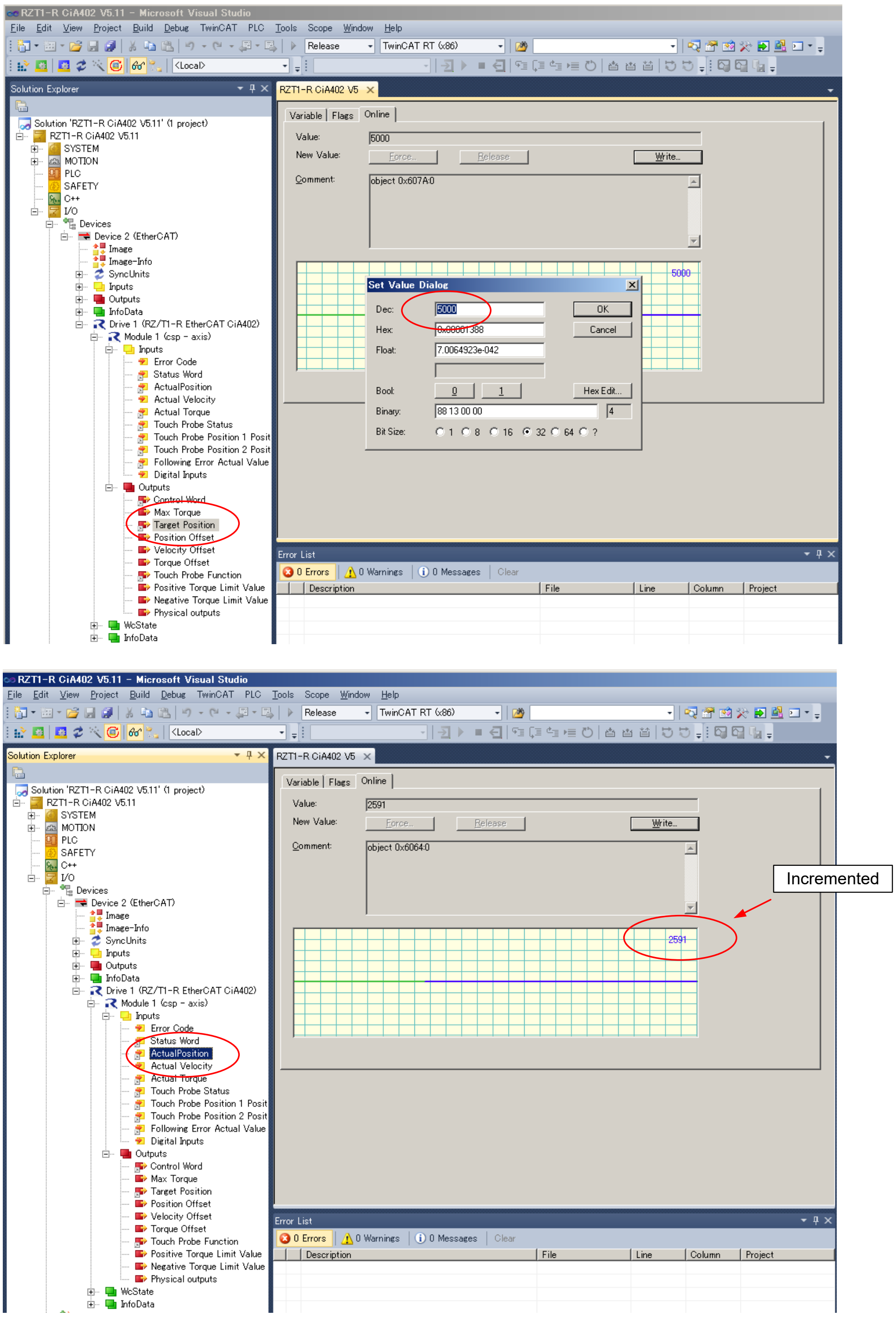


Figure 8.11 Pseudo Motor Operation

8. Sample Programs

Download the necessary sample programs from the Renesas Electronics website.

9. Reference Documents

- User's Manual: Hardware
  RZ/T1 Group User's Manual: Hardware
  (Download the latest version from the Renesas Electronics website.)

  RZ/T1 Evaluation Board RTK7910022C00000BR User's Manual
  (Download the latest version from the Renesas Electronics website.)

- Documents/Application Notes/Sample Codes
  RZ/T1 Group Application Note: Initial Settings
  (Download the latest version from the Renesas Electronics website.)

  RZ/T1 Group Application Note: Compare Match Timer (CMT)
  (Download the latest version from the Renesas Electronics website.)

  RZ/T1 Group Application Note: Procedure of EtherCAT Communication for Devices with a Built-in R-IN Engine
  (Download the latest version from the Renesas Electronics website.)

- Technical Update/Technical News
  (Download the latest version from the Renesas Electronics website.)

- User's Manual: Development Environment
  For documents of IAR Integrated Development Environment (Embedded Workbench for ARM), download the latest version from the IAR Systems website.
  (Download the latest version from the IAR Systems website.)

Website and Support

Renesas Electronics Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/contact/

Revision History	Application Note: EtherCAT Sample Program Implementation Guide for Devices with a Built-in R-IN Engine

Rev.	**Date**	**Description**	
		Page	**Summary**
1.00	Jul. 15, 2016	—	First Edition issued
1.10	Aug. 31, 2018	15	6. Procedure for Generation Sample Programs, modified.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

Colophon 7.0