RZ/V2H Group and RZ/V2N Group Power Supply Design Guide

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Summary

This document describes example configurations for the power supply of the RZ/V2H group and RZ/V2N group. The descriptions provided are examples only and do not guarantee proper operation.

Target Device

RZ/V2H Group

RZ/V2N Group

Table of Contents

1. Overview

This document presents reference circuit configurations for the following cases. For the specifications of each MPU, please refer to the documents listed in **Table 1-1**.

- RZ/V2H group power supply configuration
  - CM33 cold boot
  - CA55 cold boot
- RZ/V2N group power supply configuration
  - CM33 cold boot
  - CA55 cold boot

Table 1-1 Related files

File Name	Description
r01uh1032ejxxxx-rzv2h.pdf	RZ/V2H Group User's Manual: Hardware
r01uh1071ejxxxx-rzv2n.pdf	RZ/V2N Group User's Manual: Hardware

x: document revision

This document describes the power configuration when using the RAA215300A2GNP#HA7. The PMICs used on each Evaluation Board are as follows:

- RZ/V2H EVK (RTK0EF0168C04000BJ): RAA215300A2GNP#HA2
- RZ/V2N EVK V1.0 (RTK0EF0186C03000BJ): RAA215300A2GNP#HA2
- RZ/V2N EVK V2.0 (RTK0EF0186C03001BJ): RAA215300A2GNP#HA7

When performing a CM33 cold boot, the PMIC on each board must be controlled accordingly. For details on software control methods, refer to the RZ/V2H Group and RZ/V2N Group *Multi-OS Software Package*.

This document describes the recommended hardware control procedure (power control sequence).

2. Power Configuration for Each Boot Mode

These MPUs support both CM33 cold boot and CA55 cold boot modes. This section provides example power supply configurations for each boot mode, along with the corresponding power sequences for those configurations.

For details on boot specifications, please refer to the **1.9 Boot Operation** and **10.1.3 Power-On/Off Sequence** in the *User's Manual: Hardware*.

2.1 CM33 Cold Boot for RZ/V2H

This section describes the examples when using CM33 cold boot for RZ/V2H.

Note

When using RAA215300A2GNP#HA7, the I2C control sequence for transitioning to AWO mode provided in the Multi-OS Package cannot be used. The Multi-OS Package was developed based on the RAA215300A2GNP#HA2 chip used in the EVK. If you wish to transition to AWO mode using RAA215300A2GNP#HA7, please refer to the sequence diagram below and modify the I2C control settings accordingly.

The following describes the CM33 cold boot procedure when using the RAA215300A2GNP#HA7 with the RZ/V2H. These procedures are examples based on the power configuration described in Section **2.1.1 Block Diagram**.

Table 2-1 ALL_OFF (AWO) to ALL_ON procedure (First time booting)

Step	Software/ Hardware	Description	Register settings				Note
			Device	I2C address	Register address	Value	
1	Software	Assert the reset of units in the PD_OTHERS area / PD_CA55 area / PD_DDR area	RZ/V2H (CPG)	—	—	—	Assert the reset other than AWO
2	Software	Assert the reset of the CPG circuit in the OTHERS area CPG_OTHERS_INI.OTHERS_RST = 1b	RZ/V2H (CPG)	—	—	—	—
3	Software	Configure the polarity of PMIC_MPIO5 (BTSEL) (to low-active)	PMIC	0x12 (7-bit)	0x8F	0x02	PMIC controlled by using RIIC8
4	Hardware	3rd Grp power on, 4th Grp power on, 5th Grp power on	—	—	—	—	PMIC control
5	Software	Wait 20 ms	—	—	—	—	—
6	Software	Refer to User's Manual Table 4.5-4 Entry step 4 to step 13	RZ/V2H (CPG)	—	—	—	—
7	Software	Refer to User's Manual Table 4.5-4 Post-process step 1 to step 3	RZ/V2H (CPG)	—	—	—	—

Table 2-2 ALL_ON to AWO procedure

Step	Software/ Hardware	Description	Register settings				Note
			Device	I2C address	Register address	Value	
1	Software	Stop DMA for units	RZ/V2H (DMAC)	—	—	—	—
2	Software	Set the multiplexed pins of the PFC to port mode (PMC_mn = 0)	RZ/V2H (PFC)	—	—	—	—
3	Software	Refer to User's Manual Table 4.5-5 Entry step 1 to step 6	RZ/V2H (CPG)	—	—	—	—
4	Software	PMIC enter sleep mode	PMIC	0x12 (7-bit)	0x6C	0x80	PMIC controlled by using RIIC8
5	Software	Wait 45 ms	—	—	—	—	—
6	Software	PMIC_MPIO2 High to Low (VDD3G1G06_DDR: OFF)	PMIC	0x12 (7-bit)	0x8C	0x1E	PMIC controlled by using RIIC8
7	Software	Wait 10 ms	—	—	—	—	—
8	Software	PMIC_Buck1 OFF (VDD3G1G11_DDR: OFF)	PMIC	0x12 (7-bit)	0x20	0x04	PMIC controlled by using RIIC8
9	Software	Wait 10 ms	—	—	—	—	—
10	Software	PMIC_Buck5 OFF (VDD3G1G18_DDR OFF)	PMIC	0x12 (7-bit)	0x3C	0x04	PMIC controlled by using RIIC8

Table 2-3 AWO to ALL_ON procedure

Step	Software/ Hardware	Description	Register settings				Note
			Device	I2C address	Register address	Value	
1	Software	Assert the reset of units in the PD_OTHERS area / PD_CA55 area / PD_DDR area	RZ/V2H (CPG)	—	—	—	Assert the reset other than AWO
2	Software	Assert the reset of the CPG circuit in the OTHERS area CPG_OTHERS_INI.OTHERS_RST = 1b	RZ/V2H (CPG)	—	—	—	—
3	Software	PMIC_Buck5 ON (VDD3G1G18_DDR: ON)	PMIC	0x12 (7-bit)	0x3C	0x07	PMIC controlled by using RIIC8
4	Software	Wait 3 ms	—	—	—	—	—
7	Software	PMIC_Buck1 ON (VDD3G1G11_DDR: ON)	PMIC	0x12 (7-bit)	0x20	0x07	PMIC controlled by using RIIC8
8	Software	Wait 2 ms	—	—	—	—	—
9	Software	PMIC_MPIO2 Low to High (VDD3G1G06_DDR: ON)	PMIC	0x12 (7-bit)	0x8C	0x3E	PMIC controlled by using RIIC8
10	Software	PMIC exit sleep mode	PMIC	0x12 (7-bit)	0x6C	0x00	PMIC controlled by using RIIC8
11	Software	Wait 35 ms	—	—	—	—	—
12	Software	Refer to User's Manual Table 4.5-4 Entry step 4 to step 13	RZ/V2H (CPG)	—	—	—	—
13	Software	Refer to User's Manual Table 4.5-4 Post-process step 1 to step 3	RZ/V2H (CPG)	—	—	—	—

Table 2-4 ALL_ON to ALL_OFF (AWO to ALL_OFF) procedure

Step	Software/ Hardware	Description	Register settings				Note
			Device	I2C address	Register address	Value	
1	Software	Stop DMA for units	RZ/V2H (DMAC)	—	—	—	(ALL_ON to ALL_OFF only)
2	Software	Set the multiplexed pins of the PFC to port mode (PMC_mn = 0)	RZ/V2H (PFC)	—	—	—	(ALL_ON to ALL_OFF only)
3	Software	Refer to User's Manual Table 4.5-5 Entry step 1 to step 6	RZ/V2H (CPG)	—	—	—	(ALL_ON to ALL_OFF only)
4	Software	Configure the polarity of PMIC_MPIO5 (BTSEL) (To active-high)	PMIC	0x12 (7-bit)	0x8F	0x22	PMIC controlled by using RIIC8

2.1.1 Block Diagram

The following diagram shows an example of the power supply configuration when using CM33 cold boot mode.

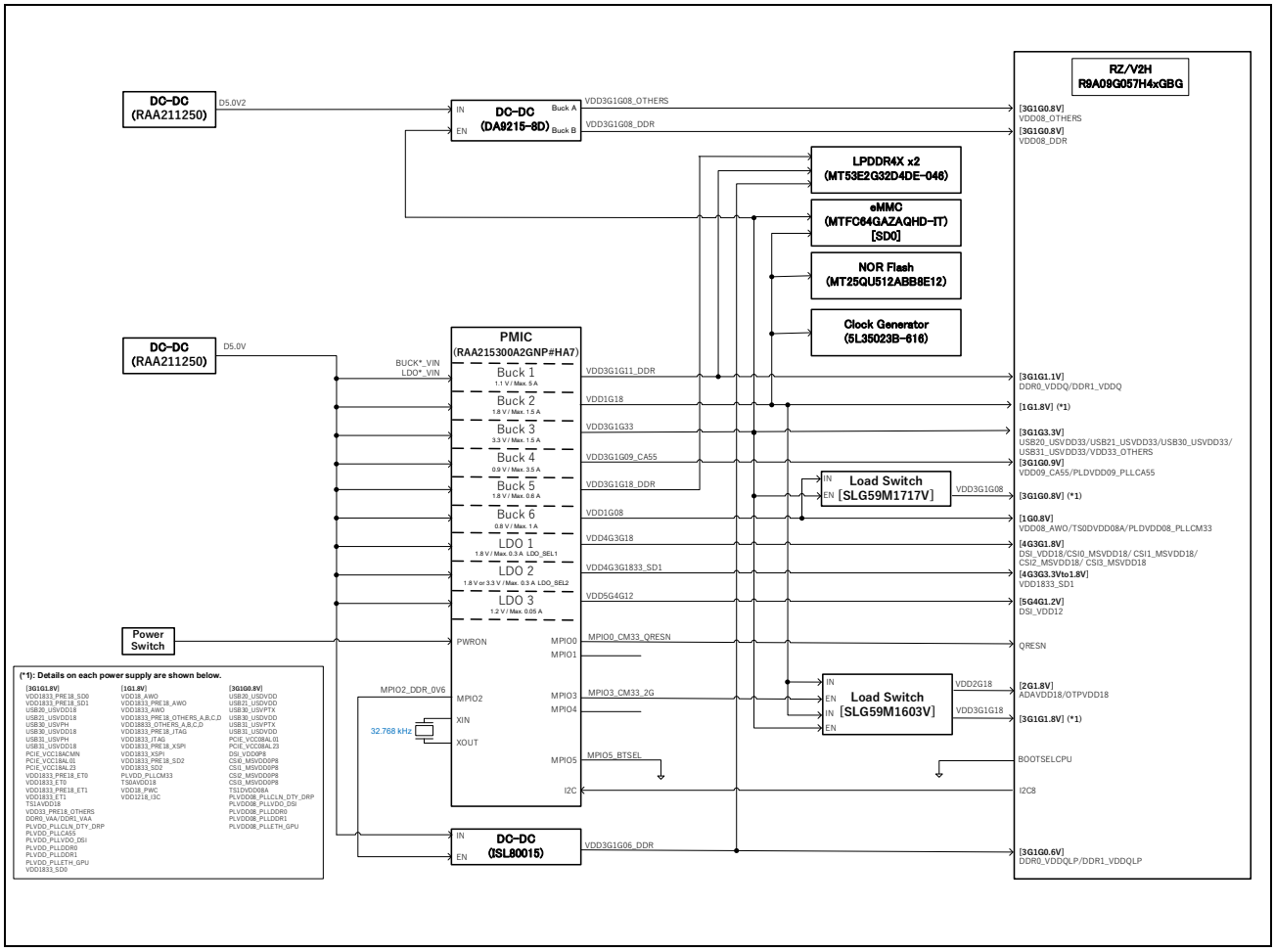

Figure 2-1 CM33 Cold Boot Block Diagram for RZ/V2H

Table 2-5 List of Main Components when Using CM33 Cold Boot for RZ/V2H

Product name	Quantity	Description
RAA215300A2GNP#HA7	1	Power management integrated circuit for RZ/V2H and RZ/V2N
RAA211250GSP#HA0	2	DC-DC converter
DA9215-8D	1	DC-DC converter
ISL80015	1	DC-DC converter
SLG59M1717V	1	Load Switch
SLG59M1603V	1	Load Switch
MT53E2G32D4DE-046	2	LPDDR4X
MTFC64GAZAQHD-IT	1	eMMC
MT25QU512ABB8E12	1	NOR Flash
5L35023B-616	1	Clock Generator

2.1.2 Sequence Diagram

The following shows the power sequence when using the configuration described in **2.1.1 Block Diagram**.

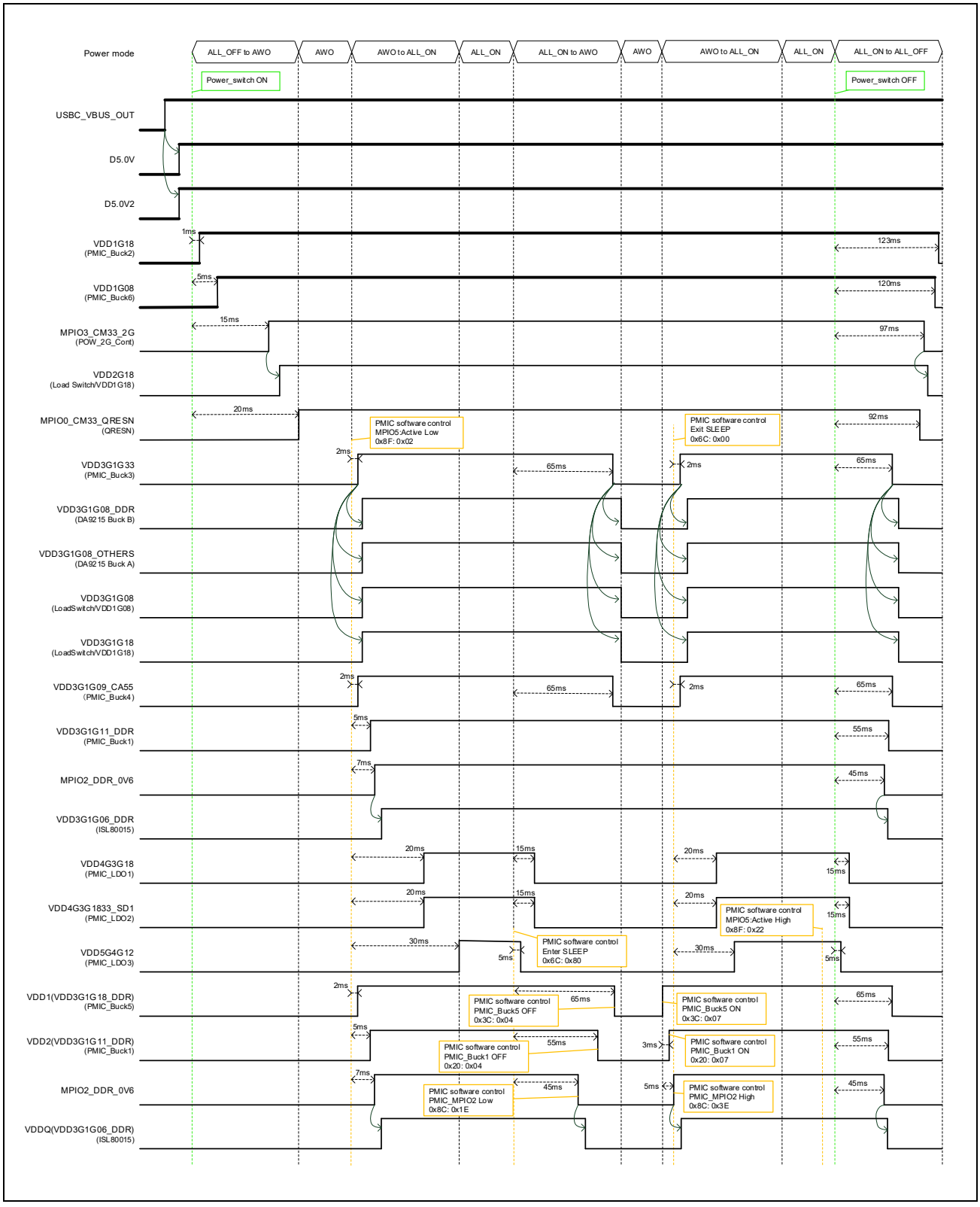

Figure 2-2 CM33 Cold Boot Sequence for RZ/V2H

2.2 CM33 Cold Boot for RZ/V2N

This section describes the examples when using CM33 cold boot for RZ/V2N.

2.2.1 Block Diagram

The following diagram shows an example of the power supply configuration when using CM33 cold boot mode.

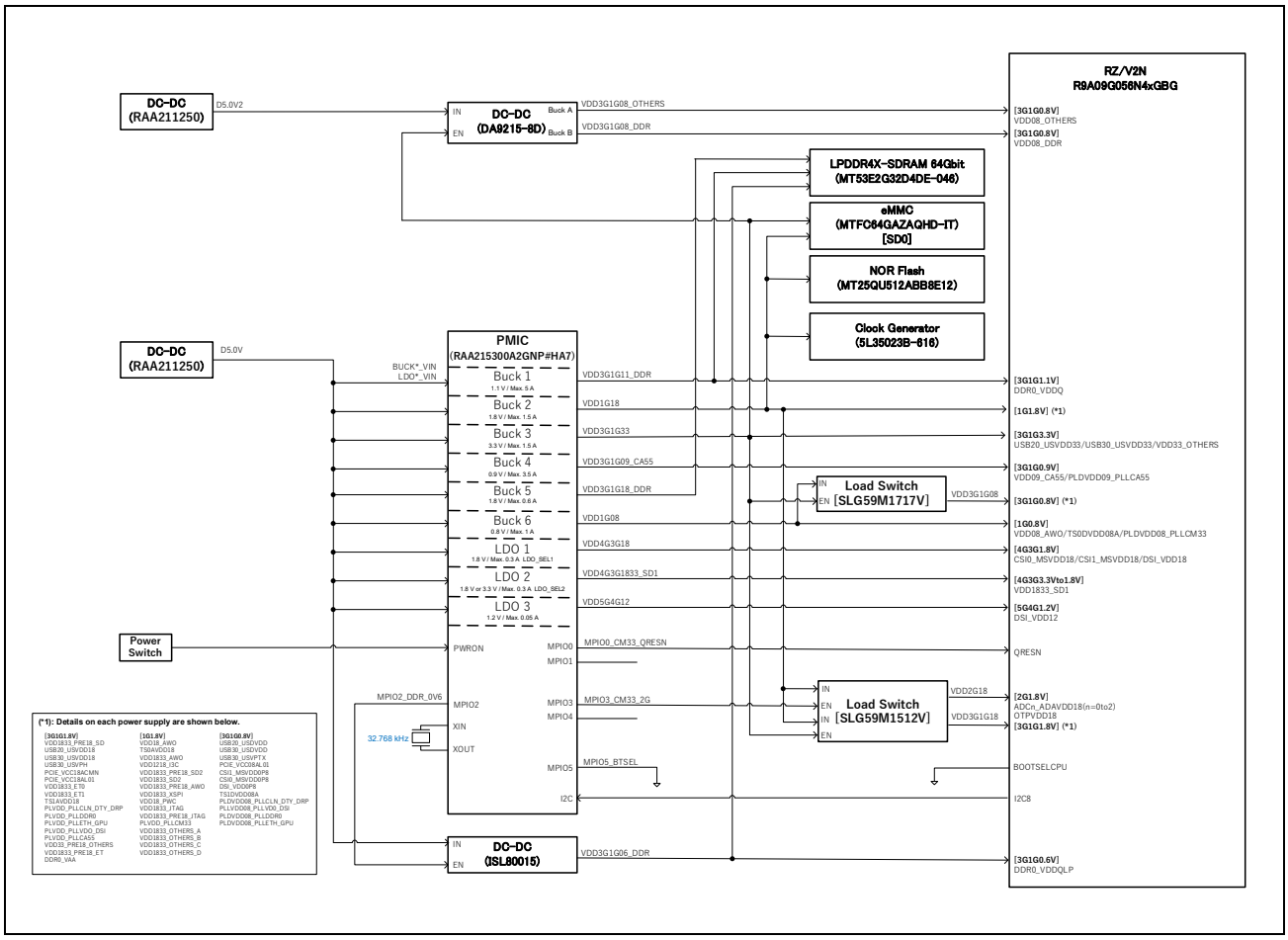

Figure 2-3 CM33 Cold Boot Block Diagram for RZ/V2N

Table 2-6 List of Main Components when Using CM33 Cold Boot for RZ/V2N

Product name	Quantity	Description
RAA215300A2GNP#HA7	1	Power management integrated circuit for RZ/V2H and RZ/V2N
RAA211250GSP#HA0	2	DC-DC converter
DA9215-8D	1	DC-DC converter
ISL80015	1	DC-DC converter
SLG59M1717V	1	Load Switch
SLG59M1512V	1	Load Switch
MT53E2G32D4DE-046	1	LPDDR4X
MTFC64GAZAQHD-IT	1	eMMC
MT25QU512ABB8E12	1	NOR Flash
5L35023B-616	1	Clock Generator

2.2.2 Sequence Diagram

The following shows the power sequence when using the configuration described in **2.1.1 Block Diagram**.

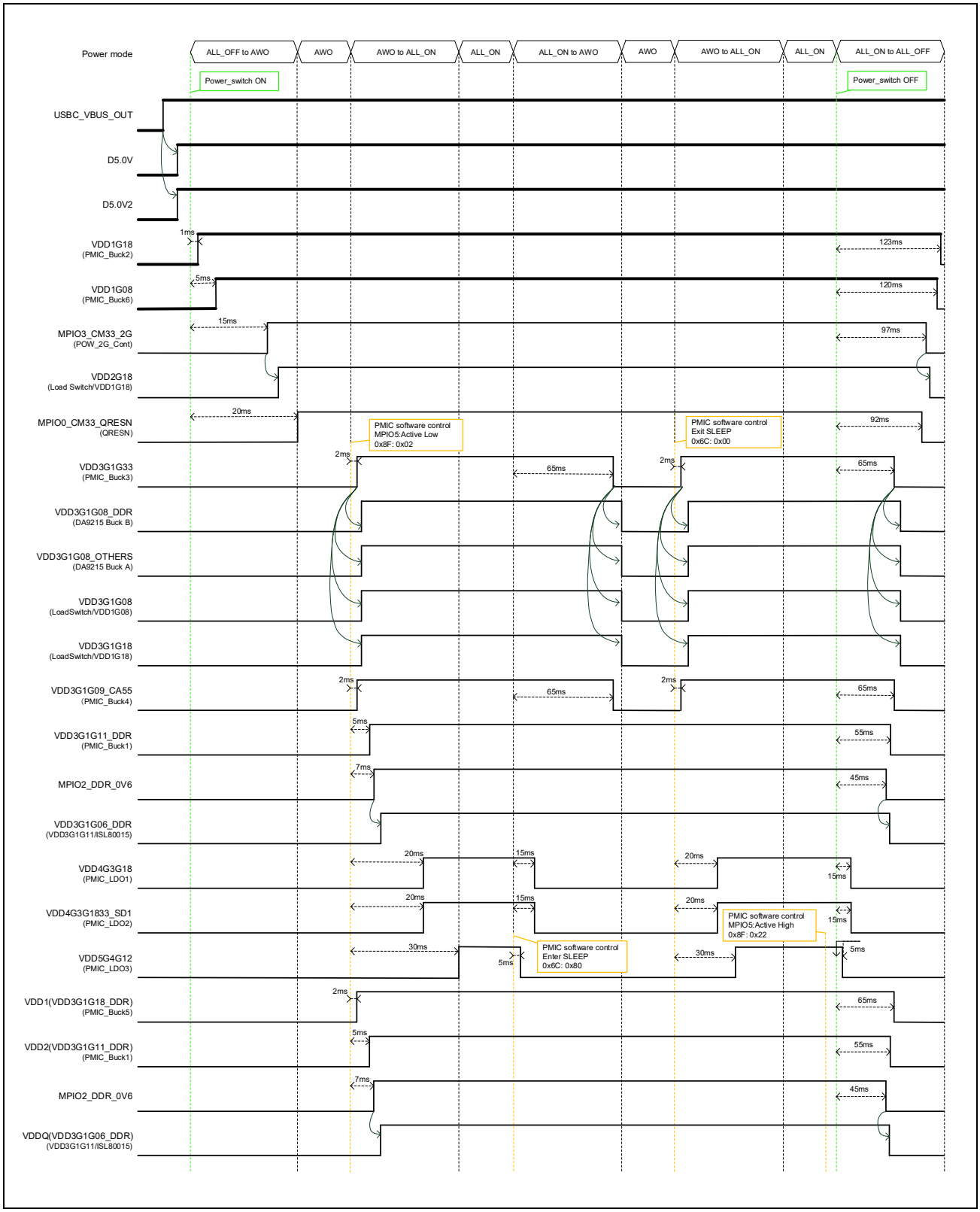

Figure 2-4 CM33 Cold Boot Sequence for RZ/V2N

2.3 CA55 cold boot for RZ/V2H

This section describes the examples when using CA55 cold boot for RZ/V2H.

2.3.1 Block diagram

The following diagram shows an example of the power supply configuration when using CA55 cold boot mode.

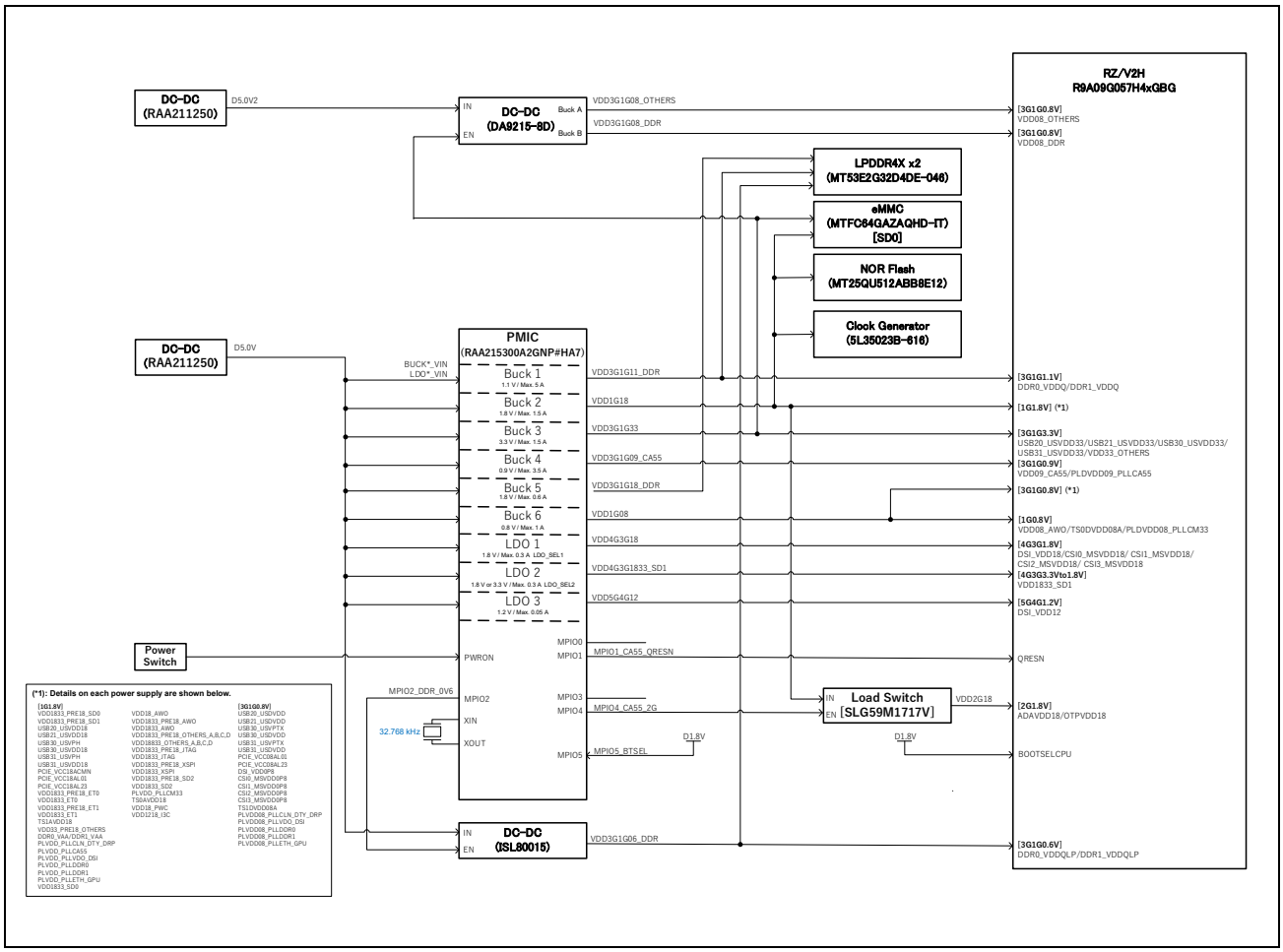

Figure 2-5 CA55 Cold Boot Block Diagram for RZ/V2H

Table 2-7 List of Main Components when Using CA55 Cold Boot for RZ/V2H

Product name	Quantity	Description
RAA215300A2GNP#HA7	1	Power Management Integrated Circuit
RAA211250GSP#HA0	2	DC-DC converter
DA9215-8D	1	DC-DC converter
ISL80015	1	DC-DC converter
SLG59M1717V	1	Load Switch
MT53E2G32D4DE-046	2	LPDDR4X
MTFC64GAZAQHD-IT	1	eMMC
MT25QU512ABB8E12	1	NOR Flash
5L35023B-616	1	Clock Generator

2.3.2 Sequence diagram

The following shows the power sequence when using the configuration described in **2.3.1 Block diagram**.

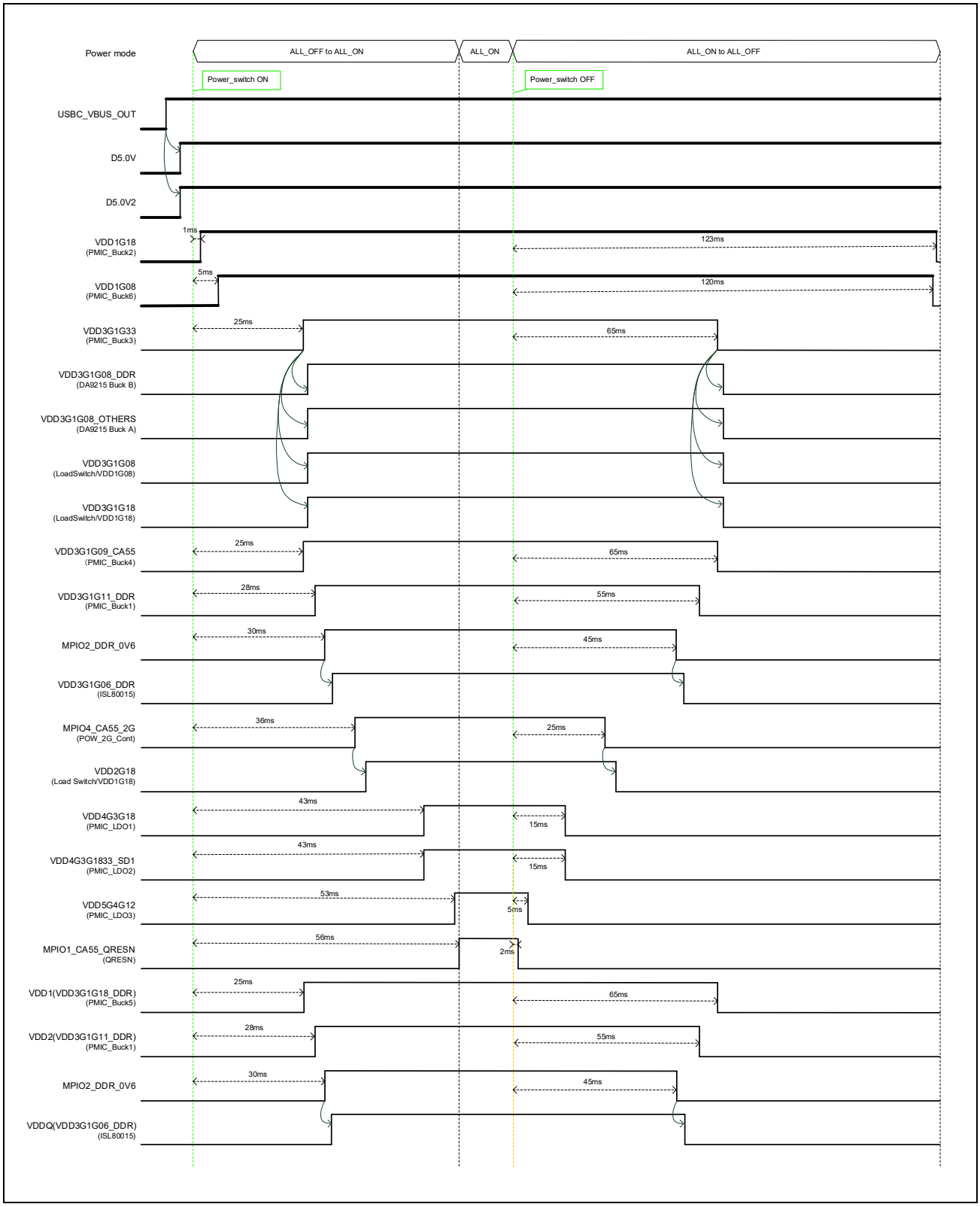

Figure 2-6 CA55 Cold Boot Sequence for RZ/V2H

2.4 CA55 cold boot for RZ/V2N

This section describes the examples when using CA55 cold boot for RZ/V2N.

2.4.1 Block diagram

The following diagram shows an example of the power supply configuration when using CA55 cold boot mode.

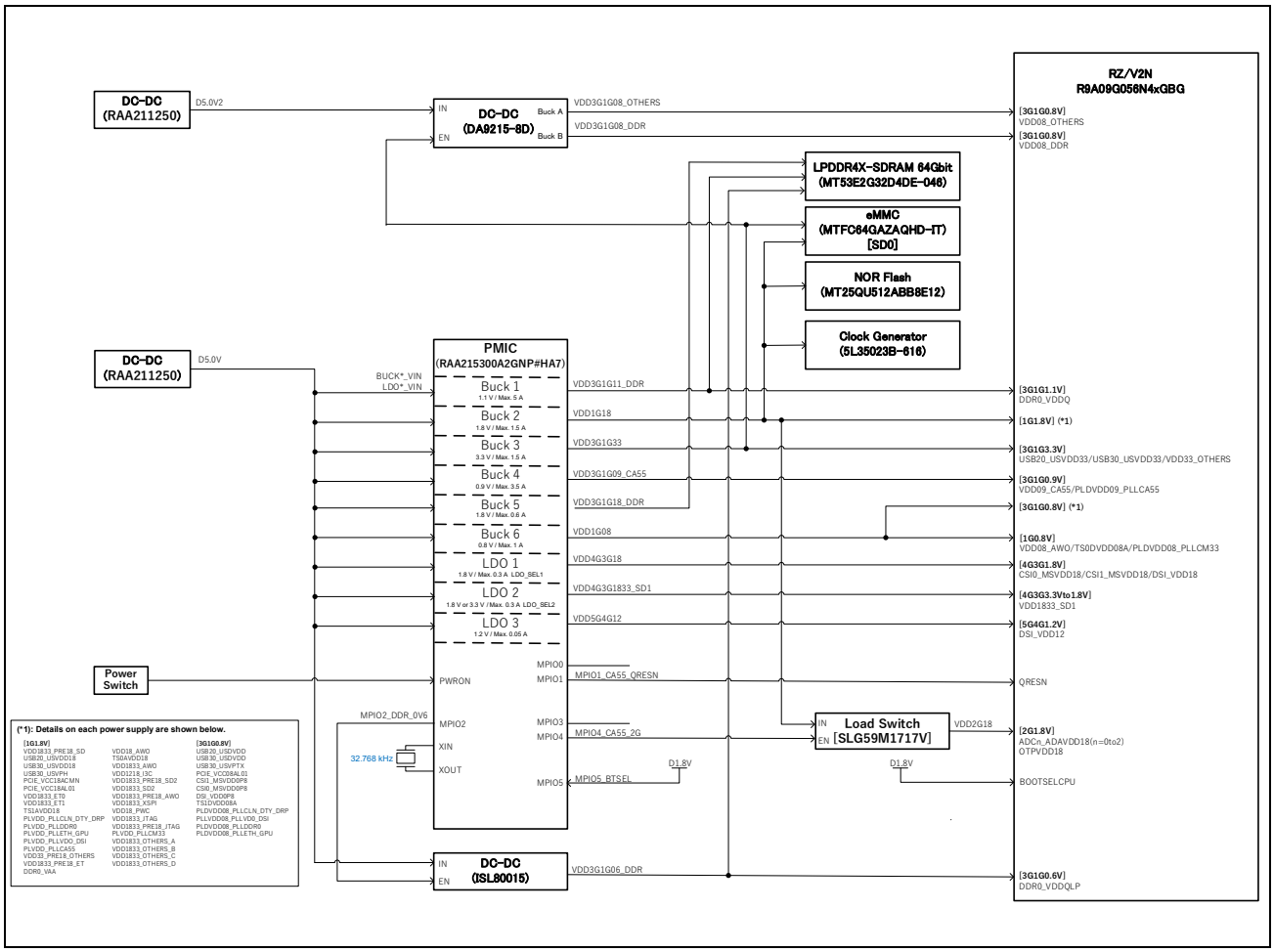

Figure 2-7 CA55 Cold Boot Block Diagram for RZ/V2N

Table 2-8 List of Main Components when Using CA55 Cold Boot for RZ/V2N

Product name	Quantity	Description
RAA215300A2GNP#HA7	1	Power Management Integrated Circuit
RAA211250GSP#HA0	2	DC-DC converter
DA9215-8D	1	DC-DC converter
ISL80015	1	DC-DC converter
SLG59M1717V	1	Load Switch
MT53E2G32D4DE-046	1	LPDDR4X
MTFC64GAZAQHD-IT	1	eMMC
MT25QU512ABB8E12	1	NOR Flash
5L35023B-616	1	Clock Generator

2.4.2 Sequence diagram

The following shows the power sequence when using the configuration described in **2.3.1 Block diagram**.

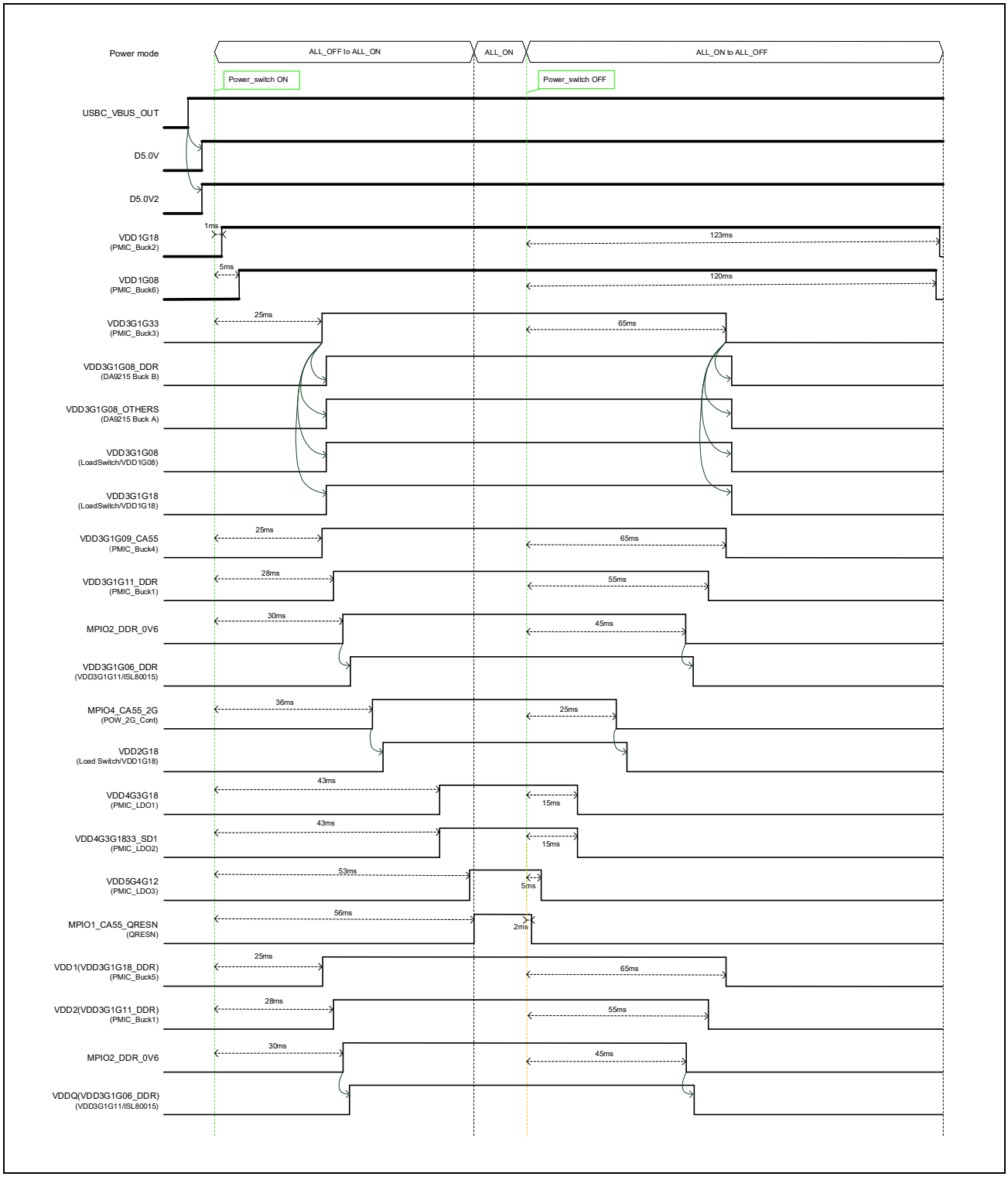

Figure 2-8 CA55 Cold Boot Sequence for RZ/V2N

REVISION HISTORY	RZ/V2H Group and RZ/V2N Group Power Supply Design Guide

Rev.	Date	Description	
		Page	Summary
1.00	Mar 13, 2026	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

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1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide, and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
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   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
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   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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