RZ/V2H Group CRU Application Note

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Summary

This document describes setting examples for the CRU function of RZ/V2H Group.

These setting examples are for reference only, so please modify the setting values to suit your application system.

Target Device

RZ/V2H Group

Table of Contents

1. CRU Setting Examples

This section provides a configuration example for inputting data from an external sensor using the Camera Data Receive Unit (CRU). Settings for modules other than CRU and CPG are not included. The requirements for each setting example are as follows.

Table 1-1 Requirements for each setting example

Category	Description
Clock and reset setting examples	CRU clock and reset setting
4K RAW12 30fps input setting (Full bypass) examples	RAW12 Full Bypass: 4K (3840 × 2160): outputs RAW12
4K RAW10 60fps input setting (Full bypass) examples	RAW10 Full Bypass: 4K (3840 × 2160): outputs RAW10
IMX415 DOL2 frame input examples	Full bypass SVC0 = VC0 (inputs RAW10, outputs RAW10) SVC1 = VC1 (inputs RAW10, outputs RAW10)
Dual YUV camera module connection examples	In this case, two e-CAM22_CURZH*1 camera modules are used. Dual channel (CRU0 and CRU1), FHD (1920 × 1080): inputs: YUV422, outputs: YUV422
Virtual channel camera input examples	Virtual channels input such as GMSL cameras. CRU0: SVC0=VC0 CRU1: SVC0=VC1 (Input from the MIPI-CSI block in CRU0)

Note: For details on the settings, refer to each setting example.

Note 1. This module includes ISP functions. For details, please refer to *e-con Systems* website.

Note

- The configurations described in this document are examples. Please modify them according to your system requirements.
- This document uses Sony's IMX415 as an example of a sensor.

1.1 Clock and Reset Setting

Table 1-2 and **Table 1-3** indicate examples of clock and reset settings (register settings). For the setting procedure, follow the instructions in CRU in the *RZ/V2H Group User's Manual: Hardware*.

Table 1-2 Clock Setting Examples (Register settings)

Register Name	Address	Setting Value	Read Check	CRU CH	Comments
CPG_CDDIV3	0x1042_040c	bit12=0x0 (default)	–	Common	VCLK frequency = 630MHz
CPG_CDDIV4	0x1042_0410	bit0=0x0 (default) bit4=0x0 (default) bit8=0x0 (default)	–	Common	
CPG_CLKON_13	0x1042_0634	bit2=0x1	–	CRU0	aclk locks supply
		bit3=0x1	–	CRU0	vclk clocks supply
		bit4=0x1	–	CRU0	pclk clocks supply
		bit5=0x1	–	CRU1	aclk locks supply
		bit6=0x1	–	CRU1	vclk clocks supply
		bit7=0x1	–	CRU1	pclk clocks supply
		bit8=0x1	–	CRU2	aclk locks supply
		bit9=0x1	–	CRU2	vclk clocks supply
		bit10=0x1	–	CRU2	pclk clocks supply
		bit11=0x1	–	CRU3	aclk locks supply
		bit12=0x1	–	CRU3	vclk clocks supply
		bit13=0x1	–	CRU3	pclk clocks supply
CPG_CLKMON_6	0x1042_0818	–	bit18=0x1	CRU0	Clock supply start confirmation Check aclk clocks started
		–	bit19=0x1	CRU0	Clock supply start confirmation Check vclk clocks started
		–	bit20=0x1	CRU0	Clock supply start confirmation Check pclk clocks started
		–	bit21=0x1	CRU1	Clock supply start confirmation Check aclk clocks started
		–	bit22=0x1	CRU1	Clock supply start confirmation Check vclk clocks started
		–	bit23=0x1	CRU1	Clock supply start confirmation Check pclk clocks started
		–	bit24=0x1	CRU2	Clock supply start confirmation Check aclk clocks started
		–	bit25=0x1	CRU2	Clock supply start confirmation Check vclk clocks started
		–	bit26=0x1	CRU2	Clock supply start confirmation Check pclk clocks started
		–	bit27=0x1	CRU3	Clock supply start confirmation Check aclk clocks started
		–	bit28=0x1	CRU3	Clock supply start confirmation Check vclk clocks started
		–	bit29=0x1	CRU3	Clock supply start confirmation Check pclk clocks started

Table 1-3 Reset Setting Examples (Register settings)

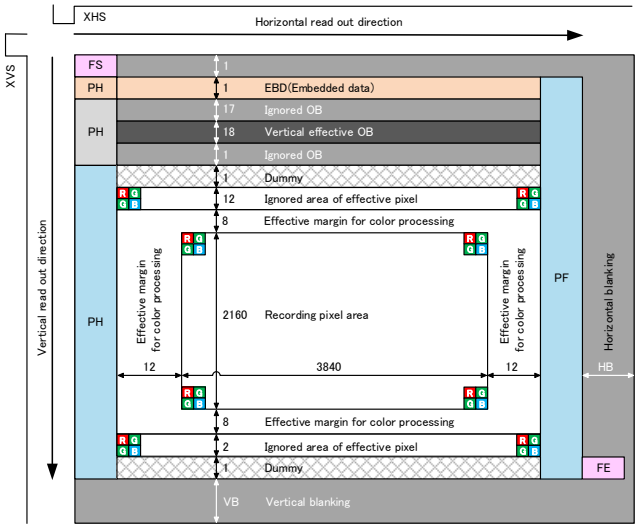
Register Name	Address	Setting Value	Read Check	CRU CH	Comments
CPG_RST_12	0x1042_0930	bit5=0x1	–	CRU0	CRU Reset Release 1 (entire CRU) (PRESETN Release)
		bit6=0x1	–	CRU0	CRU Reset Release 1 (entire CRU) (ARESETN Release)
		bit7=0x1	–	CRU0	CRU Reset Release 2 (D-PHY) (S_RESETN Release)
		bit8=0x1	–	CRU1	CRU Reset Release 1 (entire CRU) (PRESETN Release)
		bit9=0x1	–	CRU1	CRU Reset Release 1 (entire CRU) (ARESETN Release)
		bit10=0x1	–	CRU1	CRU Reset Release 2 (D-PHY) (S_RESETN Release)
		bit11=0x1	–	CRU2	CRU Reset Release 1 (entire CRU) (PRESETN Release)
		bit12=0x1	–	CRU2	CRU Reset Release 1 (entire CRU) (ARESETN Release)
		bit13=0x1	–	CRU2	CRU Reset Release 2 (D-PHY) (S_RESETN Release)
		bit14=0x1	–	CRU3	CRU Reset Release 1 (entire CRU) (PRESETN Release)
		bit15=0x1	–	CRU3	CRU Reset Release 1 (entire CRU) (ARESETN Release)
CPG_RST_13	0x1042_0934	bit0=0x1	–	CRU3	CRU Reset Release 2 (D-PHY) (S_RESETN Release)
CPG_RSTMON_5	0x1042_0A14	–	bit22=0x0	CRU0	CRU Reset Release confirmation 1 (entire CRU) (PRESETN Release confirmation) Check PRESETN Release
		–	bit23=0x0	CRU0	CRU Reset Release confirmation 1 (entire CRU) (ARESETN Release confirmation) Check ARESETN Release
		–	bit24=0x0	CRU0	CRU Reset Release confirmation 2 (D-PHY) (S_RESETN Release confirmation) Check S_RESETN Release
		–	bit25=0x0	CRU1	CRU Reset Release confirmation 1 (entire CRU) (PRESETN Release confirmation) Check PRESETN Release
		–	bit26=0x0	CRU1	CRU Reset Release confirmation 1 (entire CRU) (ARESETN Release confirmation) Check ARESETN Release
		–	bit27=0x0	CRU1	CRU Reset Release confirmation 2 (D-PHY) (S_RESETN Release confirmation) Check S_RESETN Release
		–	bit28=0x0	CRU2	CRU Reset Release confirmation 1 (entire CRU) (PRESETN Release confirmation) Check PRESETN Release
		–	bit29=0x0	CRU2	CRU Reset Release confirmation 1 (entire CRU) (ARESETN Release confirmation) Check ARESETN Release
		–	bit30=0x0	CRU2	CRU Reset Release confirmation 2 (D-PHY) (S_RESETN Release confirmation) Check S_RESETN Release
		–	bit31=0x0	CRU3	CRU Reset Release confirmation 1 (entire CRU) (PRESETN Release confirmation) Check PRESETN Release
CPG_RSTMON_6	0x1042_0A18	–	bit0=0x0	CRU3	CRU Reset Release confirmation 1 (entire CRU) (ARESETN Release confirmation) Check ARESETN Release
		–	bit1=0x0	CRU3	CRU Reset Release confirmation 2 (D-PHY) (S_RESETN Release confirmation) Check S_RESETN Release

1.2 4K RAW12 32.4fps Input Setting (Full Bypass)

The requirements for 4K RAW12 32.4fps Input Setting (Full bypass) examples are indicated in **Table 1-4**. The register settings are indicated in **Table 1-5**. For the setting procedure, follow the instructions in the *RZ/V2H Group User's Manual: Hardware* for starting MIPI® CSI-2® input reception.

Table 1-4 4K RAW12 32.4fps Input Setting (Full Bypass) Examples

Category	Description
Input format, size	IMX415 full screen mode assumed(Recording Pixel area：3840 × 2160, 32.4fps) Pixel area: ● RAW12: (3840 + 12 + 12) × (2160 + 21 + 11), 32.4fps Other than images: ● EBD (Embedded Data): 1 line ● Optical Black (User Defined 8-bit Data Type 8): 17 + 18 + 1 line (Ignored included)



Transfer rate	891Mbps/lane × 4 lanes
Virtual channel	SVC0=VC0 (SVC1 to 3 is unused)
Input format	MIPI CSI-2 Input: RAW12, User Defined 8-bit Data Type 8
Interrupt settings	MIPI CSI-2: Enable only error related interrupts, disable interrupts for normal operation. Image Converter: Error and Designated address forwarding completion interrupt settings
Header, Footer	Header (for each line): Yes Footer (for each line): Yes
Image stride	0x0_0000_1780 (6016byte)
Output start address	Uses 2 memory banks (MB1,2) Output in MIPI recommended memory storage format. MB1: 0x0_4000_0000 (Start address of Recording Pixel area: 0x0_4005_3BB2) MB2: 0x0_4100_0000 (Start address of Recording Pixel area: 0x0_4105_3BB2)
Memory image	See **Figure 1.2-1** for details.
Output format	RAW12, Optical Black (User Defined 8-bit Data Type 8) Does not output EBD (Embedded Data). *1

Note 2. Please make additional settings if necessary.

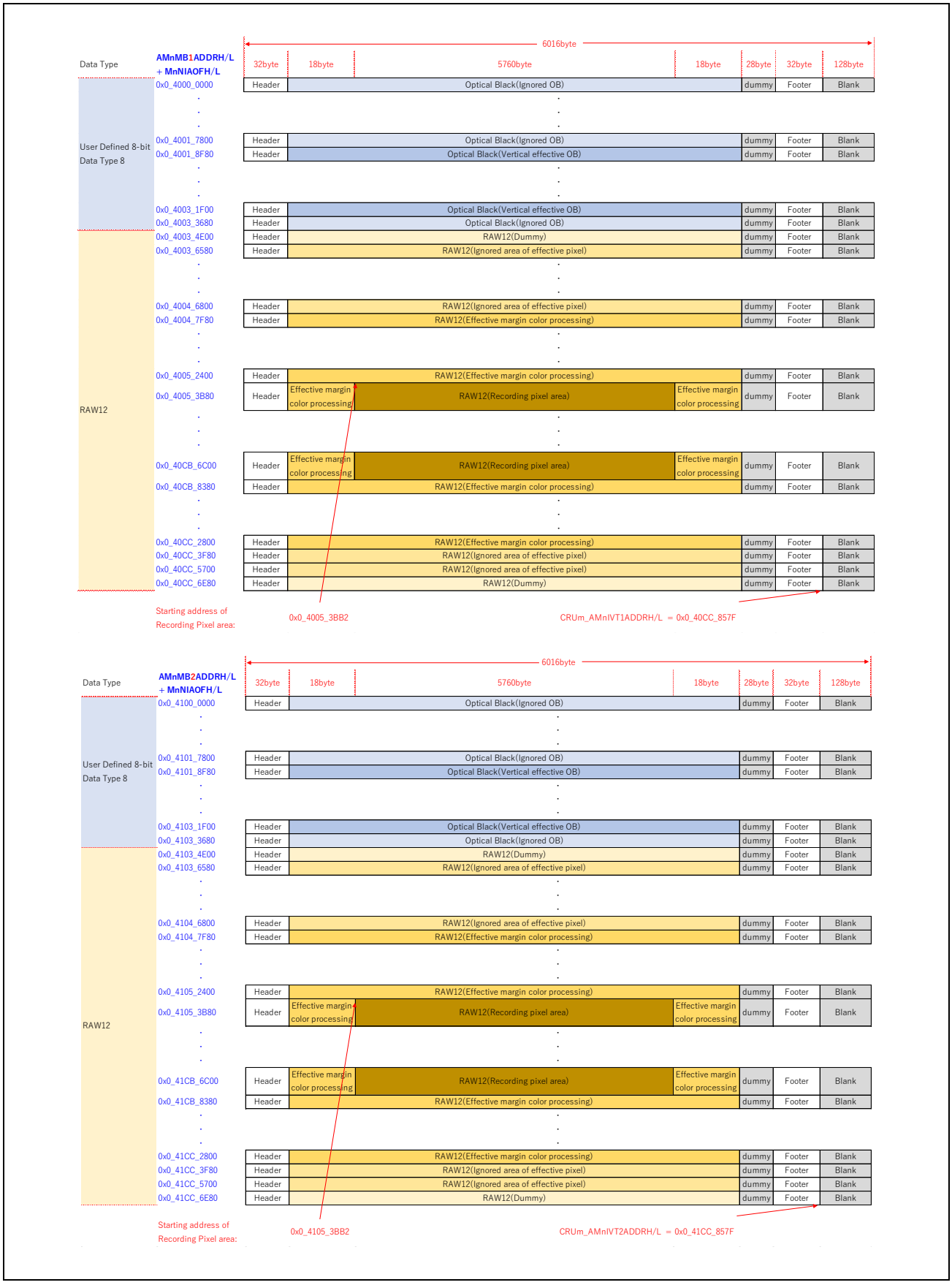


Figure 1.2-1 Memory Image Table 1

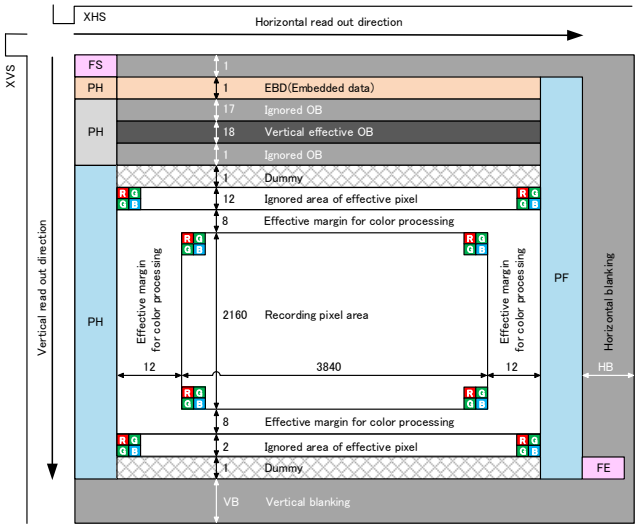
Table 1-5 4K RAW12 32.4fps Input Setting (Full Bypass) Examples

Block	Register Name	Address				Initial Value	Setting Value	comments
		CRU0	CRU1	CRU2	CRU3			
D-PHY	SWAPCTL	0x1600_0838	0x1601_0838	0x1602_0838	0x1603_0838	0x00000000	0x00000000	DP/DN Swap Control Register Does not swap.
	S_DPHYCTL_MSB	0x1600_0834	0x1601_0834	0x1602_0834	0x1603_0834	0x00000090	0x00000090	bit1: DeSkew Calibration Function Enable/Disable Control 0b: DeSkew Calibration Disable
	S_TIMCTL	0x1600_081C	0x1601_081C	0x1602_081C	0x1603_081C	0x00000000	0x00001300	Slave Data Lane Control Register for THS-SETTLE. 891Mbps/lane: S_HSSETTLECTL[7:0]=13h
LINK	CSI2nMCT0	0x1600_0410	0x1601_0410	0x1602_0410	0x1603_0410	0x02000004	0x00000004	[25]: 0b: Disables de-scrambling. [3:0]: 4h: Operates on 4 lanes
	CSI2nMCT2	0x1600_0418	0x1601_0418	0x1602_0418	0x1603_0418	0x00000000	0x00110009	[24:16]: When the vclk frequency is 630MHz and the transfer rate is 891Mbps, set to "11h": ROUNDDOWN((3*630/(891/8)), 0) + 1 = 17 [8:0] : When the vclk frequency is 630MHz and the transfer rate is 891Mbps, set to "9h": ROUNDDOWN((1.5*630/(891/8)), 0) + 1 = 9
	CSI2nDTEL	0x1600_0460	0x1601_0460	0x1602_0460	0x1603_0460	0x0000000f	0xF77CFF0F	Select all Data Types supported by image_converter.
	CSI2nDTEH	0x1600_0464	0x1601_0464	0x1602_0464	0x1603_0464	0x00000000	0x00FFFF1F	
	CSI2nDLIE0	0x1600_0488	0x1601_0488	0x1602_0488	0x1603_0488	0x00000000	0x0000000D	Data Lane 0 Interrupt Enable Register bit3=1: When a escape mode entry error (ErrESC) occurs in lane 0 bit2=1: When a control error (ErrControl) occurs in lane 0 bit0=1: When a SoT error (ErrSotHS) occurs in lane 0
	CSI2nDLIE1	0x1600_0498	0x1601_0498	0x1602_0498	0x1603_0498	0x00000000	0x0000000D	Data Lane 1 Interrupt Enable Register bit3=1: When a escape mode entry error (ErrESC) occurs in lane 1 bit2=1: When a control error (ErrControl) occurs in lane 1 bit0=1: When a SoT error (ErrSotHS) occurs in lane 1
	CSI2nDLIE2	0x1600_04A8	0x1601_04A8	0x1602_04A8	0x1603_04A8	0x00000000	0x0000000D	Data Lane 2 Interrupt Enable Register bit3=1: When a escape mode entry error (ErrESC) occurs in lane 2 bit2=1: When a control error (ErrControl) occurs in lane 2 bit0=1: When a SoT error (ErrSotHS) occurs in lane 2
	CSI2nDLIE3	0x1600_04B8	0x1601_04B8	0x1602_04B8	0x1603_04B8	0x00000000	0x0000000D	Data Lane 3 Interrupt Enable Register bit3=1: When a escape mode entry error (ErrESC) occurs in lane 3 bit2=1: When a control error (ErrControl) occurs in lane 3 bit0=1: When a SoT error (ErrSotHS) occurs in lane 3
	CSI2nVCIE0	0x1600_0508	0x1601_0508	0x1602_0508	0x1603_0508	0x00000000	0x0000033F	Virtual Channel 0 Interrupt Enable Register bit9=1: When ErrFrameData is detected bit8=1: When ErrFrameSync is detected bit5=1: When a 1bit error is detected and corrected by ECC check bit4=1: When data payload length of the packet is detected to be shorter than the value indicated by WC bit3=1: When detecting ErrID and discarding the packet bit2=1: When a CRC error is detected in a received packet bit1=1: When a 2bit error is detected and corrected by ECC check bit0=1: When a packet less than 4 bytes is received
Image Converter	CRUnCTRL	0x1600_0000	0x1601_0000	0x1602_0000	0x1603_0000	0x00000000	0x00000002	bit1: 1b: All ignore (Bypasses the Virtual Channel and Data Type set by registers ICnSVC and ICnNIPDT_C0 to 3L/H)
	CRUnIE1	0x1600_0004	0x1601_0004	0x1602_0004	0x1603_0004	0x00000000	0x00000007	CRU Interrupt Enable Register1 bit2=1: When Video Data AXI-VD DECERR error occurs bit1=1: When Video Data AXI-VD SLVERR error occurs bit0=1: When FIFO overflows
	CRUnIE2	0x1600_0008	0x1601_0008	0x1602_0008	0x1603_0008	0x00000000	0x00060000	CRU Interrupt Enable Register2 bit18 AXI-VD bus write completion interrupt enable control for designated address 2 bit17 AXI-VD bus write completion interrupt enable control for designated address 1
	AMnMBVALID	0x1600_0088	0x1601_0088	0x1602_0088	0x1603_0088	0x00000001	0x00000003	Video Data transfer destination valid address [0]: 1: MB1 valid [1]: 1: MB2 valid [2 to 7]: 0: MB3 to 8 invalid
	AMnMB1ADDRL	0x1600_0040	0x1601_0040	0x1602_0040	0x1603_0040	0x00000000	0x40000000	Video Data transfer destination base address 1
	AMnMB1ADDRH	0x1600_0044	0x1601_0044	0x1602_0044	0x1603_0044	0x00000000	0x00000000	MB1 base address: 0x4000_0000
	AMnMB2ADDRL	0x1600_0048	0x1601_0048	0x1602_0048	0x1603_0048	0x00000000	0x41000000	Video Data transfer destination base address 2
	AMnMB2ADDRH	0x1600_004C	0x1601_004C	0x1602_004C	0x1603_004C	0x00000000	0x00000000	MB2 base address: 0x4100_0000
	AMnNIAOFL	0x1600_0094	0x1601_0094	0x1602_0094	0x1603_0094	0x00000000	0x00000000	Non Image Process address offset relative to Image Process for Video Data Non Image Process address offset: 0x0000_0000
	AMnNIAOFH	0x1600_0098	0x1601_0098	0x1602_0098	0x1603_0098	0x00000000	0x00000000	
	AMnIVT1ADDRL	0x1600_00BC	0x1601_00BC	0x1602_00BC	0x1603_00BC	0x00000000	0x40CC857F	AXI-VD Bus Transfer Completion Event Address 1: 0x0_40CC_857F
	AMnIVT1ADDRH	0x1600_00C0	0x1601_00C0	0x1602_00C0	0x1603_00C0	0x00000000	0x00000000	
	AMnIVT2ADDRL	0x1600_00C4	0x1601_00C4	0x1602_00C4	0x1603_00C4	0x00000000	0x41CC857F	AXI-VD Bus Transfer Completion Event Address 2: 0x0_40CC_857F
	AMnIVT2ADDRH	0x1600_00C8	0x1601_00C8	0x1602_00C8	0x1603_00C8	0x00000000	0x00000000	
	AMnIS	0x1600_0128	0x1601_0128	0x1602_0128	0x1603_0128	0x00000000	0x00001780	Setting the Line Beginning Address Offset for Image Stride You can set 128 to 32640byte (128byte step) by setting AMnIS[31:0]. Image stride : 0x0000_1780 (6016byte : 3840pixel*1.5byte+ 36byte(Effective margin)+32byte(Header)+28byteDummy+ 32byte(Footer)=5880byte : 128byteBlank)
	AMnAXIATTR	0x1600_00EC	0x1601_00EC	0x1602_00EC	0x1603_00EC	0x00200150	0x0020015F	Setting the maximum value of AXI-VD Burst Length for Video Data (prohibiting change during AXI-VD operation) [3:0]: Fh : Up to 16 Burst
	ICnDTVP	0x1600_01F4	0x1601_01F4	0x1602_01F4	0x1603_01F4	0x00000003	0x00000030	[4]: 1: Adds Header [5]: 1: Adds Footer
	ICnSVCNUM	0x1600_01F8	0x1601_01F8	0x1602_01F8	0x1603_01F8	0x00000000	0x00000000	Set how many of SVC0 to 3 to use. [1:0]: 00b : SVC0 only, SVC1 to 3 disable (initial value)
	ICnSVC	0x1600_01FC	0x1601_01FC	0x1602_01FC	0x1603_01FC	0x00003210	0x00003210	Selected Virtual Channel 0 (SVC0) [3:0]: 0h: Virtulal Channel 0 Selection (initial value)
	ICnNIPDT_C0L	0x1600_0204	0x1601_0204	0x1602_0204	0x1603_0204	0x00000000	0x00000000	Data Type code selection for Non Image Process selected with SVC0 0x2C(44d):RAW12 0x37(55d):User Defined 8-bit Data Type 8
	ICnNIPDT_C0H	0x1600_0208	0x1601_0208	0x1602_0208	0x1603_0208	0x00000000	0x00801000	

1.3 4K RAW10 60.4fps Input Setting (Full Bypass)

The requirements for the 4K RAW10 60.4fps input setting (using Full bypass) examples are indicated in **Table 1-6**. The register settings are indicated in **Table 1-7**. For the setting procedure, follow the instructions in the *RZ/V2H Group User's Manual: Hardware* for starting MIPI CSI-2 input reception.

Table 1-6 4K RAW10 60.4fps Input Setting (Full Bypass) Examples

Category	Description
Input format, size	IMX415 full screen mode assumed(Recording Pixel area：3840 × 2160, 60.4fps) Pixel area: ● RAW10: (3840 + 12 + 12) × (2160 + 21 + 11), 60.4fps Other than images: ● EBD (Embedded Data): 1 line ● Optical Black (User Defined 8-bit Data Type 8): 17 + 18 + 1 line (Ignored included) 
Transfer rate	1440Mbps/lane × 4 lanes
Virtual channel	SVC0=VC0 (SVC1 to 3 is unused)
Input format	MIPI CSI-2 Input: RAW10, User Defined 8-bit Data Type 8
Interrupt settings	MIPI CSI2: Enable only error related interrupts, disable interrupts for normal operation. Image Converter: Error and Designated address forwarding completion interrupt settings
Header, Footer	Header (for each line): Yes Footer (for each line): Yes
Image stride	0x0_0000_1380(4992byte)
Output starting address	Uses 2 memory banks (MB1,2) Output in MIPI recommended memory storage format. MB1: 0x0_4000_0000（Starting address of Recording Pixel area:0x0_4004_57AF） MB2: 0x0_4100_0000（Starting address of Recording Pixel area:0x0_4104_57AF）
Memory image	See **Figure 1.3-1** for details.
Output format	RAW10, Optical Black (User Defined 8-bit Data Type 8) Does not output EBD (Embedded Data). *1

Note 1. Please make additional settings if necessary.

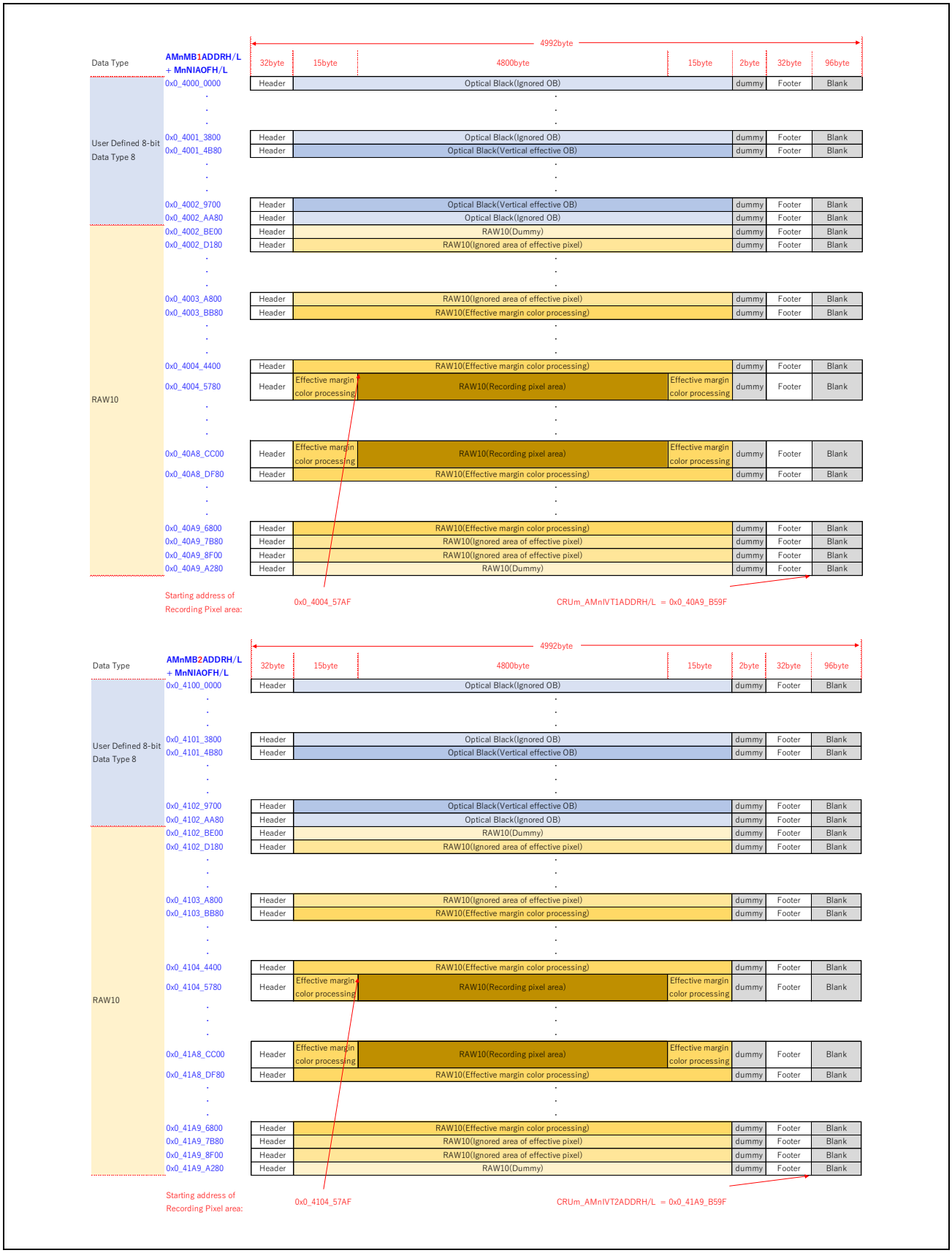


Figure 1.3-1 Memory Image Table 2

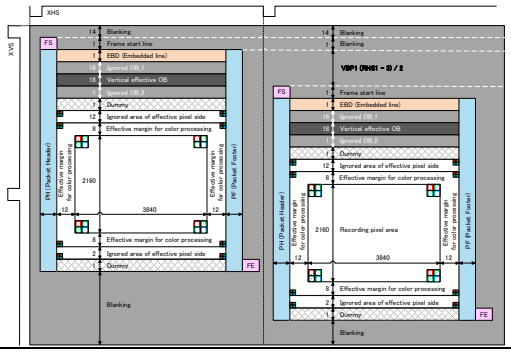
Table 1-7 4K RAW10 60.4fps Input Setting (Full Bypass) Examples

	Register Name	Address				Initial Value	Setting Value	Comments
		CRU0	CRU1	CRU2	CRU3			
D-PHY	SWAPCTL	0x1600_0838	0x1601_0838	0x1602_0838	0x1603_0838	0x00000000	0x00000000	DP/DN Swap Control Register Does not swap.
	S_DPHYCTL_MSB	0x1600_0834	0x1601_0834	0x1602_0834	0x1603_0834	0x00000090	0x00000090	bit1: DeSkew Calibration Function Enable/Disable Control 0b: DeSkew Calibration Disable
	S_TIMCTL	0x1600_081C	0x1601_081C	0x1602_081C	0x1603_081C	0x00000000	0x00001F00	Slave Data Lane Control Register for THS-SETTLE. 1440Mbps/lane: S_HSSETTLECTL[7:0]=1Fh
LINK	CSI2nMCT0	0x1600_0410	0x1601_0410	0x1602_0410	0x1603_0410	0x02000004	0x00000004	[25]: 0b: Disables de-scrambling. [3:0]: 4h: Operates on 4 lanes
	CSI2nMCT2	0x1600_0418	0x1601_0418	0x1602_0418	0x1603_0418	0x00000000	0x000B0006	[24:16]: When the vclk frequency is 630MHz and the transfer rate is 1440Mbps, set to "0Bh": ROUNDDOWN((3*630/(1440/8)), 0) + 1 = 11 [8:0]: When the vclk frequency is 630MHz and the transfer rate is 1440Mbps, set to "6h": ROUNDDOWN((1.5*630/(1440/8)), 0) + 1 = 6
	CSI2nDTEL	0x1600_0460	0x1601_0460	0x1602_0460	0x1603_0460	0x0000000f	0xF77CFF0F	Select all Data Types supported by image_converter.
	CSI2nDTEH	0x1600_0464	0x1601_0464	0x1602_0464	0x1603_0464	0x00000000	0x00FFFF1F	
	CSI2nDLIE0	0x1600_0488	0x1601_0488	0x1602_0488	0x1603_0488	0x00000000	0x0000000D	Data Lane 0 Interrupt Enable Register bit3=1: When a escape mode entry error (ErrESC) occurs in lane 0 bit2=1: When a control error (ErrControl) occurs in lane 0 bit0=1: When a SoT error (ErrSotHS) occurs in lane 0
	CSI2nDLIE1	0x1600_0498	0x1601_0498	0x1602_0498	0x1603_0498	0x00000000	0x0000000D	Data Lane 1 Interrupt Enable Register bit3=1: When a escape mode entry error (ErrESC) occurs in lane 1 bit2=1: When a control error (ErrControl) occurs in lane 1 bit0=1: When a SoT error (ErrSotHS) occurs in lane 1
	CSI2nDLIE2	0x1600_04A8	0x1601_04A8	0x1602_04A8	0x1603_04A8	0x00000000	0x0000000D	Data Lane 2 Interrupt Enable Register bit3=1: When a escape mode entry error (ErrESC) occurs in lane 2 bit2=1: When a control error (ErrControl) occurs in lane 2 bit0=1: When a SoT error (ErrSotHS) occurs in lane 2
	CSI2nDLIE3	0x1600_04B8	0x1601_04B8	0x1602_04B8	0x1603_04B8	0x00000000	0x0000000D	Data Lane 3 Interrupt Enable Register bit3=1: When a escape mode entry error (ErrESC) occurs in lane 3 bit2=1: When a control error (ErrControl) occurs in lane 3 bit0=1: When a SoT error (ErrSotHS) occurs in lane 3
	CSI2nVCIE0	0x1600_0508	0x1601_0508	0x1602_0508	0x1603_0508	0x00000000	0x0000033F	Virtual Channel 0 Interrupt Enable Register bit9=1: When ErrFrameData is detected bit8=1: When ErrFrameSync is detected bit5=1: When a 1bit error is detected and corrected by ECC check bit4=1: When data payload length of the packet is detected to be shorter than the value indicated by WC bit3=1: When detecting ErrID and discarding the packet bit2=1: When a CRC error is detected in a received packet bit1=1: When a 2bit error is detected and corrected by ECC check bit0=1: When a packet less than 4 bytes is received
Image Converter	CRUnCTRL	0x1600_0000	0x1601_0000	0x1602_0000	0x1603_0000	0x00000000	0x00000002	bit1: 1: All ignore (Bypasses the Virtual Channel and Data Type set by registers ICnSVC and ICnNIPDT_C0 to 3L/H)
	CRUnIE1	0x1600_0004	0x1601_0004	0x1602_0004	0x1603_0004	0x00000000	0x00000007	CRU Interrupt Enable Register1 bit2=1: When Video Data AXI-VD DECERR error occurs bit1=1: When Video Data AXI-VD SLVERR error occurs bit0=1: When FIFO overflows
	CRUnIE2	0x1600_0008	0x1601_0008	0x1602_0008	0x1603_0008	0x00000000	0x00060000	CRU Interrupt Enable Register2 bit18 AXI-VD bus write completion interrupt enable control for designated address 2 bit17 AXI-VD bus write completion interrupt enable control for designated address 1
	AMnMBVALID	0x1600_0088	0x1601_0088	0x1602_0088	0x1603_0088	0x00000001	0x00000003	Video Data transfer destination valid address [0]: 1: MB1 valid [1]: 1: MB2 valid [2 to 7]: 0: MB3 to 8 invalid
	AMnMB1ADDRL	0x1600_0040	0x1601_0040	0x1602_0040	0x1603_0040	0x00000000	0x40000000	Video Data transfer destination base address 1
	AMnMB1ADDRH	0x1600_0044	0x1601_0044	0x1602_0044	0x1603_0044	0x00000000	0x00000000	MB1 base address: 0x4000_0000
	AMnMB2ADDRL	0x1600_0048	0x1601_0048	0x1602_0048	0x1603_0048	0x00000000	0x41000000	Video Data transfer destination base address 2
	AMnMB2ADDRH	0x1600_004C	0x1601_004C	0x1602_004C	0x1603_004C	0x00000000	0x00000000	MB2 base address: 0x4100_0000
	AMnNIAOFL	0x1600_0094	0x1601_0094	0x1602_0094	0x1603_0094	0x00000000	0x00000000	Non Image Process address offset relative to Image Process for Video Data Non Image Process address offset: 0x0000_0000
	AMnNIAOFH	0x1600_0098	0x1601_0098	0x1602_0098	0x1603_0098	0x00000000	0x00000000	
	AMnIVT1ADDRL	0x1600_00BC	0x1601_00BC	0x1602_00BC	0x1603_00BC	0x00000000	0x40A9B59F	AXI-VD Bus Transfer Completion Event Address 1: 0x0_40A9_B59F
	AMnIVT1ADDRH	0x1600_00C0	0x1601_00C0	0x1602_00C0	0x1603_00C0	0x00000000	0x00000000	
	AMnIVT2ADDRL	0x1600_00C4	0x1601_00C4	0x1602_00C4	0x1603_00C4	0x00000000	0x41A9B59F	AXI-VD Bus Transfer Completion Event Address 2: 0x0_41A9_B59F
	AMnIVT2ADDRH	0x1600_00C8	0x1601_00C8	0x1602_00C8	0x1603_00C8	0x00000000	0x00000000	
	AMnIS	0x1600_0128	0x1601_0128	0x1602_0128	0x1603_0128	0x00000000	0x00001380	Setting the Line Beginning Address Offset for Image Stride You can set 128 to 32640byte (128byte step) by setting AMnIS[31:0]. Image stride: 0x0000_1380 (4992byte : 3840pixel*1.25byte+ 30byte(Effective margin)+32byte(Header)+ 2byteDummy+32byte(Footer)=4894byte: 98byteBlank)
	AMnAXIATTR	0x1600_00EC	0x1601_00EC	0x1602_00EC	0x1603_00EC	0x00200150	0x0020015F	Setting the maximum value of AXI-VD Burst Length for Video Data (prohibiting change during AXI-VD operation) [3:0]: Fh: Up to 16 Burst
	ICnDTVP	0x1600_01F4	0x1601_01F4	0x1602_01F4	0x1603_01F4	0x00000003	0x00000030	[4]: 1: Adds Header [5]: 1: Adds Footer
	ICnSVCNUM	0x1600_01F8	0x1601_01F8	0x1602_01F8	0x1603_01F8	0x00000000	0x00000000	Set how many of SVC0 to 3 to use. [1:0]: 00: SVC0 only, SVC1 to 3 disable (initial value)
	ICnSVC	0x1600_01FC	0x1601_01FC	0x1602_01FC	0x1603_01FC	0x00003210	0x00003210	Selected Virtual Channel 0 (SVC0) [3:0]: 0h: Virtulal Channel 0 Selection (initial value)
	ICnNIPDT_C0L	0x1600_0204	0x1601_0204	0x1602_0204	0x1603_0204	0x00000000	0x00000000	Data Type code selection for Non Image Process selected with SVC0 0x2B(43d): RAW10
	ICnNIPDT_C0H	0x1600_0208	0x1601_0208	0x1602_0208	0x1603_0208	0x00000000	0x00800800	0x37(55d): User Defined 8-bit Data Type 8

1.4 IMX415 DOL 2 Frame Input Setting

The requirements for the IMX415 DOL 2 frame input examples are indicated in **Table 1-8**. The register settings are indicated in **Table 1-9**. For the setting procedure, follow the instructions in the *RZ/V2H Group User's Manual: Hardware* for starting MIPI CSI-2 input reception.

Table 1-8 IMX415 DOL 2 Frame Input Examples

Category	Description
Input format, size	IMX415 DOL 2 frame/full screen mode/Virtual Channel Output (No XVS spanning) assumed (Recording Pixel area: 3840 × 2160, 31.5fps [Before synthesis]) Pixel area: • RAW10: (3840 + 12 + 12) × (2160 + 21 + 11), 31.5fps [Before synthesis] Other than images: • EBD (Embedded Data): 1 line • Optical Black (User Defined 8-bit Data Type 8): 16 + 18 + 1 line (Ignored included) 
Transfer rate	1440Mbps/lane × 4 lanes
Virtual channel	SVC0=VC0, SVC1=VC1 (SVC2 to 3 is unused)
Input format	MIPI CSI-2 Input: RAW10, User Defined 8-bit Data Type 8
Interrupt setting	MIPI CSI-2: Enable only error related interrupts, disable interrupts for normal operation Image Converter: Error and Designated address forwarding completion interrupt settings
Header, Footer	Header (for each line): Yes Footer (for each line): Yes
Image stride	0x0_0000_1380(4992byte)
Output starting address	Uses 2 memory banks (MB1,2), uses SVC0 to 1(SVCAOF) Outputs in MIPI recommended memory storage format. MB1: 0x0_4000_0000 (Starting address of Recording Pixel area: 0x0_4004_442F) MB2: 0x0_5000_0000 (Starting address of Recording Pixel area: 0x0_5004_442F) SVCAOF: 0x0_0100_0000
Memory image	See **Figure 1.4-1** and **Figure 1.4-2** for details.
Output format	RAW10, Optical Black (User Defined 8-bit Data Type 8) Does not output EDB (Embedded Data). *1

Output Frame	Virtual Channel [1:0]	
	DOL 2 frame	DOL 3 frame
LEF	0h	0h
SEF1	1h	1h
SEF2	-	2h

Note 1. Please make additional settings if necessary.

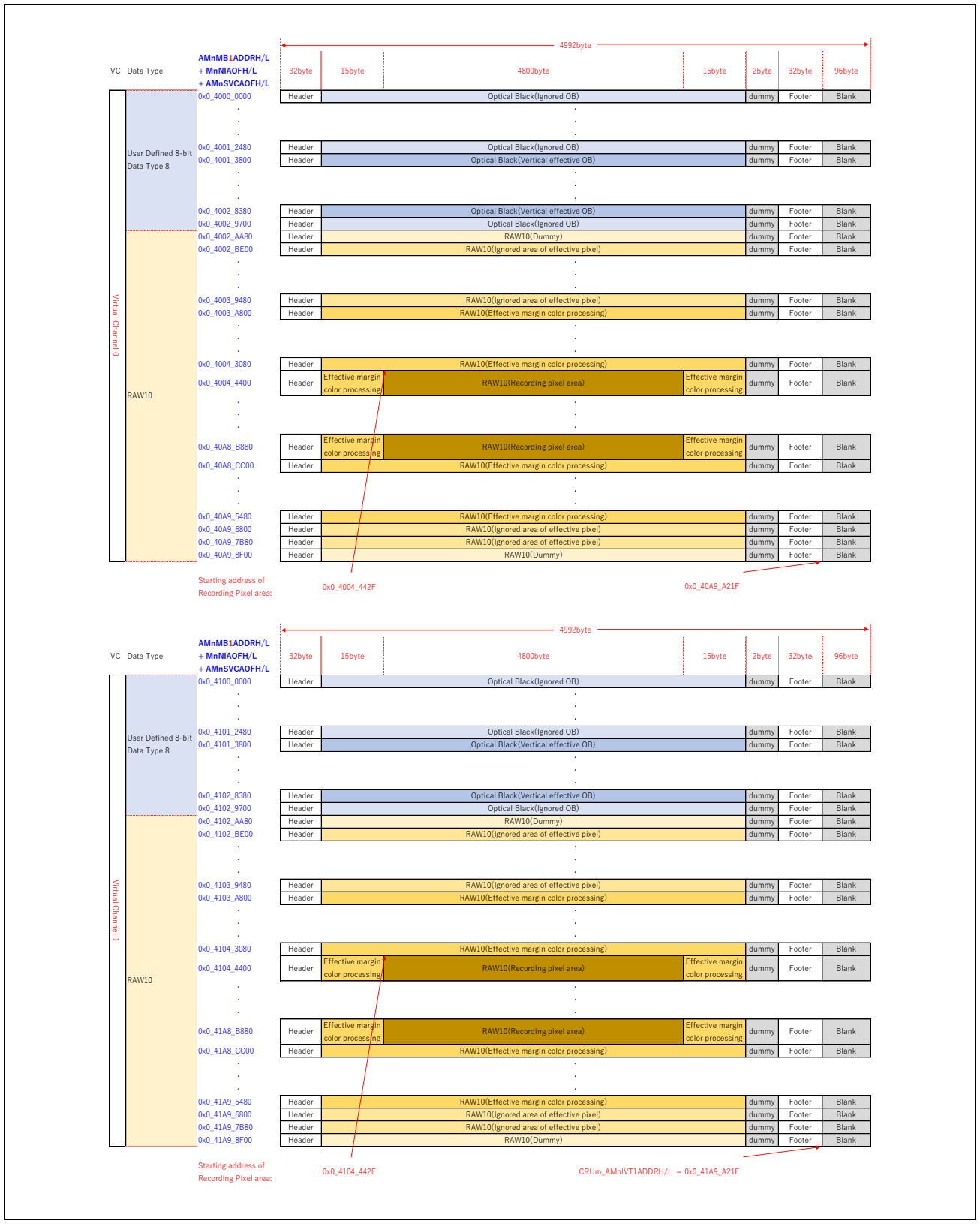


Figure 1.4-1 Memory image (MB1) Table 3

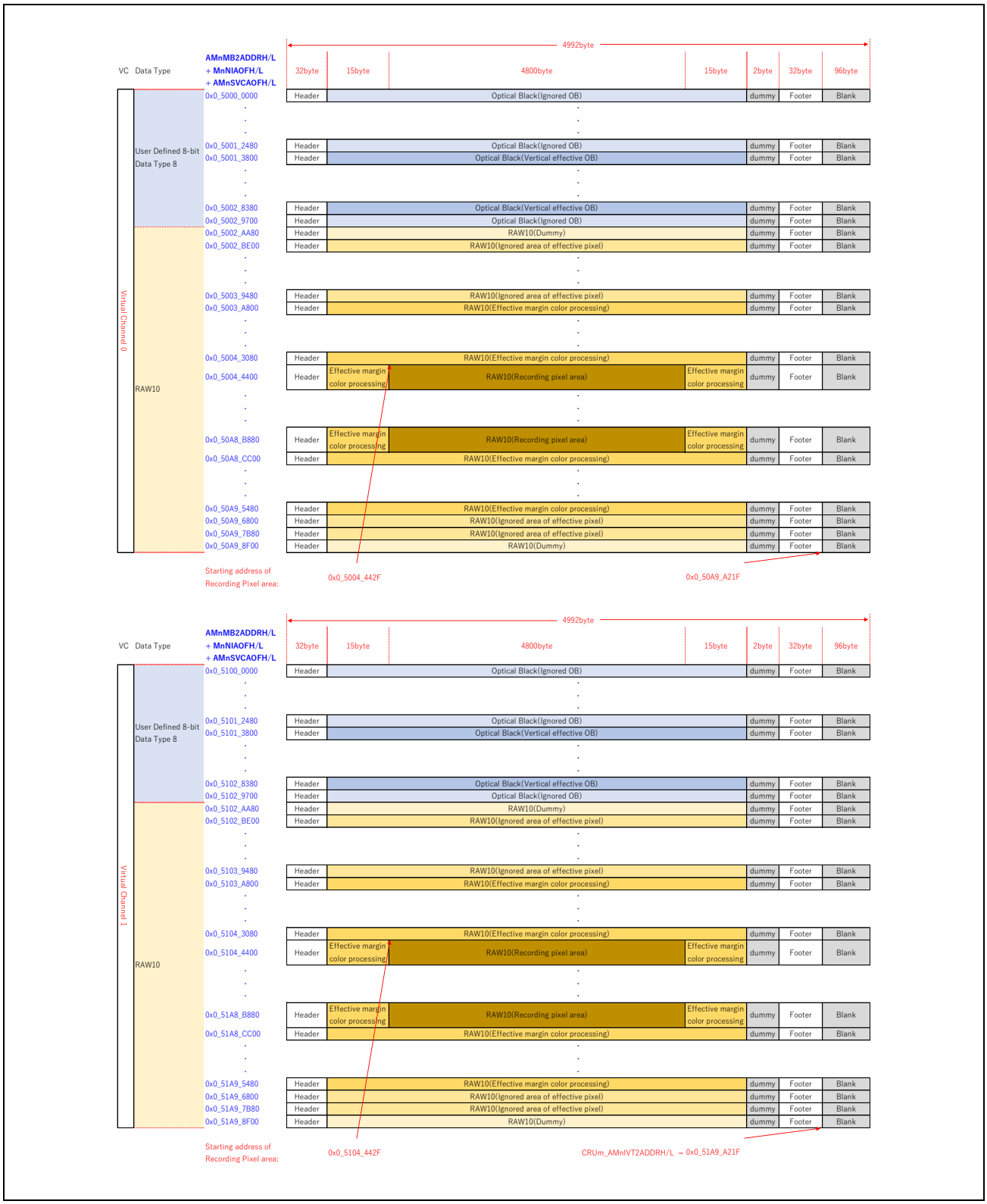


Figure 1.4-2 Memory image (MB2) Table 4

Table 1-9 IMX415 DOL 2 Frame Input Examples (Register settings)

Block	Register Name	Address				Initial Value	Setting Value	Comments
		CRU0	CRU1	CRU2	CRU3			
D-PHY	SWAPCTL	0x1600_0838	0x1601_0838	0x1602_0838	0x1603_0838	0x00000000	0x00000000	DP/DN Swap Control Register Does not swap.
	S_DPHYCTL_MSB	0x1600_0834	0x1601_0834	0x1602_0834	0x1603_0834	0x00000090	0x00000090	bit1: DeSkew Calibration Function Enable/Disable Control 0b: DeSkew Calibration Disable
	S_TIMCTL	0x1600_081C	0x1601_081C	0x1602_081C	0x1603_081C	0x00000000	0x00001F00	Slave Data Lane Control Register for THS-SETTLE. 1440Mbps/lane: S_HSSETTLECTL[7:0]=1Fh
LINK	CSI2nMCT0	0x1600_0410	0x1601_0410	0x1602_0410	0x1603_0410	0x02000004	0x00000004	[25]: 0b: Disables de-scrambling. [3:0]: 4h: Operates on 4 lanes
	CSI2nMCT2	0x1600_0418	0x1601_0418	0x1602_0418	0x1603_0418	0x00000000	0x000B0006	[24:16]: When the vclk frequency is 630MHz and the transfer rate is 1440Mbps, set to "0Bh": ROUNDDOWN((3*630/(1440/8)), 0) + 1 = 11 [8:0]: When the vclk frequency is 630MHz and the transfer rate is 1440Mbps, set to "6h": ROUNDDOWN((1.5*630/(1440/8)), 0) + 1 = 6
	CSI2nDTEL	0x1600_0460	0x1601_0460	0x1602_0460	0x1603_0460	0x0000000f	0xF77CFF0F	Select all Data Types supported by image_converter.
	CSI2nDTEH	0x1600_0464	0x1601_0464	0x1602_0464	0x1603_0464	0x00000000	0x00FFFF1F	
	CSI2nDLIE0	0x1600_0488	0x1601_0488	0x1602_0488	0x1603_0488	0x00000000	0x0000000D	Data Lane 0 Interrupt Enable Register bit3=1: When a escape mode entry error (ErrESC) occurs in lane 0 bit2=1: When a control error (ErrControl) occurs in lane 0 bit0=1: When a SoT error (ErrSotHS) occurs in lane 0
	CSI2nDLIE1	0x1600_0498	0x1601_0498	0x1602_0498	0x1603_0498	0x00000000	0x0000000D	Data Lane 1 Interrupt Enable Register bit3=1: When a escape mode entry error (ErrESC) occurs in lane 1 bit2=1: When a control error (ErrControl) occurs in lane 1 bit0=1: When a SoT error (ErrSotHS) occurs in lane 1
	CSI2nDLIE2	0x1600_04A8	0x1601_04A8	0x1602_04A8	0x1603_04A8	0x00000000	0x0000000D	Data Lane 2 Interrupt Enable Register bit3=1: When a escape mode entry error (ErrESC) occurs in lane 2 bit2=1: When a control error (ErrControl) occurs in lane 2 bit0=1: When a SoT error (ErrSotHS) occurs in lane 2
	CSI2nDLIE3	0x1600_04B8	0x1601_04B8	0x1602_04B8	0x1603_04B8	0x00000000	0x0000000D	Data Lane 3 Interrupt Enable Register bit3=1: When a escape mode entry error (ErrESC) occurs in lane 3 bit2=1: When a control error (ErrControl) occurs in lane 3 bit0=1: When a SoT error (ErrSotHS) occurs in lane 3
	CSI2nVCIE0	0x1600_0508	0x1601_0508	0x1602_0508	0x1603_0508	0x00000000	0x0000033F	Virtual Channel 0 Interrupt Enable Register bit9=1: When ErrFrameData is detected bit8=1: When ErrFrameSync is detected bit5=1: When a 1bit error is detected and corrected by ECC check bit4=1: When data payload length of the packet is detected to be shorter than the value indicated by WC bit3=1: When detecting ErrID and discarding the packet bit2=1: When a CRC error is detected in a received packet bit1=1: When a 2bit error is detected and corrected by ECC check bit0=1: When a packet less than 4 bytes is received
Image Converter	CRUnCTRL	0x1600_0000	0x1601_0000	0x1602_0000	0x1603_0000	0x00000000	0x00000002	bit1: 1: All ignore (Bypasses the Virtual Channel and Data Type set by registers ICnSVC and ICnNIPDT_C0 to 3L/H)
	CRUnIE1	0x1600_0004	0x1601_0004	0x1602_0004	0x1603_0004	0x00000000	0x00000007	CRU Interrupt Enable Register1 bit2=1: When Video Data AXI-VD DECERR error occurs bit1=1: When Video Data AXI-VD SLVERR error occurs bit0=1: When FIFO overflows
	CRUnIE2	0x1600_0008	0x1601_0008	0x1602_0008	0x1603_0008	0x00000000	0x00060000	CRU Interrupt Enable Register2 bit18 AXI-VD bus write completion interrupt enable control for designated address 2 bit17 AXI-VD bus write completion interrupt enable control for designated address 1
	AMnMBVALID	0x1600_0088	0x1601_0088	0x1602_0088	0x1603_0088	0x00000001	0x00000003	Video Data transfer destination valid address [0]: 1: MB1 valid [1]: 1: MB2 valid [2 to 7]: 0: MB3 to 8 invalid
	AMnMB1ADDRL	0x1600_0040	0x1601_0040	0x1602_0040	0x1603_0040	0x00000000	0x40000000	Video Data transfer destination base address 1
	AMnMB1ADDRH	0x1600_0044	0x1601_0044	0x1602_0044	0x1603_0044	0x00000000	0x00000000	MB1 base address: 0x4000_0000
	AMnMB2ADDRL	0x1600_0048	0x1601_0048	0x1602_0048	0x1603_0048	0x00000000	0x50000000	Video Data transfer destination base address 2
	AMnMB2ADDRH	0x1600_004C	0x1601_004C	0x1602_004C	0x1603_004C	0x00000000	0x00000000	MB2 base address: 0x5000_0000
	AMnNIAOFL	0x1600_0094	0x1601_0094	0x1602_0094	0x1603_0094	0x00000000	0x00000000	Non Image Process address offset relative to Image Process for Video Data Non Image Process address offset: 0x0000_0000
	AMnNIAOFH	0x1600_0098	0x1601_0098	0x1602_0098	0x1603_0098	0x00000000	0x00000000	
	AMnSVCAOFL	0x1600_009C	0x1601_009C	0x1602_009C	0x1603_009C	0x00000000	0x01000000	SVC Data Address Offset Register : 0x0_0100_0000
	AMnSVCAOFH	0x1600_00A0	0x1601_00A0	0x1602_00A0	0x1603_00A0	0x00000000	0x00000000	
	AMnIVT1ADDRL	0x1600_00BC	0x1601_00BC	0x1602_00BC	0x1603_00BC	0x00000000	0x41A9A21F	AXI-VD Bus Transfer Completion Event Address 1: 0x0_41A9_A21F
	AMnIVT1ADDRH	0x1600_00C0	0x1601_00C0	0x1602_00C0	0x1603_00C0	0x00000000	0x00000000	
	AMnIVT2ADDRL	0x1600_00C4	0x1601_00C4	0x1602_00C4	0x1603_00C4	0x00000000	0x51A9A21F	AXI-VD Bus Transfer Completion Event Address 2: 0x0_51A9_A21F
	AMnIVT2ADDRH	0x1600_00C8	0x1601_00C8	0x1602_00C8	0x1603_00C8	0x00000000	0x00000000	
	AMnIS	0x1600_0128	0x1601_0128	0x1602_0128	0x1603_0128	0x00000000	0x00001380	Setting the Line Beginning Address Offset for Image Stride You can set 128 to 32640byte (128byte step) by setting AMnIS[31:0]. Image stride: 0x0000_1380 (4992byte : 3840pixel*1.25byte + 30byte(Effective margin) + 32byte(Header) + 2byteDummy+32byte(Footer)=4894byte: 98byteBlank)
	AMnAXIATTR	0x1600_00EC	0x1601_00EC	0x1602_00EC	0x1603_00EC	0x00200150	0x0020015F	Setting the maximum value of AXI-VD Burst Length for Video Data (prohibiting change during AXI-VD operation) [3:0]: Fh: Up to 16 Burst
	ICnDTVP	0x1600_01F4	0x1601_01F4	0x1602_01F4	0x1603_01F4	0x00000003	0x00000030	[4]: 1: Adds Header [5]: 1: Adds Footer
	ICnSVCNUM	0x1600_01F8	0x1601_01F8	0x1602_01F8	0x1603_01F8	0x00000000	0x00000001	Set how many of SVC0 to 3 to use. [1:0]: 01b : SVC0 and 1 enabled; SVC2 and 3 disabled
	ICnSVC	0x1600_01FC	0x1601_01FC	0x1602_01FC	0x1603_01FC	0x00003210	0x00003210	Selected Virtual Channel 0 (SVC0) [3:0]: 0h: Virtulal Channel 0 Selection (initial value)
	ICnNIPDT_C0L	0x1600_0204	0x1601_0204	0x1602_0204	0x1603_0204	0x00000000	0x00000000	Data Type code selection for Non Image Process selected with SVC0 0x2B(43d): RAW10 0x37(55d): User Defined 8-bit Data Type 8
	ICnNIPDT_C0H	0x1600_0208	0x1601_0208	0x1602_0208	0x1603_0208	0x00000000	0x00800800	
	ICnNIPDT_C1L	0x1600_0264	0x1601_0264	0x1602_0264	0x1603_0264	0x00000000	0x00000000	Data Type code selection for Non Image Process selected with SVC1 0x2B(43d): RAW10 0x37(55d): User Defined 8-bit Data Type 8
	ICnNIPDT_C1H	0x1600_0268	0x1601_0268	0x1602_0268	0x1603_0268	0x00000000	0x00800800	

1.5 Dual YUV Camera Module Connection Setting

The specifications of this example are shown in **Table 1-10**. The input data specifications follow those of the camera module (e-CAM22_CURZH). The register settings are indicated in **Table 1-11**. For the setting procedure, follow the instructions in the *RZ/V2H Group User's Manual: Hardware* for starting MIPI CSI-2 input reception.

Table 1-10 Dual YUV Camera Module Connection Examples

Category	Description
Input format, size	Input data: • Format: YUV422 (UYVY) • Size: FHD (1920 × 1080) • Frame rate: 60 fps
Transfer rate	841 Mbps/lane × 4 lanes
Virtual channel	CRU0: SVC0=VC0 (SVC1 to 3 is unused) CRU1: SVC0=VC0 (SVC1 to 3 is unused)
Input format	MIPI CSI-2 Input: YUV422 8-bit
Interrupt setting	MIPI CSI-2: Disable Image Converter: Enable only the frame end interrupt of SVC0
Header, Footer	Header (for each line): No Footer (for each line): No
Image stride	0x0_0000_0F00 (3840 byte)
Output starting address	Uses 1 memory banks (MB1) Outputs in CRU 64-bit packed pixel format. CRU0 MB1: 0x0_5A80_0000 (Starting address of Recording Pixel area: 0x0_5AA9_C460) CRU1 MB1: 0x0_5CC0_0000 (Starting address of Recording Pixel area: 0x0_5CD5_3BA0)
Output format	YUYV format (Y 1st)
CRU vclk frequency	315 MHz

Table 1-11 Dual YUV Camera Module Connection Examples (Register settings)

	Register Name	Address				Initial Value	Setting Value	Comments
		CRU0	CRU1	CRU2	CRU3			
D-PHY	SWAPCTL	0x1600_0838	0x1601_0838	0x1602_0838	0x1603_0838	0x00000000	0x00000000	DP/DN Swap Control Register Does not swap.
	S_DPHYCTL_MSB	0x1600_0834	0x1601_0834	0x1602_0834	0x1603_0834	0x00000090	0x00000090	bit1: DeSkew Calibration Function Enable/Disable Control 0b: DeSkew Calibration Disable
	S_TIMCTL	0x1600_081C	0x1601_081C	0x1602_081C	0x1603_081C	0x00000000	0x00001200	Slave Data Lane Control Register for THS-SETTLE. 850 Mbps/lane: S_HSSETTLECTL[7:0]=12h
LINK	CSI2nMCT0	0x1600_0410	0x1601_0410	0x1602_0410	0x1603_0410	0x02000004	0x00000004	[25]: 0b: Disables de-scrambling. [3:0]: 4: Operates on 4 lanes
	CSI2nMCT2	0x1600_0418	0x1601_0418	0x1602_0418	0x1603_0418	0x00000000	0x00090005	[24:16]: When the vclk frequency is 315MHz and the transfer rate is 841Mbps, set to "9h": ROUNDDOWN((3*315/(841/8)), 0) + 1 = 9 [8:0]: When the vclk frequency is 315MHz and the transfer rate is 841Mbps, set to "5h": ROUNDDOWN((1.5*315/(841/8)), 0) + 1 = 5
	CSI2nDTEL	0x1600_0460	0x1601_0460	0x1602_0460	0x1603_0460	0x0000000f	0xF77CFF0F	Select all Data Types supported by image_converter.
	CSI2nDTEH	0x1600_0464	0x1601_0464	0x1602_0464	0x1603_0464	0x00000000	0x00FFFF1F	
Image Converter	CRUnIE2	0x1600_0008	0x1601_0008	0x1602_0008	0x1603_0008	0x00000000	0x00000002	CRU Interrupt Enable Register2 bit1 SVC0 Frame end interrupt enable control
	AMnMBVALID	0x1600_0088	0x1601_0088	0x1602_0088	0x1603_0088	0x00000001	0x0000000F	Video Data transfer destination valid address [0]: 1: MB1 valid [1]: 1: MB2 valid [2]: 1: MB3 valid [3]: 1: MB4 valid [4 to 7]: 0: MB5 to 8 invalid
	AMnMB1ADDRL	0x1600_0040	0x1601_0040	0x1602_0040	0x1603_0040	0x00000000	CRU0: 0x5A800000 CRU1: 0x5CC00000	Video Data transfer destination base address 1 MB1 base address: CRU0: 0x5A80_0000 CRU1: 0x5CC0_0000
	AMnMB1ADDRH	0x1600_0044	0x1601_0044	0x1602_0044	0x1603_0044	0x00000000	0x00000000	
	AMnNIAOFL	0x1600_0094	0x1601_0094	0x1602_0094	0x1603_0094	0x00000000	0x00000000	Non Image Process address offset relative to Image Process for Video Data Non Image Process address offset: 0x0000_0000
	AMnNIAOFH	0x1600_0098	0x1601_0098	0x1602_0098	0x1603_0098	0x00000000	0x00000000	
	AMnIS	0x1600_0128	0x1601_0128	0x1602_0128	0x1603_0128	0x00000000	0x00000F00	Setting the Line Beginning Address Offset for Image Stride You can set 128 to 32640byte (128byte step) by setting AMnIS[31:0]. Image stride: 0x0000_0F00 (3840byte)
	AMnAXIATTR	0x1600_00EC	0x1601_00EC	0x1602_00EC	0x1603_00EC	0x00200150	0x00200158	Setting the maximum value of AXI-VD Burst Length for Video Data (prohibiting change during AXI-VD operation) [3:0]: 8h: Up to 8 Burst
	ICnSVC	0x1600_01FC	0x1601_01FC	0x1602_01FC	0x1603_01FC	0x00003210	0x00003210	Selected Virtual Channel 0 (SVC0) [3:0]: 0h: Virtual Channel 0 Selection (initial value)

1.6 Virtual Channel Camera input Setting

The specifications of this example are shown in **Table 1-12**. In this example, two virtual channels (VC0 and VC1) are input to the MIPI-CSI block of CRU0, and then the Image Converter block of CRU0 processes VC0 while the Image Converter block of CRU1 processes VC1. (see **Figure 1.6-1**)

The register settings are indicated in **Table 1-13**. For the setting procedure, follow the instructions in the *RZ/V2H Group User's Manual: Hardware* for starting MIPI CSI-2 input reception.

Table 1-12 Dual Camera Connection with Virtual Channel Examples

Category	Description
Input format, size	IMX415 full screen mode assumed (Recording Pixel area：3840 × 2160, 32.4fps) Pixel area: ● RAW10: (3840 + 12 + 12) × (2160 + 21 + 11), 32.4fps
Transfer rate	1782 Mbps/lane × 4 lanes
Virtual channel	CRU0: SVC0=VC0 (SVC1 to 3 is unused) CRU1: SVC0=VC1 (SVC1 to 3 is unused)
Input format	MIPI CSI-2 Input: RAW10
Interrupt setting	MIPI CSI-2: Disable. Image Converter: Error and Designated address forwarding completion interrupt settings
Header, Footer	Header (for each line): No Footer (for each line): No
Image stride	0x0_0000_1E80 (7808 byte)
Output starting address	Uses 4 memory banks (MB1 to MB4) Outputs in MIPI recommended memory storage format. CRU0 MB1: 0x0_B400_0000 (Starting address of Recording Pixel area: 0x0_B504_9000) MB2: 0x0_B520_0000 (Starting address of Recording Pixel area: 0x0_B624_9000) MB3: 0x0_B640_0000 (Starting address of Recording Pixel area: 0x0_B744_9000) MB4: 0x0_B760_0000 (Starting address of Recording Pixel area: 0x0_B864_9000) CRU1 MB1: 0x0_B880_0000 (Starting address of Recording Pixel area: 0x0_B984_9000) MB2: 0x0_B9A0_0000 (Starting address of Recording Pixel area: 0x0_BAA4_9000) MB3: 0x0_BBE0_0000 (Starting address of Recording Pixel area: 0x0_BCE4_9000) MB4: 0x0_BD00_0000 (Starting address of Recording Pixel area: 0x0_BE04_9000)
Output format	RAW10

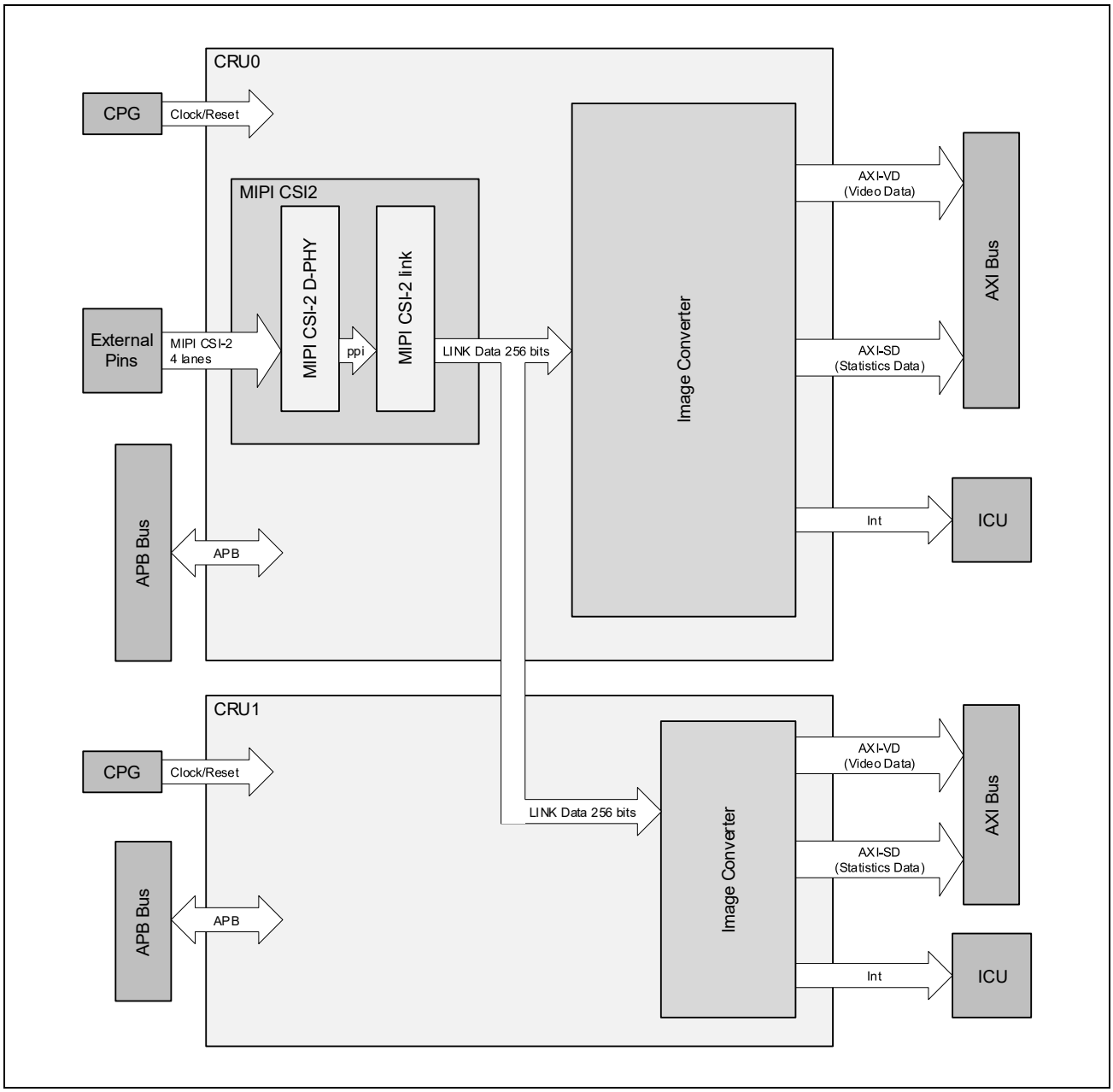


Figure 1.6-1 CRU0 and CRU1 Block Diagram for VC Camera Case

Table 1-13 Dual Camera Connection with Virtual Channel Examples (Register settings)

Block	Register Name	Address				Initial Value	Setting Value	Comments
		CRU0	CRU1	CRU2	CRU3			
D-PHY	SWAPCTL	0x1600_0838	0x1601_0838	0x1602_0838	0x1603_0838	0x00000000	0x00000000	DP/DN Swap Control Register Does not swap.
	S_DPHYCTL_MSB	0x1600_0834	0x1601_0834	0x1602_0834	0x1603_0834	0x00000092	0x00000092	bit1: DeSkew Calibration Function Enable/Disable Control 1b: DeSkew calibration enable
	S_TIMCTL	0x1600_081C	0x1601_081C	0x1602_081C	0x1603_081C	0x00000000	0x00002700	Slave Data Lane Control Register for THS-SETTLE. 1782Mbps/lane: S_HSSETTLECTL[7:0]=27h
LINK	CSI2nMCT0	0x1600_0410	0x1601_0410	0x1602_0410	0x1603_0410	0x02000004	0x00000004	[25]: 0b: Disables de-scrambling. [3:0]: 4h: Operates on 4 lanes
	CSI2nMCT2	0x1600_0418	0x1601_0418	0x1602_0418	0x1603_0418	0x00000000	0x00090005	[24:16]: When the vclk frequency is 630MHz and the transfer rate is 1782Mbps, set to "09h": ROUNDDOWN((3*630/(1782/8)), 0) + 1 = 9 [8:0]: When the vclk frequency is 630MHz and the transfer rate is 1782Mbps, set to "5h": ROUNDDOWN((1.5*630/(1440/8)), 0) + 1 = 5
	CSI2nDTEL	0x1600_0460	0x1601_0460	0x1602_0460	0x1603_0460	0x0000000f	0xF77CFF0F	Select all Data Types supported by image_converter.
	CSI2nDTEH	0x1600_0464	0x1601_0464	0x1602_0464	0x1603_0464	0x00000000	0x00FFFF1F	
Image Converter	CRUnCTRL	0x1600_0000	0x1601_0000	0x1602_0000	0x1603_0000	0x00000000	CRU0: 0x00000000 CRU1: 0x00000001	bit0: 1: MIPI data input from CH0
	CRUnIE1	0x1600_0004	0x1601_0004	0x1602_0004	0x1603_0004	0x00000000	0x00000007	CRU Interrupt Enable Register1 bit2=1: When Video Data AXI-VD DECERR error occurs bit1=1: When Video Data AXI-VD SLVERR error occurs bit0=1: When FIFO overflows
	CRUnIE2	0x1600_0008	0x1601_0008	0x1602_0008	0x1603_0008	0x00000000	0x001E0002	CRU Interrupt Enable Register2 [20:17] AXI-VD bus write completion interrupt enable (video data-related) for designated address 1 to 4. [1] SVC0 Frame end interrupt enable
	AMnMBVALID	0x1600_0088	0x1601_0088	0x1602_0088	0x1603_0088	0x00000001	0x0000000F	Video Data transfer destination valid address [0]: 1: MB1 valid [1]: 1: MB2 valid [2]: 1: MB3 valid [3]: 1: MB4 valid [4 to 7]: 0: MB5 to 8 invalid
	AMnMB1ADDRL	0x1600_0040	0x1601_0040	0x1602_0040	0x1603_0040	0x00000000	CRU0: 0xB4000000 CRU1: 0xB8800000	Video Data transfer destination base address 1 MB1 base address: CRU0: 0xB400_0000 CRU1: 0xB880_0000
	AMnMB1ADDRH	0x1600_0044	0x1601_0044	0x1602_0044	0x1603_0044	0x00000000	0x00000000	
	AMnMB2ADDRL	0x1600_0048	0x1601_0048	0x1602_0048	0x1603_0048	0x00000000	CRU0: 0xB5200000 CRU1: 0xB9A00000	Video Data transfer destination base address 2 MB2 base address: CRU0: 0xB520_0000 CRU1: 0xB9A0_0000
	AMnMB2ADDRH	0x1600_004C	0x1601_004C	0x1602_004C	0x1603_004C	0x00000000	0x00000000	
	AMnMB3ADDRL	0x1600_0050	0x1601_0050	0x1602_0050	0x1603_0050	0x00000000	CRU0: 0xB6400000 CRU1: 0xBBE00000	Video Data transfer destination base address 3 MB3 base address: CRU0: 0xB640_0000 CRU1: 0xBBE0_0000
	AMnMB3ADDRH	0x1600_0054	0x1601_0054	0x1602_0054	0x1603_0054	0x00000000	0x00000000	
	AMnMB4ADDRL	0x1600_0058	0x1601_0058	0x1602_0058	0x1603_0058	0x00000000	CRU0: 0xB7600000 CRU1: 0xBD000000	Video Data transfer destination base address 4 MB4 base address: CRU0: 0xB760_0000 CRU1: 0xBD00_0000
	AMnMB4ADDRH	0x1600_005C	0x1601_005C	0x1602_005C	0x1603_005C	0x00000000	0x00000000	
	AMnNIAOFL	0x1600_0094	0x1601_0094	0x1602_0094	0x1603_0094	0x00000000	0x00000000	Non Image Process address offset relative to Image Process for Video Data Non Image Process address offset: 0x0000_0000
	AMnNIAOFH	0x1600_0098	0x1601_0098	0x1602_0098	0x1603_0098	0x00000000	0x00000000	
	AMnSVCAOFL	0x1600_009C	0x1601_009C	0x1602_009C	0x1603_009C	0x00000000	0x01049000	SVC Data Address Offset Register : 0x0_1049_0000
	AMnSVCAOFH	0x1600_00A0	0x1601_00A0	0x1602_00A0	0x1603_00A0	0x00000000	0x00000000	
	AMnIVT1ADDRL	0x1600_00BC	0x1601_00BC	0x1602_00BC	0x1603_00BC	0x00000000	CRU0: 0xB5049000 CRU1: 0xB9849000	AXI-VD Bus Transfer Completion Event Address 1: CRU0: 0xB504_9000 CRU1: 0xB984_9000
	AMnIVT1ADDRH	0x1600_00C0	0x1601_00C0	0x1602_00C0	0x1603_00C0	0x00000000	0x00000000	
	AMnIVT2ADDRL	0x1600_00C4	0x1601_00C4	0x1602_00C4	0x1603_00C4	0x00000000	CRU0: 0xB6249000 CRU1: 0xBAA49000	AXI-VD Bus Transfer Completion Event Address 2: CRU0: 0xB624_9000 CRU1: 0xBAA4_9000
	AMnIVT2ADDRH	0x1600_00C8	0x1601_00C8	0x1602_00C8	0x1603_00C8	0x00000000	0x00000000	
	AMnIVT3ADDRL	0x1600_00CC	0x1601_00CC	0x1602_00CC	0x1603_00CC	0x00000000	CRU0: 0xB7449000 CRU1: 0xBCE49000	AXI-VD Bus Transfer Completion Event Address 3: CRU0: 0xB744_9000 CRU1: 0xBCE4_9000
	AMnIVT3ADDRH	0x1600_00D0	0x1601_00D0	0x1602_00D0	0x1603_00D0	0x00000000	0x00000000	
	AMnIVT4ADDRL	0x1600_00D4	0x1601_00D4	0x1602_00D4	0x1603_00D4	0x00000000	CRU0: 0xB8649000 CRU1: 0xBE049000	AXI-VD Bus Transfer Completion Event Address 4: CRU0: 0xB864_9000 CRU1: 0xBE04_9000
	AMnIVT4ADDRH	0x1600_00D8	0x1601_00D8	0x1602_00D8	0x1603_00D8	0x00000000	0x00000000	
	AMnIS	0x1600_0128	0x1601_0128	0x1602_0128	0x1603_0128	0x00000000	0x00001E80	Setting the Line Beginning Address Offset for Image Stride You can set 128 to 32640byte (128byte step) by setting AMnIS[31:0]. Image stride: 0x0000_1E80 (7808byte)
	AMnAXIATTR	0x1600_00EC	0x1601_00EC	0x1602_00EC	0x1603_00EC	0x00200150	0x00200156	Setting the maximum value of AXI-VD Burst Length for Video Data (prohibiting change during AXI-VD operation) [3:0]: 6h: Up to 7 Burst
	ICnSVCNUM	0x1600_01F8	0x1601_01F8	0x1602_01F8	0x1603_01F8	0x00000000	0x00000000	Set how many of SVC0 to 3 to use. [1:0]: 00b : SVC0 enabled; SVC1 to 3 disabled
	ICnSVC	0x1600_01FC	0x1601_01FC	0x1602_01FC	0x1603_01FC	0x00003210	CRU0: 0x00003210 CRU1: 0x00003211	Selected Virtual Channel 0 (SVC0) CRU0: [3:0]: 0h: Virtulal Channel 0 Selection (initial value) CRU1: [3:0]: 1h: Virtulal Channel 1 Selection
	ICnNIPDT_C0L	0x1600_0204	0x1601_0204	0x1602_0204	0x1603_0204	0x00000000	0x00000000	Data Type code selection for Non Image Process selected with SVC0 0x2B(43d): RAW10
	ICnNIPDT_C0H	0x1600_0208	0x1601_0208	0x1602_0208	0x1603_0208	0x00000000	0x00000800	

REVISION HISTORY — RZ/V2H Group CRU Application Note

Rev.	Date	Description	
		Page	Summary
1.00	Dec 11, 2024	—	First edition issued
1.10	Jun 30, 2025	—	Following examples, deleted 4K RAW12 32.4fps Input Setting (Demosaic) 4K RAW10 60.4fps Input Setting (Demosaic) Demosaic, Statistics Usage Setting Four VC Input IMX415 DOL2 Frame (Image Processing) Input
		1.2 4K RAW12 32.4fps Input Setting (Full Bypass)	
		8	The setting value of CSI2nDLIE0 to 3 registers, modified
		1.3 4K RAW10 60.4fps Input Setting (Full Bypass)	
		9	Table 1-14 4K RAW10 60.4fps Input Setting (Full Bypass) Examples Setting examples of input format, modified
		11	The setting value of CSI2nDLIE0 to 3 registers, modified
		1.4 IMX415 DOL2 Frame Input	
		13	Figure 1.6-2 Memory image (MB1) Table 9 The addresses of the optical black, modified
		14	Figure 1.6-3 Memory image (MB2) Table 10 The addresses of the optical black, modified
1.20	Jan 19, 2026	—	The titles, modified (All bypass → Full bypass)
		1.2 4K RAW12 32.4fps Input Setting (Full Bypass)	
		8	The comments of CSI2nMCT2 and CRUnIE1, modified
		1.3 4K RAW10 60.4fps Input Setting (Full Bypass)	
		11	The comments of CSI2nMCT2 and CRUnIE1, modified
		1.4 IMX415 DOL2 Frame Input	
		12	The output standing address, modified
		1.5 Dual YUV Camera Module Connection Setting	
		16, 17	Section, added
		1.6 Virtual Channel Camera input Setting	
		18 to 20	Section, added

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide, and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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