Shielded Inductive Position Sensor Designs

Introduction

Inductive position sensors, consisting of transmitter and receiver coil sets are used to generate and measure electromagnetic fields. To keep the signal clean and robust, the area above and around the coils should normally remain free of conductive elements such as ICs and passive components, since these can disturb the field.

Tight layouts can present difficulties, as components occasionally must be positioned directly above the coil area. When interference arises, a layer of metal shielding is placed between the coils and the components to block it. This shield also reduces the received signal strength, and the system must still meet the minimum coil voltage needed for proper IC operation. The shield is commonly positioned on an internal layer near the components, ensuring maximum distance from the coils to reduce signal loss.

This Renesas patented (U.S. provisional patent application No. 63/396,314) application note explains how to create shielded designs and how the shield affects the received signal.

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1. Introduction

Shielded inductive position sensor designs (IPS) allow customers to design very compact sensors by distributing the chip and passive elements in the same area defined from the sensing element. This method is ideal when a module's mechanical housing doesn't allow designers to place chips and other passive electronic components outside of the sensing element's area.

The major benefit is the small overall design footprint. The disadvantage might occur on the PCB cost end, but not always necessarily. Due to implementing a conductive shield layer on one of the inner PCB layers, its distance needs to be larger to the coil design pattern to ensure sufficient receiver signal amplitude. Using blind-vias with small designs (less than approximately 40 mm outer diameter) could also raise the production costs.

Typical field of usage is replacement of old rotary resolver designs with low profile, lightweight, low BOM inductive position sensor solutions. The principle can be reused with any shape and complexity of inductive position sensors if the physical limitations are considered.

Please visit our Industry 4.0 targeted reference design catalog with more than 80 different, validated designs including downloadable Gerbers and Measurement Reports. The so called "Backward compatible resolver 4.0" selection covers 18 different prototypes:

https://www.renesas.com/en/products/sensor-products/inductive-position-sensors/ips2x-customer-reference-board-catalog

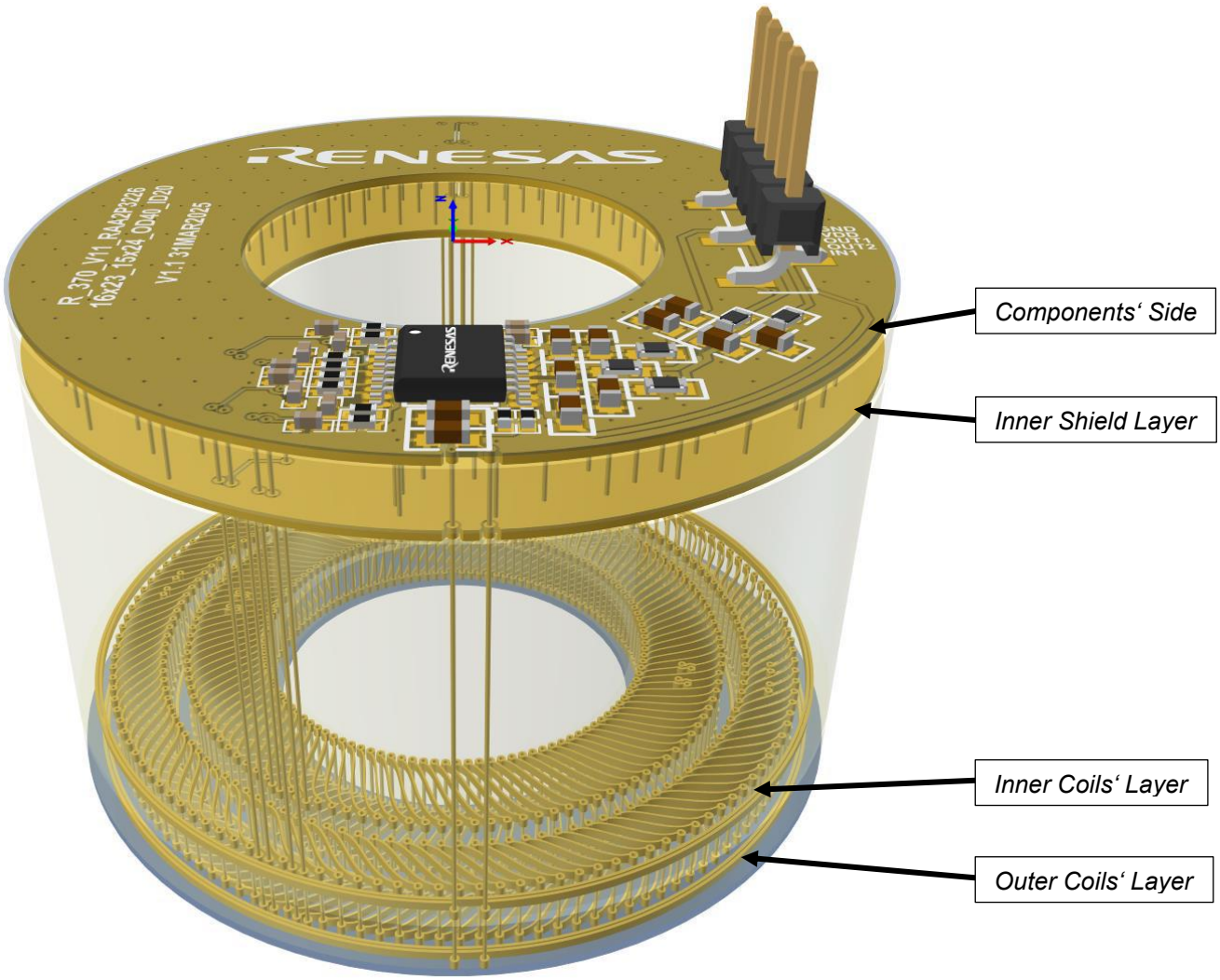

Figure 1. Layer Stack Up of a Shielded IPS

2. Design Process

- Use IPSCO (Inductive position sensor coil optimizer) tool on the Renesas webpage: https://ips.renesas.com/
- Select a 2-layer template that allows shielded designs:
  - Rotary – Singe – 2-layer design
  - Rotary – Dual – Common TX (High-resolution)
  - Arc – Single – 2 layers with 1 TX
  - Arc – Single – 2 layers with 2 TX
  - Arc – Single – 2 layers butterfly
  - Linear – Single – 2 layers with 1 TX
  - Linear – Single – 2 layers with 2 TX.
- Select one of them depending on your design needs and input the necessary requirements.
- Read the manual for in-depth explanations and useful information about the simulation process before starting: https://www.renesas.com/en/software-tool/inductive-position-sensor-coil-optimizer
- After you successfully simulate your design, check the simulation results, especially the receiver voltage at maximum air gap. This is typically the lowest amplitude among the results.
- Calculate remaining voltage from the Table 2 in the section 4. The copper shield on the next inner layer to the sensor design reduces the voltage depending on its distance.
- Make sure the calculated remaining RX input voltage stays above the specified minimum to work correctly with the designated IPS chips. Typically, the remaining voltage needs to stay above 8 mV, the higher the better.
- Based on Table 1 in the section 3 you can select a PCB layer stack with your vendor, which still allows high enough receiver voltages. See Example Workflow in section 5.
- Import the IPSCO produced Gerbers to your layout design software or use its Altium Designer outputs. Make sure you put the sensor coils in the upper (or lower) 2 layers, and the preferably uninterrupted shield layer to the next inner layer. The fourth layer (Top or bottom) can be used for component placement and wiring.
- For importing Gerbers to Altium Designer, feel free to use our Tutorial: https://www.renesas.com/en/document/tra/import-sensing-element-altium

3. Remaining RX Voltage Calculations

3.1 Table of Simulated Voltages vs. Remaining Voltages

Table 1. Remaining Receiver Voltages

		Simulated VppRX [mV] from IPSCO simulation results page: value taken from maximum air gap																			
		11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
		Remaining VppRX [mV] including the dampening effect of the shield layer																			
Typical “ coil to shield layer” distances [mm]	0.9	1.3	1.4	1.6	1.7	1.8	1.9	2.0	2.2	2.3	2.4	2.5	2.6	2.8	2.9	3.0	3.1	3.2	3.4	3.5	3.6
	1.1	1.8	2.0	2.1	2.3	2.5	2.6	2.8	3.0	3.1	3.3	3.5	3.6	3.8	4.0	4.1	4.3	4.5	4.6	4.8	5.0
	1.2	2.0	2.2	2.4	2.6	2.8	3.0	3.1	3.3	3.5	3.7	3.9	4.1	4.3	4.4	4.6	4.8	5.0	5.2	5.4	5.6
	1.5	2.7	2.9	3.2	3.4	3.7	3.9	4.2	4.4	4.7	4.9	5.1	5.4	5.6	5.9	6.1	6.4	6.6	6.9	7.1	7.4
	1.9	3.6	3.9	4.2	4.6	4.9	5.2	5.5	5.9	6.2	6.5	6.8	7.2	7.5	7.8	8.1	8.5	8.8	9.1	9.4	9.8
	2.3	4.4	4.8	5.2	5.6	6.0	6.4	6.8	7.2	7.6	8.0	8.4	8.8	9.2	9.6	10.0	10.4	10.8	11.2	11.6	12.0
	2.6	5.0	5.5	5.9	6.4	6.8	7.3	7.7	8.2	8.6	9.1	9.6	10.0	10.5	10.9	11.4	11.8	12.3	12.7	13.2	13.7

		Simulated VppRX [mV] from IPSCO simulation results page: value taken from maximum air gap																		
		31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
		Remaining VppRX [mV] including the dampening effect of the shield layer																			
Typical “ coil to shield layer” distances [mm]	0.9	3.7	3.8	4.0	4.1	4.2	4.3	4.4	4.6	4.7	4.8	4.9	5.0	5.2	5.3	5.4	5.5	5.6	5.8	5.9	6.0
	1.1	5.1	5.3	5.4	5.6	5.8	5.9	6.1	6.3	6.4	6.6	6.8	6.9	7.1	7.3	7.4	7.6	7.8	7.9	8.1	8.3
	1.2	5.7	5.9	6.1	6.3	6.5	6.7	6.8	7.0	7.2	7.4	7.6	7.8	8.0	8.1	8.3	8.5	8.7	8.9	9.1	9.3
	1.5	7.6	7.8	8.1	8.3	8.6	8.8	9.1	9.3	9.6	9.8	10.0	10.3	10.5	10.8	11.0	11.3	11.5	11.8	12.0	12.3
	1.9	10.1	10.4	10.7	11.1	11.4	11.7	12.0	12.4	12.7	13.0	13.3	13.7	14.0	14.3	14.6	15.0	15.3	15.6	15.9	16.3
	2.3	12.4	12.8	13.2	13.6	14.0	14.4	14.8	15.2	15.6	16.0	16.4	16.8	17.2	17.6	18.0	18.4	18.8	19.2	19.6	20.0
	2.6	14.1	14.6	15.0	15.5	15.9	16.4	16.8	17.3	17.7	18.2	18.7	19.1	19.6	20.0	20.5	20.9	21.4	21.8	22.3	22.8

		Simulated VppRX [mV] from IPSCO simulation results page: value taken from maximum air gap																		
		51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70
		Remaining VppRX [mV] including the dampening effect of the shield layer																			
Typical “ coil to shield layer” distances [mm]”	0.9	6.1	6.2	6.4	6.5	6.6	6.7	6.8	7.0	7.1	7.2	7.3	7.4	7.6	7.7	7.8	7.9	8.0	8.2	8.3	8.4
	1.1	8.4	8.6	8.7	8.9	9.1	9.2	9.4	9.6	9.7	9.9	10.1	10.2	10.4	10.6	10.7	10.9	11.1	11.2	11.4	11.6
	1.2	9.4	9.6	9.8	10.0	10.2	10.4	10.5	10.7	10.9	11.1	11.3	11.5	11.7	11.8	12.0	12.2	12.4	12.6	12.8	13.0
	1.5	12.5	12.7	13.0	13.2	13.5	13.7	14.0	14.2	14.5	14.7	14.9	15.2	15.4	15.7	15.9	16.2	16.4	16.7	16.9	17.2
	1.9	16.6	16.9	17.2	17.6	17.9	18.2	18.5	18.9	19.2	19.5	19.8	20.2	20.5	20.8	21.1	21.5	21.8	22.1	22.4	22.8
	2.3	20.4	20.8	21.2	21.6	22.0	22.4	22.8	23.2	23.6	24.0	24.4	24.8	25.2	25.6	26.0	26.4	26.8	27.2	27.6	28.0
	2.6	23.2	23.7	24.1	24.6	25.0	25.5	25.9	26.4	26.8	27.3	27.8	28.2	28.7	29.1	29.6	30.0	30.5	30.9	31.4	31.9

		Simulated VppRX [mV] from IPSCO simulation results page: value taken from maximum air gap																			
		71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90
		Remaining VppRX [mV] including the dampening effect of the shield layer																			
Typical “ coil to shield layer” distances [mm]	0.9	8.5	8.6	8.8	8.9	9.0	9.1	9.2	9.4	9.5	9.6	9.7	9.8	10.0	10.1	10.2	10.3	10.4	10.6	10.7	10.8
	1.1	11.7	11.9	12.0	12.2	12.4	12.5	12.7	12.9	13.0	13.2	13.4	13.5	13.7	13.9	14.0	14.2	14.4	14.5	14.7	14.9
	1.2	13.1	13.3	13.5	13.7	13.9	14.1	14.2	14.4	14.6	14.8	15.0	15.2	15.4	15.5	15.7	15.9	16.1	16.3	16.5	16.7
	1.5	17.4	17.6	17.9	18.1	18.4	18.6	18.9	19.1	19.4	19.6	19.8	20.1	20.3	20.6	20.8	21.1	21.3	21.6	21.8	22.1
	1.9	23.1	23.4	23.7	24.1	24.4	24.7	25.0	25.4	25.7	26.0	26.3	26.7	27.0	27.3	27.6	28.0	28.3	28.6	28.9	29.3
	2.3	28.4	28.8	29.2	29.6	30.0	30.4	30.8	31.2	31.6	32.0	32.4	32.8	33.2	33.6	34.0	34.4	34.8	35.2	35.6	36.0
	2.6	32.3	32.8	33.2	33.7	34.1	34.6	35.0	35.5	35.9	36.4	36.9	37.3	37.8	38.2	38.7	39.1	39.6	40.0	40.5	41.0

Color coding:

- Green = high enough RX voltage
- Light green = close to the minimum specification of IPS2550
- Orange = close to the minimum specification of RAA2P3XXX and RAA2P4XXX
- Red = below specification, not recommended

3.2 Bases of the Calculation in the Table on the Previous Page

Table 2. Layer Distance and Remaining Voltage

Coil to shield layer distance [mm]	Remaining RX voltage [%]
0.9	12.0
1.1	16.5
1.2	18.5
1.5	24.5
1.9	32.5
2.3	40.0
2.6	45.5

3.3 Interactive Chart of Shielded RX Voltages

A lookup Table 1 with specific values of remaining, shielded voltages is good to have, but it is always better to have an online available, interactive, more intuitive tool with additional information, better insights and overview. After loading a finished, 2-layer simulation in IPSCO, you will find the shielded voltages chart close the bottom of the page.

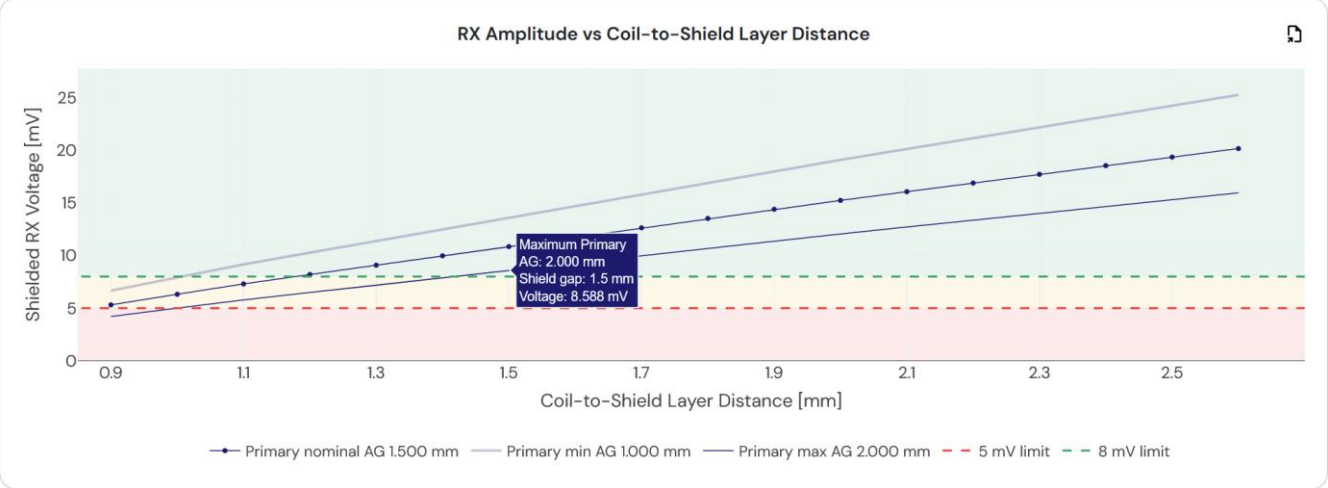

Figure 2. Receiver Amplitude over Coil to Shield Layer Distance

In Figure 2, the X-axis shows the shield layer distance to the next coil containing copper layer. The Y-axis holds the information of remaining, shielded voltage. This is the receiver amplitude we are looking for. By hovering the mouse pointer over one of the 3 lines (light blue, blue, blue with dots), representing 3 different simulated air gaps, you will see the predicted voltages. It is highly recommended to check the curve for maximum air gap, as it is always the lowest amplitude.

The red, yellow and green ranges help you identify if your remaining shielded voltage is sufficient for the IPS chip inputs. It is advised to avoid the red range, which is any value under 5 mV. The yellow range between 5 mV to 8 mV should work for the RAA3/4xxx chip portfolio, but not for the IPS2550. For the latter you need at least 8 mV.

To identify a minimum shield distance, you can check the values throughout the X-axis. In the example, in Figure 2 around 1.5 mm inner layer distance is needed, which can be achieved in a 2 mm overall thickness PCB layer stack.

3.4 PCB Layer Stack (Stack up)

A PCB layer stack creates reference among TOP (VS), INNER1 (L2), INNER2 (L3) and BOTTOM (RS) copper layers, which are colored red in the layer stack below.

The light yellow prepreg thickness between outer and next inner layer is usually ranging from 0.05 mm to 0.5 mm, we often simulate with an average 0.2 mm distance, but if you have a specific stack up, please use its given values. Your simulated coils are placed on the outer layers. In a 4-layer PCB stack, they are either on TOP-INNER1 or INNER2-BOT layers.

The shield layer will be the other, yet unused INNER layer. The distance between INNER1-INNER2 is the so called “coil to shield” distance, that you need to check in Table 1. In other words, which is the core thickness in the layer stack.

In this Wuerth ML-4 FR4 layer stack its value is 2.3 mm. You may round or estimate any values that aren't explicitly mentioned in Table 1.

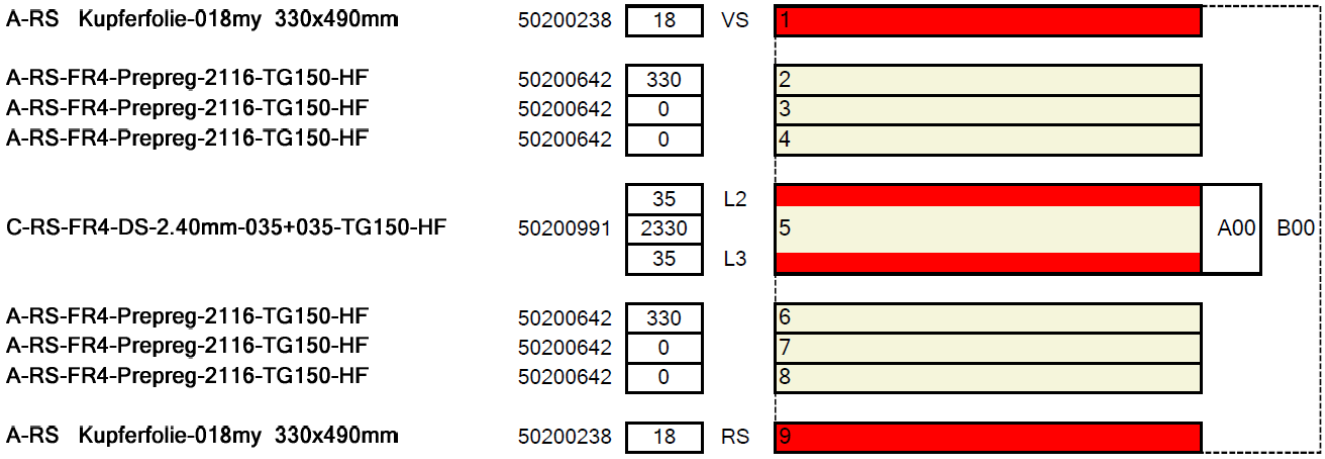

Figure 3. A Typical 3.2 mm Thick 4-Layer Stack, Source: wedirekt.com

4. Best PCB Layout Practices

4.1 Via Type

4.1.1 Through-Hole Via

If enough space is available for all interlayer connections for the inductive sensor coils, the IPS chip, and its passive components, it is advisable to use low-cost through-hole (TH) vias. Typically, designs over 40 mm inner diameter and 60 mm outer diameter are supporting this type of via. This is not a strict rule, even smaller designs might support this goal if the period counts are small (low pole pair count). When choosing between types of vias, it's advisable to check for collisions involving components with the largest footprints, like IPS chips and connectors.

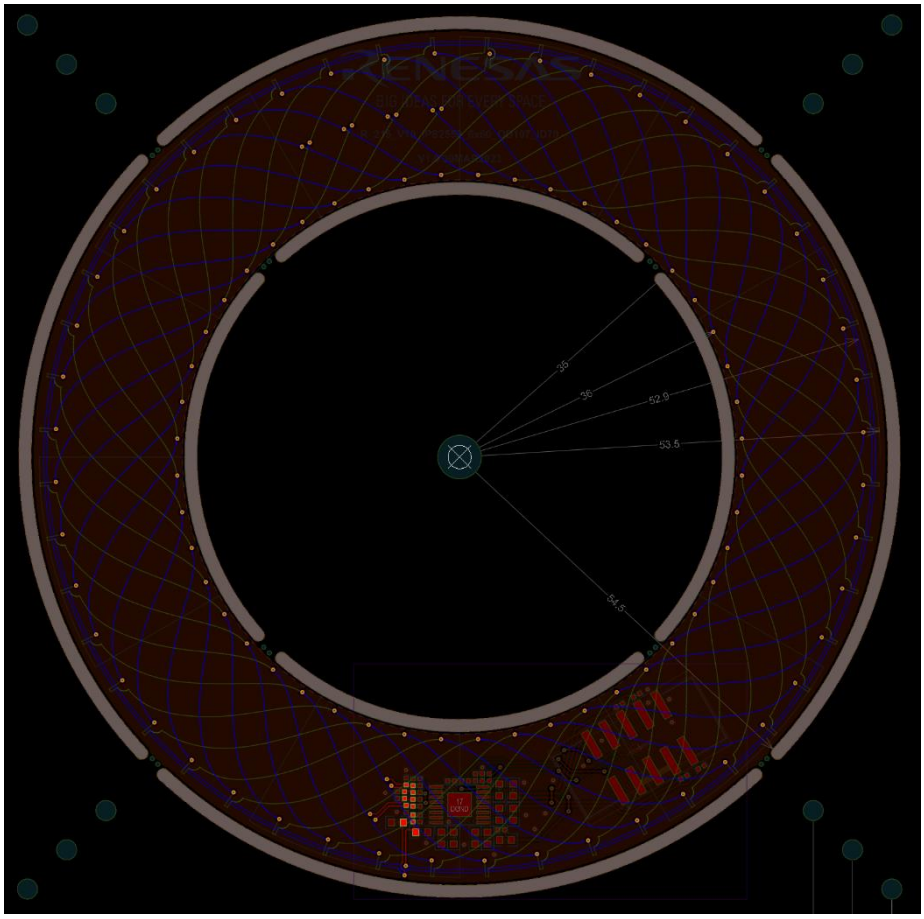

Figure 4. Top View of a PCB Layout with TH-Vias

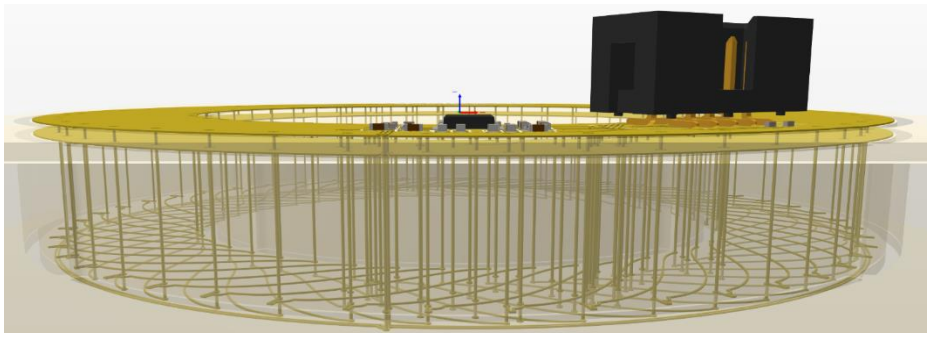

Figure 5. TH-Vias in 3D Side View

4.1.2 Blind Via

When the available layout area is too small (typically less than 50 mm outer diameter), or the inductive coil design is too dense (multiperiod, doubled receiver), incorporating so many vias, the usage of blind vias is inevitable. On the other hand, it makes the layout work much faster and easier. Watch out for via drill size to connecting layer distance, as the aspect ratio should be 1:1. Example: if the TOP-INNER1 or BOT-INNER2 distances are 0.2 mm then the laser drilled via hole size can and should also be 0.2 mm. These vias are not suitable for the limited number of through-hole vias that ultimately connect the coils to the passive components and then to the chip. These vias need to be standard sized, mechanically drilled vias, because their aspect ratio is much more flexible.

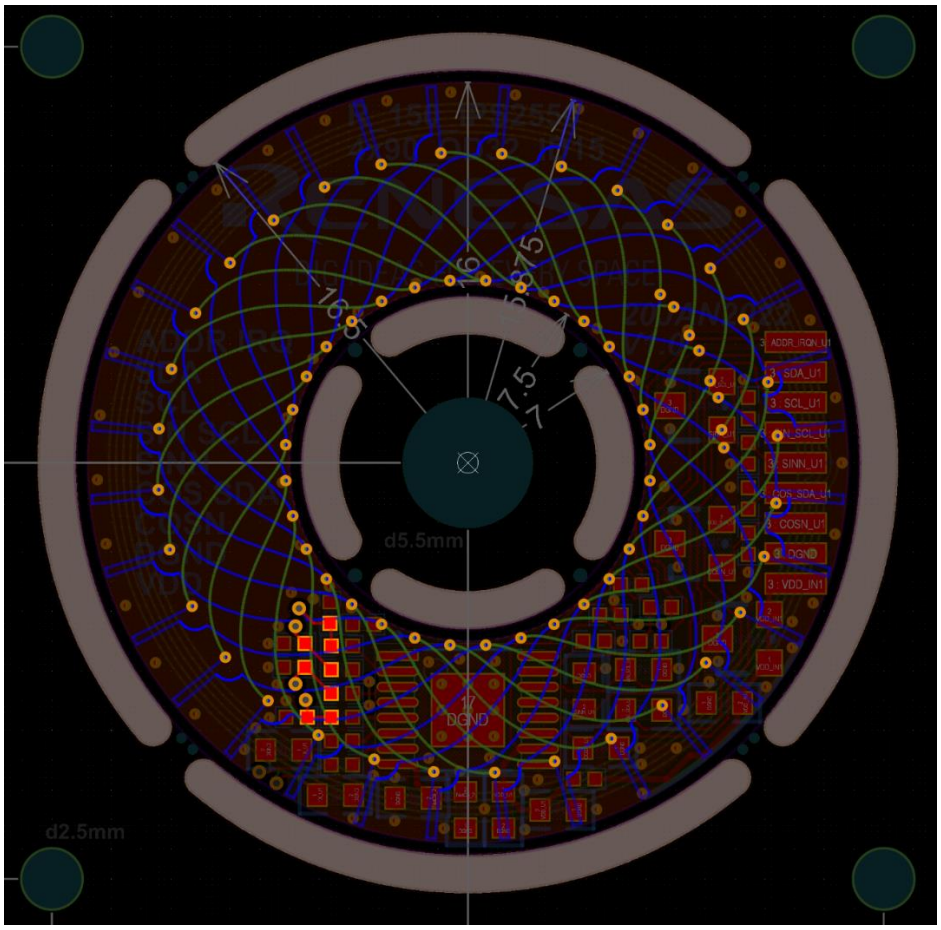

Figure 6. Top View of a PCB Layout with Blind Vias

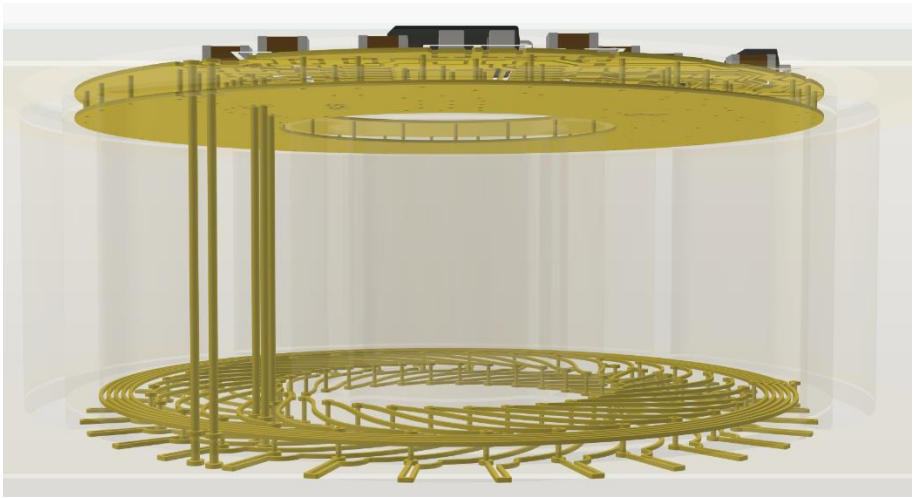

Figure 7. Blind Vias in 3D Side View

4.2 Shield

The shield serves several functions: it ensures a uniform inductive field on the sensing element's side, efficiently blocks the effects of conductive patterns such as footprints, traces, and planes on the component's side, and can act as a ground layer positioned near the chip.

The shield design should cover the entire PCB layout, but at least the area of the sensing element (inductive coil pattern). Small cutouts, such as TH-via holes or short traces that cannot be routed on an outer layer, are permitted. Try to minimize the via groups as well; no more than 2-3 vias next to each other should cut into the shield. If having more routed wires in proximity, try to separate them and let the shield fill out the area around each of them.

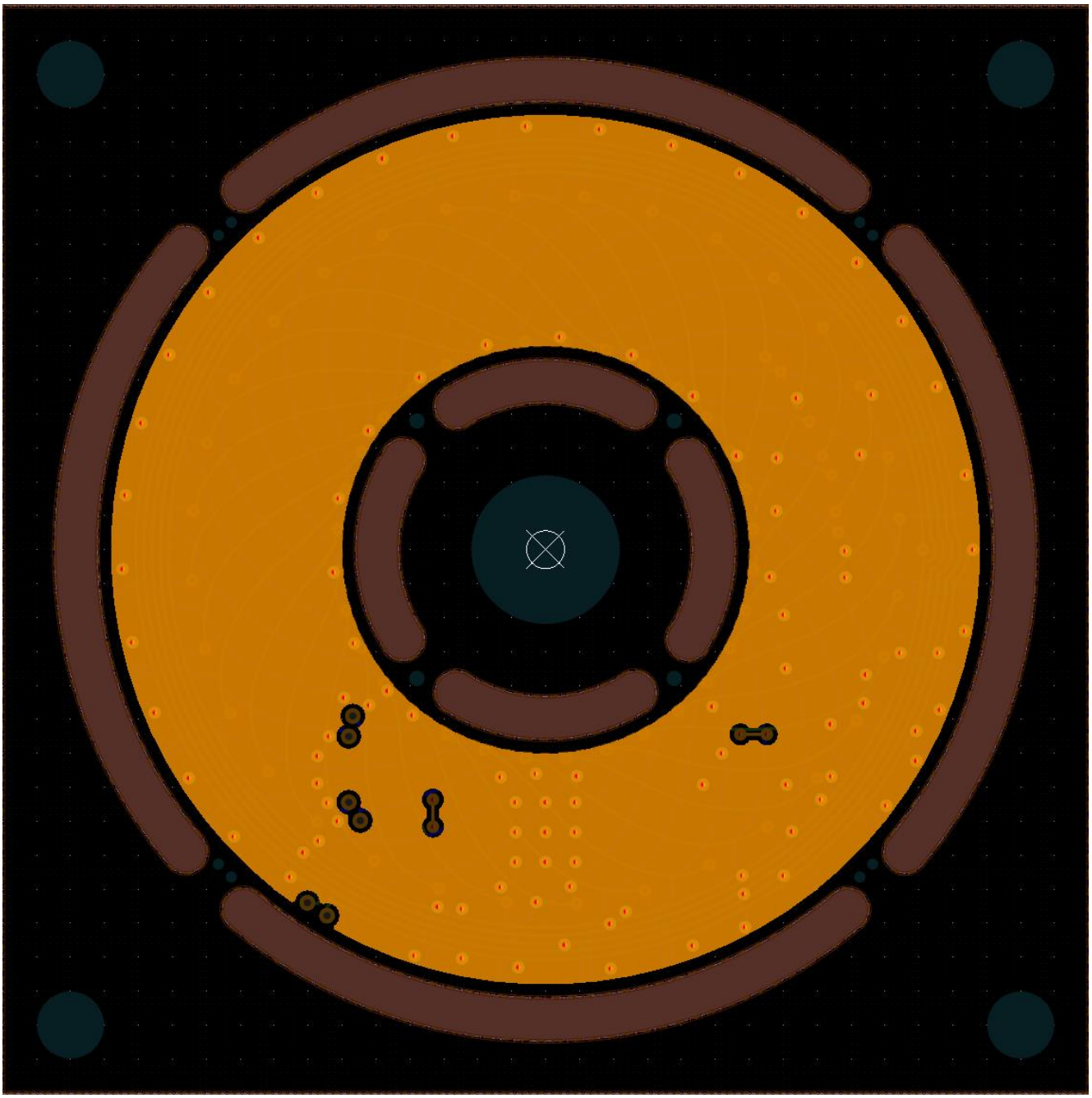

Figure 8. Mostly Blind Vias, Short Cuts in the Shield are Allowed

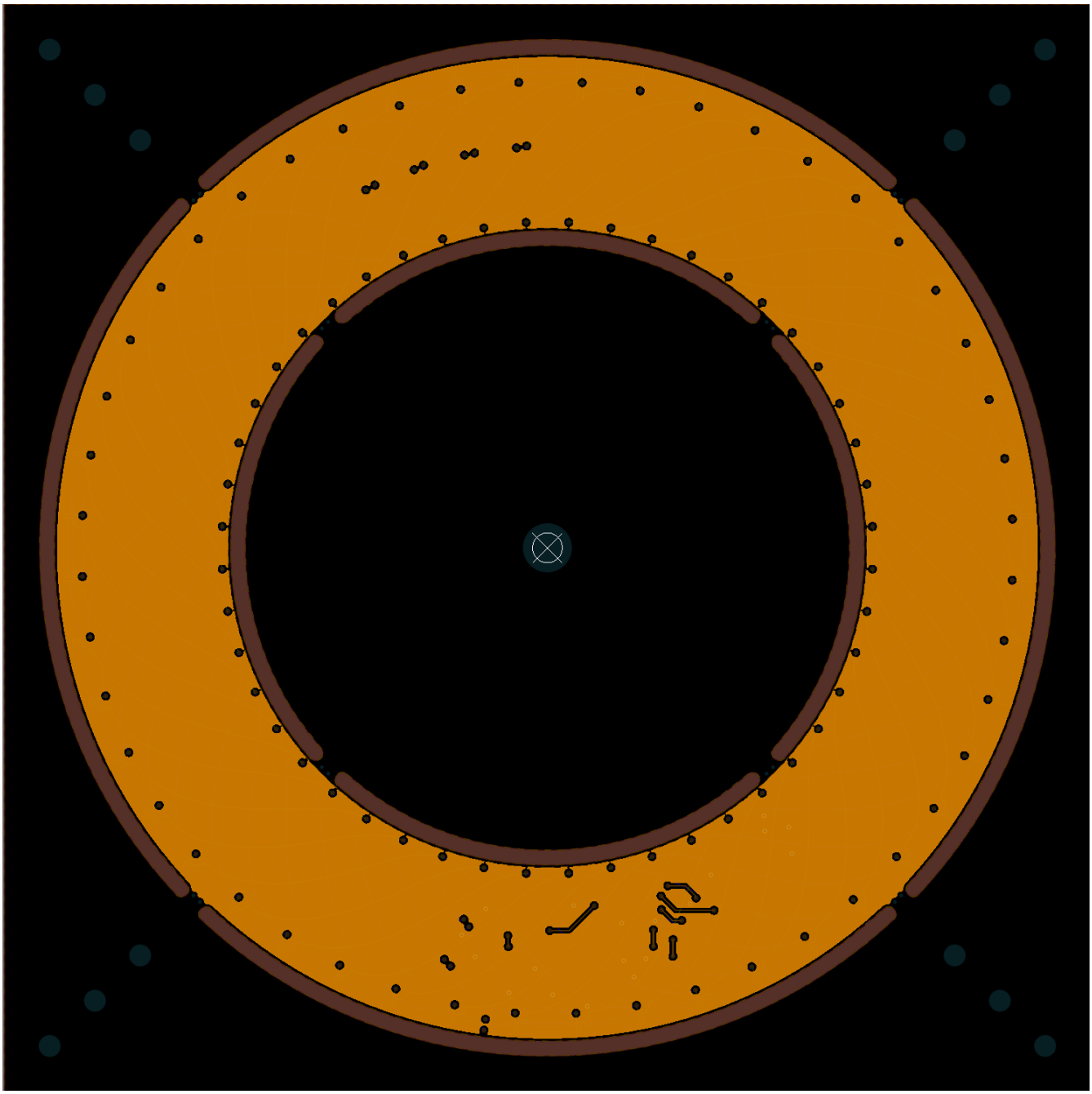

Figure 9. Short, Separated Traces and TH-Via Cuts are Allowed

4.3 Coil Connections

A major benefit of placing the chip and its passives in the sensing element footprint are the short connections from coils to chip. Transmitter and receiver coils are simulated as closed loops, allowing you to open any part of them to form an antenna. If the original design includes any exits, ensure that these are closed before opening the coils at a new location.

Try to keep the traces as short as technically possible. In small designs the passive component pads can be right at the connecting vias. In larger designs, less than 10 mm of parallelly routed traces are always allowed. If you have a feeling, that you would need longer traces, please consider an optimized component placement.

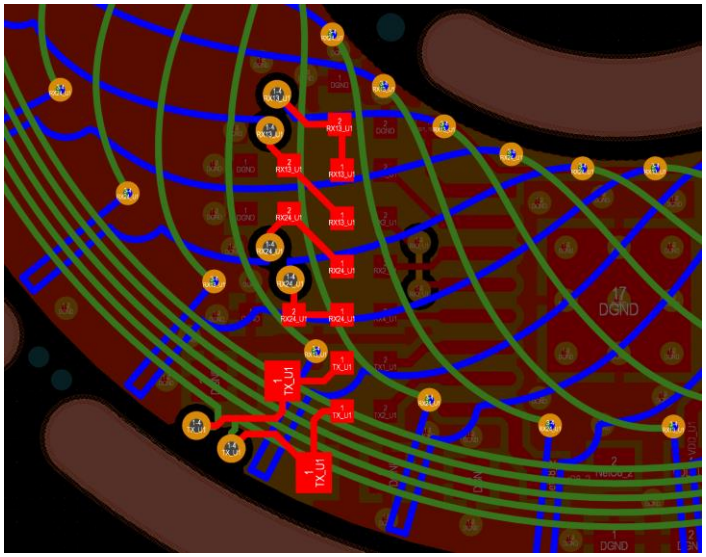

Figure 10. Small Design with Short Connections

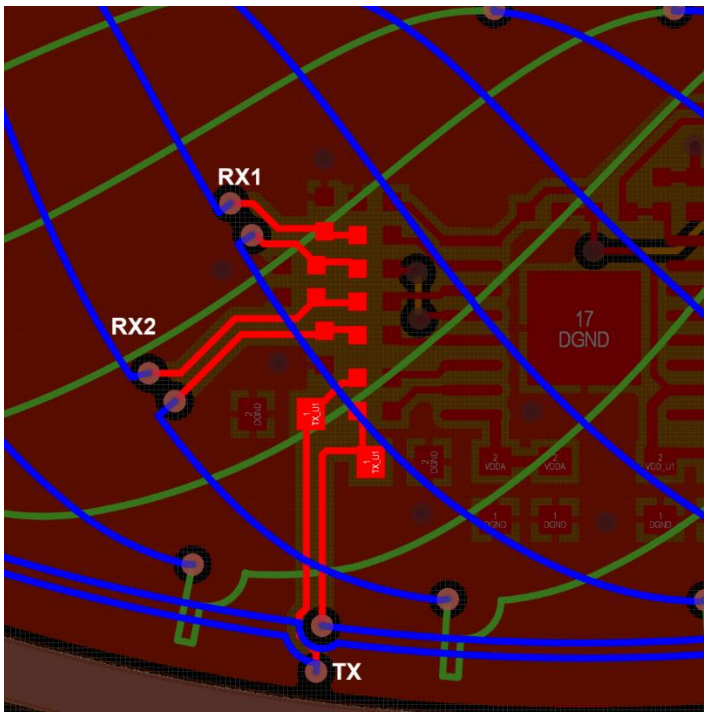

Figure 11. Large Sensor Design with 5 mm Parallel Traces

5. Example Workflow

5.1 IPSCO Coil Design

5.1.1 Input

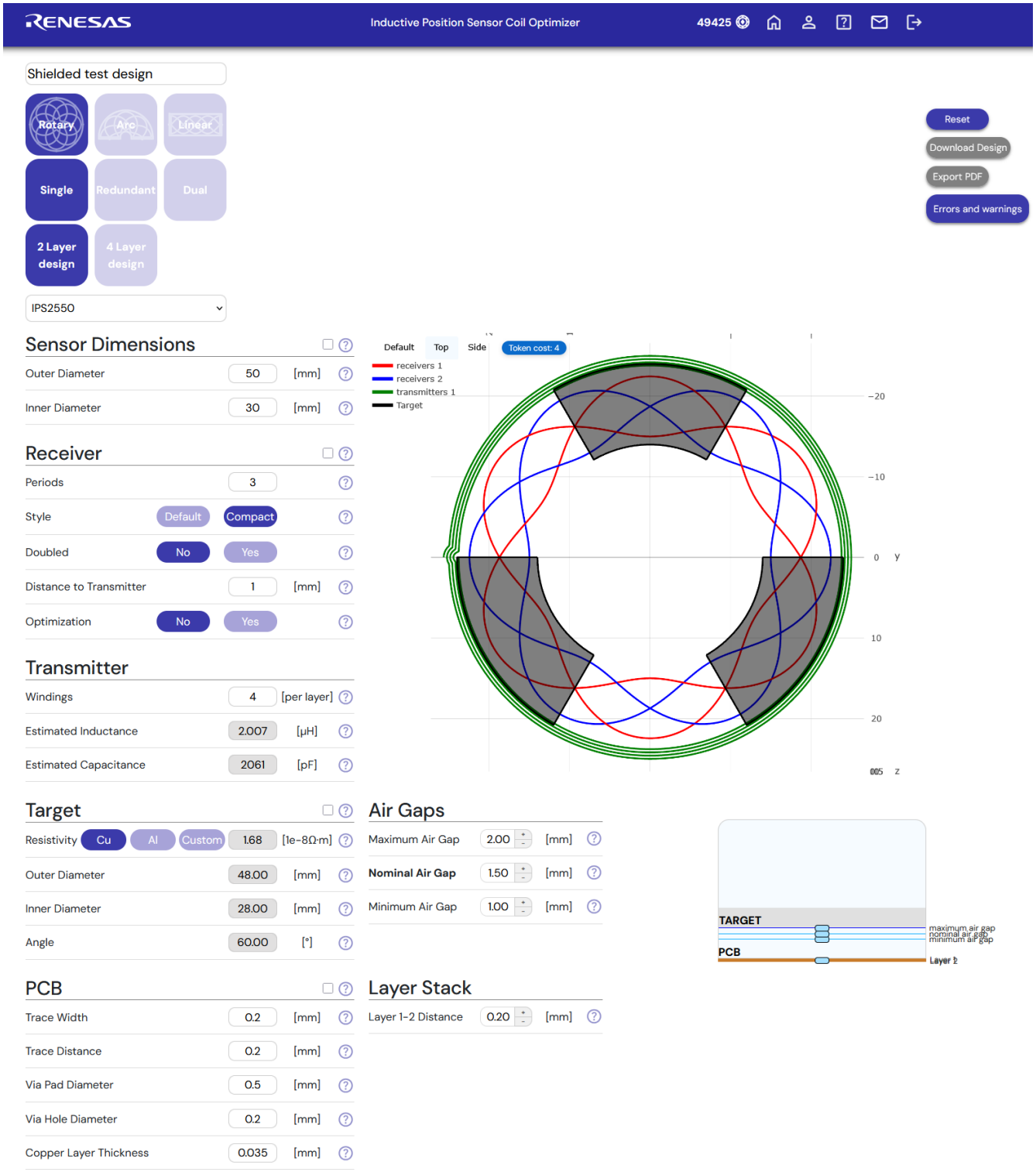

Figure 12. ips.renesas.com IPSCO GUI

5.1.2 Start Simulation

After all inputs are updated, you can start a simulation. To estimate the receiver amplitude at maximum air gap, you can run it without optimization. It is quicker to get the voltage results this way. Note the estimated time and check the result later.

When the simulation is completed, you will receive an email notification (if the box is checked in your user menu) and a red dot notification in the web GUI as well.

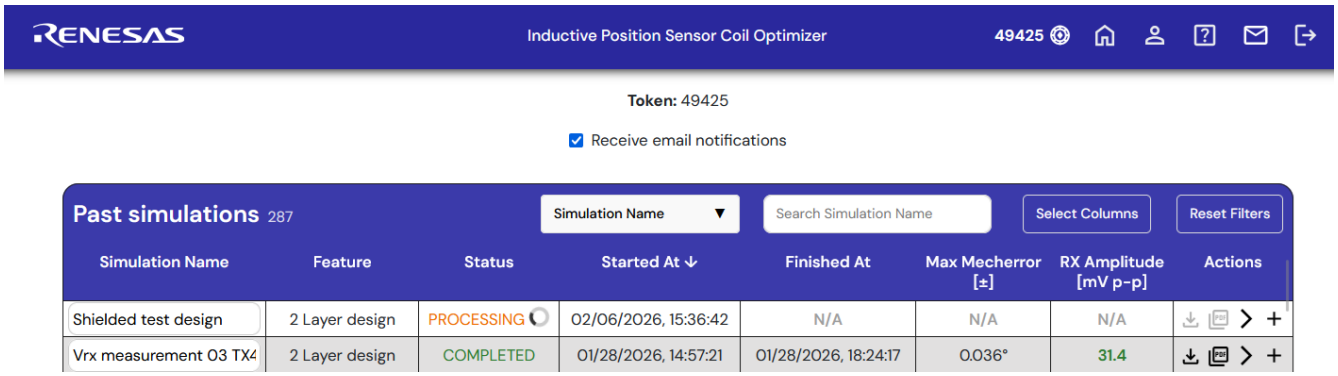

Figure 13. Checking the Status in the User Menu

After the simulation is successfully completed, you can view the results online with the right arrow button.

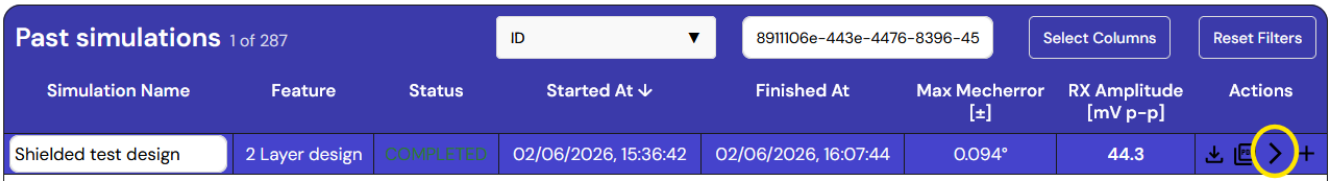

Figure 14. Completed Simulation can be Viewed with the Arrow Button

5.1.3 Simulation Results Interactive Lookup

Look for the RX amplitudes at maximum air gap in the table, and for the interactive remaining voltage chart at the lower end of the page.

RENESAS Inductive Position Sensor Coil Optimizer 49425

Parameter	Minimum airgap	Nominal airgap	Maximum airgap	Unit
Air Gap	1.00	1.50	2.00	mm
		Primary Sensor		
Mechanical Error	0.041	0.094	0.143	±°
RX1 Amplitude	55.51	44.30	35.05	mV
RX2 Amplitude	55.51	44.30	35.05	mV
RX1 Offset	-24.17	-24.17	-24.17	µV
RX2 Offset	-21.66	-21.66	-21.66	µV
TX Inductance	1.67	1.71	1.74	µH
TX Resistance	1.78	1.78	1.78	Ω
TX Capacitance	2475	2413	2372	pF
Quality Factor	27	27	27	

Reset
Download Design
Export PDF
Errors and warnings

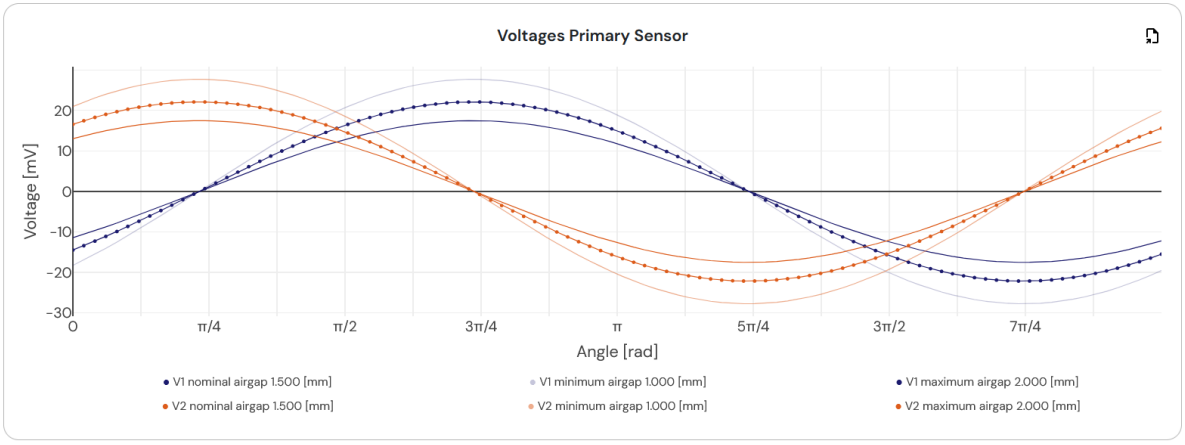

Figure 15. Sensor Simulation Results

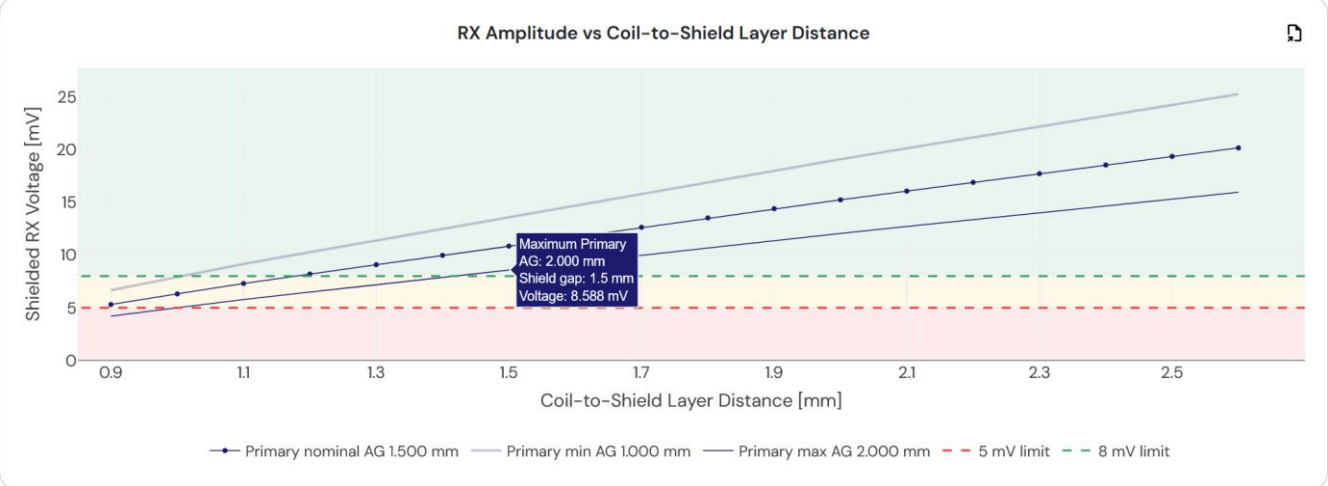

Figure 16. Amplitude at Max Air Gap with Shield

5.2 Remaining RX Voltage Manual Lookup

Always take the receiver amplitude value from your expected maximum air gap, as it is always the lowest and even with shield, the sensor must be operational at maximum air gap. Then take your core distance from the desired PCB layer stack and check Table 1 at the matching parameters.

If you have a high voltage, you might further reduce the core layer thickness, resulting in cheaper PCB production costs.

Table 3. Lookup Table for Shielded RX Voltages

		Simulated VppRX [mV] from IPSCO simulation results page: value taken from maximum air gap																		
		31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
		Remaining VppRX [mV] including the dampening effect of the shield layer																			
Typical “ Coil to Shield layer” distances [mm]	0.9	3.7	3.8	4.0	4.1	4.2	4.3	4.4	4.6	4.7	4.8	4.9	5.0	5.2	5.3	5.4	5.5	5.6	5.8	5.9	6.0
	1.1	5.1	5.3	5.4	5.6	5.8	5.9	6.1	6.3	6.4	6.6	6.8	6.9	7.1	7.3	7.4	7.6	7.8	7.9	8.1	8.3
	1.2	5.7	5.9	6.1	6.3	6.5	6.7	6.8	7.0	7.2	7.4	7.6	7.8	8.0	8.1	8.3	8.5	8.7	8.9	9.1	9.3
	1.5	7.6	7.8	8.1	8.3	8.6	8.8	9.1	9.3	9.6	9.8	10.0	10.3	10.5	10.8	11.0	11.3	11.5	11.8	12.0	12.3
	1.9	10.1	10.4	10.7	11.1	11.4	11.7	12.0	12.4	12.7	13.0	13.3	13.7	14.0	14.3	14.6	15.0	15.3	15.6	15.9	16.3
	2.3	12.4	12.8	13.2	13.6	14.0	14.4	14.8	15.2	15.6	16.0	16.4	16.8	17.2	17.6	18.0	18.4	18.8	19.2	19.6	20.0
	2.6	14.1	14.6	15.0	15.5	15.9	16.4	16.8	17.3	17.7	18.2	18.7	19.1	19.6	20.0	20.5	20.9	21.4	21.8	22.3	22.8

To be in the light green zone, you need to have **at least 1.5 mm** core thickness, which results in an approximate 2 mm overall thickness of the produced PCB. Ideally you should aim for amplitudes over 10 mV for robustness.

5.3 PCB Layout

Without deeper explanation, the next step is to import the fully optimized (another simulation start needed) simulation output Gerber files to your layout software. Feel free to use our guidelines if you work with Altium Designer.

The coil layers should be positioned on the two outermost layers of a 4-layer PCB, oriented directly toward the rotating (moving) target. The next inner layer is the shield, and the last outer layer is the component side.

Finish routing or reuse one of our catalog designs or freely downloadable design templates. Make sure you connect the coils as short as possible.

6. Revision History

Revision	Date	Description
01.00	Mar 11, 2026	Initial release.

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