U2A-EVA, U2A16, U2A8, U2A6 Switching voltage regulator(SVR) guideline

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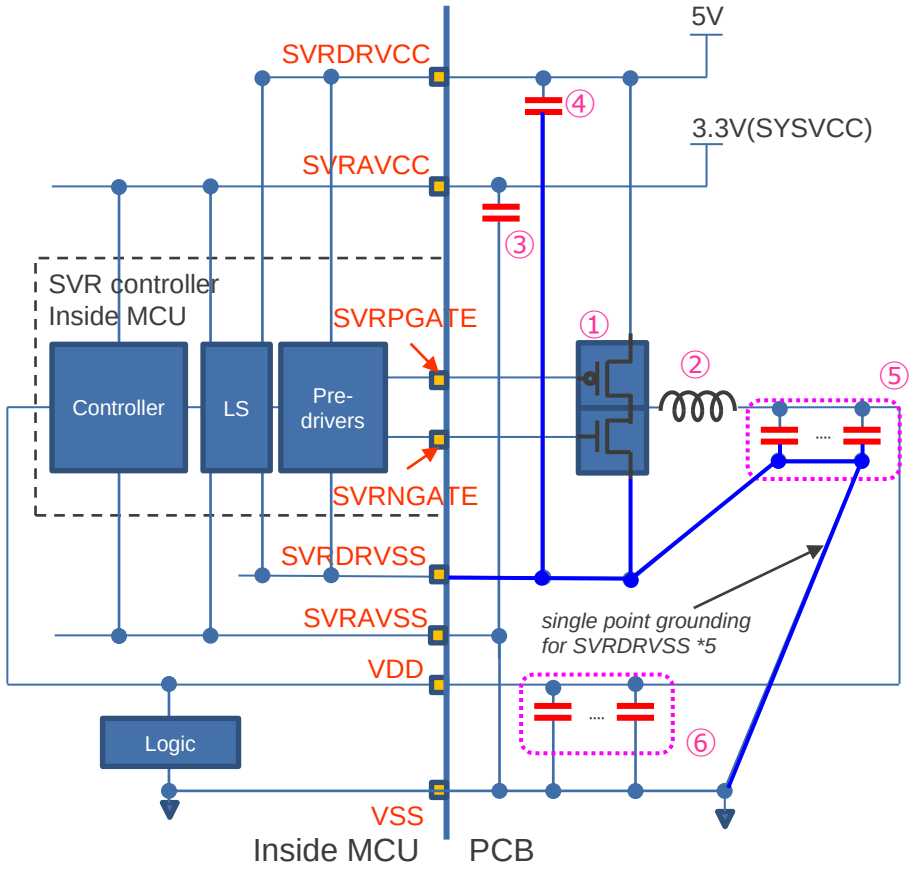
(Rev.5.0-1 October 2020)

U2A-EVA, U2A16, U2A8, U2A6 SVR circuit

Updated on ver1.5

Case1: SVRDRVCC=5V and SYSVCC=VCC=SVRAVCC=3.3V

Comply with the guidelines below in mounting to obtain a VDD within the specified range if you are using a Target MOSFETs as an SVR drivers to handle the VDD power supply. However, the guidelines specifically apply when the SVR is that stated above. Using a different transistor will require separate detailed consideration.



Item	#	Reference value (typ.)	Note	Placement
MOSFET	①	See page 5	Target MOSFETs is shown on the next page.	Close to SVRPGATE and SVRNGATE pin of MCU. Connect Pch MOSFET's source to SVRDRVCC. Connect Nch MOSFET's source to SVRDRVSS.
Inductor	②	See page 6 and 7	Recommend parts is shown on pages 6 and 7. When using other parts, select parts with the same inductance value and close DC resistance(DCR) value as the recommend parts.	Close to MOSFET
Capacitor (between SVRAVCC and SVRAVSS)	③	1uF	Capacitance tolerance: ±10%, Temperature characteristics: X7R, X8R, ESR: <50 mΩ	Close to SVRAVCC and SVRAVSS pin of MCU
Capacitor (between SVRDRVCC and SVRDRVSS)	④	≥ 14uF	Capacitance tolerance: ±10%, Temperature characteristics: X7R, X8R, ESR <10 mΩ (@0.1MHz to 5MHz, total value of parts)	Close to SVRDRVCC and SVRDRVSS pin of MCU
Capacitor (between VDD and SVRDRVSS)	⑤	See page 6 and 7	Capacitance tolerance: ±10%, Temperature characteristics: X7R, X8R, ESR <10 mΩ (@0.1MHz to 5MHz, total value of parts)	Close to Inductor
Capacitor (between VDD and VSS)	⑥	0.1uF x 8	Capacitance tolerance: ±10%, Temperature characteristics: X7R, X8R, ESR: <50 mΩ	Close to thermal ball of MCU (opposite side of MCU of PCB)

CAUTION

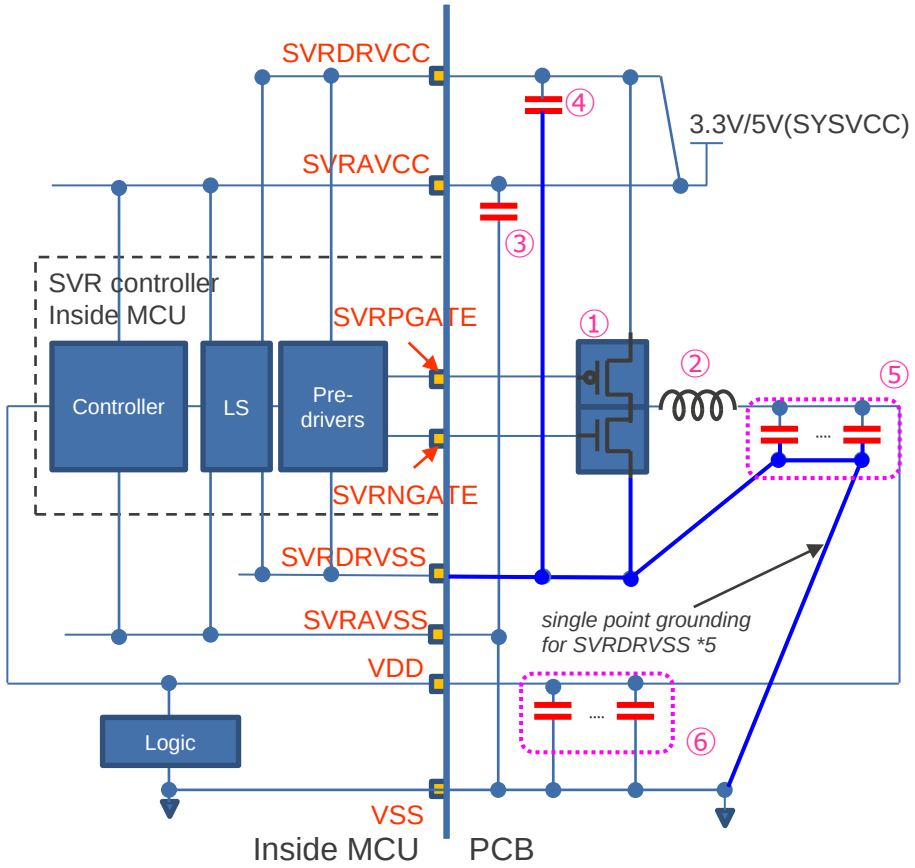
1. Load transient current of VDD (dI) should be kept the specification. Please refer the user's manual.
2. SVRDRVCC and SVRDRVSS should be separated from other power/ground for EMC improving. (e.g. single point grounding)
3. Output resistance and dead time of SVRPGATE and SVRNGATE can be configured by option byte settings. Please refer the user's manual.

U2A-EVA, U2A16, U2A8, U2A6 SVR circuit

Updated on ver1.5

Case2: SVRDRVCC=SYSVCC=VCC=SVRAVCC=3.3V/5V

Comply with the guidelines below in mounting to obtain a VDD within the specified range if you are using a Target MOSFETs as an SVR drivers to handle the VDD power supply. However, the guidelines specifically apply when the SVR is that stated above. Using a different transistor will require separate detailed consideration.



Item	#	Reference value (typ.)	Note	Placement
MOSFET	①	See page 5	Target MOSFETs is shown on the next page.	Close to SVRPGATE and SVRNGATE pin of MCU. Connect Pch MOSFET's source to SVRDRVCC. Connect Nch MOSFET's source to SVRDRVSS.
Inductor	②	See page 6 and 7	Recommend parts is shown on pages 6 and 7. When using other parts, select parts with the same inductance value and close DC resistance(DCR) value as the recommend parts.	Close to MOSFET
Capacitor (between SVRAVCC and SVRAVSS)	③	1uF	Capacitance tolerance: ±10%, Temperature characteristics: X7R, X8R, ESR: <50 mΩ	Close to SVRAVCC and SVRAVSS pin of MCU
Capacitor (between SVRDRVCC and SVRDRVSS)	④	≥ 14uF	Capacitance tolerance: ±10%, Temperature characteristics: X7R, X8R, ESR <10 mΩ (@0.1MHz to 5MHz, total value of parts)	Close to SVRDRVCC and SVRDRVSS pin of MCU
Capacitor (between VDD and SVRDRVSS)	⑤	See page 6 and 7	Capacitance tolerance: ±10%, Temperature characteristics: X7R, X8R, ESR <10 mΩ (@0.1MHz to 5MHz, total value of parts)	Close to Inductor
Capacitor (between VDD and VSS)	⑥	0.1uF x 8	Capacitance tolerance: ±10%, Temperature characteristics: X7R, X8R, ESR: <50 mΩ	Close to thermal ball of MCU (opposite side of MCU of PCB)

CAUTION

1. Load transient current of VDD (dI) should be kept the specification. Please refer the user's manual.
2. SVRDRVCC and SVRDRVSS should be separated from other power/ground for EMC improving. (e.g. single point grounding)
3. Output resistance and dead time of SVRPGATE and SVRNGATE can be configured by option byte settings. Please refer the user's manual.

①MOSFETs

The following table shows the combinations used for evaluation.

Supplier	Nch/Pch		Rdson[mOhm]		Vth[V]	Ciss[pF]	Crss[pF]
			Typ	Max	Max	Typ	Typ
ROHM	Nch	RTR040N03HZGTL	36	50	1.5	475	70
	Pch	RTR030P02HZGTL	60	85	-2.0	840	100

For details of MOSFET, please contact each supplier.

Note:
If prefer using the different transistor other than the above, please choose the transistor as equivalent as the above each specification, and fully evaluate and judge by customer liability.

Updated on ver1.3

②⑤Configuration of Lout and Cout for U2AEVA, U2A16

The following table shows the two combinations（a,b）used for evaluation.

	Value	Recommended parts, Supplier	a	b
Switching frequency (Option byte)	-	-	434kHz	868kHz
②Inductor (Lout)	4.7uH	SPM5030VT-4R7M-D, TDK	✓	N/A
	2.2uH	SPM5030VT-2R2M-D, TDK	N/A	✓
⑤Capacitor (between VDD and VSS) (Cout)	22uF	GCM32ER71A226KE12, Murata	✓	✓
	22uF	GCM32ER71A226KE12, Murata	✓	✓
	22uF	GCM32ER71A226KE12, Murata	✓	✓
	22uF	GCM32ER71A226KE12, Murata	✓	✓
	22uF	GCM32ER71A226KE12, Murata	✓	✓
	22uF	GCM32ER71A226KE12, Murata	✓	N/A
	22uF	GCM32ER71A226KE12, Murata	✓	N/A
	22uF	GCM32ER71A226KE12, Murata	✓	N/A
	Total		176uF	110uF

For details of Inductor and Capacitor, please contact each supplier.

Updated on ver1.5

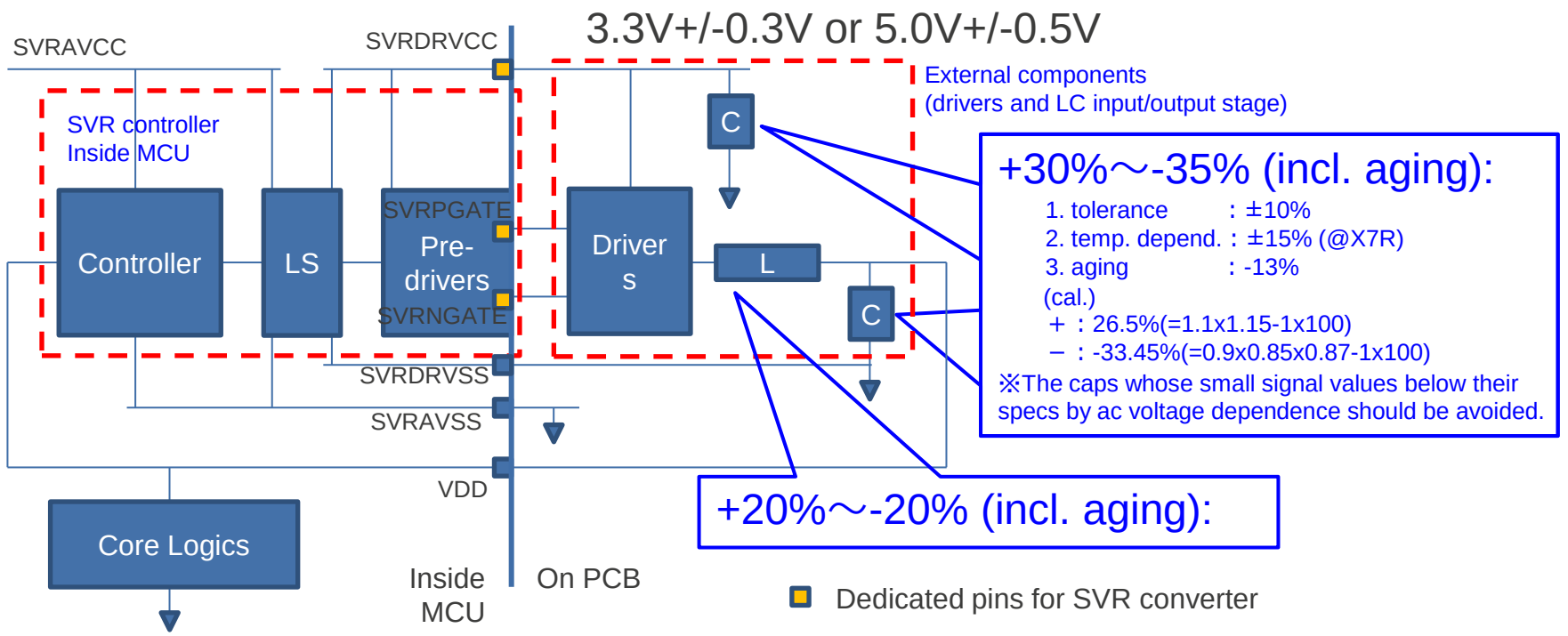
②⑤Configuration of Lout and Cout for U2A8, U2A6

The following table shows the two combinations（a,b）used for evaluation.

	Value	Recommended parts, Supplier	a	b
Switching frequency (Option byte)	-	-	434kHz	868kHz
②Inductor (Lout)	10uH	SPM6545VT-100M-D, TDK	✓	N/A
	4.7uH	SPM5030VT-4R7M-D, TDK	N/A	✓
⑤Capacitor (between VDD and VSS) (Cout)	47uF	GCM32ER70J476ME19, Murata	✓	✓
	47uF	GCM32ER70J476ME19, Murata	✓	N/A
	Total		94uF	47uF

For details of Inductor and Capacitor, please contact each supplier.

L,C variations acceptable for SVR



Option byte settings for U2A-EVA [1/3]

Table 1: Option byte settings are fixed values for each configurations (SVRDRVCC, Fsw, Cout, Lout).
Table 2:

- Basically, set SVRAJPRDSR [3:0] with 4'b1111. However, adjustment for EMC noise reduction is possible. When adjusting, efficiency will worse, so please consider the trade-off between efficiency and noise reduction.
- Adjusting SVRAJDTP [2:0] and SVRAJDTN [2:0] to match the MOSFET can optimize efficiency.
  Please refer to the following page.

Table1 Option byte for PID, internal ADC and output pulse width setting

Configurations				Option byte setting								
SVRDRVCC [V]	Fsw [MHz]	Cout [uF]	Lout [uH]	SVRFSWMODE[1:0]	SVRKPVSCL[13:0]	SVRKIVSCL[13:0]	SVRKDVSCL[13:0]	SVRADNSMP[7:0]	SVRADTHRESH[7:0]	SVRADTHRESHE[7:0]	SVRMINSKIPDUTY[1:0]	SVRMAXDUTY[7:0]
5	0.434	176	4.7	2'b00	14'b00001110000101	14'b00010010111000	14'b00001111101100	8'b00010010	8'b01111101	8'b11111001	2'b11	8'b11111100
5	0.868	110	2.2	2'b01	14'b00010000011111	14'b00010110000110	14'b00010010010111	8'b00010010	8'b01111101	8'b01111001	2'b11	8'b01111100
3.3	0.434	176	4.7	2'b00	14'b00010101100001	14'b00011100110110	14'b00010111111110	8'b00010010	8'b01111101	8'b11111001	2'b11	8'b11111100
3.3	0.868	110	2.2	2'b01	14'b00011001001100	14'b00100001110001	14'b00011100000011	8'b00010010	8'b01111101	8'b01111001	2'b11	8'b01111100

Table2 Option byte for gate driver

Option byte setting		
SVRAJPRDSR[3:0]	SVRAJDTP[2:0]	SVRAJDTN[2:0]
4'b1111	3'b111	3'b111

Option byte settings for U2A16 [2/3]

Table 1: Option byte settings are fixed values for each configurations (SVRDRVCC, Fsw, Cout, Lout).
Table 2:

- Basically, set SVRAJPRDSR [3:0] with 4'b1111. However, adjustment for EMC noise reduction is possible. When adjusting, efficiency will worse, so please consider the trade-off between efficiency and noise reduction.
- Adjusting SVRAJDTP [2:0] and SVRAJDTN [2:0] to match the MOSFET can optimize efficiency.
  Please refer to the following page.

Table1 Option byte for PID, internal ADC and output pulse width setting

Configurations				Option byte setting								
SVRDRVCC [V]	Fsw [MHz]	Cout [uF]	Lout [uH]	SVRFSWMODE[1:0]	SVRKPVSCL[13:0]	SVRKIVSCL[13:0]	SVRKDVSCL[13:0]	SVRADNSMP[7:0]	SVRADTHRESH[7:0]	SVRADTHRESHE[7:0]	SVRMINSKIPDUTY[1:0]	SVRMAXDUTY[7:0]
5	0.434	176	4.7	2'b00	14'b00001110000101	14'b00010010111000	14'b00001111101100	8'b00010000	8'b10101010	8'b11111001	2'b11	8'b11111100
5	0.868	110	2.2	2'b01	14'b00010000011111	14'b00010110000110	14'b00010010010111	8'b00010000	8'b00101010	8'b01111001	2'b11	8'b01111100
3.3	0.434	176	4.7	2'b00	14'b00010101100001	14'b00011100110110	14'b00010111111110	8'b00010000	8'b10101010	8'b11111001	2'b11	8'b11111100
3.3	0.868	110	2.2	2'b01	14'b00011001001100	14'b00100001110001	14'b00011100000011	8'b00010000	8'b00101010	8'b01111001	2'b11	8'b01111100

Table2 Option byte for gate driver

Option byte setting		
SVRAJPRDSR[3:0]	SVRAJDTP[2:0]	SVRAJDTN[2:0]
4'b1111	3'b111	3'b111

Updated on ver1.5

Option byte settings for U2A8, U2A6 [2/3]

Table 1: Option byte settings are fixed values for each configurations (SVRDRVCC, Fsw, Cout, Lout).
Table 2:

- Basically, set SVRAJPRDSR [3:0] with 4'b1111. However, adjustment for EMC noise reduction is possible. When adjusting, efficiency will worse, so please consider the trade-off between efficiency and noise reduction.
- Adjusting SVRAJDTP [2:0] and SVRAJDTN [2:0] to match the MOSFET can optimize efficiency.
  Please refer to the following page.

Table1 Option byte for PID, internal ADC and output pulse width setting

Configurations				Option byte setting								
SVRDRVCC [V]	Fsw [MHz]	Cout [uF]	Lout [uH]	SVRFSWMODE[1:0]	SVRKPVSCL[13:0]	SVRKIVSCL[13:0]	SVRKDVSCL[13:0]	SVRADNSMP[7:0]	SVRADTHRESH[7:0]	SVRADTHRESHE[7:0]	SVRMINSKIPDUTY[1:0]	SVRMAXDUTY[7:0]
5	0.434	94	10	2'b00	14'b00011001000001	14'b00101001111010	14'b00010110010010	8'b00010000	8'b10101010	8'b11111001	2'b11	8'b11111100
5	0.868	47	4.7	2'b01	14'b00010100000010	14'b00011110111111	14'b00010011010101	8'b00010000	8'b00101010	8'b01111001	2'b11	8'b01111100
3.3	0.434	94	10	2'b00	14'b00100110001110	14'b01000000000010	14'b00100010000011	8'b00010000	8'b10101010	8'b11111001	2'b11	8'b11111100
3.3	0.868	47	4.7	2'b01	14'b00011110100111	14'b00101111010110	14'b00011101100011	8'b00010000	8'b00101010	8'b01111001	2'b11	8'b01111100

Table2 Option byte for gate driver

Option byte setting		
SVRAJPRDSR[3:0]	SVRAJDTP[2:0]	SVRAJDTN[2:0]
4'b1111	3'b111	3'b111

Option byte settings [3/3]

In order to avoid excessive current, the switching timing of MOSFETs should be controlled to have non-overlap time between the on-times of Hi-side(PMOS) and Lo-side(NMOS). So dead time should be set to satisfy the following relations.

Dead time of Hi-side:OFF->Lo-side:ON min > PMOS Turn off time max

Dead time of Lo-side:OFF->Hi-side:ON min > NMOS Turn off time max

Regarding the turn off time of MOSFETs, could you please get their information from the MOSFETs supplier you choose.

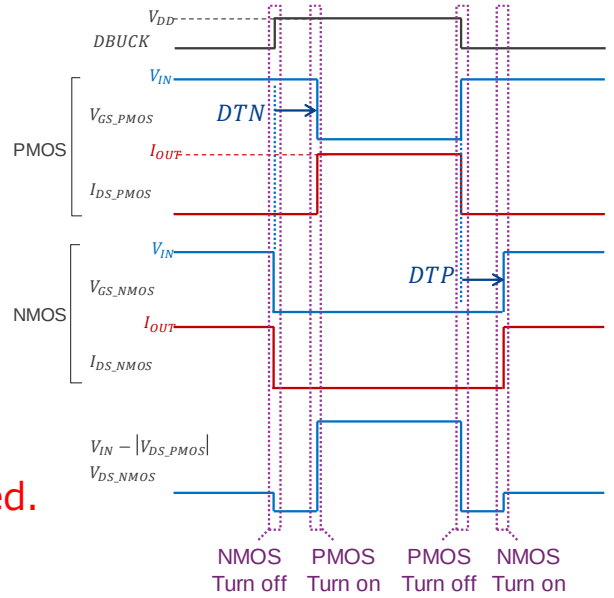
Note: The values in the following tables are simulation results and are not guaranteed.

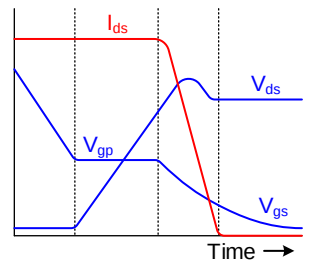
#	Pin conditions SVRAJPRDSR[3:0] [3:2] for SVRNGATE [1:0] for SVRPGATE	Output resistance [ohm] VCC=3.0～3.3～3.6[V] PMOS (pull-up) Min	Typ	Max	NMOS (pull-down) Min	Typ	Max	VCC=4.5～5.0～5.5[V] PMOS (pull-up) Min	Typ	Max	NMOS (pull-down) Min	Typ	Max	Descriptions
1	4'b1111	10.4	15.1	26.3	9.9	15.0	26.5	8.4	11.5	19.2	8.5	12.5	21.2	
2	4'b1010	13.5	19.8	34.9	12.8	19.5	35.3	10.8	15.0	25.3	10.7	15.8	27.5	@Vds=0.2V
3	4'b0101	19.3	28.6	51.0	18.3	28.4	51.4	15.3	21.5	36.7	15.5	23.3	40.8	
4	4'b0000	25.4	37.9	68.2	24.1	37.5	69.0	20.0	28.4	48.9	19.9	29.9	53.3	
1	4'b1111	12.4	18.1	31.6	11.5	17.4	30.9	-	-	-	-	-	-	
2	4'b1010	16.3	23.9	42.0	15.4	23.5	42.4	-	-	-	-	-	-	@Vds=1.0V
3	4'b0101	23.5	34.8	61.6	21.7	33.4	60.3	-	-	-	-	-	-	
4	4'b0000	31.2	46.4	82.5	29.5	45.7	83.4	-	-	-	-	-	-	
1	4'b1111	-	-	-	-	-	-	11.8	16.4	27.3	11.1	16.3	28.1	
2	4'b1010	-	-	-	-	-	-	15.5	21.6	36.3	15.1	22.1	38.8	@Vds=2.5V
3	4'b0101	-	-	-	-	-	-	22.4	31.5	53.2	21.0	31.2	54.7	
4	4'b0000	-	-	-	-	-	-	29.7	42.0	71.2	29.0	43.0	76.2	

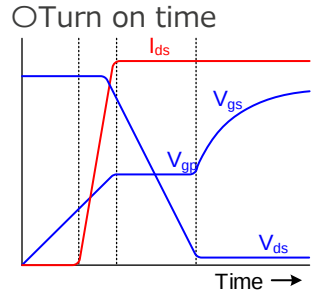
#	Pin conditions SVRAJDTP[2:0]	Dead time of Hi-side:OFF->Lo-side:ON_P [ns] VCC=3.0～3.3～3.6[V] Min	Typ	Max	VCC=4.5～5.0～5.5[V] Min	Typ	Max
1	3'b000	18	26	39	17	25	36
2	3'b001	41	53	71	41	52	68
3	3'b010	65	80	103	64	79	99
4	3'b011	88	107	135	88	106	131
5	3'b100	112	134	166	111	133	163
6	3'b101	135	161	198	135	160	195
7	3'b110	159	188	230	158	187	227
8	3'b111	182	215	262	182	214	258

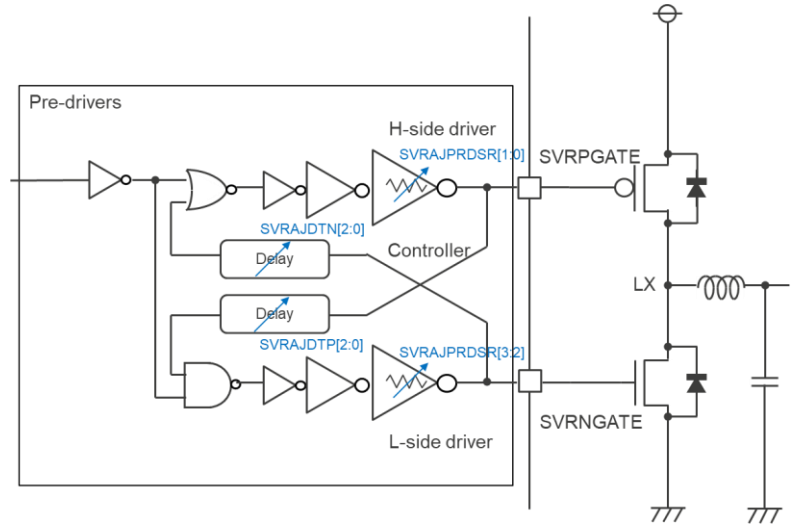
#	Pin conditions SVRAJDTN[2:0]	Dead time of Lo-side:OFF->Hi-side:ON [ns] VCC=3.0～3.3～3.6[V] Min	Typ	Max	VCC=4.5～5.0～5.5[V] Min	Typ	Max
1	3'b000	18	26	39	17	25	36
2	3'b001	41	53	70	41	52	68
3	3'b010	65	80	102	64	79	99
4	3'b011	88	107	134	88	106	131
5	3'b100	112	134	166	111	133	163
6	3'b101	135	161	197	134	160	195
7	3'b110	159	188	229	158	187	227
8	3'b111	182	215	261	181	214	258

: Default code





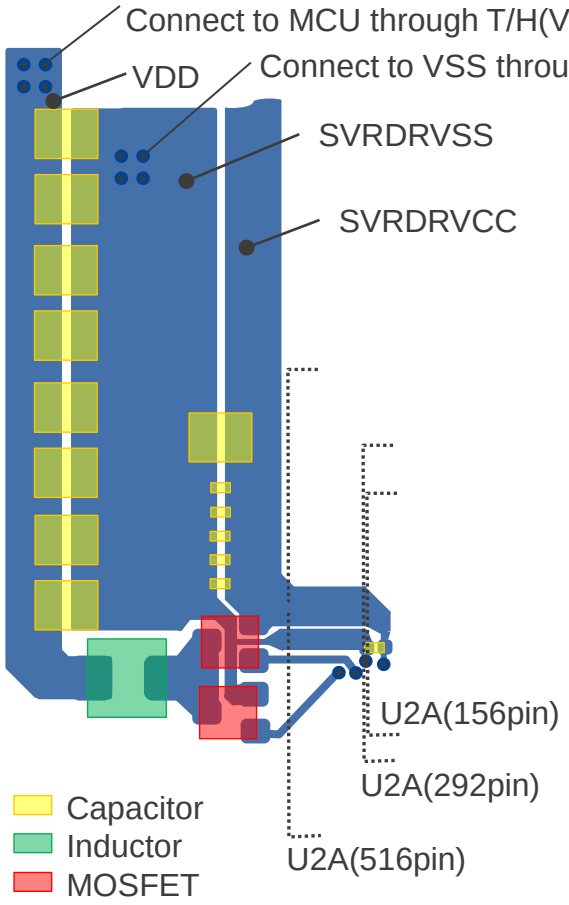




PCB layout guideline [1/3]
for BGA package

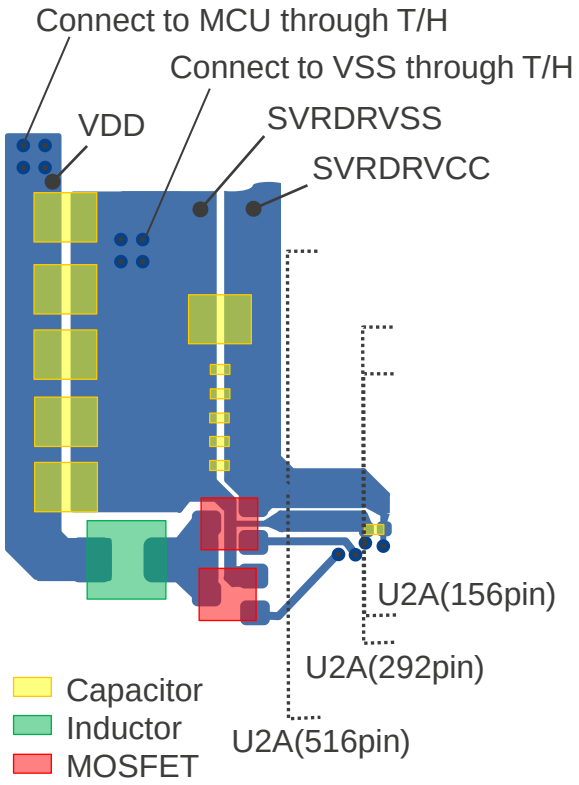
Updated on ver1.5

Example of PCB layout



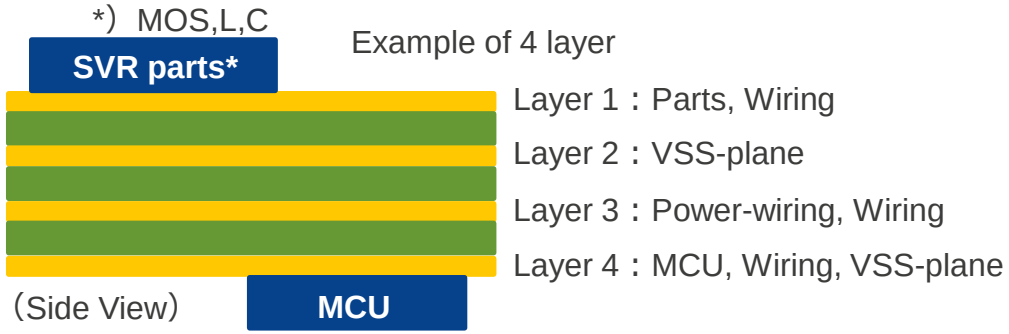
fsw*=434kHz

（Top View）



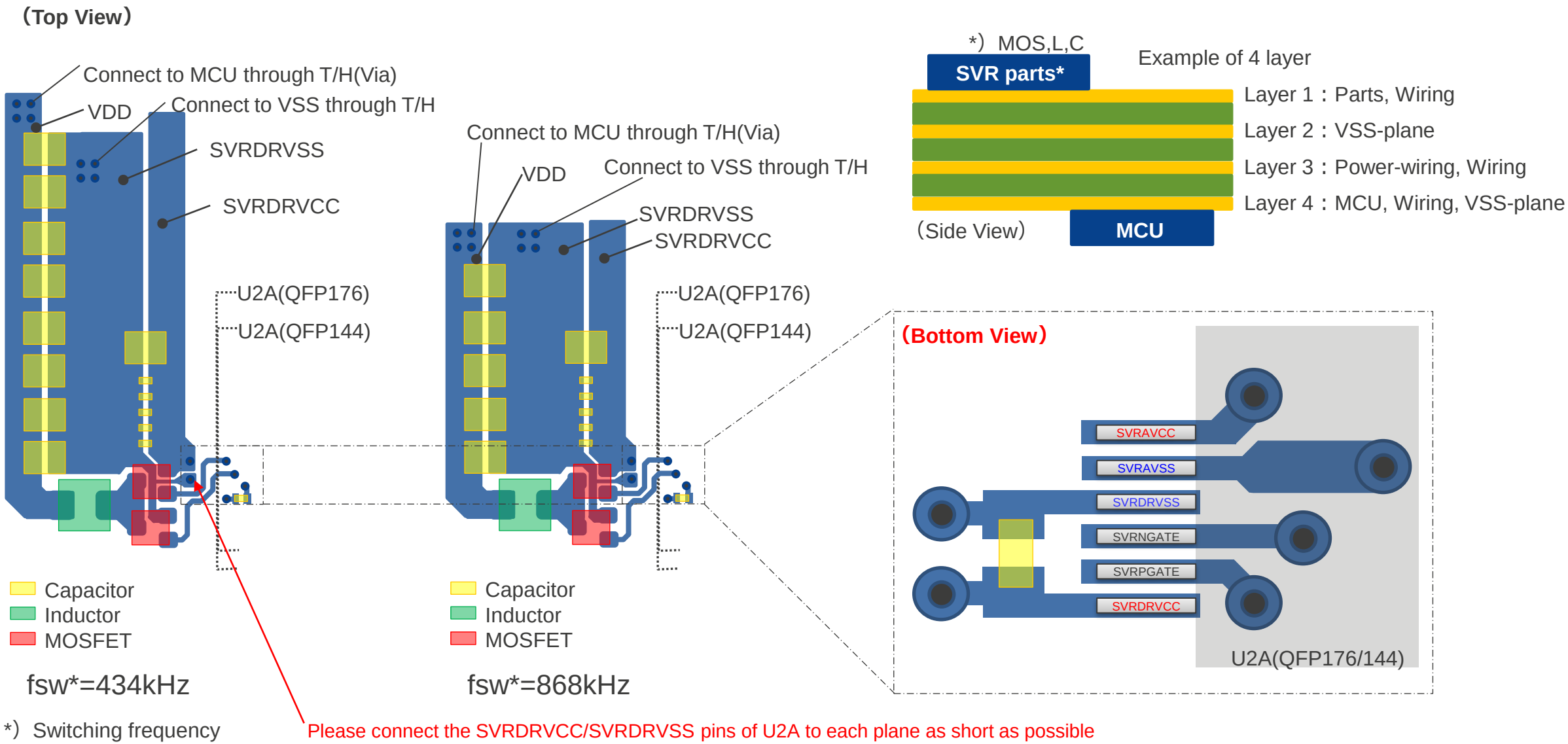
fsw*=868kHz

*） Switching frequency



PCB layout guideline [2/3]
for QFP package

Added on ver1.5



*) Switching frequency

Please connect the SVRDRVCC/SVRDRVSS pins of U2A to each plane as short as possible

PCB layout guideline [3/3]

Recommended PCB design rule:

1) The part (C, MOS, L) of SVRDRVCC and the part (C) of VDD are arranged in the same layer (Layer 1). The distance between MOS and L, L and VDD-C should be within 3 mm each.
2) The VSS plane is arranged in the layer adjacent to the SVR part area (Layer 2) of Layer 1.
3) The MCU may be mounted on the same surface (Layer 1) as the component of the SVR.
4) Power supplies (including SVRAVCC) other than SVRDRVCC and VDD should be placed in the layer (Layer 3) between the VSS plane layer (Layer 2) and Layer 4.
5) In the case of a six-layer board, add two layers between Layer 3 (power supply wiring layer) and Layer 4. (eg Layer 3 = power supply, wiring, Layer 4 = VSS)
6) The pattern width of SVRDRVCC and VDD is 3 mm or more. The number of vias is 4 or more @ Φ0.6 mm (8 or more @ Φ0.3 mm).
7) Wiring the pattern width of SVRDRVSS at 1 mm or more. When the pattern width is less than 1 mm, it may be combined with the adjacent layer (eg Layer 1 = 0.5 mm, Layer 2 = 0.5 mm).
8) SVRDRVSS should be connected to VSS through via(4 or more @Φ0.6mm) of SVRDRVSS in the vicinity of C located far from L.
9) C between SVRDRVCC and SVRDRVSS is located close to the MCU from the small capacity C.
10) C of SVRAVCC and SVRAVSS are placed closest to MCU. SVRAVCC is connected to SYSVCC and VCC. SVRAVSS is connected to VSS.
11) SVRPGATE / N wiring, MOS, L, SVRDRVCC, SVRDRVSS should not run in the same layer / adjacent layer as analogue high-sensitivity wiring.

1)2)4)5)11) To prevent SVR noise from diffusing to other power supplies, analog wiring, etc.
3) When SVR components can be arranged from the MCU without using vias, MCU and SVR components may be the same layer. On the other hand, if it can not be arranged, the MCU and the SVR part are separate layers only.
6)7)8) The pattern width and the number of vias consider the current amount.
Estimated pattern width is 1 mm / 1A. As a measure of the number of vias, Φ 0.25 mm: 0.8 A / piece, Φ 0.5 mm: 1.6 A / piece, Φ 1 mm: 3.2 A / piece.
6)8) Noise of SVR is superimposed on SVRDRVSS. In order not to diffuse noise to VSS, noise is reduced with via (1.5 nH or less) and then connected to VSS.
9)10) A ceramic capacitor having a small capacitance value has a high self-resonant frequency. That is, high frequency noise suppression effect is high.
In order to maximize this effect, a ceramic capacitor is placed close to the MCU (reduces parasitic inductance of the wiring).

Added on ver1.6

Recommended settings of PWRGD_CNT

Following table shows the recommended wait time settings of PWRGD_CNT for returning from DeepSTOP when using SVR.

Configurations					Settings	
Product	SVRDRVCC [V]	Fsw [MHz]	Cout [µF]	Lout [µH]	Minimum Wait Time [µs]	PWRGD_CNT [11:0]
U2A-EVA	5	0.434	176	4.7	1140	$12D_H$
		0.868	110	2.2	1430	$17A_H$
	3.3	0.434	176	4.7	1580	$1A2_H$
		0.868	110	2.2	1900	$1F6_H$
U2A16	5	0.434	176	4.7	1130	$12B_H$
		0.868	110	2.2	1130	$12B_H$
	3.3	0.434	176	4.7	1580	$1A2_H$
		0.868	110	2.2	1580	$1A2_H$
U2A8, U2A6	5	0.434	94	10	1130	$12B_H$
		0.868	47	4.7	1120	128_H
	3.3	0.434	94	10	1590	$1A4_H$
		0.868	47	4.7	1580	$1A2_H$

Revision History [1/2]

Revision	Page	Items	Date
1.0	-	New Release	February 15, 2019
1.1	5	- Added the note. - Added the Crss value of MOSFETs as a reference. - Corrected the condition of Ciss from “Max” to “Typ”.	June 28, 2019
	9	- Updated values in tables. - Added the note.	
1.2	-	- Corrected the pin name from “DCDC_P” to ”SVRPGATE” and from “DCDC_N” to ”SVRNGATE”. - Minor updated tables and block diagrams.	September 17, 2019
	9	- Added the Option byte settings for U2A16.	
1.3	3, 4, 6	- Clarified applicable products	December 1, 2020
	7	- Added the Lout and Cout settings for U2A8.	
	11	- Added the Option byte settings for U2A8.	

Revision History [2/2]

Revision	Page	Items	Date
1.4	3, 4	- Revised note for inductor	June 16, 2021
1.5	3, 4, 7, 11	- Clarified applicable products	June 30, 2022
	13, 14	- Clarified applicable packages	
1.6	16	- Added the recommended settings of PWRGD_CNT	May 30, 2023

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