V850E/Ix3 Group, RX24T Group

V850E/Ix3 to RX24T Migration Guide

Introduction

This application note describes key points to consider when migrating from the V850E/Ix3 Group to the RX24T Group, as well as points of difference between the two groups. For detailed information on the various functions, refer to the latest User's Manual: Hardware of each product.

The descriptions in this document use the specifications of the μPD70F3454 (V850E/IG3) as representative of the V850E/Ix3 Group. Other products in the V850E/Ix3 Group have somewhat different specifications for memory capacity, etc., but their functions are equivalent to those of the μPD70F3454. Therefore this document applies to them as well. In addition, the specifications of the R5F524TA(Chip version A) are used as representative of the RX24T Group.

Note that the RX24T Group supports use of a variety of drivers and middleware (Firmware Integration Technology) and the driver generator tool (included with Smart Configurator), which helps to reduce the software development burden.

Contents

1. Overview

1.1 Product Lineup

Table 1.1 lists the product lineup (code sizes and pin counts) of the V850E/Ix3 (x = F and G) Group and RX24T Group.

Table 1.1 Code Sizes and Pin Counts of V850E/Ix3 Group and RX24T Group Products

V850E/Ix3 (x = F and G)		RX24T	
Code Flash/RAM	**Pin Count**	**Code Flash/RAM**	**Pin Count**
128 KB/8 KB	80 or 100 pins	128 KB/16 KB	64, 80, or 100 pins
256 KB/12 KB	80, 100, or 161 pins	256 KB/16 KB	64, 80, or 100 pins
—	—	256 KB/32 KB	100 pins
—	—	384 KB/32 KB	100 pins
—	—	512 KB/32 KB	100 pins

1.2 Substitutable and Non-substitutable Functions

Table 1.2 lists which functions of the V850E/Ix3 Group are substitutable with functions on the RX24T Group and which functions are not substitutable.

Table 1.2 Substitutable and Non-substitutable Functions

Function on V850E/Ix3	Substitutable on RX24T	Page with Details
Port functions	Yes	P. 8
Clock generator	Yes	P. 9
Timer functions (TAA, TAB, and TMT)	Can be implemented using the MTU3d. However, some functionality requires utilization of CPU interrupts.	P. 11
16-bit interval timer M (TMM)	Can be implemented using the CMT.	P. 13
Motor control functions	Can be implemented using the MTU3d.	P. 14
Watchdog timer functions	Can be implemented using the IWDTa.	P. 15
A/D converters 0, 1, and 2	Can be implemented using the S12ADF. However, conversion channel specification mode are not supported.	P. 16
Asynchronous serial interfaces A and B (UARTA and UARTB)	Can be implemented using the SCIg. However, FIFO transmission and reception are not implemented in hardware.	P. 18
Clocked serial interface B (CSIB)	Can be implemented using the SCIg and RSPIb.	P. 20
I^2C bus	Can be implemented using the SCIg and RIICa.	P. 22
Bus control function (external bus interface function)	—	P. 24
DMA functions (DMA controller)	Can be implemented using the DTCa. However, the RAM is used to store transfer information.	P. 25
Interrupt/exception processing function	Yes However, specifications that depend on external interrupts or peripheral modules are not supported.	P. 26
Standby function	Yes	P. 28
Low-voltage detector	Can be implemented using the LVDAb.	P. 31
Power-on-clear circuit	Can be implemented using the power-on reset circuit and the voltage monitoring 0 reset functionality of the LVDAb.	P. 33

2. On-Chip Functions

2.1 CPU Functions

2.1.1 Comparative Specifications

Table 2.1 lists comparative specifications of the CPU functions of the V850E/Ix3 Group and RX24T Group.

Table 2.1 CPU Functions of V850E/Ix3 Group and RX24T Group

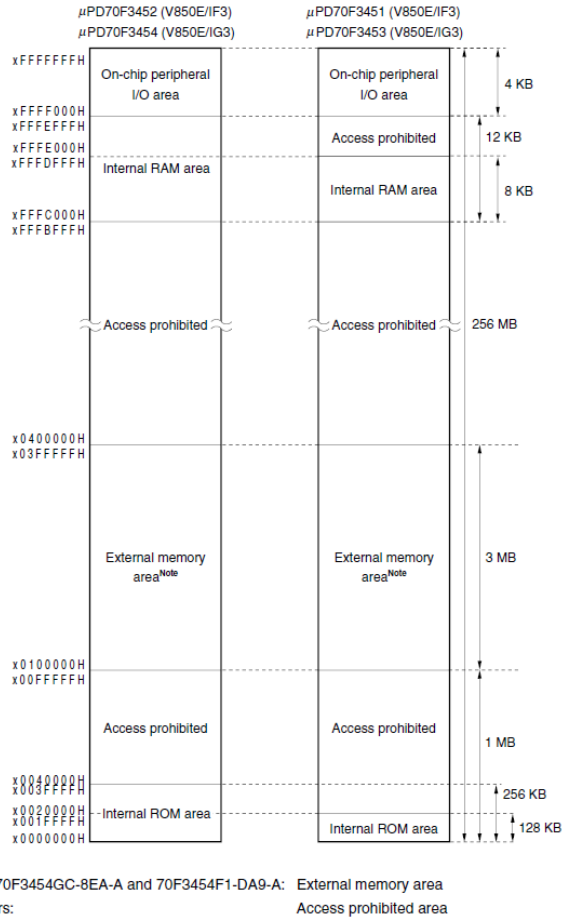
Max. operating frequency	**V850E/Ix3**	**RX24T**
	64 MHz	80 MHz

2.1.2 Memory Map

Table 2.2 shows memory maps of the V850E/Ix3 Group and RX24T Group.

Table 2.2 Memory Maps of V850E/Ix3 Group and RX24T Group

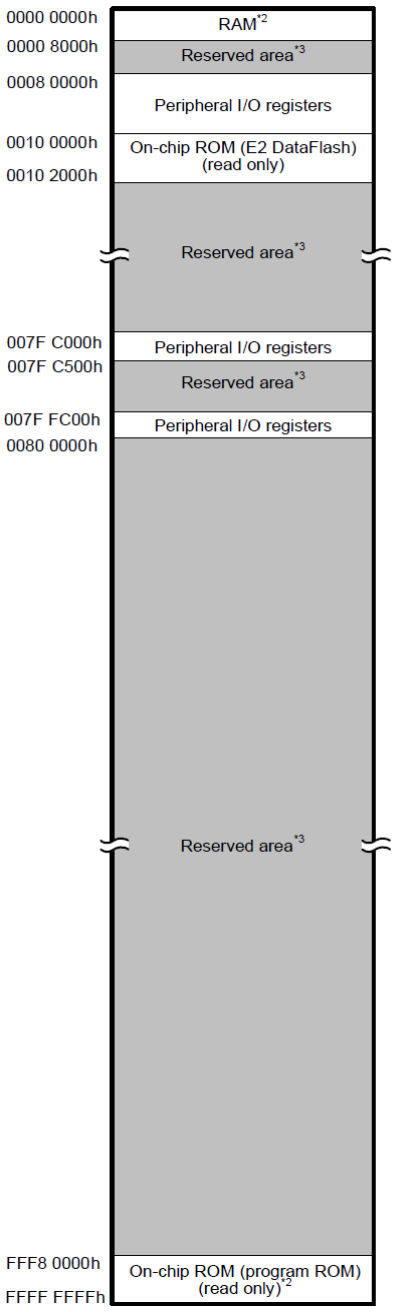
Memory map	**V850E/Ix3 Group**



Note μPD70F3454GC-8EA-A and 70F3454F1-DA9-A: External memory area
Others: Access prohibited area

Memory map	RX24T Group

Single-chip mode[*1]



Note 1. The address space in boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)		E2 DataFlash (bytes)	
Capacity	Address	Capacity	Address	Capacity	Address
512 K	FFF8 0000h to FFFF FFFFh	32 K	0000 0000h to 0000 7FFFh	8 K	0010 0000h to 0010 1FFFh
384 K	FFFA 0000h to FFFF FFFFh				
256 K	FFFC 0000h to FFFF FFFFh				
256 K	FFFC 0000h to FFFF FFFFh	16 K	0000 0000h to 0000 3FFFh		
128 K	FFFE 0000h to FFFF FFFFh				

Note: See Table 1.3 List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

2.2 Port Functions

2.2.1 Comparative Specifications

Table 2.3 lists correspondences between the specifications of I/O ports on the RX24T Group and port functions on the V850E/Ix3 Group.

Table 2.3 Port Function Correspondences

Port Function	V850E/Ix3	RX24T
CMOS output and N-ch open-drain output	Yes	Yes
Control of on-chip pull-up resistor connection	Yes	Yes
5 V tolerant	—	Yes

2.2.2 Usage Note

2.2.2.1 Unimplemented Ports

Due to different pin counts among products in the RX24T Group, some ports are not implemented on some products. It is therefore necessary to make appropriate settings in the port direction register for nonexistent ports, as described in 18.4, Initialization of the Port Direction Register (PDR), in RX24T Group User's Manual: Hardware.

This corresponds to setting the port n mode registers (PMn) on the V850E/Ix3 Group. The port n mode register (PMn) settings differ among V850E/IG3 and V850E/IF3 products, but none of the differences are due simply to differences in the pin count. For details, refer to chapter 4, PORT FUNCTIONS, in V850E/IF3, V850E/IG3 32-bit Single-Chip Microcontrollers: Hardware User's Manual.

2.3 Clock Generator

2.3.1 Comparative Specifications

Table 2.4 lists correspondences between the specifications of the clock generation circuit on the RX24T Group and the clock generator on the V850E/Ix3 Group.

Table 2.4 Clock Generator Correspondences

Item	V850E/Ix3 Clock Generator	RX24T Clock Generation Circuit
CPU clock source	Selectable among the following two: • Oscillation clock (guaranteed oscillation range: 4 MHz to 8 MHz) • PLL clock (×8 fixed)	Selectable among the following four: • Main clock (oscillation frequency: 1 MHz to 20 MHz) (Selectable between resonator and external clock.) • PLL clock (×4 to ×15.5) • HOCO (Selectable between 32 MHz and 64 MHz.) • LOCO (4 MHz)
Operating frequency	Stipulations by function • CPU clock frequency (f_{CPU}): 64 MHz (max.) Selectable from fxx to fxx/8 • Internal system clock frequency (f_{CLK}): 64 MHz (max.) • External bus clock frequency (f_{BUS}): 64 MHz (max.) • Peripheral clock frequency: 64 MHz (max.) • Watchdog timer clock: 62.5 kHz (max.)	Different clock frequencies are generated according to the function. • ICLK: 80 MHz (max.) • PCLKA: 80 MHz (max.) • PCLKB: 40 MHz (max.) • PCLKD: 40 MHz (max.) • FCLK: 1 MHz to 32 MHz (ROM) • CACCLK: Same frequency as each oscillator • IWDTCLK: 15 kHz (dedicated on-chip oscillator for IWDT) • CANMCLK: 20 MHz (max.)
Clock monitor	Motor control timer output enters high-impedance state when oscillation stop is detected.	Oscillation stop detection function*1 When main clock oscillation stop is detected: • When the main clock is selected as the system clock, the system clock source switches to LOCO.*2 • When the PLL clock is selected as the system clock, the PLL free-running frequency is used as the system clock source. • MTU output is forced into the high-impedance state. • An oscillation stop detection interrupt can be generated.*3

Notes: 1. It is not possible to transition to software standby mode when the oscillation stop detection function is enabled.
2. Automatic switching to LOCO as the system clock source only occurs if the main clock has been selected as the system clock.
3. The oscillation stop detection interrupt is non-maskable.

2.3.2 Usage Notes

2.3.2.1 Usage Note Regarding Clock Generation Circuit

On the RX24T Group, limitations apply regarding the frequencies of the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, and PCLKD), and FlashIF clock (FCLK) supplied to the various modules. For details, refer to 9.7.1, Notes on Clock Generation Circuit, in RX24T Group User's Manual: Hardware.

2.3.2.2 Changing MTU Output at Oscillation Stop Detection

On the RX24T Group, changing the MTU output when oscillation stop is detected is possible when the oscillation stop detection interrupt has been enabled by means of a setting in the port output enable (POE) module.

For details, refer to 9.4.2, Oscillation Stop Detection Interrupts, and section 21, Port Output Enable 3 (POE3b, POE3A), in RX24T Group User's Manual: Hardware. On the V850E/Ix3 Group, timer output is forced into the high-impedance state when oscillation stop is detected.

2.4 Timer Functions (TAA, TAB, and TMT)

2.4.1 Units

Table 2.5 lists the timer function units on the V850E/Ix3 Group and RX24T Group.

Table 2.5 Timer Functions on V850E/Ix3 and RX24T

	V850E/Ix3	**RX24T**
Multi-function timer/counter integrated modules	• 16-bit timer/event counter AA (TAA) • 16-bit timer/event counter AB (TAB) • 16-bit timer/event counter T (TMT)	Multi-function timer pulse unit 3 (MTU3d)

2.4.2 Comparative Specifications

Table 2.6 lists correspondences between the specifications of multi-function timer pulse unit 3 (MTU3d) on the RX24T Group and the timer functions (TAA, TAB, and TMT) on the V850E/Ix3 Group.

Table 2.6 Timer Function Correspondences

Item	**TAA, TAB, TMT (V850E/Ix3)**	**RX24T MTU3d**
Count registers	9 registers (1 each for TAA0 to TAA4, 1 each for TAB0 and TAB1, and 1 each for TMT0 and TMT1)	11 registers (1 each for MTU0 to MTU4, MTU6, MTU7, and MTU9, and 3 each for MTU5)
Modes	Interval timer Interrupt generation and square wave output at user-defined period • Counters: Up to 9 channels (TAA0 to TAA4, TAB0 and TAB1, and TMT0 and TMT1) • Outputs: Up to 22 (2 each for TAA2 to TAA4, 4 each for TAB0 and TAB1, and 2 each for TMT0 and TMT1) • TAA3 supported on V850E/IG3 only. • TAB0 and TAB1 can function as both output and input pins.	Possible using normal mode (period count operation). • Counters: Up to 8 channels (MTU0 to MTU4, MTU6, MTU7, and MTU9) • Output pins: Up to 28 (4 each for MTU0, MTU3, MTU4, MTU6, MTU7, and MTU9, 2 each for MTU1 and MTU2)
	External event count Count operation at input of user-defined external event • Up to 7 channels (1 input pin each for TAA2 to TAA4, TAB0 and TAB1, and TMT0 and TMT) • TAA3 and TMT0 supported on V850E/IG3 only.	Possible on up to 8 channels using MTU0 to MTU4, MTU6, MTU7, and MTU9, which support external clock input (1 input per channel).

Item	TAA, TAB, TMT (V850E/Ix3)	RX24T MTU3d
Modes	External trigger pulse output Count start and PWM waveform output at input of external trigger • Up to 11 outputs (1 each for TAA2 to TAA4, 3 each for TAB0 and TAB1, 1 each for TMT0 and TMT1) • TAA3 supported on V850E/IG3 only.	No equivalent functionality is implemented in hardware.*1 However, equivalent operation can be achieved using PWM mode and external input interrupts on MTU0 to MTU4, MTU6, MTU7, and MTU9. • Waveform outputs: Up to 14
	One-shot pulse output Count start and one-shot pulse output at external trigger input or external event count input • Up to 11 outputs (1 each for TAA2 to TAA4, 3 each for TAB0 and TAB1, 1 each for TMT0 and TMT1) • TAA3 supported on V850E/IG3 only.	
	PWM output • Up to 11 outputs (1 each for TAA2 to TAA4, 3 each for TAB0 and TAB1, 1 each for TMT0 and TMT1) • TAA3 supported on V850E/IG3 only.	PWM mode 1 supports up to 14 PWM outputs, and PWM mode 2 up to 11 PWM outputs.
	Free-running timer • Up to 9 channels (TAA0 to TAA4, TAB0, TAB1, TMT0, and TMT1) • TAA3 supported on V850E/IG3 only.	Possible using normal mode (free-running count operation). • Up to 11 channels (1 channel each for MTU0 to MTU4, MTU6, MTU7, and MTU9, 3 channels for MTU5)
	Pulse width measurement • Measurement of up to 7 signals (1 each for TAA2 to TAA4, 1 each for TAB0 and TAB1, 1 each for TMT0 and TMT1) • TAA3 and TMT0 supported on V850E/IG3 only.	Possible using either of the following methods: • Using input capture on each channel (1 each for MTU0 to MTU4, MTU6, MTU7, and MTU9, 3 for MTU5) • Using the pulse width measurement function on MTU5 (Supports width measurement on up to 3 external pulse inputs.)
	Triangular-wave PWM output • Up to 2 outputs (1 each for TMT0 and TMT1) • TMT0 supported on V850E/IG3 only.	Possible to generate up to 12 PWM outputs (6 positive-phase and 6 negative-phase) in complementary PWM mode on MTU3, MTU4, MTU 6, and MTU7.
	Encoder compare Up/down count operation at 2-phase encoder input • Up to 2 channels (TMT0 and TMT1) • Encoder inputs: Up to 4 (2 each for TMT0 and TMT1) • Encoder-clear inputs: Up to 2 (1 each for TMT0 and TMT1)	Possible using phase counting mode. • Up to 2 channels (MTU1 and MTU2) • 16-bit phase counting mode • Encoder-clear inputs: Up to 4 (MTU1 and MTU2)

Note: 1. Sample programs are available to demonstrate how to reproduce in software external trigger mode and one-shot pulse mode, which are not supported in hardware on the RX24T. For details, refer to section 3, Sample Programs.

2.5 16-Bit Interval Timer M (TMM)

2.5.1 Comparative Specifications

Table 2.7 lists correspondences between the specifications of the compare match timer (CMT) on the RX24T Group and 16-bit interval timer M (TMM) on the V850E/Ix3 Group.

Table 2.7 16-Bit Interval Timer M Correspondences

Item	V850E/Ix3 TMM	RX24T CMT
Number of channels	4 channels	4 channels
Counter bits	16	16
Selectable clock frequency division ratios	8 ratios A ratio of $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/64$, $f_{XX}/256$, $f_{XX}/1024$, or $f_{XX}/2048$ can be selected for each channel.	4 ratios A ratio of PCLK/8, PCLK/32, PCLK/128, PCLK/512 can be selected for each channel.

2.5.2 Usage Note

2.5.2.1 Initial Timer Counter Value

On the V850E/Ix3 Group, TMMn (n = 0 to 3) starts counting from FFFFh. The counter value is cleared to 0000h after a compare match, and the counter is reset to FFFFh asynchronously from the count clock when TMMn operation stops.

On the RX24T Group, the compare match timer's initial count register value can be changed freely. The counter value is cleared to 0000h after a compare match, and the current value is retained when counting stops.

For details, refer to 24.3.1, Periodic Count Operation in RX24T Group User's Manual: Hardware and to 9.5, Cautions, in V850E/IF3, V850E/IG3 32-bit Single-Chip Microcontrollers: Hardware User's Manual.

2.6 Motor Control Functions

2.6.1 Comparative Specifications

Table 2.8 lists correspondences between the specifications of multi-function timer pulse unit 3 (MTU3d) on the RX24T Group and the motor control functions on the V850E/Ix3 Group.

Table 2.8 Motor Control Function Correspondences

Item	V850E/Ix3 Motor Control Functions	RX24T MTU3d
Number of channels	6-phase PWM output (3 positive-phase and 3 negative-phase) • TAB and TMQOP are used in combination. • Up to 2 channels (TAB0 + TMQOP0 and TAB1 + TMQOP1)	Possible using complementary PWM mode. 12-phase PWM output (6 positive-phase and 6 negative-phase) • Up to 2 channels (MTU3 + MTU4 and MTU6 + MTU7) • Possible to toggle output in synchronization with PWM period (1 for each channel).
Dead time control	Dead time control Generation of negative-phase wave signal	Possible using timer dead time data register.
Interrupt culling (skipping)	Interrupt culling function • Specified culling count of crest interrupts and valley interrupts • Masking (masking possible up to 31 times)	Possible using timer interrupt skipping set register. (masking possible up to 7 times)
A/D conversion trigger	A/D conversion start trigger output function Trigger source selectable among the following 4: • TAB counter underflow • TAB cycle match • TAA compare match during tuning operation (2 sources)	The A/D conversion start request delaying function can be used to generate A/D conversion start requests at a user-defined cycle. • Timer A/D converter start request cycle set registers (2 registers)

2.7 Watchdog Timer Functions

2.7.1 Comparative Specifications

Table 2.9 lists correspondences between the specifications of the independent watchdog timer (IWDTa) on the RX24T Group and the watchdog timer functions on the V850E/Ix3 Group.

Table 2.9 Watchdog Timer Function Correspondences

Item	V850E/Ix3 Watchdog Timer Functions	RX24T IWDTa
Counter bit length	16-bit	14-bit
Count clock sources	Oscillation clock PLL clock	IWDT-dedicated clock (IWDTCLK) Generated by on-chip oscillator.
Overflow time selection	8 options $2^{19}/f_{xx}$, $2^{20}/f_{xx}$, $2^{21}/f_{xx}$, $2^{22}/f_{xx}$, $2^{23}/f_{xx}$, $2^{24}/f_{xx}$, $2^{25}/f_{xx}$, or $2^{26}/f_{xx}$	12 options • Timeout period: 128, 512, 1,024, or 2,048 cycles • Clock frequency division ratio: 6 options (no division, divide-by-16, divide-by-32, divide-by-64, divide-by-128, or divide-by-256)
Operating modes	Selectable between non-maskable interrupt request mode and reset mode.	Selectable between non-maskable interrupt request output mode and reset output mode.
Interrupt/reset generation source	Overflow Value other than ACH written to WDTE register	Underflow Refresh error (window function)
Count operation at transition to standby mode	Operates after transition to HALT mode; stops after transition to IDLE or STOP mode.	Ability to select count operation/stop at transition to sleep mode, software standby mode, and deep sleep mode

2.7.2 Usage Note

2.7.2.1 Count Operation

On the V850E/Ix3 Group the watchdog timer counts up, and on the RX24T Group the IWDT counts down.

2.7.2.2 IWDT Start Modes

On the RX24T Group, IWDT counting can be started in either of two ways: register start mode and auto-start mode. For details, refer to 7.2.1, Option Function Select Register 0 (OFS0), 25.3.8, Correspondence between Option Function Select Register 0 (OFS0) and IWDT Registers, and 25.3, Operation, in RX24T Group User's Manual: Hardware.

2.7.2.3 Settings when Not Using Watchdog Timer

On the V850E/Ix3 Group, set the WDTM register to 00H if the watchdog timer will not be used. On the RX24T Group, no special settings are necessary when not using the watchdog timer.

2.8 A/D Converter

2.8.1 Units

Table 2.10 lists the A/D converter units on the V850E/Ix3 Group and RX24T Group.

Table 2.10 A/D Converter Units on V850E/Ix3 and RX24T

A/D converter	**V850E/Ix3**	**RX24T**
	• A/D converters 0 and 1 • A/D converter 2	12-bit A/D converter (S12ADF)

2.8.2 Comparative Specifications

Table 2.11 lists correspondences between the specifications of the 12-bit A/D converter (S12ADF) on the RX24T Group and A/D converters 0, 1, and 2 on the V850E/Ix3 Group.

Table 2.11 A/D Converter Function Correspondences

	V850E/Ix3		**RX24T**
Item	**A/D Converters 0 and 1**	**A/D Converter 2**	**S12ADF**
Analog inputs	2 units, 10 channels • A/D converter 0: 5 channels • A/D converter 1: 5 channels	Up to 8 channels	3 units, 22 channels • S12AD: 5 channels • S12AD1: 5 channels • S12AD2: 12 channels
Resolution	12 bits	10 bits	12 bits
A/D conversion method	Successive approximation method	Successive approximation method	Successive approximation method
A/D conversion operating mode	A/D trigger mode One-time A/D conversion on arbitrarily selected channels	One-shot select mode One-time A/D conversion on arbitrarily selected channels	Possible using single scan mode.
	A/D trigger polling mode Continuous A/D conversion on arbitrarily selected channels	Continuous select mode Continuous A/D conversion on arbitrarily selected channels	Possible using continuous scan mode.
	Hardware trigger mode A/D conversion by hardware trigger	—	Possible using single scan mode by selecting synchronous trigger or asynchronous trigger.
	Conversion channel specification mode A/D conversion the specified number of times (max. 16) (hardware trigger only)	—	No equivalent functionality is implemented in hardware.
	Extension buffer mode A/D conversion on 4 arbitrarily selected channels by 2 hardware triggers	—	Possible using group scan mode by selecting synchronous triggers for up to 3 groups.
	—	Continuous scan mode Continuous A/D conversion from ANI20 pin to arbitrarily selected channel in sequence	Possible by performing A/D conversion on arbitrarily selected channels in continuous scan mode.

Item	V850E/Ix3		RX24T
	A/D Converters 0 and 1	A/D Converter 2	S12ADF
A/D conversion operating mode	—	One-shot scan mode One-time A/D conversion from ANI20 pin to arbitrarily selected channel in sequence	Possible by performing A/D conversion on arbitrarily selected channels in single scan mode.
A/D conversion trigger mode	Software processing (A/D trigger mode)	Software trigger	Software trigger
	Hardware trigger (timer)	—	Synchronous trigger Trigger from multi-function timer pulse unit (MTU), general PWM timer (GPT)[*1], or 8-bit timer (TMR)
	Hardware trigger (external)	—	Asynchronous trigger • S12AD: ADTRG0# pin • S12AD1: ADTRG1# pin • S12AD2: ADTRG2# pin
Valid edges for external trigger	• Falling edge • Rising edge • Both edges	—	Falling edge only
Input level amplification	On-chip operational amplifier (×2.5 to ×10) • A/D converter 0: ANI05 • A/D converter 1: ANI15 to ANI17	—	Programmable gain amplifier (×2 to ×4.444) • S12AD: AN000 • S12AD1: AN100 to AN102
Overvoltage detection	On-chip comparator • A/D converter 0: 1 unit • A/D converter 1: 3 units • Setting available to put motor control timer output in high-impedance state when overvoltage is detected.	—	Delectable with Comparator C (CMPC) Possible to switch to automatic high impedance by linking with POE.
Conversion time (high-speed)	2.0 µs	3.88 µs	1 µs
Interrupt sources DMA/DTC activation sources	• A/D conversion end • Overvoltage detection (full-range side and low-range side)	A/D conversion end	Scan end

Note: 1.Chip version B only can be selected.

2.8.3 Usage Note

2.8.3.1 A/D Converter Operating Status

On the V850E/Ix3 Group there are status flags that indicate when conversion operation on A/D converter n is in progress. On the RX24T Group there are no status flags for the S12ADF, but the operating status can be confirmed by checking the A/D conversion start bit in the A/D control register or the status output pin.

2.9 Asynchronous Serial Interfaces A and B (UARTA and UARTB)

2.9.1 Units

Table 2.12 lists the asynchronous serial interface units on the V850E/Ix3 Group and RX24T Group.

Table 2.12 Asynchronous Serial Interface Units on V850E/Ix3 and RX24T

	V850E/Ix3	RX24T
Asynchronous serial interface	• Asynchronous serial interface A • Asynchronous serial interface B	Asynchronous mode of serial communications interface (SCIg)

2.9.2 Comparative Specifications

Table 2.13 lists correspondences between the specifications of the asynchronous mode of the serial communications interface (SCIg) on the RX24T Group and asynchronous serial interfaces A and B (UARTA and UARTB) on the V850E/Ix3 Group.

Table 2.13 Asynchronous Serial Interface Correspondences

	V850E/Ix3		RX24T
Item	**UARTA**	**UARTB**	**Asynchronous Mode of SCIg**
Number of channels	3 channels	1 channel	3 channels Individual channels can be put into the module stop state.
Transfer speed (max.)	1.25 Mbps (when fxx = 64 MHz)	5.33 Mbps (when fxx = 64 MHz)	5 Mbps (when PCLKB = 40 MHz)
Full-duplex communications	Yes	Yes	Yes
Operating modes	Single-stage data register used for transmission and reception, respectively.	Single mode Single-stage data register used for transmission and reception, respectively.	Single-stage data register used for transmission and reception, respectively.
	—	FIFO mode Uses transmit FIFO and receive FIFO (16 stages each).	—
Character length	Selectable between 7 and 8 bits.	Selectable between 7 and 8 bits.	Selectable between 7, 8, and 9 bits.
Transmission stop bit	Selectable between 1 and 2 bits.	Selectable between 1 and 2 bits.	Selectable between 1 and 2 bits.
Parity	Selectable among odd parity, even parity, or 0 parity.	Selectable among odd parity, even parity, or 0 parity.	Selectable among odd parity, even parity, or no parity.
Data transfer	Selectable between MSB- or LSB -first.	Selectable between MSB- or LSB -first.	Selectable between MSB- or LSB -first.
Data inversion	Support for inverted input/output of transmitted/received data.	—	Support for inverted input/output of transmitted/received data.
Clock source	Internal	Internal	Selectable between internal and external.

Item	V850E/Ix3		RX24T
	UARTA	UARTB	Asynchronous Mode of SCIg
Pins	• Transmit data output • Receive data input	• Transmit data output • Receive data input	• Clock I/O • Transmit data output • Receive data input • I/O (CTS and RTS functions) for transmission/reception start control
Receive error detection	• Parity error • Framing error • Overrun error	• Overflow error (FIFO mode only) • Parity error • Framing error • Overrun error (single mode only)	• Parity error • Framing error • Overrun error
Interrupt sources	• Reception error • Reception end • Transmission enable	• Reception error • Reception end • Transmission enable • FIFO transmission end (FIFO mode only) • Reception timeout (FIFO mode only)	• Receive error • Receive data full • Transmit data empty • Transmit end
DMA activation sources	• Reception end • Transmission enable	• Reception end • Transmission enable • FIFO transmission end (FIFO mode only)	DTC activation sources • Receive data full • Transmit data empty

2.9.3 Usage Note

2.9.3.1 0 Parity

On the V850E/Ix3 Group it is possible to set the parity to 0 parity, but no setting corresponding to 0 parity exists on the RX24T Group.

2.10 Clocked Serial Interface B (CSIB)

2.10.1 Units

Table 2.14 lists the clocked serial interface units on the V850E/Ix3 Group and RX24T Group.

Table 2.14 Clocked Serial Interface Units on V850E/Ix3 Group and RX24T Group

Clocked serial interface	**V850E/Ix3**	**RX24T**
	Clocked serial interface B (CSIB)	• Clock synchronous operation of serial peripheral interface (RSPIb) • Clock synchronous mode of serial communications interface (SCIg)

2.10.2 Comparative Specifications

Table 2.15 lists correspondences between the specifications of the clock synchronous modes of the serial peripheral interface (RSPIb) and serial communications interface (SCIg) on the RX24T Group and clocked serial interface B (CSIB) on the V850E/Ix3 Group.

Table 2.15 Clocked Serial Interface Correspondences

	V850E/Ix3	**RX24T**	
Item	**CSIB**	**Clock Synchronous Operation of RSPIb**	**Clock Synchronous Mode of SCIg**
Number of channels	3 channels	1 channel	3 channels
Transfer speed (max.)	8 Mbps	20 Mbps (when PCLKB = 40 MHz)	7.5 Mbps (when PCLKB = 30 MHz)
Selection between master mode and slave mode	Selectable between master mode and slave mode	Selectable between master mode and slave mode	Selectable between master mode and slave mode
Serial clock and data phase switching	Switchable between serial clock and data phase	Ability to change RSPCK phase and polarity in master mode	Ability to change clock phase and polarity
Data length	Selectable from 8 to 16 bits.	Selectable among 8-16, 20, 24, and 32 bits.	8 bits
Data transfer	Switchable between MSB- and LSB-first.	Switchable between MSB- and LSB-first.	Switchable between MSB- and LSB-first.
Transfer modes	Single transfer mode (transmission, reception, or transmission/reception mode)	Single transfer operation possible.	Single transfer operation possible.
	Double buffer configuration for both transmission and reception in continuous transfer mode (transmission, reception, or transmission/reception mode) transmission and reception	Transmission and reception buffers are both double buffer configurations, making continuous transfer possible.	Transmission and reception buffers are both double buffer configurations, making continuous transfer possible.

Item	V850E/Ix3	RX24T	
	CSIB	Clock Synchronous Operation of RSPIb	Clock Synchronous Mode of SCIg
Pins	• Serial data output • Serial data input • Serial clock I/O	• Master transmit data I/O • Slave transmit data I/O • Clock I/O	• Clock I/O • Transmit data output • Receive data input • I/O for transmission/reception start control
Interrupt sources	• Reception end • Transmission enable • Reception error	• Receive buffer full • Transmit buffer empty • RSPI error • RSPI idle	• Reception error • Receive data full • Transmit data empty • Transmission end
DMA activation sources	• Reception end • Transmission enable	DTC activation sources • Receive buffer full • Transmit buffer empty	DTC activation sources • Receive data full • Transmit data empty

2.10.3 Usage Note

2.10.3.1 Delays during Continuous Transmission

A delay occurs for each frame during continuous transfer operation on the RSPIb of the RX24T Group. For details, refer to 29.3.10.1, Master Mode Operation, in RX24T Group User's Manual: Hardware.

2.11 I²C Bus

2.11.1 Units

Table 2.16 lists the I²C bus function units on the V850E/Ix3 Group and RX24T Group.

Table 2.16 I²C Bus Function Units on V850E/Ix3 Group and RX24T Group

I²C function	**V850E/Ix3**	**RX24T**
	I²C bus	• I²C-bus interface (RIICa) • Simple I²C bus of serial communications interface (SCIg)

2.11.2 Comparative Specifications

Table 2.17 lists correspondences between the specifications of the I²C-bus interface (RIICa) and the simple I²C bus of the serial communications interface (SCIg) on the RX24T Group and the I²C bus on the V850E/Ix3 Group.

Table 2.17 I²C Bus Correspondences

	V850E/Ix3	**RX24T**	
Item	**I²C Bus**	**RIICa**	**Simple I²C Bus of SCIg**
Number of channels	1 channel	1 channel	3 channels
Transfer rate	Standard mode: Up to 100 kbps High-speed mode: Up to 350 kbps	Standard mode: Up to 100 kbps Fast mode: Up to 400 kps	Standard mode: Up to 100 kbps Fast mode: Up to 350 kbps
Communication format	I²C bus format	• I²C bus format • SMBus format	I²C bus format
Communication operation	• Master operation (multimaster support) • Slave operation	• Master operation (multimaster support) • Slave operation	Master (single master only)
Digital filtering	Usable in high-speed mode only Adjustment of noise elimination width not supported.	The noise canceling width can be adjusted using software.	The noise canceling width can be adjusted using software.
Reduced power consumption	Operation stop mode Used when no serial transfers are performed.	Can be implemented using module stop function.	Can be implemented using module stop function.

Item	V850E/Ix3 I²C Bus	RX24T RIICa	 Simple I²C Bus of SCIg
Interrupts	1 source INTIIC interrupt • Fall of 8th or 9th clock pulse of INTIIC interrupt serial clock • Stop condition detection	4 sources EEI interrupt • Transfer error or transfer event occurrence Arbitration detection NACK detection Timeout detection Start condition (including restart condition) detection Stop condition detection RXI interrupt • Receive data full (including slave address match) TXI interrupt • Transmit data empty (including slave address match) TEI interrupt • Transmit end	3 sources RXI interrupt • ACK detection/reception TXI interrupt • NACK detection/ reception STI interrupt • Start condition, restart condition, or stop condition
DMA activation sources	Same as interrupt sources listed above	DTC activation sources: 2 sources • Receive data full • Transmit data empty	DTC activation sources: 2 sources • Receive interrupt • Transmit interrupt

2.12 Bus Control Function (External Bus Interface Function)

2.12.1 Comparative Specifications

On the V850E/Ix3 Group the external bus interface function is available only on certain products (the μPD70F3454GC-8EA-A and μPD70F3454F1-DA9-A). It is not implemented on other products in the V850E/Ix3 Group. In addition, the RX24T Group has no functionality corresponding to the external bus interface function of the V850E/Ix3 Group.

2.13 DMA Functions (DMA Controller)

2.13.1 Comparative Specifications

Table 2.18 lists correspondences between the specifications of the data transfer controller (DTCa) on the RX24T Group and the DMA functions (DMA controller) on the V850E/Ix3 Group.

Table 2.18 DMA Function Correspondences

Item	DMA Function of V850E/Ix3	RX24T DTCa
Number of channels	4 channels	The number of channels is equal to number of interrupt sources capable of DTC activation.
Transfer mode	Single transfer mode One unit of data is transferred by one transfer request.	Can be implemented using normal transfer mode.
	Single-step transfer mode One unit of data is transferred by one transfer request, after which the bus is released, and transfers continue until the transfer count is reached.	—
	Block transfer mode One transfer request causes one unit of data at a time to be transferred until the transfer count is reached.	Can be implemented using bock transfer mode.
Transfer unit	1 data unit: Selectable among 8 and 16 bits.	• 1 data unit: Selectable among 8, 16, and 32 bits. • Size of 1 block: Settable to 1 to 256 data units.
Max. transfer count	65,536 times	• Normal transfer mode: 65,536 times • Block transfer mode: 65,536 times
Transfer requests	• Request by interrupt from on-chip peripheral I/O • Request by software trigger	Corresponds to interrupt requests capable of DTC activation. Activation sources can be specified by setting the corresponding DTCERn.DTCE bit. • Interrupt request from peripheral module • Software interrupt request
Transfer targets	• On-chip memory ↔ on-chip peripheral I/O • On-chip peripheral ↔ on-chip peripheral I/O	All areas can be the target. • 16 MB in short-address mode • 4 GB in full-address mode

2.13.2 Usage Note

On the RX24T Group the DTCa makes use of a DTC vector table located in the RAM that contains transfer information. For details, refer to 17.3.1, Allocating Transfer Information and DTC Vector Table, and 17.9.2, Allocating Transfer Information in RX24T Group User's Manual: Hardware.

2.14 Interrupt/Exception Processing Function

2.14.1 Comparative Specifications

Table 2.19 lists correspondences between the specifications of the interrupt controller (ICUb) and exception handling on the RX24T Group and the interrupt and exception processing function of the V850E/Ix3 Group.

Table 2.19 Interrupt/Exception Handling Function Correspondences

Item	Interrupt/Exception Processing Function of V850E/Ix3	ICUb/Exception Handling of RX24T
Interrupts	Non-maskable interrupt: 1 source • Overflow of watchdog timer	Non-maskable interrupts: 5 sources • NMI pin interrupt • Oscillation stop detection interrupt • IWDT underflow/refresh error • Voltage monitoring 1 interrupt • Voltage monitoring 2 interrupt
	Maskable interrupts • External: 21 sources • On-chip peripheral function interrupts	Interrupts • External pin interrupts: 8 sources • Peripheral function interrupts • Software interrupt: 1 source
	8-level programmable priority control	Selectable among 16 level settings.
	External interrupt request noise elimination • Noise elimination circuit using analog filter: INTP0 to INTP13, INTP17, INTP18, INTADT0 and INTADT1 (INTP02 to INTP07 on V850E/IG3 only) • Digital noise elimination circuit: INTP14 to INTP16 — Sampling count: 3 times — Sampling clock: Selectable among fxx/4, fxx/16, fxx/64, fxx/128, fxx/256, and fxx/512.	External interrupt request pin noise canceling • Digital filter: NMI and IRQ0 to IRQ7 — Sampling cycles: 3 times — Sampling frequency: Selectable among PCLK, PCLK/8, PCLK/32, and PCLK/64. — Selectable between digital filter enabled and disabled.
	Specification of valid edge of external interrupt requests: INTP00 to INTP18 and INTADT0 and INTADT1 • Rising edge • Falling edge • Both edges	Ability to specify interrupt detection on external interrupt request pin • Low level (IRQ0 to IRQ7) • Falling edge (NMI, IRQ0 to IRQ7) • Rising edge (NMI, IRQ0 to IRQ7) • Both edges (IRQ0 to IRQ7)
Exceptions	Software exceptions • 32 sources	Unconditional trapping by means of INT and BRK instructions • Dedicated to unconditional trapping: 16 sources
	Exception trapping: 2 sources (illegal opcode exception and debug trapping)	It is possible to implement undefined instruction and privileged instruction exceptions.

2.14.2 Usage Note

2.14.2.1 Using WAIT Instruction with Non-Maskable Interrupt

Before executing the WAIT instruction on the RX24T Group, confirm that all the status flags in the non-maskable interrupt status register (NMISR) have been cleared to 0.

2.14.2.2 Non-Maskable Interrupt Vector Area

On the RX24T Group non-maskable interrupts make use of a vector area in the exception vector table. For details, refer to 2.6, Vector Table, in RX24T Group User's Manual: Hardware.

2.15 Standby Function

2.15.1 Comparative Specifications

Table 2.20 lists correspondences between the specifications of the low power consumption functions on the RX24T Group and the standby function on the V850E/Ix3 Group.

Table 2.20 Standby Function Correspondences

Item	V850E/Ix3 Standby Function	RX24T Low Power Consumption Functions
HALT mode	Mode in which only the operating clock of the CPU is stopped < Cancellation sources > • Non-maskable interrupt request signal (INTWDT) • Unmasked maskable interrupt request signal • Reset signal (RESET pin input, generation of reset signal by watchdog timer overflow, generation of reset signal by low-voltage detection, or generation of reset signal by power-on-clear circuit)	Can be implemented using sleep mode. < Cancellation sources > • Non-maskable interrupt • Unmasked maskable interrupt • Reset (RES# pin reset, power-on reset, voltage monitoring reset, independent watchdog timer reset)
IDLE mode	Mode in which operation of all internal circuits except the oscillator is stopped However, operation of the PLL, CSIB in slave mode, clock monitor, low-voltage detector, and power-on-clear circuit is still possible. < Cancellation sources > • Unmasked external interrupt request signal (INTn pin) (n = P00 to P13, P17, P18, and ADT0 and ADT1) • Unmasked internal interrupt request signal (CSIB-related interrupt request signal in slave mode) of peripheral function capable of operating in IDLE mode • Reset signal (RESET pin input, generation of reset signal by low-voltage detection, or generation of reset signal by power-on-clear circuit)	Can be implemented using sleep mode and module stop function. < Cancellation sources > • Non-maskable interrupt • Unmasked maskable interrupt • Reset (RES# pin reset, power-on reset, voltage monitoring reset, independent watchdog timer reset)

Item	V850E/Ix3 Standby Function	RX24T Low Power Consumption Functions
STOP mode	Mode in which operation of all internal circuits is stopped However, operation of the CSIB in slave mode, low-voltage detector, and power-on-clear circuit is still possible. < Cancellation sources > • Unmasked external interrupt request signal (INTn pin) (n = P00 to P13, P17, P18, and ADT0 and ADT1) • Unmasked internal interrupt request signal (CSIB-related interrupt request signal in slave mode) of peripheral function capable of operating in STOP mode • Reset signal (RESET pin input, generation of reset signal by low-voltage detection, or generation of reset signal by power-on-clear circuit)	Can be implemented using software standby mode. However, there is no operation equivalent to the CSIB in slave mode. < Cancellation sources > • External pin interrupt (NMI and IRQ0 to IRQ7) • Peripheral function interrupt (IWDT and voltage monitoring) • Reset (RES# pin reset, power-on reset, voltage monitoring reset, independent watchdog timer reset)

2.15.2 Usage Note

2.15.2.1 Operating Status when Using Standby Function

Table 2.21 lists the operating status in each mode.

Table 2.21 Operating Status after Mode Transition

Function	V850E/Ix3			RX24T		
	HALT Mode	IDLE Mode	STOP Mode	Sleep Mode	Deep Sleep Mode	Software Standby Mode
Main clock	○	*1	×	○	○	×
CPU	×	×	×	× (Retained)	× (Retained)	× (Retained)
DMA (DTC)	○	×	×	○ *5*7	× (Retained)	× (Retained)
External bus interface	○	*2	*2	—	—	—
Interrupt controller	○	×	×	○	×	×
Watchdog timer	○	×	×	○ *4	○ *4	○ *4
A/D converter	○	×	×	○ *7	○ *7	×
Clock monitor/oscillation stop detection function	○	×	×	○	○	—*6
Low-voltage detector	○	○	○	○	○	○
Power-on-clear circuit	○	○	○	○	○	○
Ports	○	Retained	Retained	○	○	Retained
Serial interface	○	*3	*3	○ *7	○ *7	Retained
RAM	Retained	Retained	Retained	× (Retained)	× (Retained)	× (Retained)
Registers	Retained	Retained	Retained	Retained	Retained	Retained

○: operating, ×: stopped, —: no equivalent function

“Retained” means that the setting values of internal registers are retained and the internal status is operation suspended.

Notes: 1. Oscillation continues, but supply of the clock signal is stopped.
2. These pins exist on the µPD70F3454GC-8EA-A and µPD70F3454F1-DA9-A only.
3. Only CSIB0 to CSIB2 are operable when the SCKBn input clock is selected as the count clock (in slave mode).
4. In IWDT auto-start mode, operation stop can be selected by setting the IWDT sleep mode count sop control bit (OFS0.IWDTSLCSTP) in option function select register 0. In other than IWDT auto-start mode, operation stop can be selected by setting the sleep mode count stop control bit (IWDTCSTPR.SLCSTP) in the IWDT count stop control register.
5. Writing to system control–related registers is prohibited in sleep mode. For details, refer to Table 5.1, List of I/O Registers (Address Order), in RX24T Group User’s Manual: Hardware.
6. It is necessary to stop the main clock in order to transition to software standby mode, so it is not possible to use the oscillation stop detection function.
7. Supply of the clock signal can be stopped by using the module stop function.

2.16 Low-Voltage Detector

2.16.1 Comparative Specifications

Table 2.22 lists correspondences between the specifications of the voltage detection circuit (LVDAb) on the RX24T Group and the low-voltage detector on the V850E/Ix3 Group.

Table 2.22 Low-Voltage Detector Correspondences

	V850E/Ix3	RX24T	
Item	**Low-Voltage Detector**	**LVDAb Voltage Monitoring 1**	**LVDAb Voltage Monitoring 2**
Operation when voltage detected	Interrupt request signal or reset signal is generated. • When power supply voltage < detection voltage, or power supply voltage > detection voltage, a maskable interrupt is generated. • When power supply voltage < detection voltage, an internal reset signal is generated.*1	Voltage monitoring 1 interrupt or voltage monitoring 1 reset is generated.*2 • When both Vdet1 > VCC and VCC > Vdet1, or either is the case, an interrupt request is generated. • When Vdet1 > VCC, a reset is generated.	Voltage monitoring 2 interrupt or voltage monitoring 2 reset is generated.*2 • When both Vdet2 > VCC and VCC > Vdet2, or either is the case, an interrupt request is generated. • When Vdet2 > VCC, a reset is generated.
Detection voltage (typ.)	Can be changed by software (two steps).*3 • 4.4 V • 4.2 V	Selectable among 9 levels by setting LVDLVLR.LVD1LVL[3:0] bits.*3 • 4.29 V • 4.14 V • 4.02 V • 3.84 V • 3.10 V • 3.00 V • 2.90 V • 2.79 V • 2.68 V	Selectable among 4 levels by setting LVDLVLR.LVD2LVL[1:0] bits.*3 • 4.29 V • 4.14 V • 4.02 V • 3.84 V
Operation when using standby function	Operation also possible in STOP mode.	Operation possible in low power consumption state.	Operation possible in low power consumption state.
Detection flag	The low-voltage detection flag is set.	The voltage monitoring 1 reset detection flag is set.	The voltage monitoring 2 reset detection flag is set.

Notes: 1. When operation is enabled and the operating mode is set to “when power supply voltage < detection voltage, an internal reset signal is generated,” it is not possible to stop operation of the low-voltage detector (LVI) until a reset request other than a reset by the low-voltage detector is generated.

2. Do not use the voltage monitoring 1 or 2 reset or the voltage monitoring 1 or 2 non-maskable interrupt to initiate writing or erasing of the flash memory.

3. For details on detection voltage ranges, refer to 28.1.14, Low-voltage detector (LVI), and 28.2.14, Low-voltage detector (LVI), in V850E/IF3, V850E/IG3 32-bit Single-Chip Microcontrollers: Hardware User’s Manual, and to 37.8, Power-On Reset Circuit and Voltage Detection Circuit Characteristics, in RX24T Group User’s Manual: Hardware.

2.16.2 Usage Note

2.16.2.1 Usage Note Regarding Start of Operation

After enabling low-voltage detection on the V850E/Ix3 Group, it is necessary to allow a software wait of 0.1 ms or more before checking the low-voltage detection flag. On the RX24T Group it is not necessary to insert a software wait. For details, refer to section 8, Voltage Detection Circuit (LVDAb), in RX24T Group User's Manual: Hardware.

2.16.2.2 Usage Note Regarding Reenabling Voltage Detection

After voltage detection has occurred once on the RX24T, allow at least two cycles of PCLKB2 to elapse before enabling the voltage monitoring 1 or 2 interrupt or reset again. For details, refer to section 8, Voltage Detection Circuit (LVDAb), in RX24T Group User's Manual: Hardware.

2.17 Power-On-Clear Circuit

2.17.1 Comparative Specifications

Table 2.23 lists correspondences between the specifications of the power-on reset circuit and the voltage monitoring 0 function of the voltage detection circuit (LVDAb) on the RX24T Group and the power-on-clear circuit on the V850E/Ix3 Group.

Table 2.23 Power-On-Clear Circuit Correspondences

	V850E/Ix3	**RX24T**	
Item	**Power-On-Clear Circuit**	**Power-On Reset Circuit**	**LVDAb Voltage Monitoring 0**
Operation when voltage detected	A reset is generated. • At power-on • When power supply voltage < detection voltage	A power-on reset is generated. • At power-on when VCC is connected to the RES# pin via a resistor	A voltage monitoring 0 reset is generated. • When the voltage drops below Vdet0
Detection voltage (typ.)	3.7 V	1.50 V	Selecting among 3 levels by setting the OFS1 register. • 3.84 V • 2.82 V • 2.51 V

For details on detection voltage ranges, refer to 28.1.13, Power-on-clear circuit (POC), and 28.2.13, Power-on-clear circuit (POC), in V850E/IF3, V850E/IG3 32-bit Single-Chip Microcontrollers: Hardware User's Manual, and to 37.8, Power-On Reset Circuit and Voltage Detection Circuit Characteristics, in RX24T Group User's Manual: Hardware.

3. Sample Programs

The distribution package containing this application note includes sample programs that reproduce in software functions of the V850E/Ix3 Group that are not implemented in hardware on the RX24T Group.

The latest versions of the sample programs are available on the Renesas Electronics website.

3.1 Operation Confirmation Conditions

Table 3.1 shows the environment on which the operation of the sample programs has been confirmed.

Table 3.1 Operation Confirmation Conditions

Item	Description
MCU used	R5F524TAADFP
Operating frequencies	• Main clock: 20.0 MHz • PLL: 80.0 MHz (main clock divided by 2 and multiplied by 8) • HOCO: Stopped • LOCO: 4 MHz • System clock (ICLK): 80.0 MHz (PLL divided by 1) • Peripheral module clock A (PCLKA): 80.0 MHz (PLL divided by 1) • Peripheral module clock B (PCLKB): 40.0 MHz (PLL divided by 2) • Peripheral module clock D (PCLKD): 40.0 MHz (PLL divided by 2) • FlashIF clock (FCLK): 20.0 MHz (PLL divided by 4)
Operating voltage	3.3 V
Integrated development environment	Renesas Electronics e^2 studio Version 2021-01
Compiler	Renesas Electronics C/C++ Compiler Package for RX Family V.3.03.00
	Default settings of integrated development environment
iodefine.h version	1.0 H
Endian order	Little endian
Operating mode	Single-chip mode
Processor mode	Supervisor mode
Sample program version	Version 1.00
Board used	Renesas Starter Kit for RX24T (product No.: RTK500524TSxxxxxBE)

3.2 Project Structure

Table 3.2 lists the sample projects accompanying this application note, and Table 3.3 lists files in which changes were made to source code generated by the code generation function.

Table 3.2 Projects

Function	Project Name	Description
External trigger PWM output function	external_input_rx24t	This project reproduces the functionality on the V850E/Ix3 Group for using external trigger input to initiate count start and PWM output on the RX24T Group using the IRQ external input interrupt and the MTU in PWM mode 1.
One-shot pulse output function	one_shot_pulse_rx24t	This project reproduces the functionality on the V850E/Ix3 Group for using external trigger input to initiate count start and one-shot pulse output on the RX24T Group using the IRQ external input interrupt and the MTU in PWM mode 1.

Table 3.3 Changes to Files Generated by Code Generation Function

Project	Folder	File Name	Description
external_input_rx24t	Config_ICU	Config_ICU_user.c	User-implemented interrupt handling
one_shot_pulse_rx24t	Config_ICU	Config_ICU_user.c	User-implemented interrupt handling
	Config_MTU0	Config_MTU0_user.c	User-implemented interrupt handling

Note: For details of the added processing, refer to 3.5, Flowcharts. Source code generated by the code generation function of Smart Configurator that has not been modified is omitted.

3.3 Functions

Table 3.4 lists the functions used by the sample programs.

Table 3.4 Functions Used by Sample Programs

Function Name	Description
main*1	Main processing routine
r_Config_ICU_irq5_interrupt*1	IRQ5 interrupt handler
r_Config_MTU0_tgib0_interrupt	MTU0 compare match interrupt processing (only used by one-shot pulse output function sample program)

Notes: Source code generated by the code generation function of Smart Configurator that has not been modified is omitted.

1. Both sample programs use the same function.

3.4 Function Specifications

The sample code function specifications are listed below.

main	
Outline	Main processing routine
Header	None
Declaration	void main(void)
Description	Makes initial settings.
Arguments	None
Return Value	None

r_Config_ICU_irq5_interrupt	
Outline	IRQ5 interrupt handler
Header	Config_ICU.h
Declaration	static void r_Config_ICU_irq5_interrupt (void)
Description	Handles the IRQ5 interrupt. The IRQ5 interrupt handler starts count operation on MTU0.
Arguments	None
Return Value	None
Remarks	This function is generated by the code generation function of Smart Configurator.

r_Config_MTU0_tgib0_interrupt	
Outline	MTU0 compare match B interrupt processing
Header	r_Config_MTU0_tgib0_interrupt.h
Declaration	static void r_Config_MTU0_tgib0_interrupt (void)
Description	Handles the MTU0 compare match interrupt. The MTU0 compare match interrupt handler stops count operation on MTU0.
Arguments	None
Return Value	None
Remarks	This function is generated by the code generation function of Smart Configurator. This function is only used by one_shot_pulse_rx24t.

3.5 Flowcharts

The sample programs make use of the code generation function. This section contains flowcharts of functions containing changes to the program code generated by e^2 studio and that are used to reproduce the hardware functionality of the V850E/Ix3 Group. For details of other peripheral functions, etc., refer to the setting screens in Smart Configurator and the generated code.

3.5.1 Main

Figure 3.1 is a flowchart of the main processing routine.

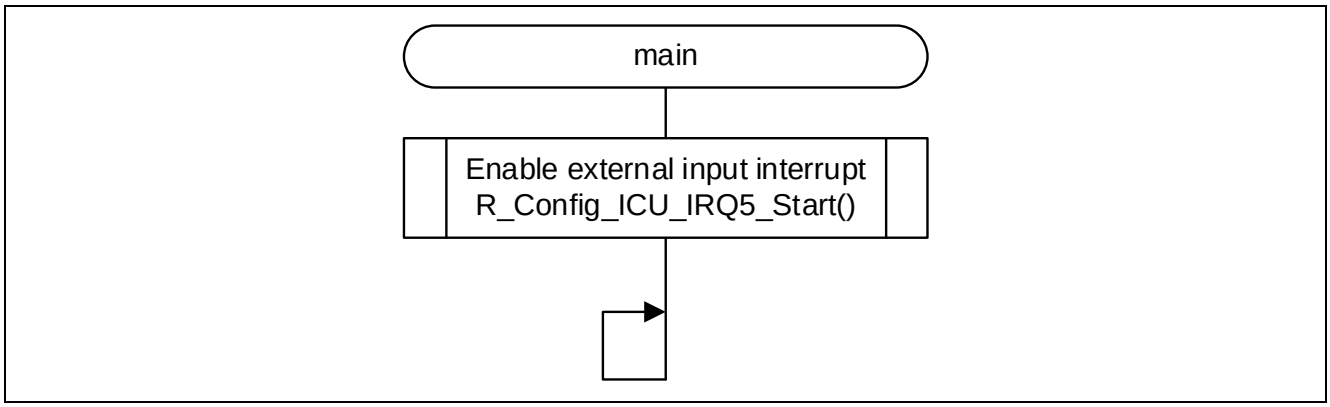


Figure 3.1 Main Processing Routine

3.5.2 External Interrupt Handler

Figure 3.2 is a flowchart of the external interrupt handler.

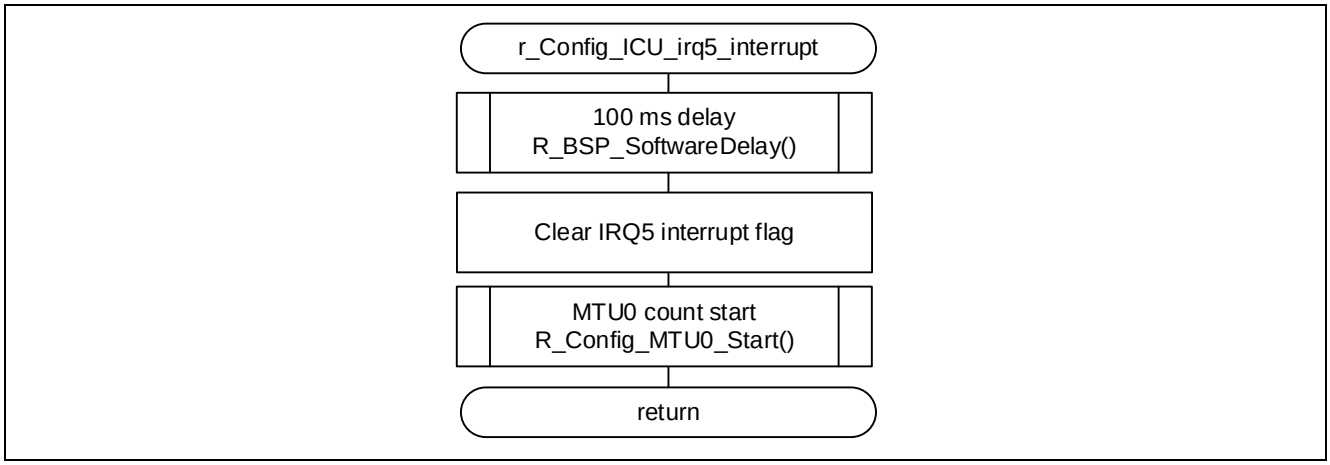


Figure 3.2 External Interrupt Handler

3.5.3 MTU0 Interrupt Handler

Figure 3.3 is a flowchart of the MTU0 interrupt handler.

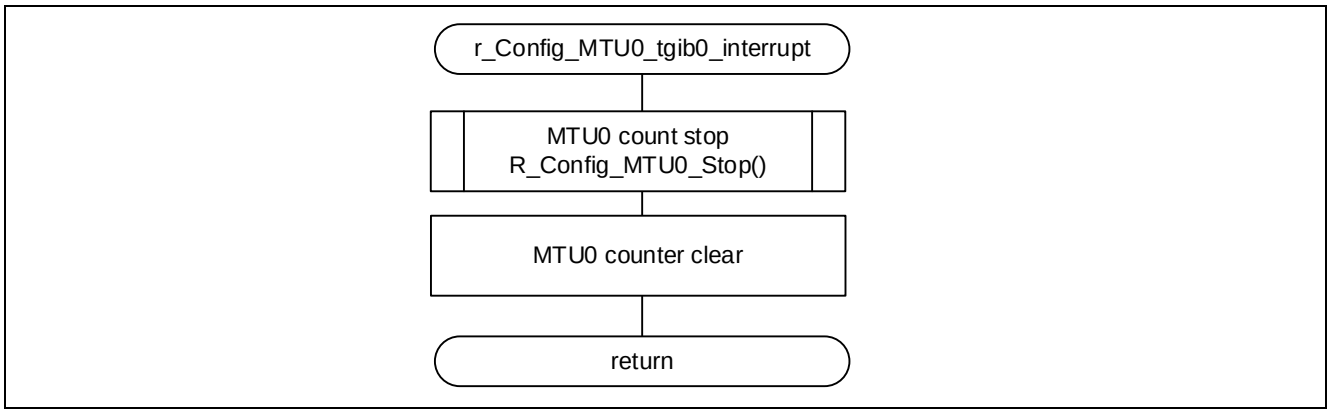


Figure 3.3 Timer Interrupt Handler

4. Importing a Project

The sample programs are distributed in e² studio project format. This section shows how to import a project into e² studio. After importing a project, check the build and debug settings.

4.1 Procedure in e² studio

To use sample programs in e² studio, follow the steps below to import them into e² studio. (Note that depending on the version of e² studio you are using, the interface may appear somewhat different from the screenshots below.)

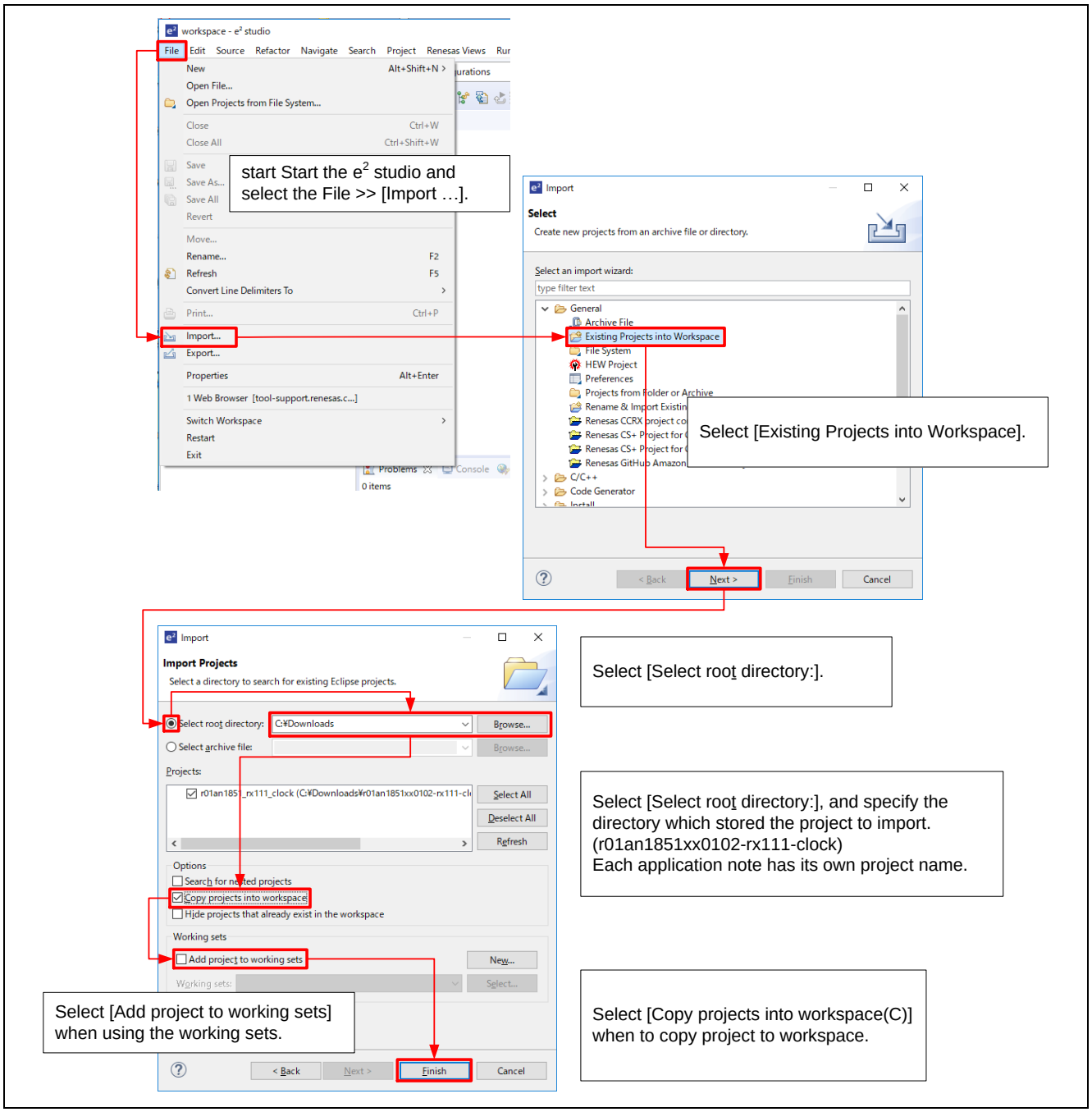


Figure 4.1 Importing a Project into e² studio

Notes: In projects managed by e² studio, do not use space codes, multibyte characters, and symbols such as "$", "#", "%" in folder names or paths to them.

4.2 Procedure in CS+

To use sample programs in CS+, follow the steps below to import them into CS+. (Note that depending on the version of CS+ you are using, the interface may appear somewhat different from the screenshots below.)

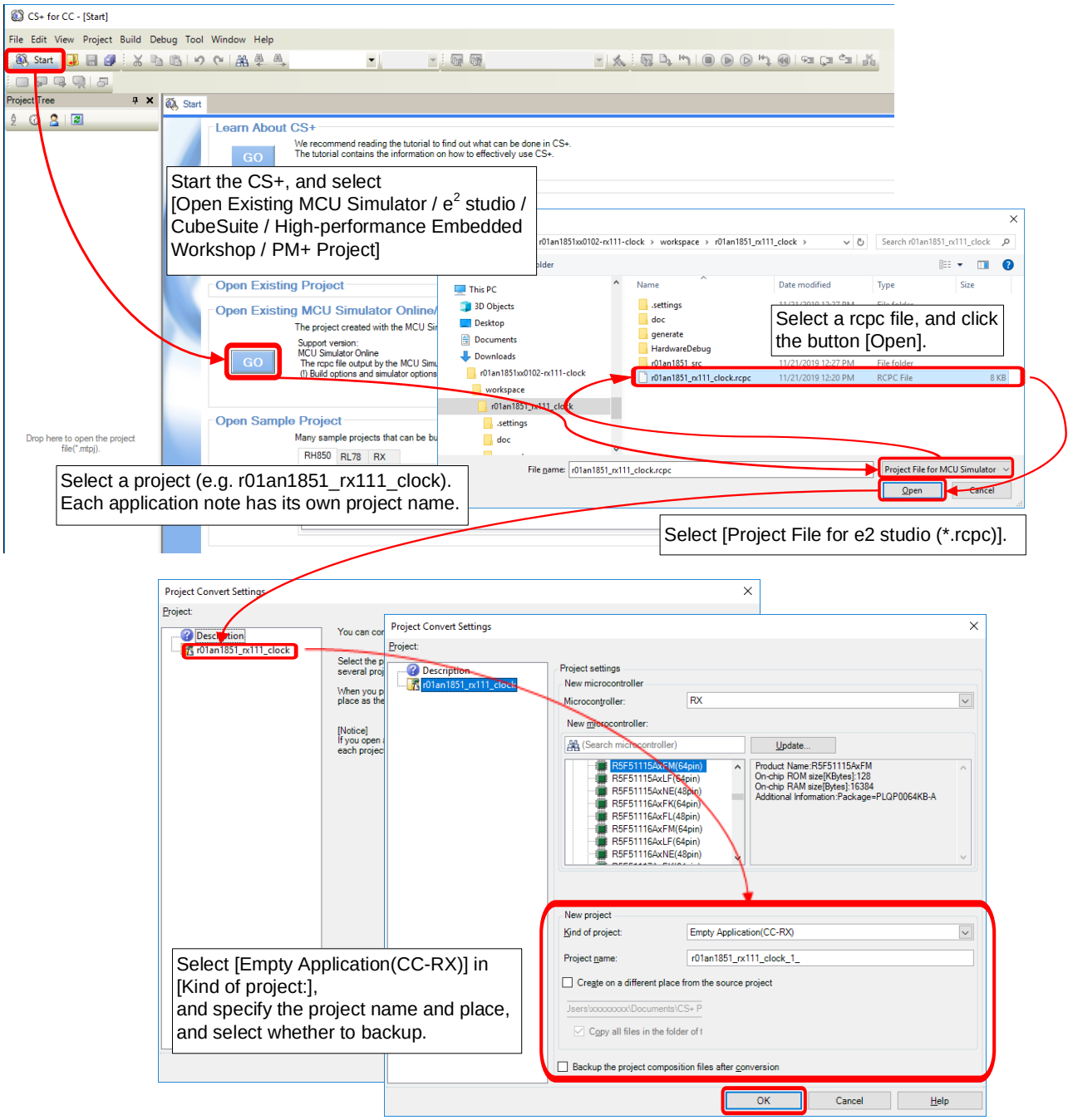


Figure 4.2 Importing a Project into CS+

Notes: In projects managed by CS+, do not use space codes, multibyte characters, and symbols such as "$", "#", "%" in folder names or paths to them.

5. Reference Documents

User's Manual: Hardware

RX24T Group User's Manual: Hardware (R01UH0576)
V850E/IF3, V850E/IG3 32-bit Single-Chip Microcontrollers Hardware User's Manual (U18279EJ3V0UD00)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Updates/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

User's Manual: Development Tools

CC-RX Compiler User's Manual (R20UT3248)
(The latest version can be downloaded from the Renesas Electronics website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Apr. 30.21	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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