

VersaClock 7 Input to Output Adjustable Delay/Advance

This document provides the steps required to control the delay or advance of clock edges from input to output for VersaClock® 7 (VC7) devices.

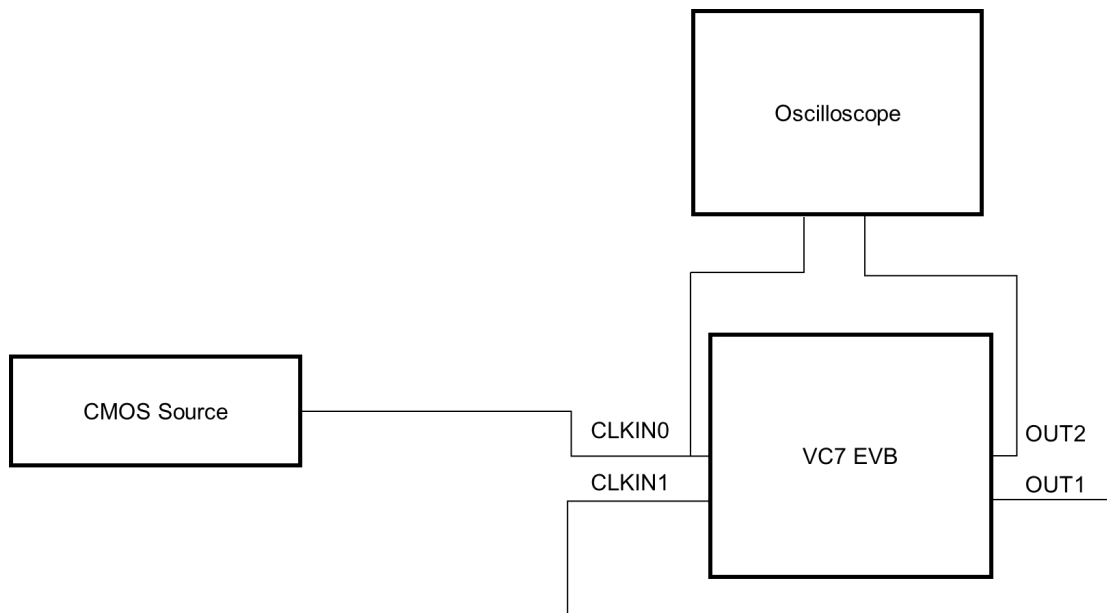
Note: For information about RICBox, see the [Renesas IC Toolbox User Guide](#).

Contents

- 1. Bench Setup 1
 - 1.1 RC31008A EVB Setup 2
 - 1.2 Oscilloscope Setup 2
 - 1.3 RICBox Installation 2
 - 1.4 Settings File 2
 - 1.5 Clock Edge Alignment (Optional) 3
- 2. Adjusting Delay/Advance 5
 - 2.1 Applying the Delay/Advance 5
- 3. Revision History 9

1. Bench Setup

Equipment used for this measurement are the RC31008A Evaluation Kit (EVB), Arbitrary Waveform Generator, and Oscilloscope with delay measurement capability. The RC31012A EVK can also be used for the measurement.



1.1 RC31008A EVB Setup

For CLKIN0, an SMA signal splitter (T adapter) can be used to observe the input clock. The board can be modified to install the sense SMB connector, J5. For OUT1 and OUT2, replace the inline capacitors with 0Ω resistors to allow for LVCMOS single-ended swing. In addition, replace the inline resistors with 33Ω resistors to meet the LVCMOS’s requirement for impedance matching. This is used to demonstrate how RICBox can delay or advance the clock edges by a predetermined amount. The length of the SMA cable plus the 5.5 in of input/output trace can be used to pick a feedback SMA cable to better edge-align on the scope if desired. The DPLL will edge-align the input clock with the feedback clock at the time-to-digital converter (TDC).

1.2 Oscilloscope Setup

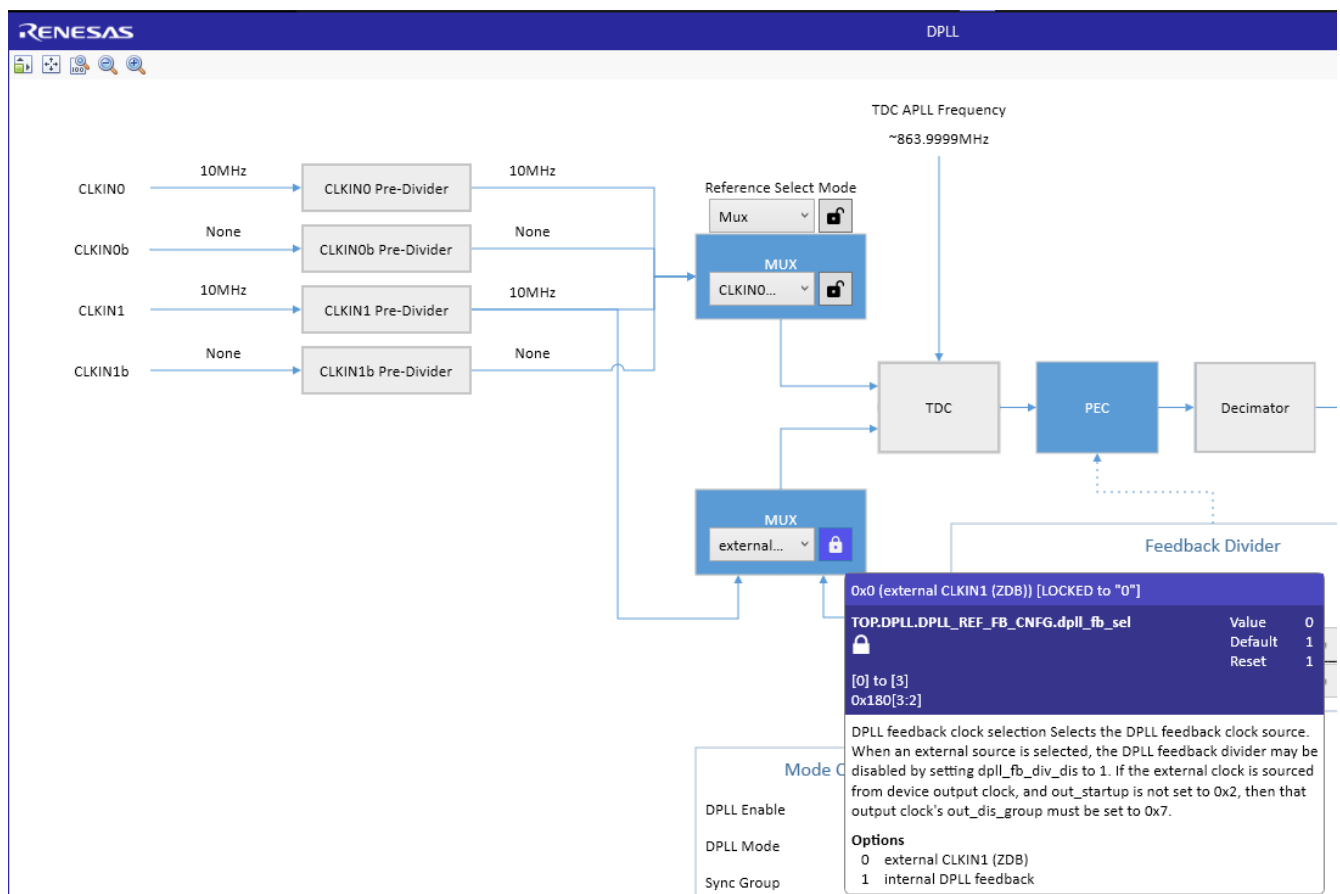
Set up a delay measurement between CH1 and CH2. Use the rising edges and set to 50% of the voltage swing. Be sure to deskew channel to channel delay.

1.3 RICBox Installation

For more information on installing RICBox software for VC7, see the [Renesas IC Toolbox User Guide](#).

1.4 Settings File

RICBox settings files or “.rbs” files are used to save and distribute custom device configurations. Each settings file contains all of a device’s registers settings. For this bench setup, load the RC31008A_Clock_delay_advance.rbs. The clock frequency used for this example is 10MHz.



Note: To access the “RC31008A_Clock_delay_advance.rbs” file, see the **Attachments** tab of this PDF.

1.5 Clock Edge Alignment (Optional)

In order to line up CLKIN0 and OUT2 on the oscilloscope, the data field “output_div_phase_adj_actual_fod1” can be adjusted. To do so, pick a value and program the VC7 device. This value will vary depending on the length of the OUT1 to CLKIN1 SMA loopback cable. The default value of -0.4ns is displayed. This step is optional because the clock edges within the DPLL are edge-aligned.



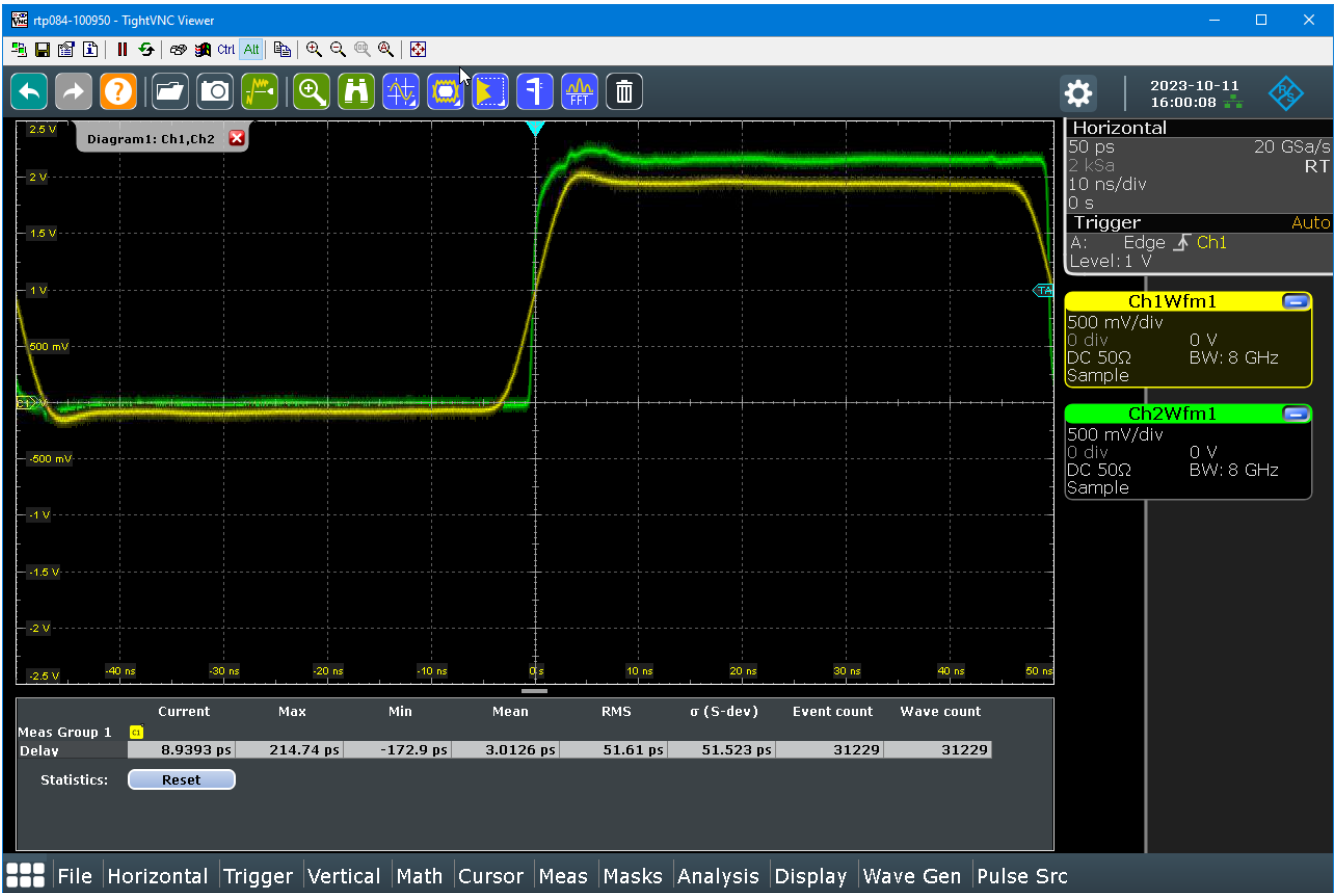
VersaClock 7 Input to Output Adjustable Delay/Advance Application Note

For the setup used in this document, a value of -6.3ns was needed to get CH1 and CH2 to edge-align.

The screenshot shows the RENESAS configuration tool interface for the RC31008A. The 'Search' tab is active, and a search for 'phase' has been performed. The results table is as follows:

Parameter Name	Value	Lock Status
output_div_phase_adj_actual_fod1	-6.3	Locked
output_div_phase_adj_actual_fod2	-0.4	Locked
output_div_phase_adj_actual_iod0	0	Locked
output_div_phase_adj_actual_iod1	0	Locked
output_div_phase_adj_actual_iod2	0	Locked
output_div_phase_adj_actual_iod3	0	Locked
output_div_phase_adj_goal_fod0	-0.4	Locked
output_div_phase_adj_goal_fod1	-6.3	Locked
output_div_phase_adj_goal_fod2	-0.4	Locked
output_div_phase_adj_goal_iod0	0	Locked
output_div_phase_adj_goal_iod1	0	Locked
output_div_phase_adj_goal_iod2	0	Locked
output_div_phase_adj_goal_iod3	0	Locked
phase_margin	-69.2417	Locked
TOP.DCD[0].DCD_CNFG.phase_wrap_ctrl	Assumes wrap when delta is less when addi...	Locked
TOP.DCD[1].DCD_CNFG.phase_wrap_ctrl	Assumes wrap when delta is less when addi...	Locked
TOP.DCD[2].DCD_CNFG.phase_wrap_ctrl	Assumes wrap when delta is less when addi...	Locked

The status bar at the bottom indicates 'Errors', 'Warnings', 'RC31008A', and 'Connected'.



2. Adjusting Delay/Advance

By definition, each step that a clock edge can be delayed or advanced is as follows:

$$step = \frac{1}{4 * VCO\ freq}$$

If the VCO frequency is 10GHz, then the step (or granularity) is calculated to be as follows:

$$\frac{1}{4 * 10GHz} = 25ps$$

The register called TOP.FOD[1].FOD_PHASE_CNFG.fod_phase is a signed two's compliment number that contains 10 bits. The range of adjustment is as follows:

$$-\frac{2^{10}}{2} * step \leq lag \leq \frac{2^{10} - 1}{2} * step$$

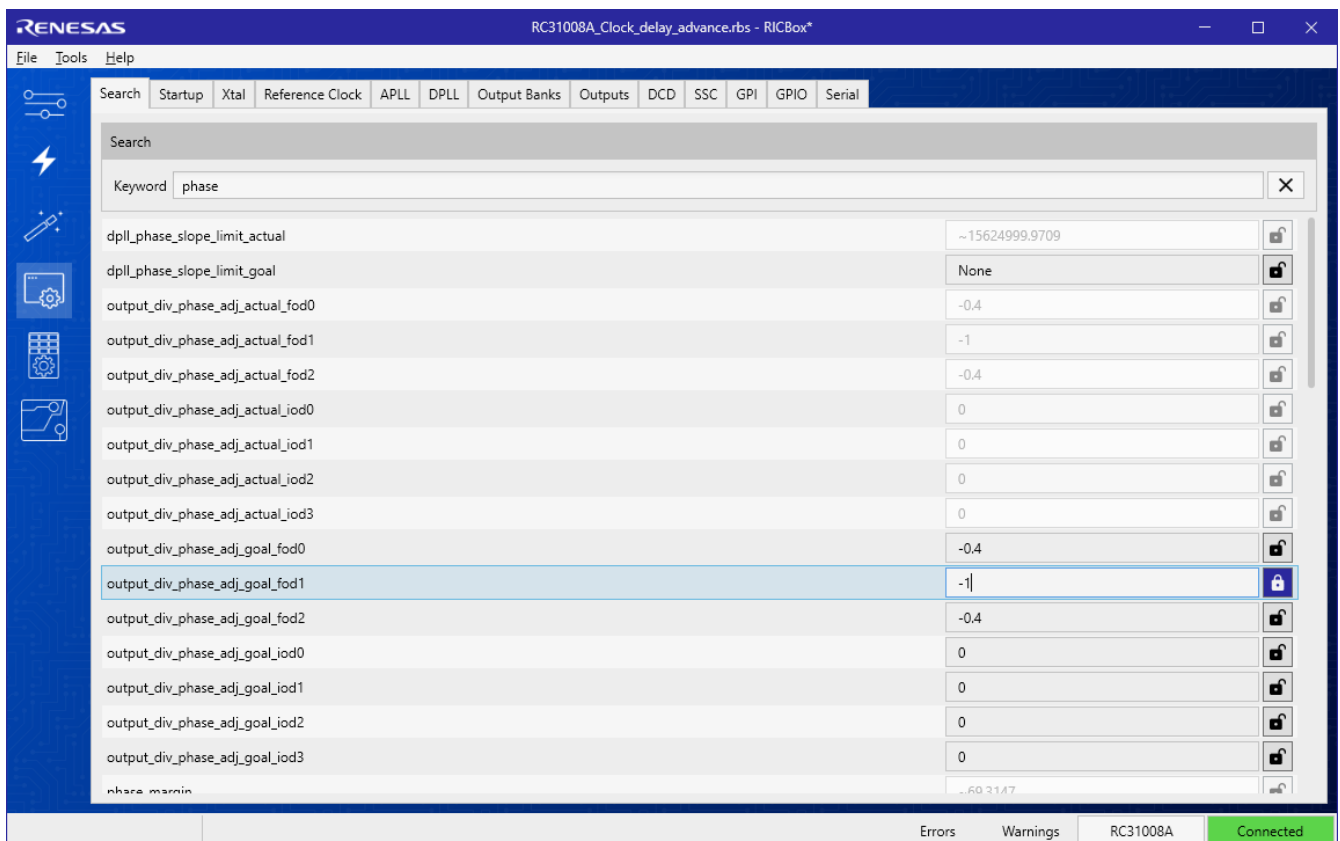
For this bench setup, the range is as follows:

$$-512 * 25ps \leq lag \leq 511 * 25ps$$

$$-12.8ns \leq lag \leq 12.775ns$$

2.1 Applying the Delay/Advance

In the RICBox GUI for VC7, the data field “output_div_phase_adj_actual_fod1” can be used to apply the desired delay or advance. Enter the amount (in nanoseconds) to shift into this data field.



VersaClock 7 Input to Output Adjustable Delay/Advance Application Note

Next, search for the register “TOP.FOD[1].FOD_PHASE_CNFG.fod_ph_adj_now”.

The screenshot shows the Renesas RICBox software interface. The search bar contains the keyword "phase". The search results list several registers, with the register `TOP.FOD[1].FOD_PHASE_CNFG.fod_ph_adj_now` selected. A tooltip for this register is displayed, showing its address as `0x0` and its description: "Fraction Output Divider Phase Adjustment Now When this bit is written from 0 to 1, the phase adjustment in `fod_phase` is applied to the divider. This bit self-clears when the adjust completes."

Register Name	Value	Default	Reset
TOP.DPLL.DPLL_PHASE_SLOPE_LIMIT.phase_slope_limit	0x1FFFFFFF		
TOP.DPLL.DPLL_PHASE_STS.phase_status	-3		
TOP.FOD[0].FOD_PHASE_CNFG.fod_ph_adj_now			
TOP.FOD[0].FOD_PHASE_CNFG.fod_ph_adj_post_sync			
TOP.FOD[0].FOD_PHASE_CNFG.fod_phase	0x3F0		
TOP.FOD[0].FOD_PHASE_CNFG.fod_slow_freq_en			
TOP.FOD[0].FOD_PHASE_CNFG.fod_sync_group	group0		
TOP.FOD[1].FOD_PHASE_CNFG.fod_ph_adj_now			
TOP.FOD[1].FOD_PHASE_CNFG.fod_ph_adj_post_sync			
TOP.FOD[1].FOD_PHASE_CNFG.fod_phase			
TOP.FOD[1].FOD_PHASE_CNFG.fod_slow_freq_en			
TOP.FOD[1].FOD_PHASE_CNFG.fod_sync_group			
TOP.FOD[2].FOD_PHASE_CNFG.fod_ph_adj_now			
TOP.FOD[2].FOD_PHASE_CNFG.fod_ph_adj_post_sync			
TOP.FOD[2].FOD_PHASE_CNFG.fod_phase	0x3F0		
TOP.FOD[2].FOD_PHASE_CNFG.fod_slow_freq_en			
TOP.FOD[2].FOD_PHASE_CNFG.fod_sync_group	group0		

VersaClock 7 Input to Output Adjustable Delay/Advance Application Note

To apply the shift, toggle this bit and check the oscilloscope. You can see the shift has been applied.



toggling this bit again will apply the desired shift again.



VersaClock 7 Input to Output Adjustable Delay/Advance Application Note

Updating “output_div_phase_adj_actual_iod1” to +1 and toggling “TOP.FOD[1].FOD_PHASE_CNFG.fod_ph_adj_now” twice will bring back the clock edges.



Toggling “TOP.FOD[1].FOD_PHASE_CNFG.fod_ph_adj_now” twice more will result in a 2ns shift.



3. Revision History

Revision	Date	Description
1.00	Nov 15, 2023	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.