VersaClock 7 Input to Output Adjustable Delay/Advance

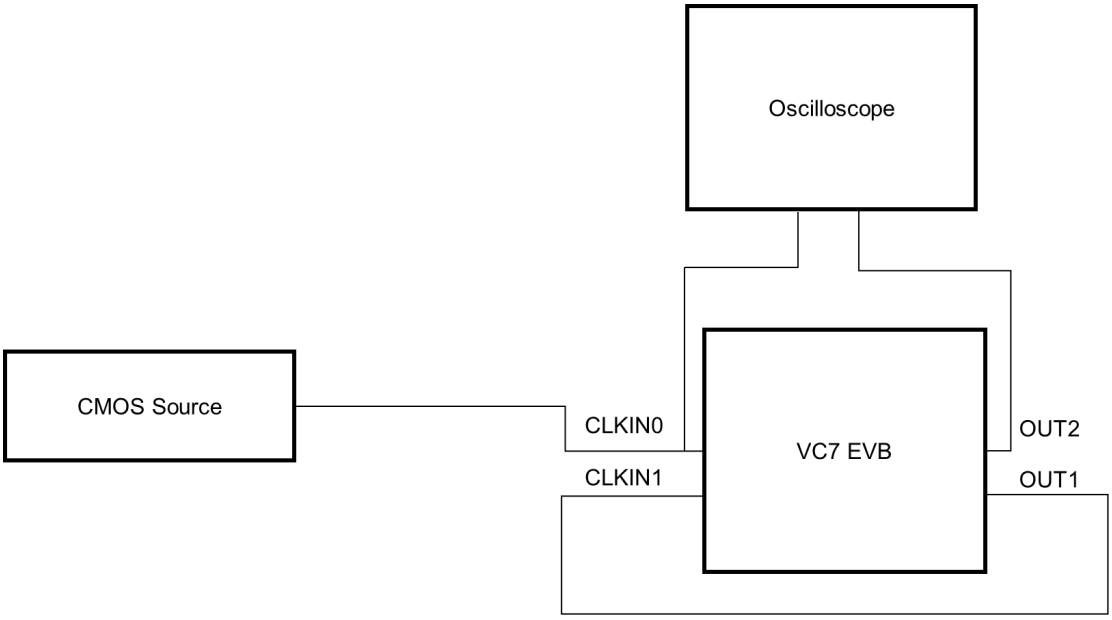
This document provides the steps required to control the delay or advance of clock edges from input to output for VersaClock® 7 (VC7) devices.

Note: For information about RICBox, see the Renesas IC Toolbox User Guide.

Contents

1. Bench Setup

Equipment used for this measurement are the RC31008A Evaluation Kit (EVK), Arbitrary Waveform Generator, and Oscilloscope with delay measurement capability. The RC31012A EVK can also be used for the measurement.



1.1 RC31008A EVB Setup

For CLKIN0, an SMA signal splitter (T adapter) can be used to observe the input clock. The board can be modified to install the sense SMB connector, J5. For OUT1 and OUT2, replace the inline capacitors with 0Ω resistors to allow for LVCMOS single-ended swing. In addition, replace the inline resistors with 33Ω resistors to meet the LVCMOS's requirement for impedance matching. This is used to demonstrate how RICBox can delay or advance the clock edges by a predetermined amount. The length of the SMA cable plus the 5.5 in of input/output trace can be used to pick a feedback SMA cable to better edge-align on the scope if desired. The DPLL will edge-align the input clock with the feedback clock at the time-to-digital converter (TDC).

1.2 Oscilloscope Setup

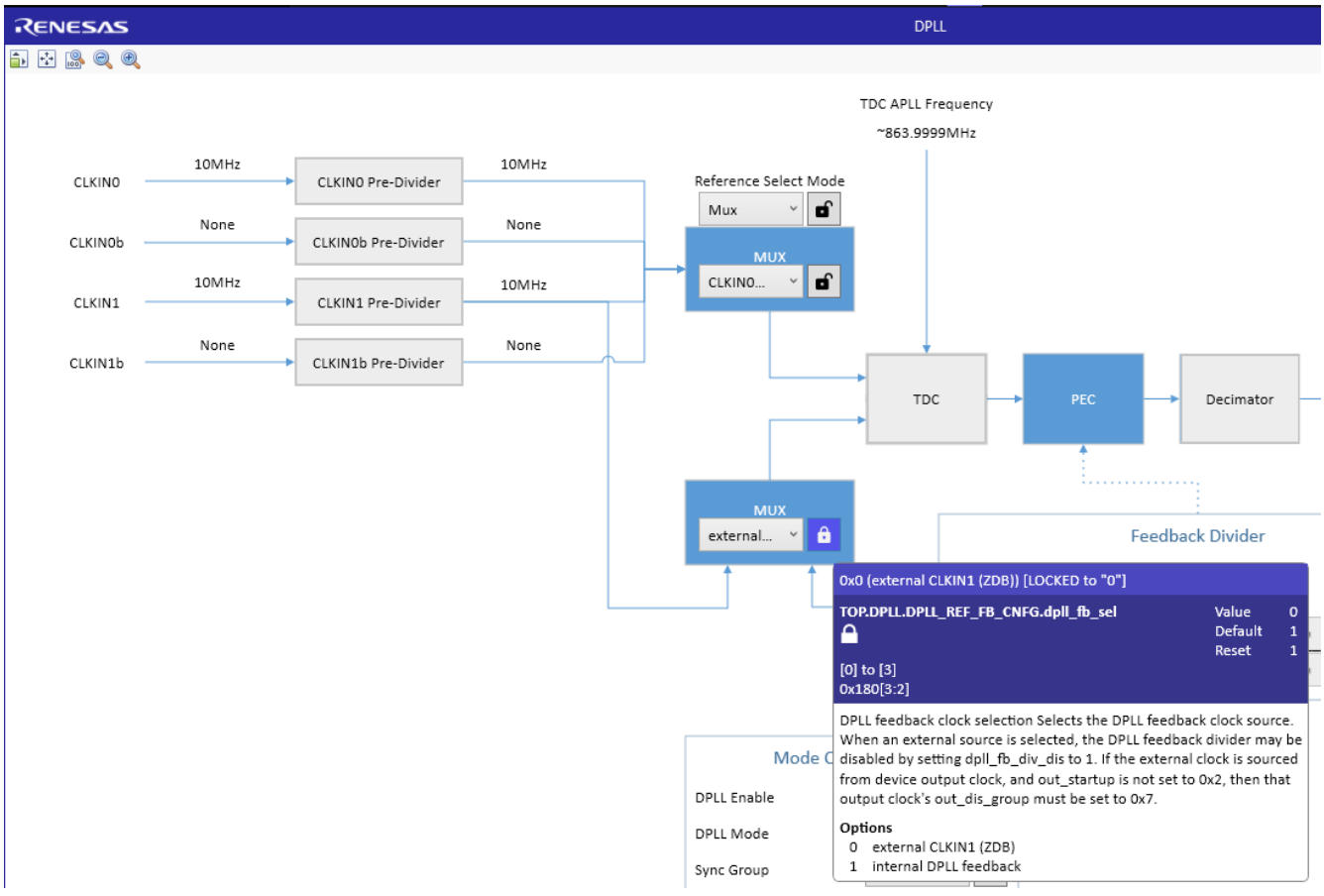
Set up a delay measurement between CH1 and CH2. Use the rising edges and set to 50% of the voltage swing. Be sure to deskew channel to channel delay.

1.3 RICBox Installation

For more information on installing RICBox software for VC7, see the Renesas IC Toolbox User Guide.

1.4 Settings File

RICBox settings files or ".rbs" files are used to save and distribute custom device configurations. Each settings file contains all of a device's registers settings. For this bench setup, load the RC31008A_Clock_delay_advance.rbs. The clock frequency used for this example is 10MHz.

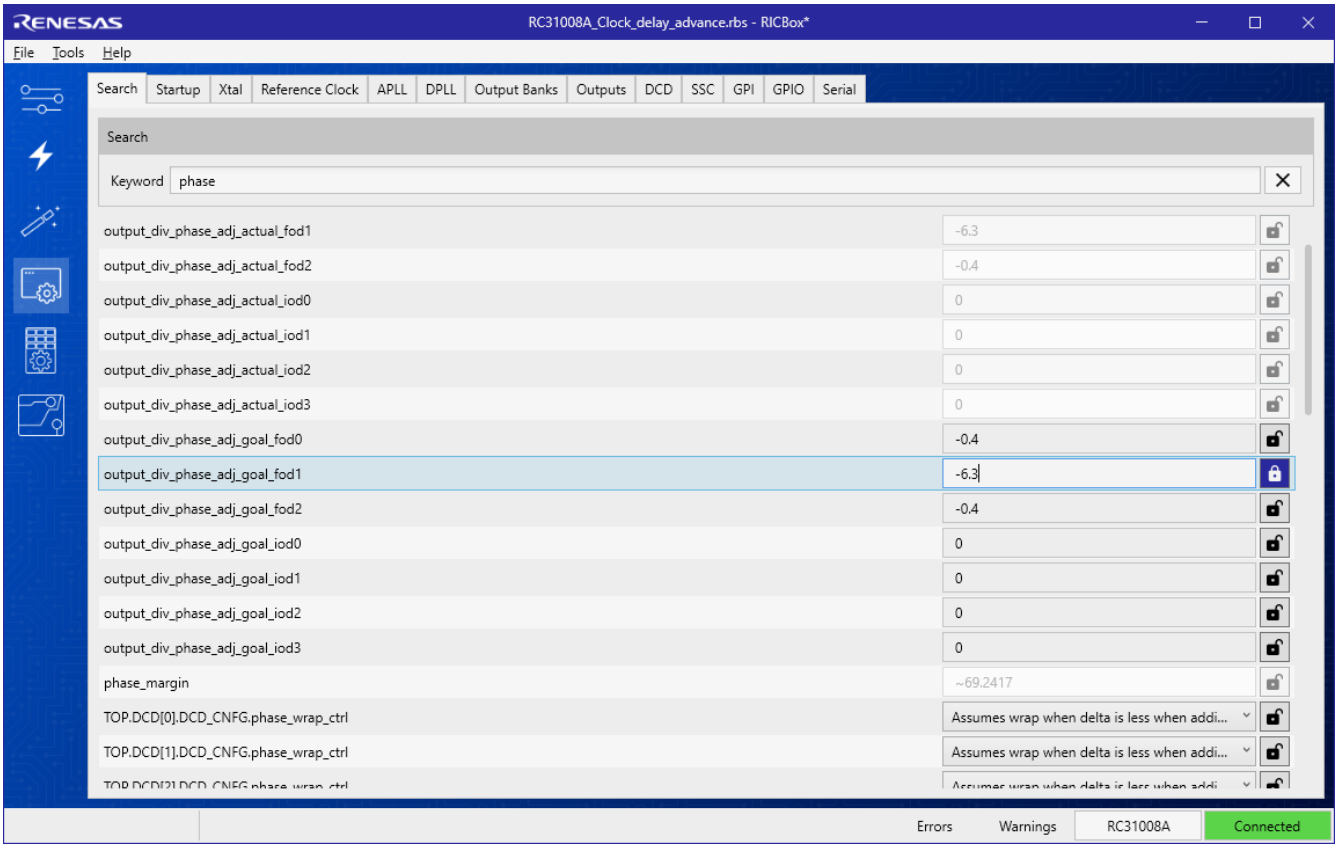


Note: To access the "RC31008A_Clock_delay_advance.rbs" file, see the **Attachments** tab of this PDF.

1.5 Clock Edge Alignment (Optional)

In order to line up CLKIN0 and OUT2 on the oscilloscope, the data field “output_div_phase_adj_actual_fod1” can be adjusted. To do so, pick a value and program the VC7 device. This value will vary depending on the length of the OUT1 to CLKIN1 SMA loopback cable. The default value of -0.4ns is displayed. This step is optional because the clock edges within the DPLL are edge-aligned.

For the setup used in this document, a value of -6.3ns was needed to get CH1 and CH2 to edge-align.



2. Adjusting Delay/Advance

By definition, each step that a clock edge can be delayed or advanced is as follows:

$$step = \frac{1}{4 * VCO\ freq}$$

If the VCO frequency is 10GHz, then the step (or granularity) is calculated to be as follows:

$$\frac{1}{4 * 10GHz} = 25ps$$

The register called TOP.FOD[1].FOD_PHASE_CNFG.fod_phase is a signed two's compliment number that contains 10 bits. The range of adjustment is as follows:

$$-\frac{2^{10}}{2} * step \leq \boldsymbol{lag} \leq \frac{2^{10}-1}{2} * step$$

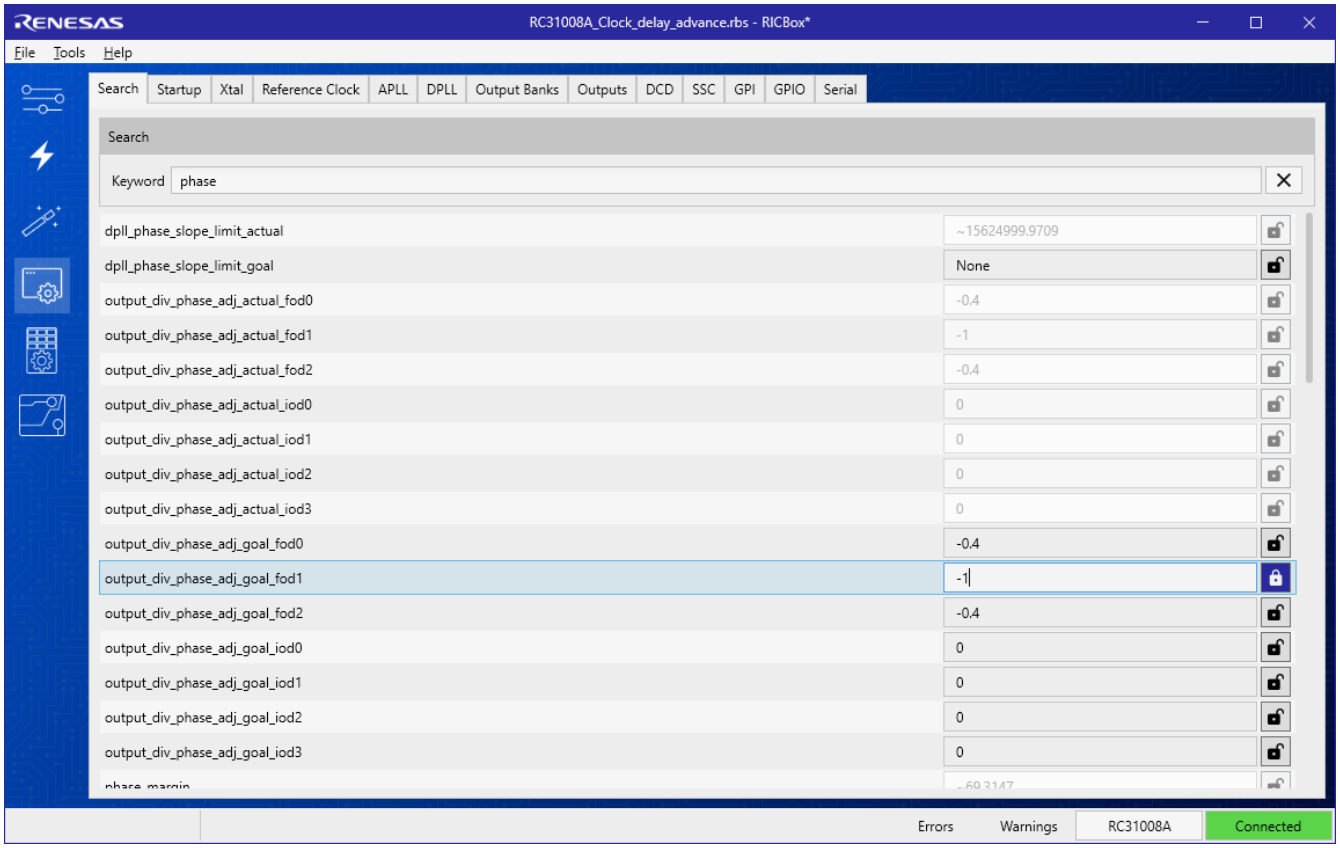
For this bench setup, the range is as follows:

$$-512 * 25ps \leq \boldsymbol{lag} \leq 511 * 25ps$$

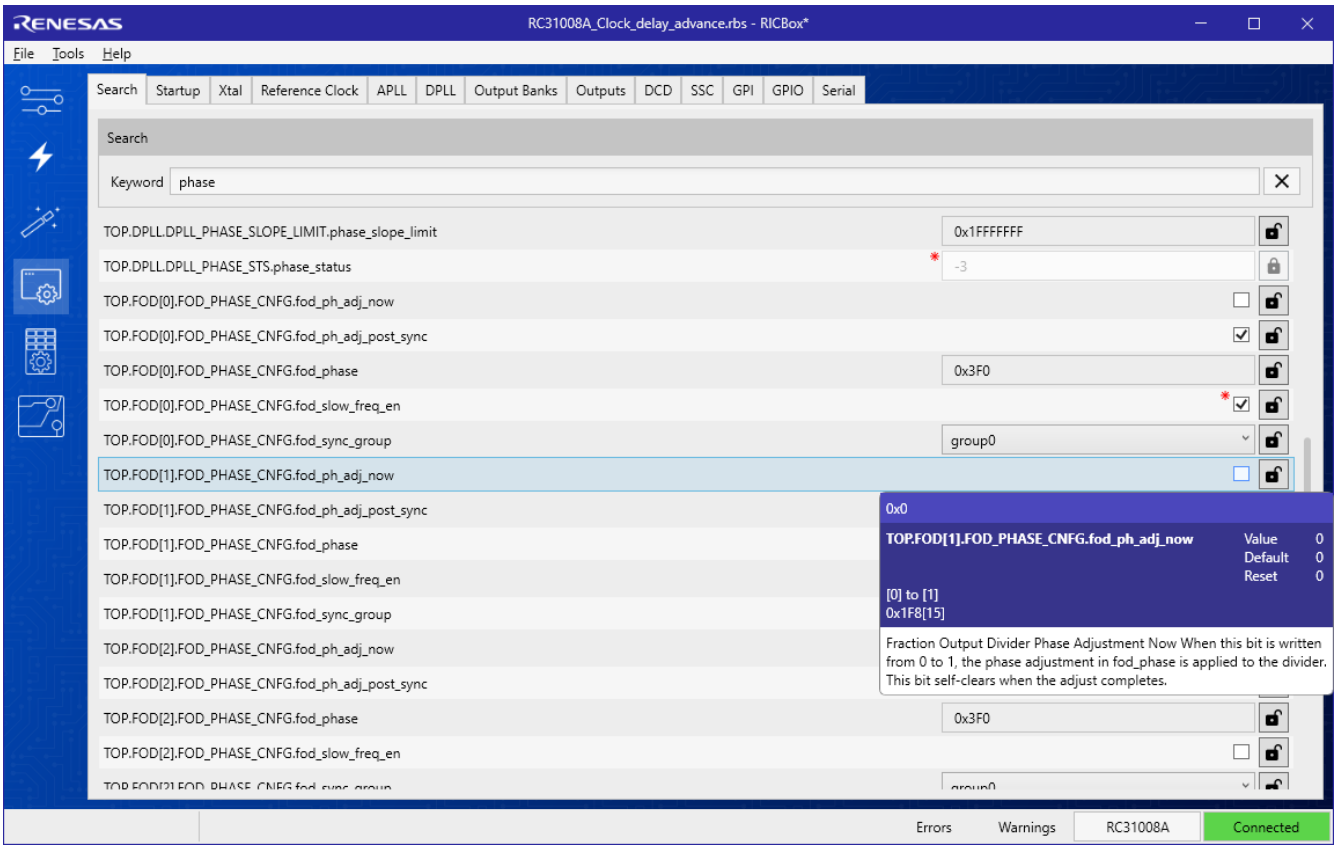
$$-12.8ns \leq \boldsymbol{lag} \leq 12.775ns$$

2.1 Applying the Delay/Advance

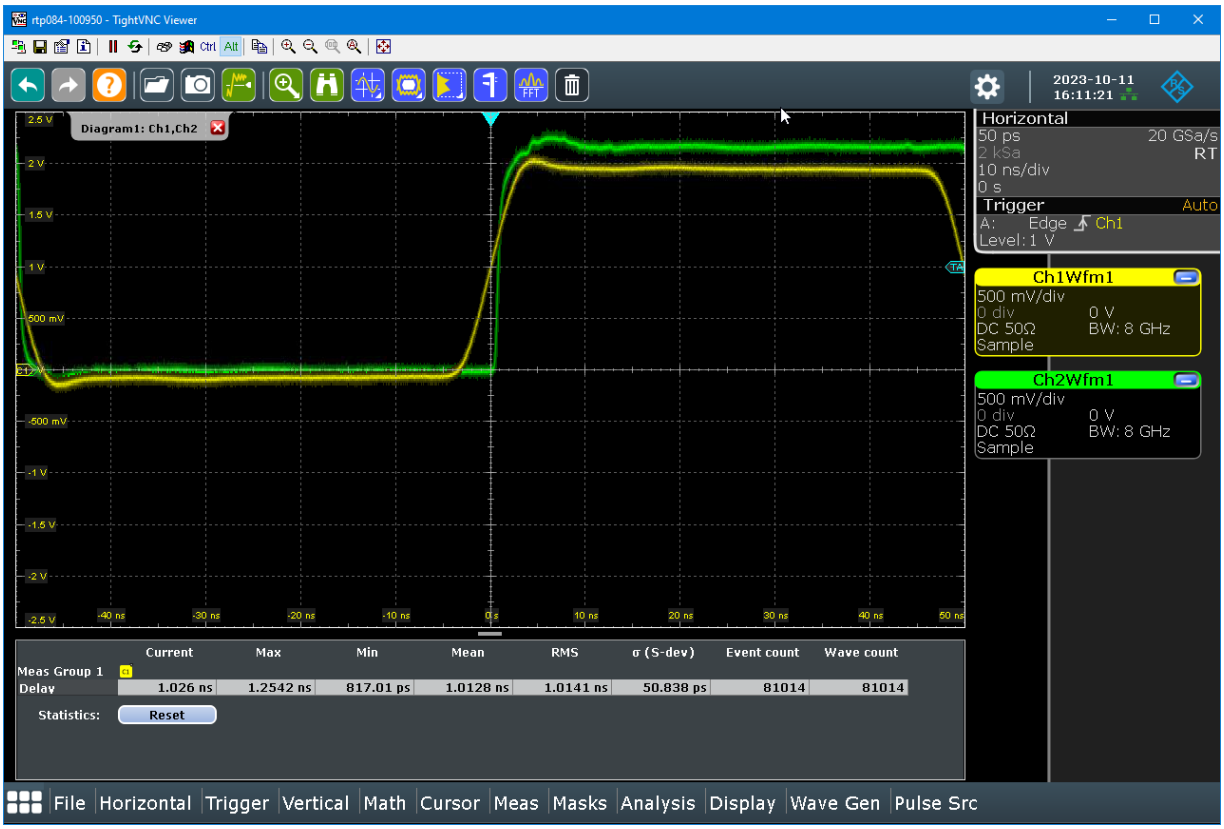
In the RICBox GUI for VC7, the data field "output_div_phase_adj_actual_fod1" can be used to apply the desired delay or advance. Enter the amount (in nanoseconds) to shift into this data field.



Next, search for the register “TOP.FOD[1].FOD_PHASE_CNFG.fod_ph_adj_now”.



To apply the shift, toggle this bit and check the oscilloscope. You can see the shift has been applied.



Toggling this bit again will apply the desired shift again.

Updating “output_div_phase_adj_actual_iod1” to +1 and toggling “TOP.FOD[1].FOD_PHASE_CNFG.fod_ph_adj_now” twice will bring back the clock edges.

Toggling “TOP.FOD[1].FOD_PHASE_CNFG.fod_ph_adj_now” twice more will result in a 2ns shift.

3. Revision History

Revision	Date	Description
1.00	Nov 15, 2023	Initial release.

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