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April 1st, 2010
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APPLICATION NOTE

Watchdog Timer

Introduction

The watchdog timer is operated.

Target Device

H8/300H Tiny Series H8/3664

Contents

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1. Specifications

1. The watchdog timer is operated.
2. The overflow cycle for timer counter WD is set to 122.88 ms. An internal reset signal is generated unless timer counter WD is initialized within this 122.88 ms.
3. In normal operation, the LED is turned on and off at specific intervals, and timer counter WD is initialized before it overflows.
4. Turning on the switch connected to the $\overline{\text{IRQ0}}$ input pin stops the reinitialization of timer counter WD so that it overflows, and generates an internal reset signal.
5. The LED is connected to the $P7_4$ output pin in port 7.

Figure 1.1 shows an example of connecting a switch to the $\overline{\text{IRQ0}}$ input pin.

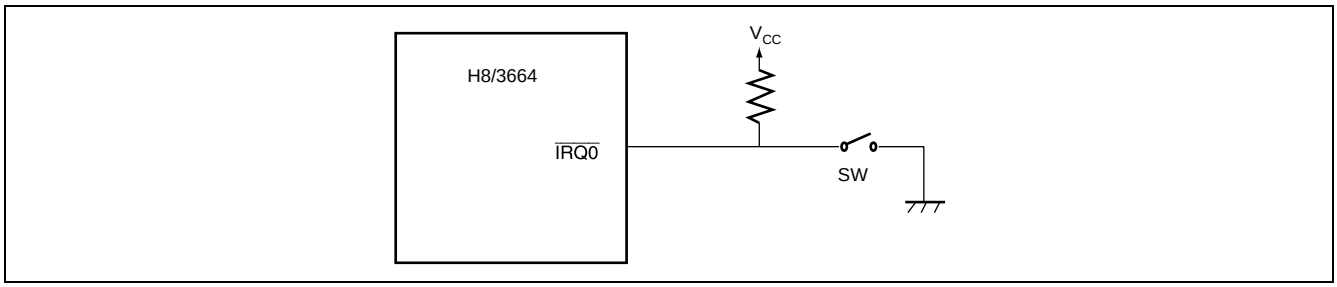


Figure 1.1 Example of Connecting Switch to $\overline{\text{IRQ0}}$ Input Pin

2. Description of Functions Used

In this sample task, the watchdog timer is operated.

Figure 2.1 is a block diagram of the watchdog timer. The elements of the block diagram are described below.

- The system clock (ϕ) is a 16-MHz OSC clock that is used as a reference clock for operating the CPU and peripheral functions.
- Prescaler S (PSS) is a 13-bit counter with clock input of ϕ. PSS is incremented every cycle.
- Timer counter WD (TCWD) is an 8-bit readable/writable up-counter that is incremented by internal clock input. The input clock is system clock/8192.
- Timer control/status register WD (TCSRWD) is an 8-bit readable/writable register that controls write to TCSRWD and TCWD, controls watchdog timer operation, and reflects the operation states.
- The TCWD overflow cycle in this sample task is calculated by the following equation:

$$\text{TCWD overflow cycle} = \frac{1}{\text{System clock/8192}} \times (256 - (\text{TCWD reload value}))$$

$$= 0.152\ \text{ms} \times (256 - 16)$$

$$= 122.88\ \text{ms}$$

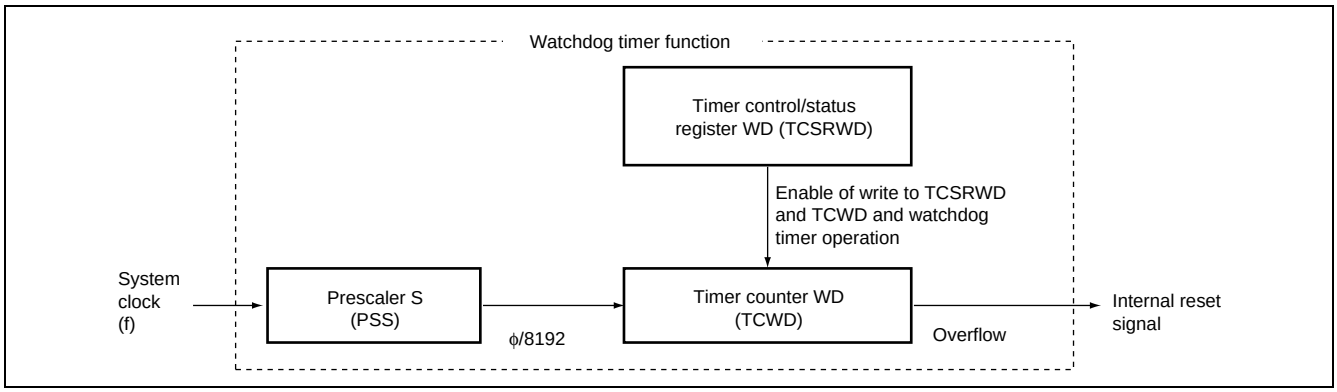


Figure 2.1 Watchdog Timer

Table 2.1 lists the function allocation for this sample task. The functions listed in table 2.1 are allocated so that the watchdog timer is operated.

Table 2.1 Function Allocation

Function	Description
PSS	13-bit counter with system clock input
TCWD	8-bit counter with clock input of system clock/8192
TCSRWD	Controls write to TCSRWD and TCWD, controls watchdog timer operation, and shows the operation states
$\overline{\text{IRQ0}}$	Switch input pin
$P7_4$	LED output

3. Description of Operations

Figure 3.1 shows this sample task's principle of operation. The hardware and software processing shown in figure 3.1 applies the watchdog timer to operate.

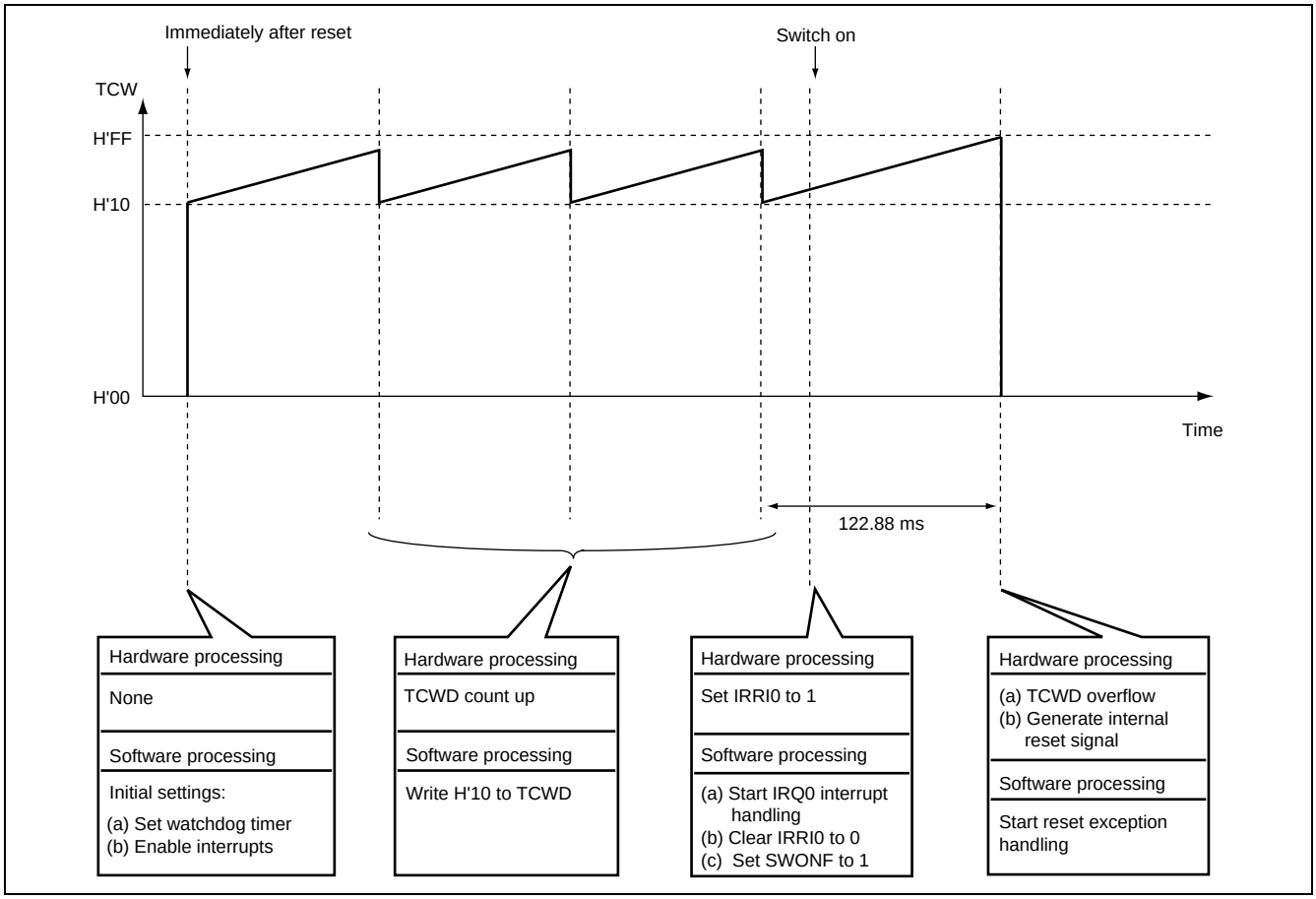


Figure 3.1 Operation Principle: Watchdog Timer Operation

4. Description of Software

4.1 Description of Modules

Table 4.1 describes the software used in this sample task.

Table 4.1 Description of Modules

Module Name	Label Name	Function
Main routine	main	Sets the watchdog timer to operate, enables interrupts, controls the LED, and judges whether or not the switch connected to the $\overline{\text{IRQ0}}$ input pin is turned on.
Switch on	IRQ0	During the IRQ_0 interrupt handling routine, sets SWONF to 1.

4.2 Description of Arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers

Table 4.2 describes the internal registers used in this sample task.

Table 4.2 Description of Internal Registers

Register Name		Function	Address	Setting
TCSRWD	B6W1	Timer control/status register WD (bit 6 write inhibit): When B6W1 is cleared to 0, writing to bit 6 in TCSRWD is enabled. When B6W1 is set to 1, writing to bit 6 in TCSRWD is disabled.	H'FFC0 Bit 7	 1
	TCWE	Timer control/status register WD (timer counter WD write enable): When TWCE is set to 1, writing of 8-bit data to TCWD is enabled.	H'FFC0 Bit 6	 1
	B4W1	Timer control/status register WD (bit 4 write inhibit): When B4W1 is cleared to 0, writing to bit 4 in TCSRWD is enabled. When B4W1 is set to 1, writing to bit 4 in TCSRWD is disabled.	H'FFC0 Bit 5	 1
	TCSRWE	Timer control/status register WD (timer control/status register W write enable): When TCSRWE is set to 1, writing to bits 2 and 0 in TCSRWD is enabled.	H'FFC0 Bit 4	 1

Table 4.2 Description of Internal Registers (cont)

Register Name		Function	Address	Setting
TCSRWD (cont)	B2W1	Timer control/status register WD (bit 2 write inhibit): When B2W1 is cleared to 0, writing to bit 2 in TCSRWD is enabled. When B2W1 is set to 1, writing to bit 2 in TCSRWD is disabled.	H'FFC0 Bit 3	 1
	WDON	Timer control/status register WD (watchdog timer on): When WDON is set to 1, watchdog timer operation is enabled.	H'FFC0 Bit 2	 1
	B0W1	Timer control/status register WD (bit 0 write inhibit): When B0W1 is cleared to 0, writing to bit 0 in TCSRWD is enabled. When B0W1 is set to 1, writing to bit 0 in TCSRWD is disabled.	H'FFC0 Bit 1	 1
	WRST	Timer control/status register WD (watchdog timer reset): When WRST is cleared to 0, TCWD has not overflowed and no internal reset signal has been generated. When WRST is set to 1, TCWD has overflowed and an internal reset signal has been generated.	H'FFC0 Bit 0	 1
TCWD		Timer counter WD: 8-bit counter incremented by clock input of system clock/8192.	H'FFC1	H'10
TMWD		Timer mode register WD (clock select 3 to 0): Selects TCWD input clock as system clock/8192.	H'FFC2	H'FF
PDR7	P74	Port data register 7 (port data register 7_4): When P74 is cleared to 0, the $P7_4$ pin output level is low. When P74 is set to 1, the $P7_4$ pin output level is high.	H'FFDA Bit 4	 0
PCR7	PCR74	Port control register 7 (port control register 7_4): When PCR74 is cleared to 0, the $P7_4$ pin functions as an input pin. When PCR74 is set to 1, the $P7_4$ pin functions as an output pin.	H'FFEA Bit 4	 1
PMR1	IRQ0_SET	Port mode register 1 ($P1_4$/$\overline{IRQ0}$ pin function switch): When IRQ0 is set to 1, the $P1_4$/$\overline{IRQ0}$ pin functions as the $\overline{IRQ0}$ input pin.	H'FFE0 Bit 4	 1
IEGR1	IEG0	Interrupt edge select register 1 (IRQ0 edge select): When IEG0 is cleared to 0, the falling edge of the $\overline{IRQ0}$ pin input is detected. When IEG0 is set to 1, the rising edge of the $\overline{IRQ0}$ pin input is detected.	H'FFF2 Bit 0	 0
IENR1	IEN0	Interrupt enable register 1 (IRQ0 interrupt enable): When IEN0 is set to 1, interrupt requests from the $\overline{IRQ0}$ pin are enabled.	H'FFF4 Bit 0	 1
IRR1	IRRI0	Interrupt flag register 1 (IRQ0 interrupt request flag): When IRRI0 is cleared to 0, no IRQ_0 interrupt is requested. When IRRI0 is set to 1, an IRQ_0 interrupt is requested.	H'FFF6 Bit 0	 0

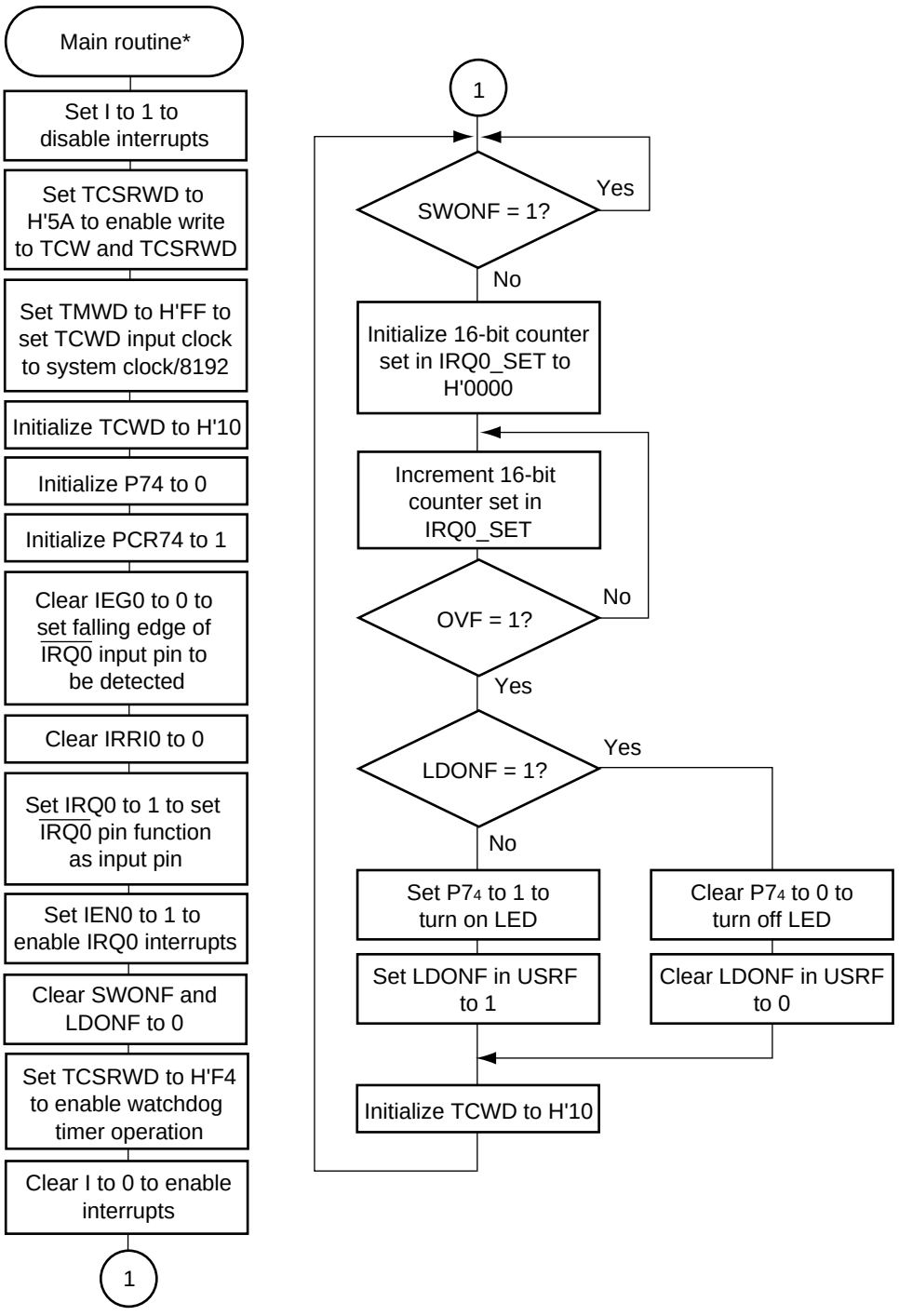
4.4 Description of RAM

Table 4.3 describes the RAM used in this sample task.

Table 4.3 Description of RAM

Label Name		Function	Address	Used in
counter_int		Up-counter that turns on or off the LED	H'FB80	Main routine
USRF	SWONF	Flag for judging on/off of the switch	H'FB82 Bit 0	Main routine Switch on
	LDONF	Flag for judging on/off of the LED	H'FB82 Bit 1	Main routine

5. Flowcharts



Note: In this sample task, the stack pointer is set in INIT.SRC (assembly).

Figure 5.1 Flowchart for Main Routine

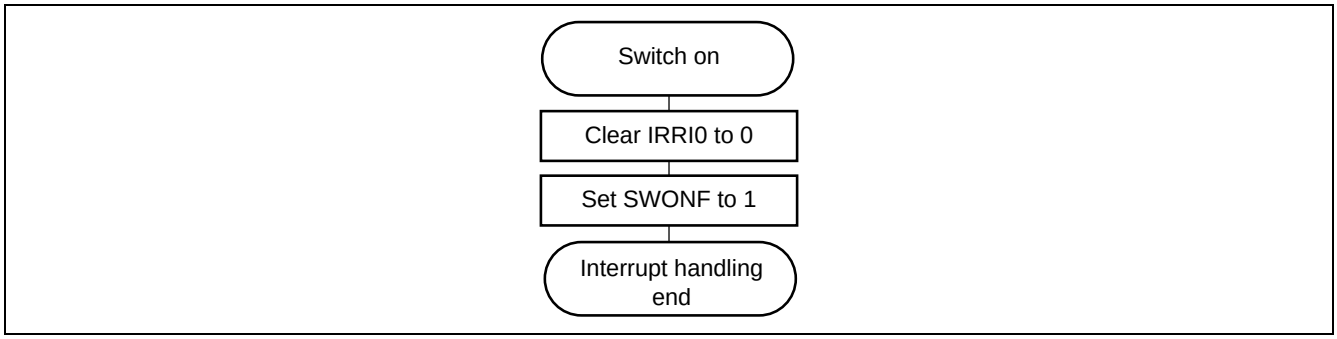


Figure 5.2 Flowchart for IRQ_0 Interrupt Handling Routine

6. Program Listing

INIT.SRC (Program listing)

```
      .EXPORT  _INIT
      .IMPORT  _main
 ;
      .SECTION    P,CODE
 _INIT:
      MOV.W    #H'FF80,R7
      LDC.B    #B'10000000,CCR
      JMP      @_main
 ;
      .END
```

```
/************************************************************/
/*                                                          */
/*    H8/300H Tiny Series -H8/3664-                         */
/*    Application Note                                      */
/*                                                          */
/*    'Watchdog Timer'                                      */
/*                                                          */
/*    Function                                              */
/*    : Watchdog Timer                                      */
/*                                                          */
/*    External Clock : 16MHz                                */
/*    Internal Clock : 16MHz                                */
/*    Sub Clock      : 32.768kHz                            */
/*                                                          */
/************************************************************/

#include    <machine.h>
```

```
/************************************************************/
/*    Symbol Defnition                                      */
/************************************************************/
struct BIT {
    unsigned char    b7:1;      /* bit7 */
    unsigned char    b6:1;      /* bit6 */
    unsigned char    b5:1;      /* bit5 */
    unsigned char    b4:1;      /* bit4 */
    unsigned char    b3:1;      /* bit3 */
    unsigned char    b2:1;      /* bit2 */
    unsigned char    b1:1;      /* bit1 */
    unsigned char    b0:1;      /* bit0 */
};

#define    TCSRWD     *(volatile unsigned char *)0xFFC0  /* Timer Control/Status Register WD             */
#define    TCSRWD_BIT (*(struct BIT *)0xFFC0)            /* Timer Control/Status Register WD             */
#define    B6WI       TCSRWD_BIT.b7                      /* Bit-6 Write Disable                          */
#define    TCWE       TCSRWD_BIT.b6                      /* Timer Counter W Write Enable                 */
#define    B4WI       TCSRWD_BIT.b5                      /* Bit-4 Write Disable                          */
#define    TCSRWE     TCSRWD_BIT.b4                      /* Timer Control/Status Register W Write Enable */
#define    B2WI       TCSRWD_BIT.b3                      /* Bit-2 Write Disable                          */
#define    WDON       TCSRWD_BIT.b2                      /* Watchdog Timer ON                            */
#define    B0WI       TCSRWD_BIT.b1                      /* Bit-0 Write Disable                          */
#define    WRST       TCSRWD_BIT.b0                      /* Watchdog Timer Reset                         */
#define    TCWD       *(volatile unsigned char *)0xFFC1  /* Timer Counter WD                             */
#define    TMWD       *(volatile unsigned char *)0xFFC2  /* Timer Mode WD                                */
#define    PDR7_BIT   (*(struct BIT *)0xFFDA)            /* Port Data Register 7                         */
#define    P74        PDR7_BIT.b4                        /* Port Data Register 7 bit4                    */
#define    PCR7_BIT   (*(struct BIT *)0xFFEA)            /* Port Control Register 7                      */
#define    PCR74      PCR7_BIT.b4                        /* Port Control Register 7 bit4                 */
#define    IEGR1_BIT  (*(struct BIT *)0xFFF2)            /* Interupt Edge Select Register 2              */
#define    IEG0       IEGR1_BIT.b0                       /* IEG0 Edge Select                             */
#define    IENR1_BIT  (*(struct BIT *)0xFFF4)            /* Interrupt Enable Register 1                  */
#define    IEN0       IENR1_BIT.b0                       /* IEN0 Inetrrupt Enable                        */
#define    IRR1_BIT   (*(struct BIT *)0xFFF6)            /* Interrupt Request Register 1                 */
#define    IRRI0      IRR1_BIT.b0                        /* IRRI0 Interrupt Request Register             */
#define    PMR1_BIT   (*(struct BIT *)0xFFE0)            /* Prot Mode Register 1                         */
#define    IRQ0_SET   PMR1_BIT.b4                        /* Prot Mode Register 1 bit4                    */
```

```
#pragma        interrupt    (IRQ0)

/************************************************************/
/*     Function Definition                                  */
/************************************************************/
extern    void    INIT ( void );                    /* SP Set                              */
void    main ( void );
void    IRQ0 ( void );

/************************************************************/
/*    RAM define                                            */
/************************************************************/
    unsigned int    counter_int;
    unsigned char    USRF;                          /* User Flag Erea                      */

#define        USRF_BIT    (*(struct BIT *)&USRF)
#define        SWONF        USRF_BIT.b0
#define        LDONF        USRF_BIT.b1

/************************************************************/
/*    Vector Address                                        */
/************************************************************/
#pragma    section        V1                         /* VECTOR SECTOIN SET                  */
void (*const VEC_TBL1[])(void) = {
    INIT                                              /* 00 Reset                            */
};
#pragma    section        V2                         /* VECTOR SECTOIN SET                  */
void (*const VEC_TBL2[])(void) = {
    IRQ0                                              /* IRQ0  Interrupt                     */
};
#pragma    section                                   /* P                                   */
```

```
/************************************************************/
/*    Main Program                                          */
/************************************************************/
void    main ( void )
{

    set_imask_ccr(1);                           /* Interrupt Disable                        */

    TCSRWD = 0x5A;                              /* TCWD And TCSRWD Write Enable             */

    TMWD = 0xFF;                                /* Initialize TMWD                          */

    TCWD = 0x10;                                /* Initialize TCWD                          */

    P74 = 0;                                    /* Initialize P74 Terminal Output Level     */

    PCR74 = 1;                                  /* Initialize PCR74  Output Terminal Function */

    IEG0 = 1;                                   /* Initialize IRQ0  Terminal Input Edge     */
    IRRI0 = 0;                                  /* Initialize IRQ0 Interrupt Request Flag   */
    IRQ0_SET = 1;                               /* Initialize IRQ0  Input Terminal          */
    IEN0 = 1;                                   /* IRQ0 Interrupt Enabie                    */

    SWONF = 0;                                  /* Initialize SWONF                         */
    LDONF = 0;                                  /* Initialize LDONF                         */

    TCSRWD = 0xF4;                              /* Watchdog Timer On                        */

    set_imask_ccr(0);                           /* Interrupt Enable                         */

    while(1){
        while(SWONF == 1){                      /* SWONF = 1 ?                              */
            ;
        }

        counter_int = 0;                        /* counter Clear                            */
        do{
            counter_int ++;                     /* counter Countup                          */
        }while(counter_int != 0);               /* counter_int = FFFF ?                     */
```

```
        if(LDONF == 1){

           P74 = 0;                                  /* Turn    Off    LED                  */
            LDONF = 0;                               /* LDONF Clear                         */
        }else{
            P74 = 1;                                 /* Turn    On    LED                   */
            LDONF = 1;                               /* LDONF set                           */
    }

    TCWD = 0x10;                                     /* Initialize TCWD                     */

    }


}
/************************************************************/
/*    IRQ0 Interrupt                                        */
/************************************************************/
void    IRQ0 ( void )
{

    IRRI0 = 0;                                       /* Clear    IRRI0                      */

    SWONF = 1;                                       /* Set SWONF                           */

}
```

Link Address Setting:

Section Name	Address
CV1	H'0000
CV2	H'001C
P	H'0100
B	H'FB80