ZSC31050 / Differential Sensor Signal Conditioner

Application Circuits for Serial Communication

Abstract

This application note describes the basic theories and application circuits for the ZSC31050's various types of communication.

Contents

Figures

Tables

1. Basics of Serial Communication with ZSC31050

The ZSC31050 acts as slave module only with the standard slave address “0x78”. But it is possible to set an individual 7-bit slave address for a selective I2C communication with a single ZSC31050 slave (not valid for ZACwire™ and SPI communication). By the PMOS transistor the ZSC31050 can be turned ON/OFF, thus a controlled START-STOP sequence can be programmed by using the implemented **P**ower **O**n **R**eset functionality of the ZSC31050. For details please refer the ZSC31050’s functional description. In terms of the module’ s PCB layout cross-coupling between the chosen serial interface and the input lines of the sensor element must be avoided, otherwise a running communication could cause additional noise or incorrect output values.

2. I²C Communication

At the SCL line, the master generates the clock signal. The SDA line is used for data transmission from master to slave and vice versa, controlled by the master.

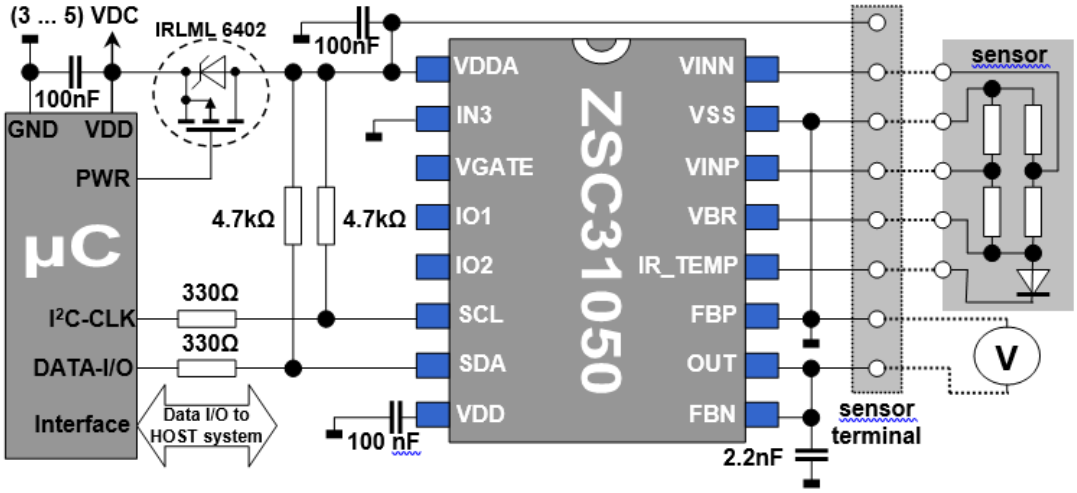


Figure 1. ZSC31050 Application Circuit, I²C Communication

3. ZACwire™ Communication

The ZACwire™-line is used for data transmission from master to slave and vice versa, controlled by the master. No separate clock signal is needed to synchronize the communication.

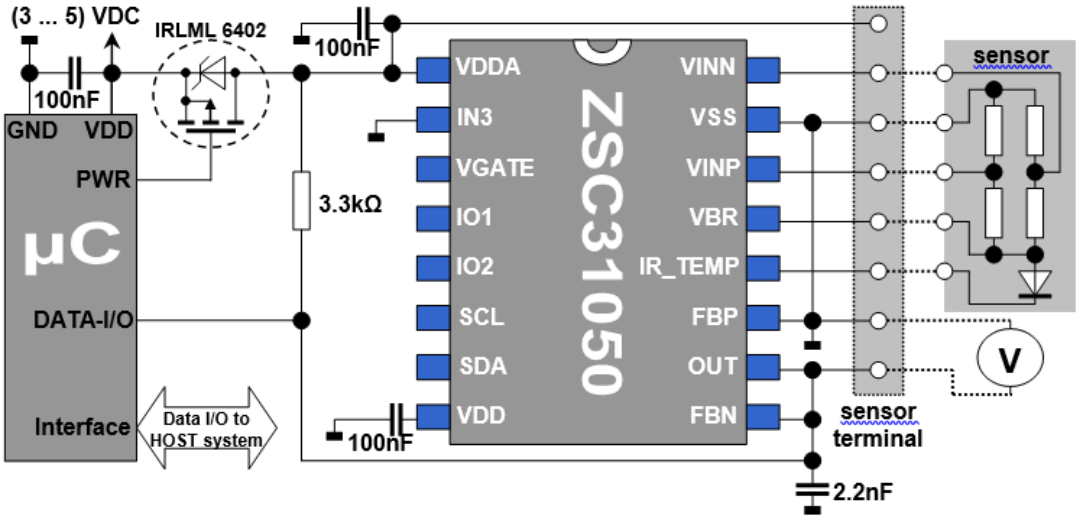


Figure 2. ZSC31050 Application Circuit, ZACwire™ Communication

The bit-time can be adjusted by the ZACwire-master between 20µs and 100µs, the ZACwire-slave (= ZSC31050) is synchronized by the bit-time of the last received bit before a STOP condition is detected. The bit-time depends on the values of the external pull-up-resistor and of the capacitive load at the ZACwire line. The calculation of these values and of the allowed ZACwire line resistance is specified in chapter 5.5.2 of the datasheet, please refer also chapter 4.3 of the functional description.

4. SPI Communication

At the SCL line the master generates the SPI clock signal. The SDA line is used for data transmission from master to slave (MOSI), the IO1 line is used for data transmission from slave to master (MISO) and the IO2 line is used for the slave select signal (/SS).

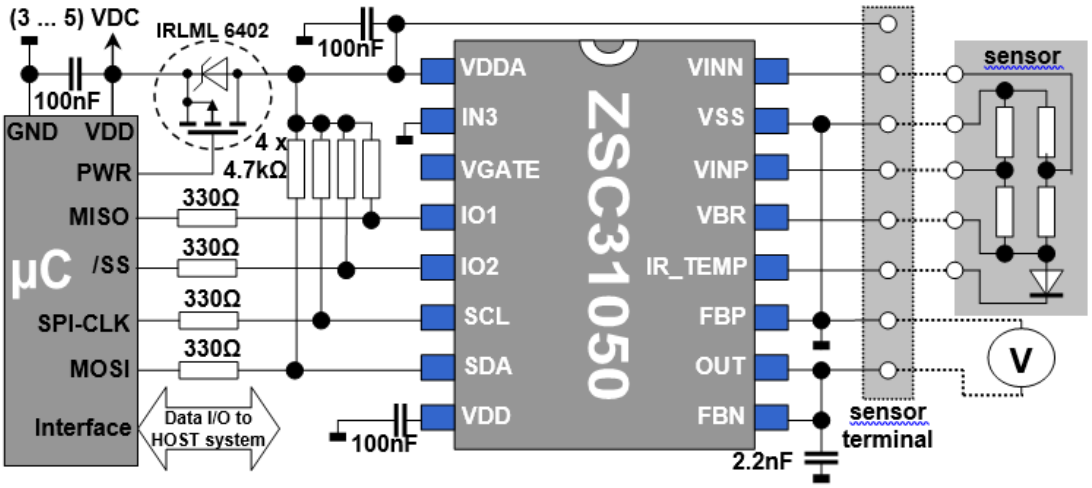


Figure 3. ZSC31050 Application Circuit, SPI Communication

For correct communication via SPI, the /SS signal needs to be detected by the slave (= ZSC31050) before the first sampling edge of the SPI clock signal is detected by this slave. This timing has to be controlled by the SPI master with respect to:

- The SPI configuration of the ZSC31050 (bit 1 and 2 of register 23 / refer functional description)
- The adjusted clock frequency of the ZSC31050 (default value = 2MHz / refer chapter 4.1)
- The application circuit (e.g. the values of the pull-up-resistors)
- The layout of the module's PCB (load capacitances of the SPI communication lines)
- The wiring to the SPI slave (e.g. impedances of the SPI communication lines)

4.1 Initialization of SPI Communication

The default communication initialization of ZSC31050 is OWI (= ZACwire™) or I2C communication. To configure the ZSC31050 for SPI communication an OWI- or I2C command sequence has to be send to re-program register 23 of the ZSC31050 (for details, refer to chapter 4.3).

- SPI-communication has to be programmed in SPI mode in register CFGSIF (0x17) of ZSC31050 depending on the master's SPI communication adjust. SPI communication with the SSC Communication Board (CB) of ZSC31050 Evaluation Kit requires the described adjustment for the interface open command:

  SO_200011 = > CFGSIF:SIFMD = 1, CFGSIF:SPICKP = 0 and CFGSIF:SPICKE = 0

- SPI communication speed has to be adjusted in such manner that SPI clock frequency is in minimum 5 times slower than ZSC31050's internal clock frequency. Thus, the use of the CB's clock frequency adjust of 500kHz (➔ "SO_2…") is recommended for ZSC31050's default clock frequency initialization.

4.2 SPI Connection Wires

CB Pin	SCK	MOSI	MISO	/SS
ZSC31050 Pin	SCL	SDA	IO1	IO2

4.3 SPI Communication Example

The I2C communication is used in following examples to adjust/program SPI communication mode of ZSC31050.

4.3.1. SPI Activation by Usage of Communication Mode Adjust Command

- I2C wiring (connect SCL, SDA, VSS and VDDA (KS5V) only and left IO2 open)

  T11100
  IWT7800172
  IW_7800151 (set interface = SPI – only in RAM)
  ➔ Rewire for SPI (don't disconnect power) and send SPI commands (refer chapter 4.4)

4.3.2. Writing SPI Mode into EEPROM

- Use I2C to initialize SPI communication in EEPROM
- I2C wiring (connect SCL, SDA, VSS and VDDA (KS5V) only and left IO2 open)

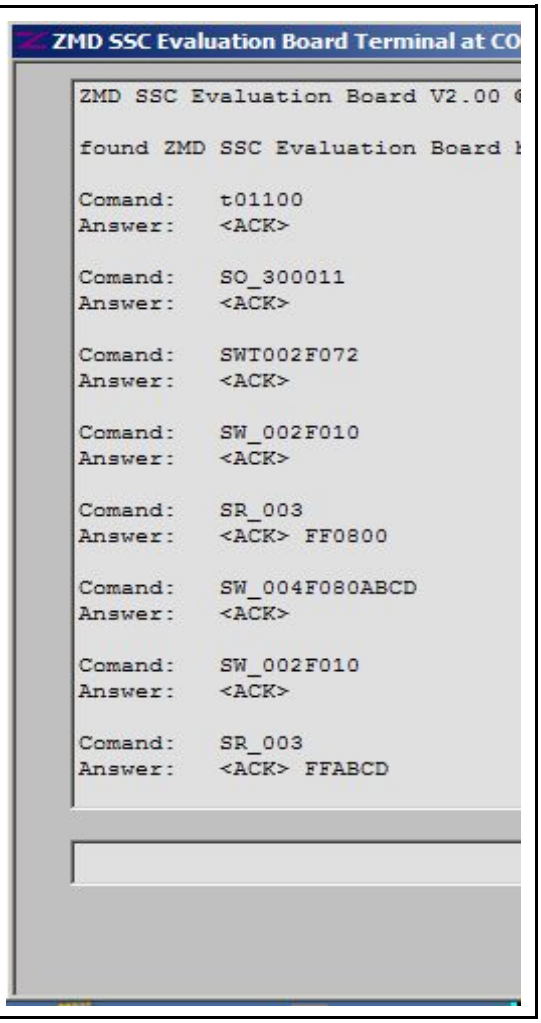
  T11100 : trigger timer for I^2C
  IWT7800172 : command mode
  IW_7800327 : command to read register 0x17
  IR_78002 : read register content
  => "F034" : content is 0xF034
  IW_78003B7F031 : write SPI communication setup for SO_200011 into EEPROM
  IW_78001C9 : recalculate and write EEPROM signature
  …Power ➔ OFF, re-wire for SPI and send SPI commands (refer chapter 4.4)

4.4 Communication (USB-KIT Commands)

Use the terminal program "ZMDI SSC terminal" or "ZSC31050.exe" for communication verification. Refer SPI page at CB command description “ZSC31xxxKIT_CommandSyntax_Rev_*.xls” for details.

Table 1. Communication (USB-KIT Commands)

Command	Description
T01100	Use KS5V supply channel with 100ms communication delay
SO_200011	Configure SPI Interface for ZSC31050-IF mode = “51” or 3 LSB-bits of register 0x17 = “001” (500kHz, CKP=LOW, CPE = LOW, low active chip select)
SWT002F072	Power On and setting Cmd-Mode
SW_002F010	Cmd for reading register 0x00
SR_003	3 Byte SIF Read
=> "FF0800"	Result is: "FF0800" register 0x00 content = "0800"
SW_004F080ABCD	Writing data “ABCD” to reg 0x00
SW_002F010	Cmd for reading register 0x00 (= write verification)
SR_003	3 Byte SIF Read
=> "FFABCD"	Result is: "FFABCD" register 0x00 content = "ABCD"



5. Revision History

Revision	Date	Description
1.00	Mar.17.20	Initial release.

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