Interface IP

MIPI D-PHY Receiver for TSMC 22nm ULP

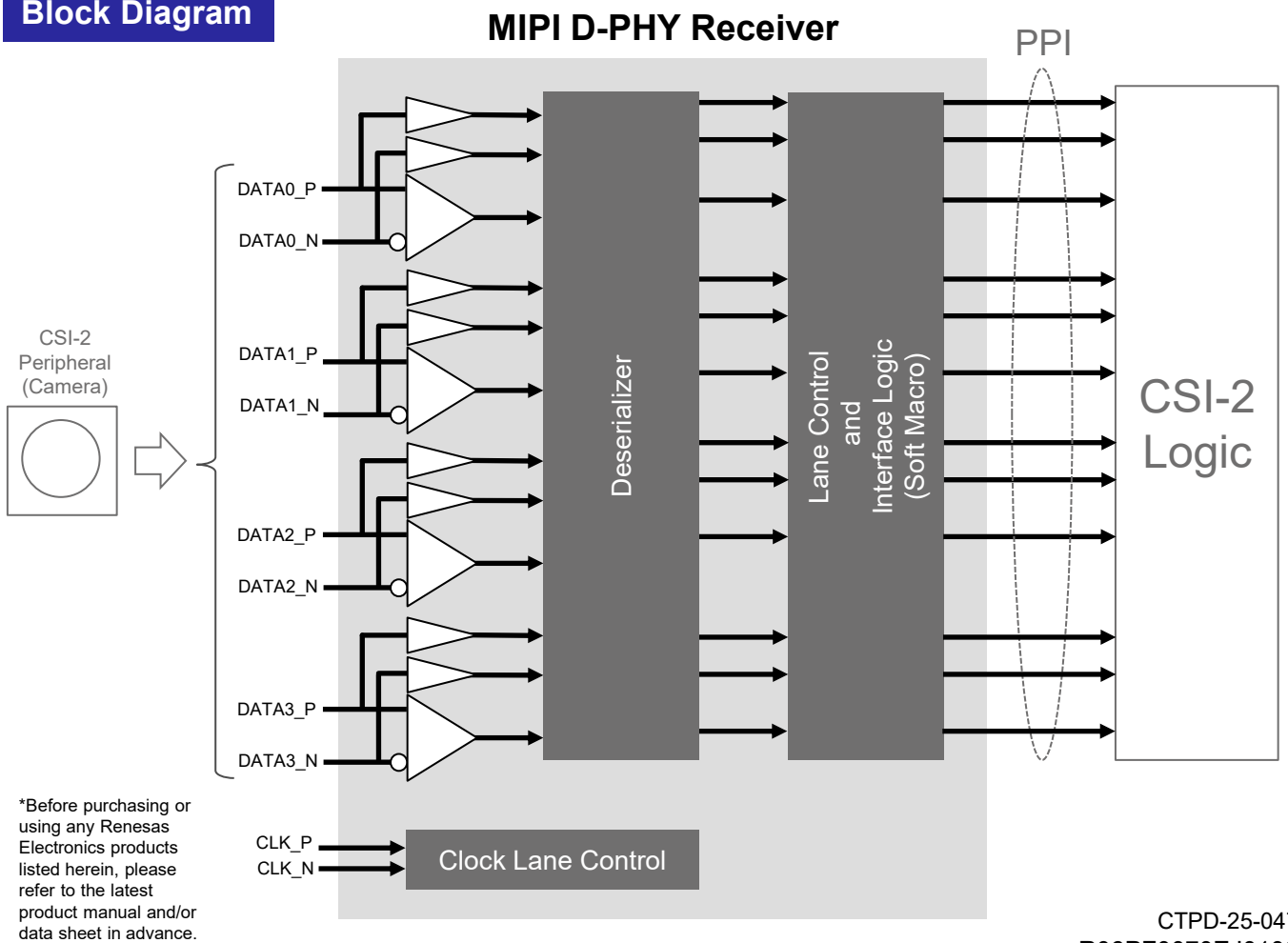
Overview

The Renesas MIPI® D-PHY™ Receiver is useful 4 Data Lanes receiver hard macro for CSI-2® of TSMC 22nm ULP process.

Features

- Renesas MIPI D-PHY Receiver can be used for analog Receiver of following interface .
  - MIPI alliance Specification for D-PHY Version 2.1 15 December 2016.
  - MIPI alliance Specification for Camera Serial Interface 2 (CSI-2) Version 2.0 7 Dec 2016.
- Technology is TSMC 22nm ULP 1p10M.
- Supply voltage can be applied 0.9V for core voltage, 1.8V for IO voltage.
- Maximum data rate of each channel is 1.5Gbps at High-speed mode.

Block Diagram



*Before purchasing or using any Renesas Electronics products listed herein, please refer to the latest product manual and/or data sheet in advance.

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