Interface IP

MIPI D-PHY Transmitter/Receiver for TSMC 40nm LP

Overview

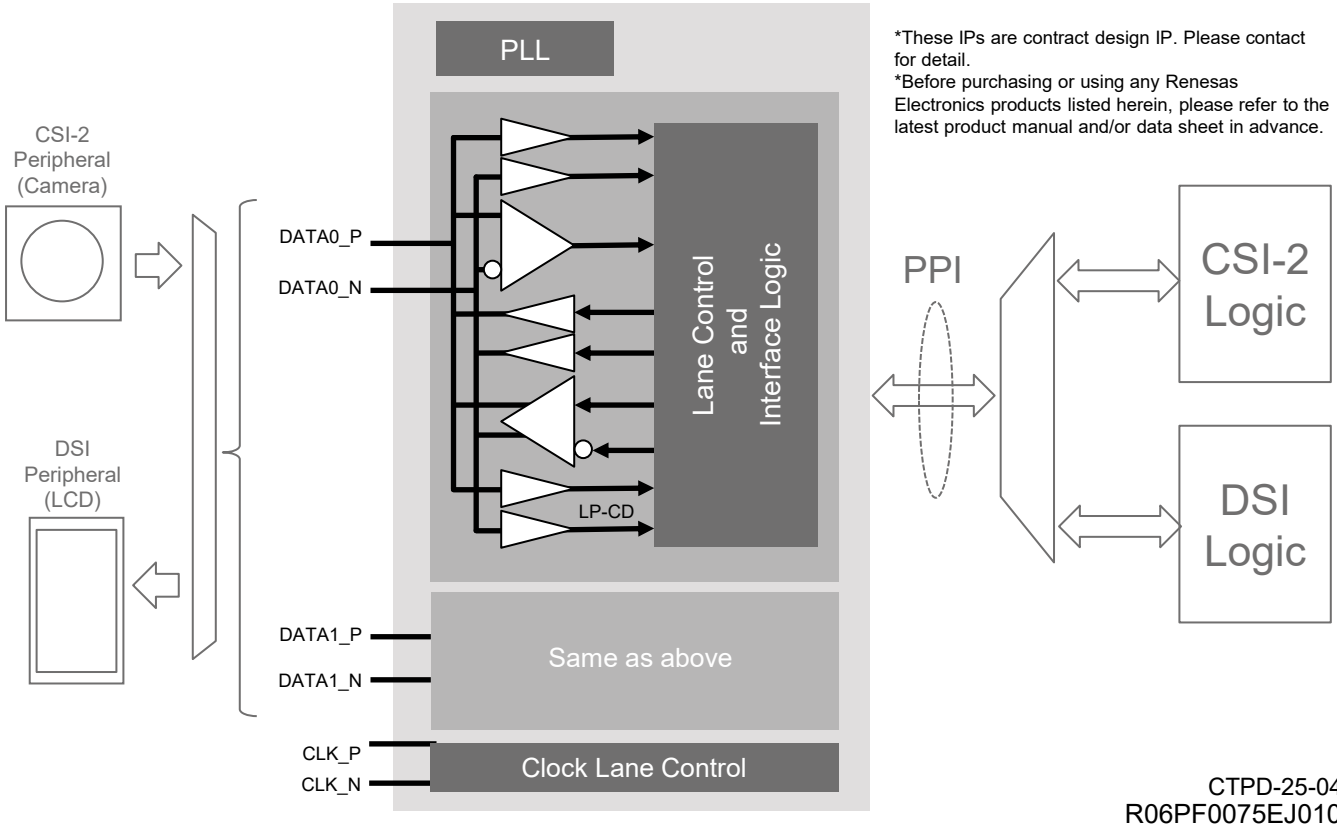
The Renesas MIPI® D-PHY™ Transmitter/Receiver is useful 2 Data Lanes transmitter/receiver hard macro for DSI℠/CSI-2® of TSMC 40nm LP process.

Features

- Renesas MIPI D-PHY Transmitter/Receiver can be used for analog Transmitter/Receiver of following interface .
  - MIPI alliance Specification for D-PHY Version 2.1 15 December 2016.
  - MIPI alliance Specification for Display Serial Interface (DSI) Version 1.3.1 Aug 2015.
  - MIPI alliance Specification for Camera Serial Interface 2 (CSI-2) Version 2.0 7 Dec 2016.
- Technology is TSMC 40nm LP 1p6M.
- Supply voltage can be applied 1.1V for core voltage, 1.8V for IO voltage.
- Maximum data rate of each channel is 0.72Gbps at High-speed mode.

Block Diagram

MIPI D-PHY Transmitter/Receiver



*These IPs are contract design IP. Please contact for detail.
*Before purchasing or using any Renesas Electronics products listed herein, please refer to the latest product manual and/or data sheet in advance.

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