



IDTP95020 Data Sheet Errata

Revision A03

This errata sheet only pertains to the IDTP95020 integrated circuit revision with part marking ZC and ZD and the IDTP95020 datasheet (Revision 1.3, dated September 2, 2011) and describes situations where the IDTP95020 component may perform differently than expected or differently than shown in the datasheet. Integrated Device Technology, Inc. intends to correct errata items in a subsequent revision of the device. For more information on the IDT95020, please visit our website at <http://www.idt.com/?genID=IDTP95020>.

Revision History

June 9, 2011; Rev. A01 errata sheet created with item #1.

July 28, 2011; Rev. A02 errata sheet added items #2 and #3.

September 02, 2011; Rev. A03 errata sheet removed items #2 and #3 which have been added to the datasheet.

Errata Items:

1 - Buck Regulators – Control Register - Cycle by Cycle Current Limit [3:2] (Table 149 on page 90 in the datasheet and below) - Use of this control register allows for the peak inductor current to be programmed to 1 of 4 ratios of the current limit; however, the lower three settings are disabled and must not be used. The only valid setting is the 100% [1:1] limit (see I_{CLP} electrical characteristic on page 94 in the datasheet and below). Use of the other three register settings may result in catastrophic damage or reduced lifespan of the regulator, the IC, or the load that the regulator is supporting. It is not recommended that this register be programmed to any value other than 100% [1:1] of the current limit which is the default register setting.

Table 1. Control Register Cycle by Cycle Current Limit (I_{LIM}) Settings for Bits [3:2]

BIT 3	BIT 2	DESCRIPTION
0	0	Current Limit = 25 % (Do Not Use this setting)
0	1	Current Limit = 50 % (Do Not Use this setting)
1	0	Current Limit = 75 % (Do Not Use this setting)
1	1	Current Limit = 100 % [Note]above

Note: Current Limit is at maximum when bits [3:2] are both set to 1.

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
I_{CLP}	Full Scale Cycle by Cycle Current Limit (BUCK500) Full Scale Cycle by Cycle Current Limit (BUCK1000)	0xA081 [3:2], 0xA083 [3:2], 0xA085 [3:2] both bits set to 1	650 1200		1050 1800	mA _{PK}



IDTP95020 Data Sheet Errata

Revision A03



www.IDT.com

**6024 Silver Creek Valley Road
San Jose, California 95138**

Tel: 800-345-7015

DISCLAIMER Integrated Device Technology, Inc. (IDT) and its subsidiaries reserve the right to modify the products and/or specifications described herein at any time and at IDT's sole discretion. All information in this document, including descriptions of product features and performance, is subject to change without notice. Performance specifications and the operating parameters of the described products are determined in the independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties. IDT's products are not intended for use in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

Integrated Device Technology, IDT and the IDT logo are registered trademarks of IDT. Other trademarks and service marks used or design, are the property of IDT or their respective third party owners.

© Copyright 2011. All rights reserved.