1.8V to 3.3V, High-Performance 1:4 Clock Buffer

2304NZL

DATASHEET

Description

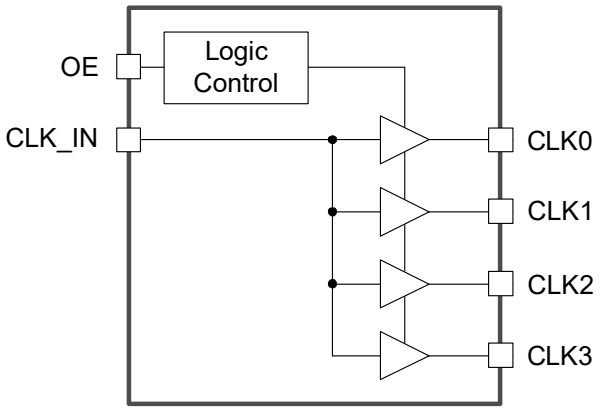
The 2304NZL is a high-performance, low skew, low jitter 1:4 LVCMOS clock buffer. The 2304NZL is ideal for PCI/PCI-X or networking applications.

The 2304NZL supports a synchronous glitch-free Output Enable function to eliminate any potential intermediate incorrect output clock cycles when enabling or disabling outputs.

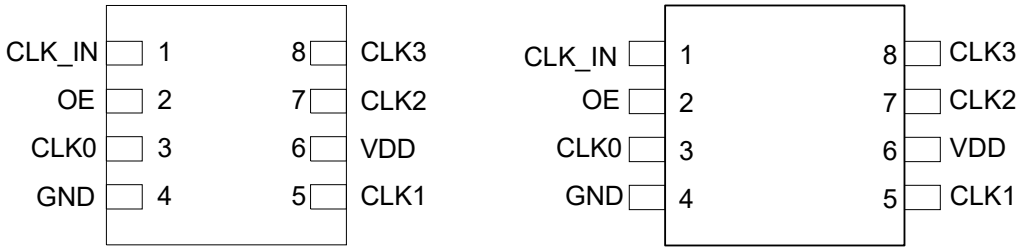
Features

- Low input to output propagation delay (1.8ns, 3.3V)
- Low output skew: 40ps max
- Glitch-free Output Enable Function
- 1.8V to 3.3V power supply
- Packaged in small 8-pin 2 x 2 mm DFN package, as well as standard TSSOP and SOIC packages
- Industrial temperature range (-40°C to +85°C)

Block Diagram



Pin Assignment



8-pin DFN

8-pin TSSOP/SOIC

Functionality Table

Inputs		Outputs
CLK_IN	**OE**	**CLK(3:0)**
0	0	Low
0	1	0
1	0	Low
1	1	1

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	CLK_IN	Input	Clock input.
2	OE	Input	Output Enable for the clock outputs. Outputs are enabled when forced HIGH. Outputs are forced to logic LOW when OE is forced LOW.
3	CLK0	Output	Clock output 0.
4	GND	Power	Power supply ground.
5	CLK1	Output	Clock output 1.
6	VDD	Power	Connect +1.8V, +2.5V or +3.3V power supply.
7	CLK2	Output	Clock output 2.
8	CLK3	Output	Clock output 3.

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01µF should be connected between VDD on pin 6 and GND on pin 4, as close to the device as possible. A termination resistor should be used on each clock output if the trace is longer than 1 inch. See the Test Loads section for recommended values.

To achieve the low output skew that the 2304NZL is capable of, careful attention must be paid to board layout. Essentially, all four outputs must have identical terminations, identical loads and identical trace geometries. If they do not, the output skew will be degraded.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 2304NZL. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	Power supply			4.6	V
Output Enable and All Outputs	V_{IO}	With respect to GND	-0.5		VDD+0.5	V
ICLK	V_{IN}	Input Voltage	-0.5		4.6	V
Ambient Operating Temperature	T_{AMB}	Industrial Temperature	-40		85	°C
Storage Temperature	T_{STORE}	Storage Temperature	-65		150	°C
Junction Temperature	T_J	Junction Temperature			125	°C
Soldering Temperature	T_{SOLDER}	Soldering Temperature			260	°C
ESD	ESD	Human Body Model	2000			V

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Temperature	T_{AMB}	Ambient	-40	25	85	°C
Power Supply Voltage	V_{DD}	With respect to GND	1.7		3.465	V

DC Electrical Characteristics

VDD = 1.8 V ±5%, Ambient temperature -40° to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Voltage	V_{DD}		1.71	1.8	1.89	V
Input High Voltage (CLK_IN, OE)	V_{IH}	Note 1	0.8xVDD		3.45	V
Input Low Voltage (CLK_IN, OE)	V_{IL}	Note 1			0.2xVDD	V
Output High Voltage	V_{OH}	I_{OH} = -2 mA	0.9xVDD			V
Output Low Voltage	V_{OL}	I_{OH} = 2 mA			0.1xVDD	V
Operating Supply Current	I_{DD}	No load, 50MHz		8		mA
Nominal Output Impedance	Z_O			20		Ω
Input Capacitance	C_{IN}	CLK_IN, OE pin		5		pF

Notes: 1. Nominal switching threshold is VDD/2.

VDD = 2.5 V ±5%, Ambient temperature -40° to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Voltage	V_{DD}		2.375	2.5	2.625	V
Input High Voltage(CLK_IN, OE)	V_{IH}	Note 1	0.8xVDD		3.45	V
Input Low Voltage(CLK_IN, OE)	V_{IL}	Note 1			0.2xVDD	V
Output High Voltage	V_{OH}	I_{OH} = -2 mA	0.9xVDD			V
Output Low Voltage	V_{OL}	I_{OH} = 2 mA			0.1xVDD	V
Operating Supply Current	I_{DD}	No load, 50MHz		10		mA
Nominal Output Impedance	Z_O			21		Ω
Input Capacitance	C_{IN}	CLK_IN, OE pin		5		pF

Notes: 1. Nominal switching threshold is VDD/2.

VDD = 3.3 V ±5%, Ambient temperature -40° to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Voltage	V_{DD}		3.135	3.3	3.465	V
Input High Voltage(CLK_IN, OE)	V_{IH}	Note 1	0.8xVDD		3.45	V
Input Low Voltage(CLK_IN, OE)	V_{IL}	Note 1			0.2xVDD	V
Output High Voltage	V_{OH}	I_{OH} = -2 mA	0.9xVDD			V
Output Low Voltage	V_{OL}	I_{OH} = 2 mA			0.1xVDD	V
Operating Supply Current	I_{DD}	No load, 50MHz		12		mA
Nominal Output Impedance	Z_O			25		Ω
Input Capacitance	C_{IN}	CLK_IN, OE pin		5		pF

Notes: 1. Nominal switching threshold is VDD/2.

AC Electrical Characteristics

VDD = 1.8V ±5%, Ambient Temperature -40° to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Frequency	Fin		0		170	MHz
Output Rise Time	t_{OR}	20% to 80% of VDD, C_L = 5 pF	0.7	1.1	1.5	ns
Output Fall Time	t_{OF}	80% to 20% of VDD, C_L = 5 pF	0.7	1.1	1.5	ns
Propagation Delay	Note 1		2.2	2.5	3.2	ns
Additive Phase Jitter, RMS		125MHz		100		fs
Duty Cycle		50% input duty cycle	45		55	%
Output to Output Skew	Note 2	Rising edges at VDD/2		15	40	ps
Device to Device Skew		Rising edges at VDD/2			500	ps

VDD = 2.5V ±5%, Ambient Temperature -40° to +85°C, unless stated otherwise

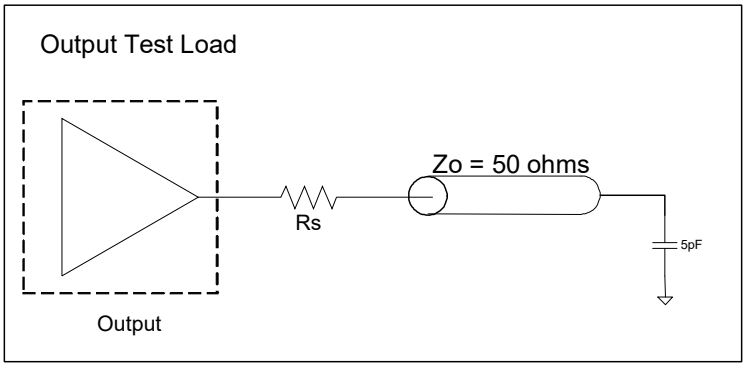
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Frequency	Fin		0		200	MHz
Output Rise Time	t_{OR}	20% to 80% of VDD, C_L = 5 pF	0.6	1	1.5	ns
Output Fall Time	t_{OF}	80% to 20% of VDD, C_L = 5 pF	0.6	1	1.5	ns
Propagation Delay	Note 1		1.4	1.9	2.4	ns
Additive Phase Jitter, RMS		125MHz		50		fs
Duty Cycle		50% input duty cycle	45		55	%
Output to Output Skew	Note 2	Rising edges at VDD/2		15	40	ps
Device to Device Skew		Rising edges at VDD/2			500	ps

VDD = 3.3 V ±5%, Ambient Temperature -40° to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Frequency	Fin		0		200	MHz
Output Rise Time	t_{OR}	20% to 80% of VDD, C_L = 5 pF	0.5	1	1.5	ns
Output Fall Time	t_{OF}	80% to 20% of VDD, C_L = 5 pF	0.5	1	1.5	ns
Propagation Delay	Note 1		1.1	1.7	2.1	ns
Additive Phase Jitter, RMS		125MHz		30		fs
Duty Cycle		50% input duty cycle	45		55	%
Output to Output Skew	Note 2	Rising edges at VDD/2		15	40	ps
Device to Device Skew		Rising edges at VDD/2			500	ps

Notes:
1. With rail to rail input clock.
2. Between any 2 outputs with equal loading.
3. Phase noise spec taken with Wenzel oscillator as reference input.

Test Load and Circuit



VDD	Rs (Ω)
1.8V	25
2.5V	29
3.3V	30

Thermal Characteristics (8DFN)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		81		°C/W
	θ_{JA}	1 m/s air flow		73		°C/W
	θ_{JA}	3 m/s air flow		70		°C/W
Thermal Resistance Junction to Case	θ_{JC}			10.6		°C/W

Thermal Characteristics (8TSSOP)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		110		°C/W
	θ_{JA}	1 m/s air flow		100		°C/W
	θ_{JA}	3 m/s air flow		80		°C/W
Thermal Resistance Junction to Case	θ_{JC}			35		°C/W

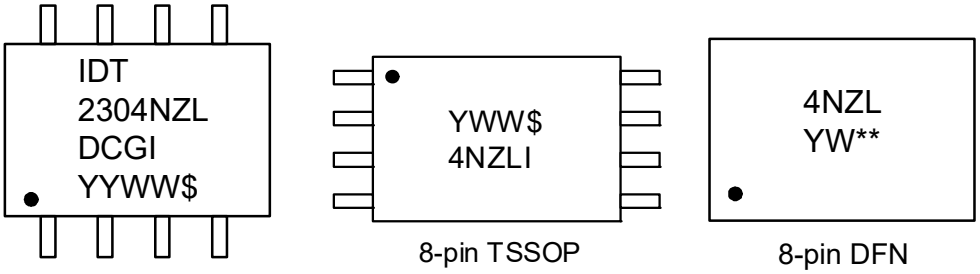
Thermal Characteristics (8SOIC)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		110		°C/W
	θ_{JA}	1 m/s air flow		100		°C/W
	θ_{JA}	3 m/s air flow		80		°C/W
Thermal Resistance Junction to Case	θ_{JC}			35		°C/W

Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

Marking Diagrams



8-pin SOIC 8-pin TSSOP 8-pin DFN

Notes:

1. "**" is the lot number (DFN only).
2. "YYWW" or "YWW" or "YW" is the digits of the year and week that the part was assembled.
3. "$" is the mark code.
4 "G" denotes RoHS compliant package.
5. "I" denotes industrial temperature range.
6. Bottom markings: lot number and country of origin for TSSOP; lot number for SOIC.

Ordering Information

Part Number	Carrier Type	Package	Temperature Range
2304NZLDCGI	Tubes	0.150" body, 0.050" pitch 8-SOIC	-40 to +85°
2304NZLDCGI8	Tape and Reel	0.150" body, 0.050" pitch 8-SOIC	-40 to +85°
2304NZLPGGI	Tubes	4.4mm body, 0.65mm pitch 8-TSSOP	-40 to +85°
2304NZLPGGI8	Tape and Reel	4.4mm body, 0.65mm pitch 8-TSSOP	-40 to +85°
2304NZLNTGI	Tubes	2.0 × 2.0 × 0.75 mm 8-DFN	-40 to +85°
2304NZLNTGI8	Tape and Reel	2.0 × 2.0 × 0.75 mm 8-DFN	-40 to +85°

"G" after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

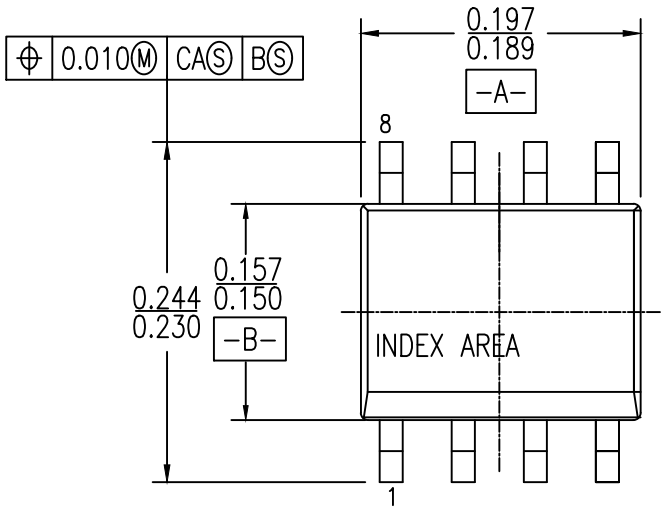
Revision History

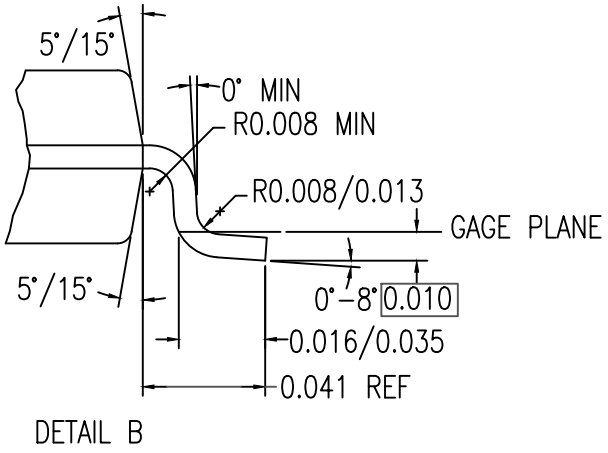
Date	Description
July 24, 2023	• Updated TSSOP marking diagram. • Updated Package Outline Drawings section. • Added POD links to ordering Information. • Rebranded to Renesas.
January 31, 2017	• Updates to operating supply current and output impedance values in DC electrical tables. • Added Rs values to test loads.
June 21, 2016	• Added marking diagrams. • Moved to final.

8-SOIC Package Outline Drawing

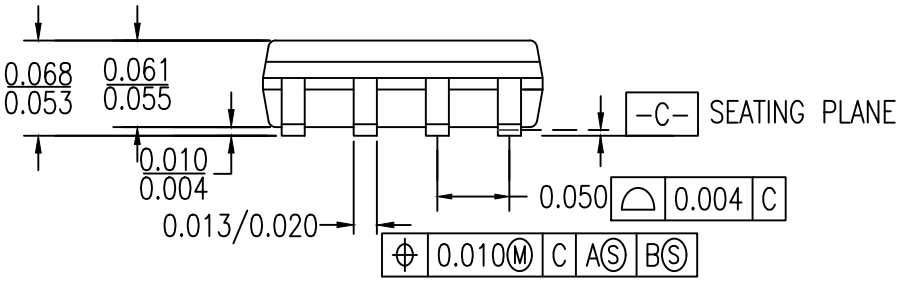
0.150" Body Width, 0.050" Pitch

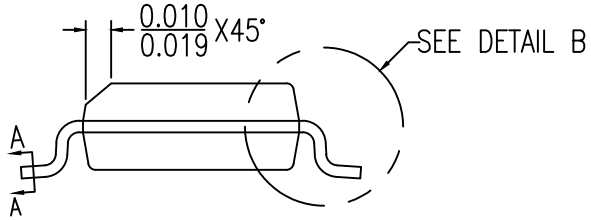
DCG8D1, PSC-4068-01, Rev 01, Page 1

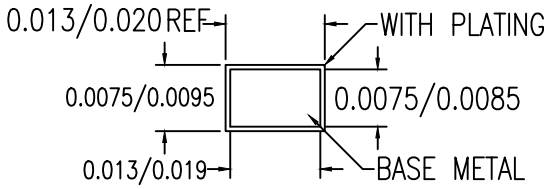




DETAIL B



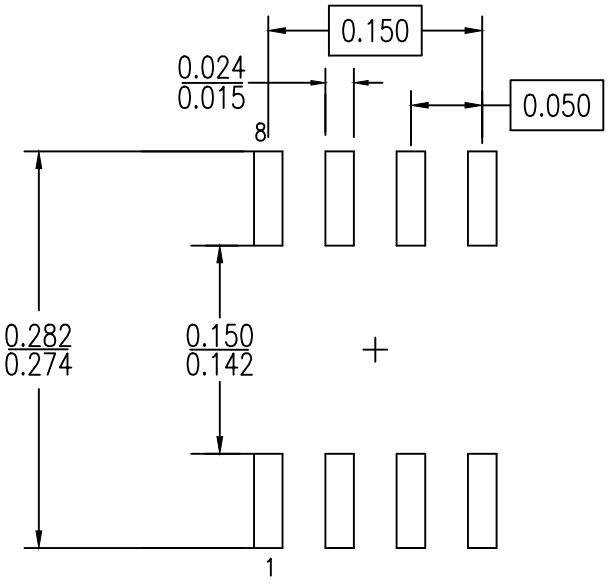




SECTION A-A

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN INCHES



RECOMMENDED LAND PATTERN DIMENSION

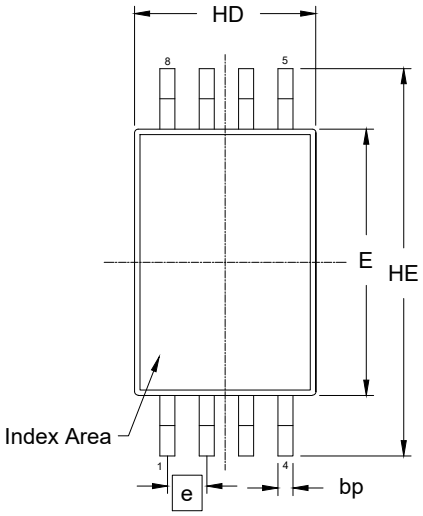
NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSIONS ARE IN INCHES

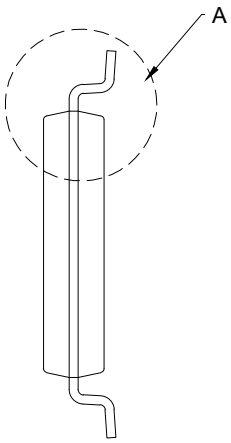
Package Revision History		
Date Created	Rev No.	Description
July 27, 2018	Rev 01	Dedicate to Package DCG8 Only
Feb 24, 2016	Rev 00	Initial Release

Package Outline Drawing

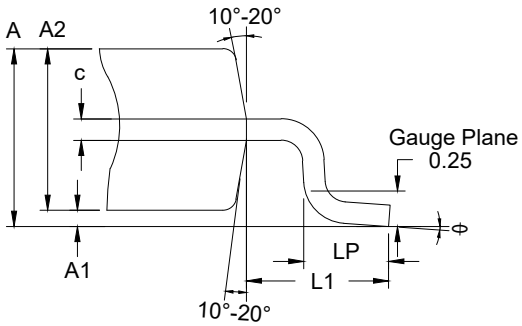
Package Code: PGG8D1
8-TSSOP 4.4 x 3.0 x 1.0 mm Body, 0.65mm Pitch
PSC-4768-01, Revision: 02, Date Created: Apr 29, 2024



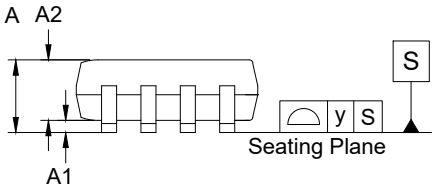
TOP VIEW



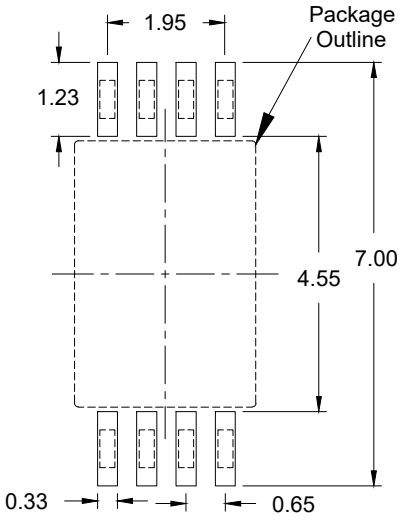
SIDE VIEW



Detail A
(Rotated 90° CW)



SIDE VIEW

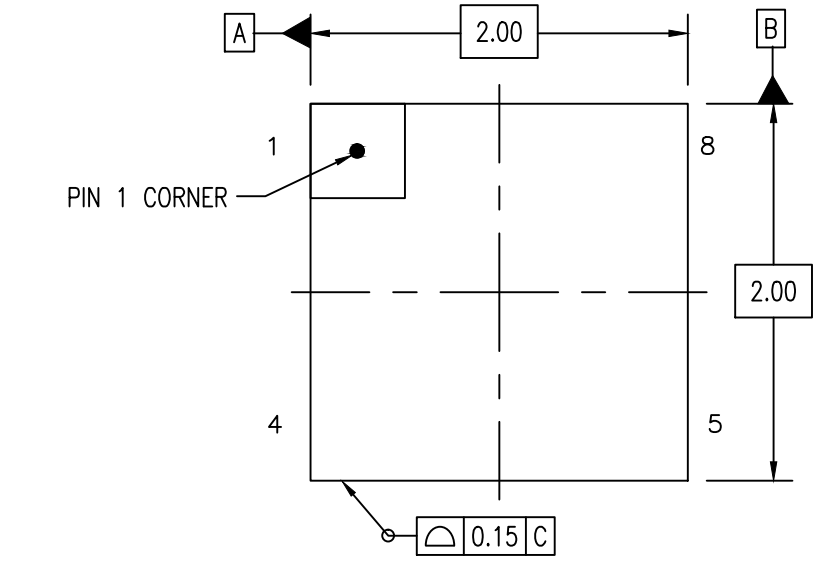


RECOMMENDED LAND PATTERN
(PCB Top View, SMD Design)

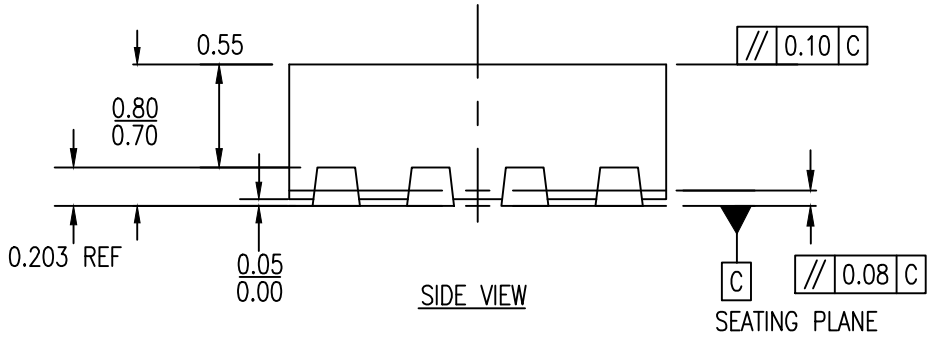
Reference Symbol	Dimension in mm		
	Min	Nom	Max
E	4.30	4.40	4.50
A2	0.80	-	1.05
HD	2.90	3.00	3.10
HE	6.20	6.40	6.60
A	0.85	-	1.20
A1	0.05	0.10	0.15
bp	0.19	0.25	0.30
c	0.09	-	0.20
θ	0.00	-	8.00
e	0.65 BSC		
y	-	-	0.10
LP	0.50	0.625	0.75
L1	-	1.00	-

NOTES:

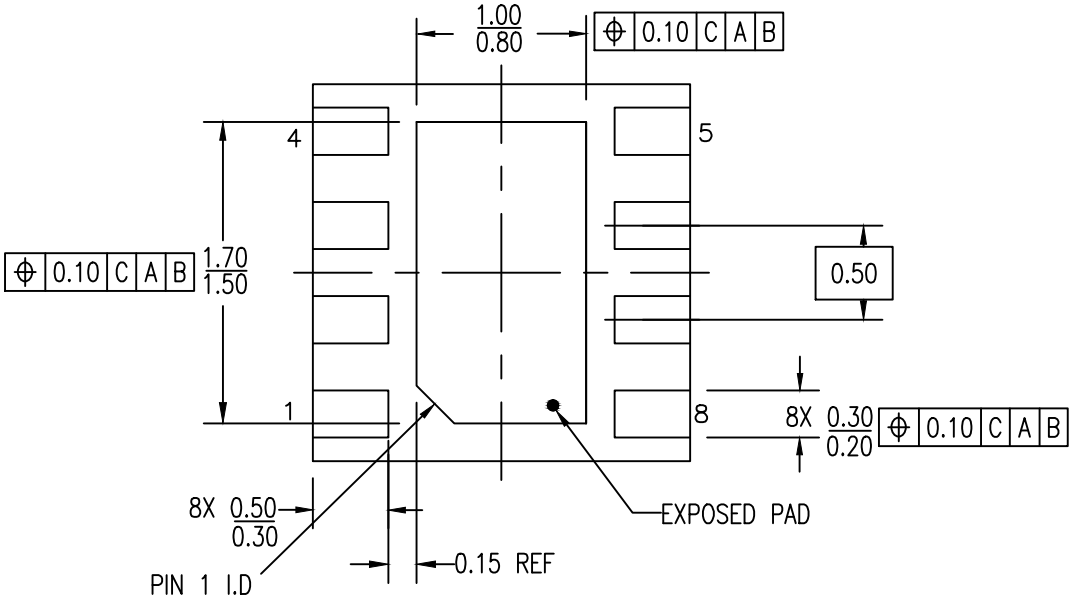
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Foot length is measured at gauge plane 0.25 mm above seating plane.



TOP VIEW



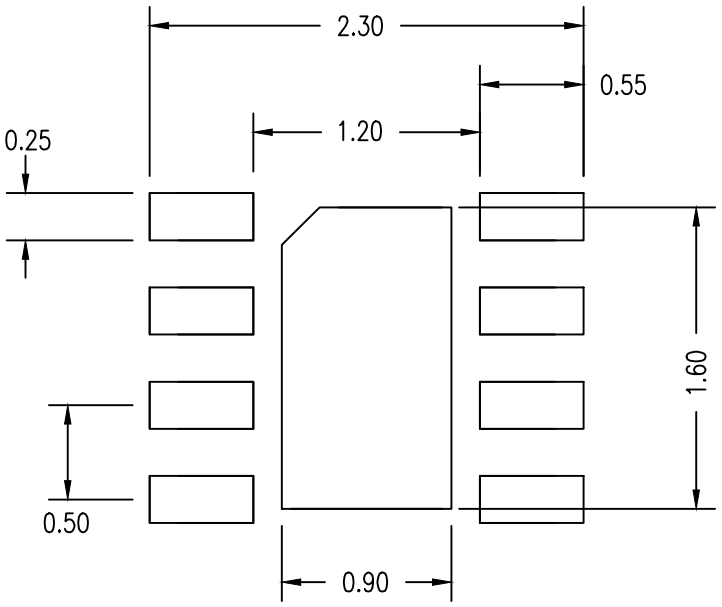
SIDE VIEW



BOTTOM VIEW

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Feb 12, 2018	Rev 01.	New Format, Change QFN to VFQFPN
April 12, 2018	Rev 02	Change from "VFQFPN" to "DFN"

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