To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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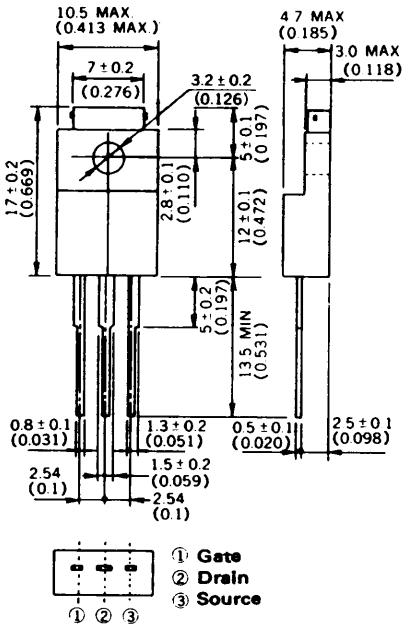
RENESAS

;HANNEL MOS FIELD EFFECT POWER TRANSISTOR

2SJ135

DESCRIPTION The 2SJ135 is P-Channel MOS Field Effect Power Transistor designed for solenoid, motor and lamp driver.

PACKAGE DIMENSIONS
in millimeters (inches)



FEATURES

- 4 V Gate Drive – Logic level –
- Low $R_{DS(on)}$
- No Second Breakdown
- High Sustaining Energy.

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . –55 to +150 °C

Channel Temperature. . . . . 150 °C Maximum

Maximum Power Dissipations

Total Power Dissipation . . . . . 2.0 W

Total Power Dissipation (T_C = 25 °C) . . . . . 30 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{DSS} Drain to Source Voltage . . . . . –100 V

V_{GSS} Gate to Source Voltage. . . . . ∓20 V

$I_{D(DC)}$ Drain Current (DC)* . . . . . ∓5 A

$I_{D(pulse)}$ Drain Current (pulse)** . . . . . ∓20 A

* T_C = 25 °C

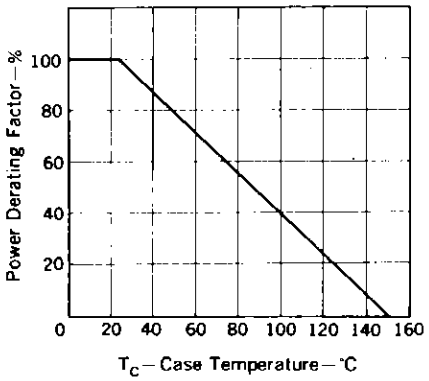
**PW ≦ 100 μs, Duty Cycle ≦ 2 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

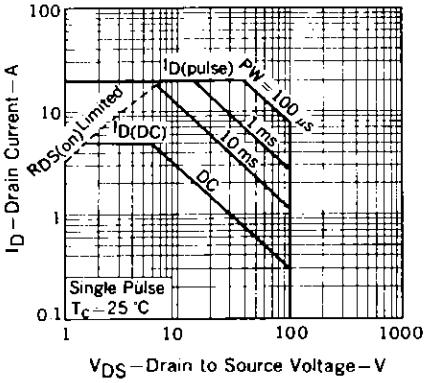
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
$R_{DS(on)}$	Drain to Source On-State Resistance		0.25	0.6	Ω	V_{GS} = –10 V, I_D = –3.5 A
$R_{DS(on)}$	Drain to Source On-State Resistance		0.5	0.9	Ω	V_{GS} = –4 V, I_D = –3.5 A
V_{SD}	Body Diode Forward Voltage Drop		0.9		V	I_{SD} = –5.0 A, V_{GS} = 0
I_{DL}	Unclamped Sustaining Energy			–5.0	A	V_{DD} = –50 V, $V_{GS(off)}$ = 0 L ≦ 100 μH, R_G ≧ 100 Ω Unclamped See Test Circuit 1
$V_{GS(off)}$	Gate to Source Cutoff Voltage	–1.0	–2.0	–3.0	V	V_{DS} = –10 V, I_D = –1 mA
$\lvert y_{fs} \rvert$	Forward Transfer Admittance	1.0	4.0		S	V_{DS} = –10 V, I_D = –3.5 A
I_{DSS}	Drain Leakage Current			–10	μA	V_{DS} = –100 V, V_{GS} = 0
I_{GSS}	Gate to Source Leakage Current			∓100	nA	V_{GS} = ∓20 V, V_{DS} = 0
C_{iss}	Input Capacitance		1600		pF	V_{DS} = –10 V V_{GS} = 0 f = 1 MHz
C_{oss}	Output Capacitance		400		pF	
C_{rss}	Reverse Transfer Capacitance		65		pF	
$t_{d(on)}$	Turn-On Delay Time		10		ns	I_D = –3.5 A, V_{DD} = –50 V $V_{GS(on)}$ = –10 V R_L = 15 Ω R_{in} = 10 Ω See Test Circuit 2
t_r	Rise Time		35		ns	
$t_{d(off)}$	Turn-Off Delay Time		55		ns	
t_f	Fall Time		40		ns	

TYPICAL CHARACTERISTICS (T_a = 25 °C)

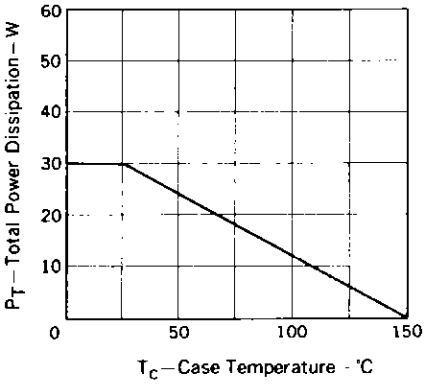
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



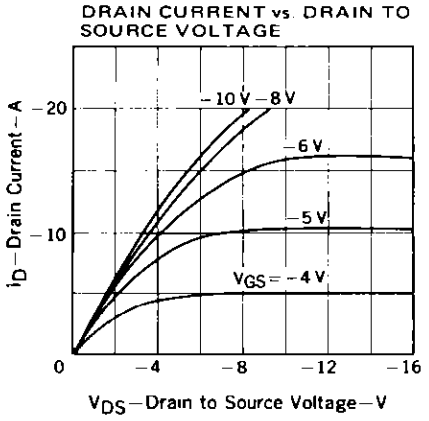
FORWARD BIAS SAFE OPERATING AREA



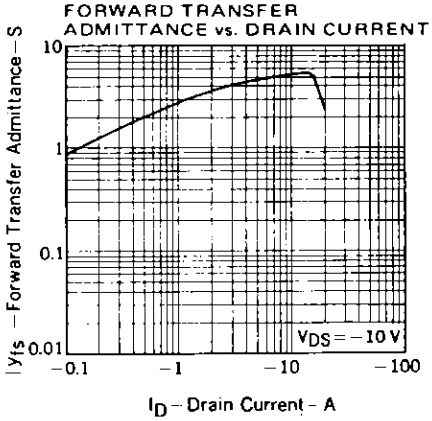
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



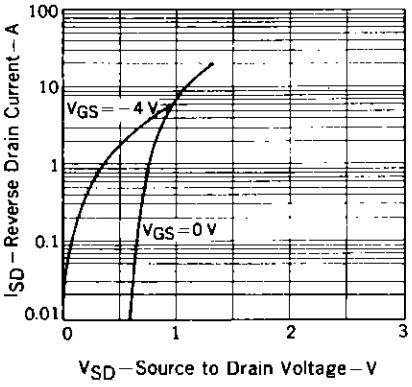
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



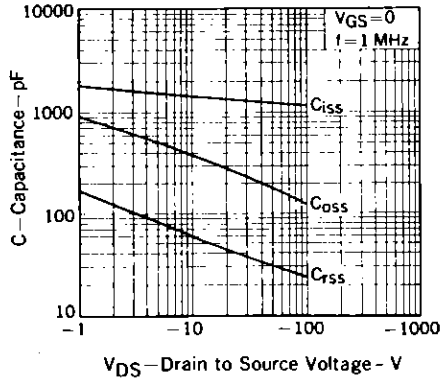
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



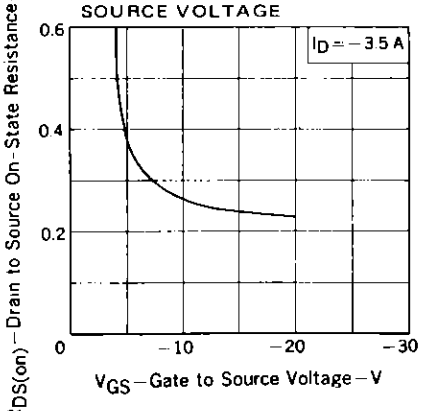
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



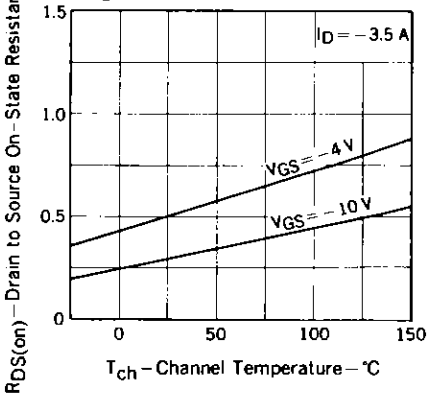
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



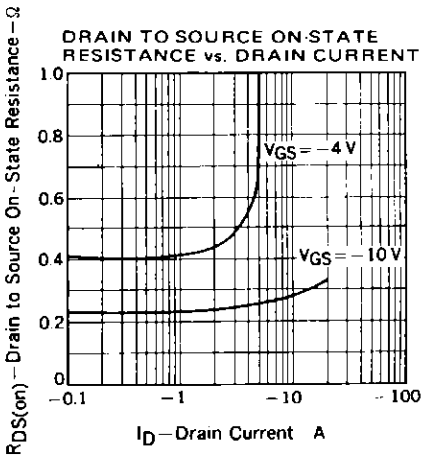
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



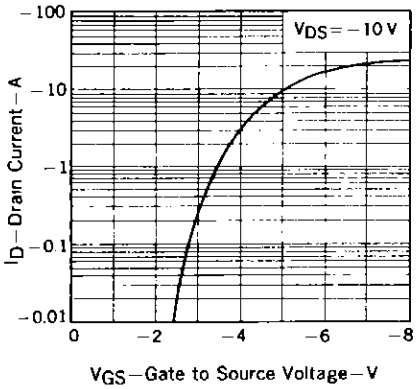
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



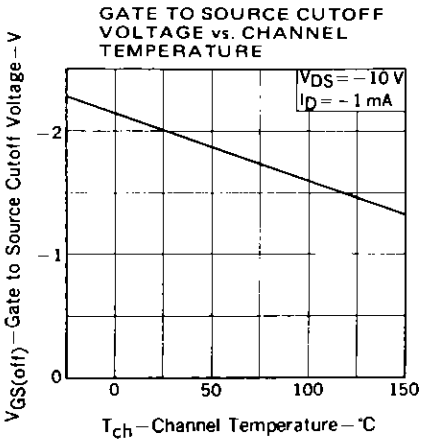
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



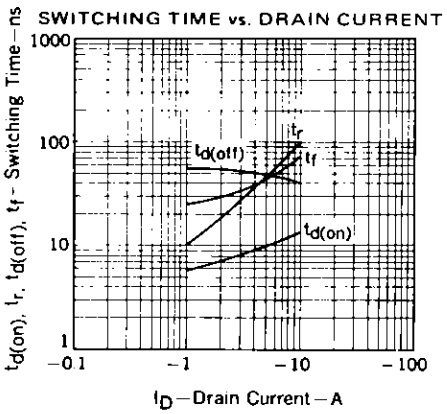
TRANSFER CHARACTERISTIC



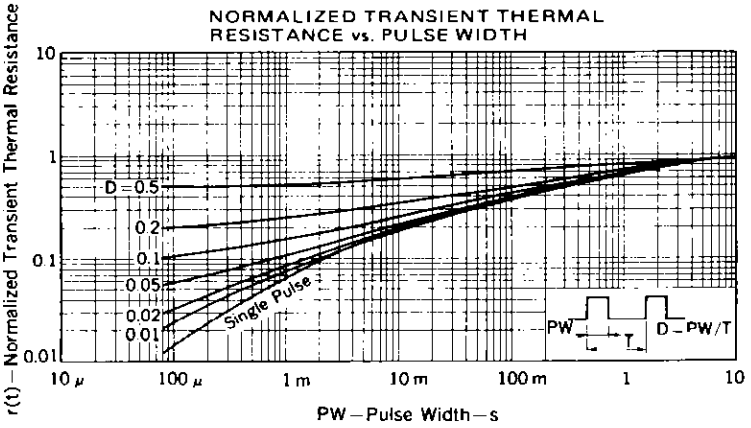
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



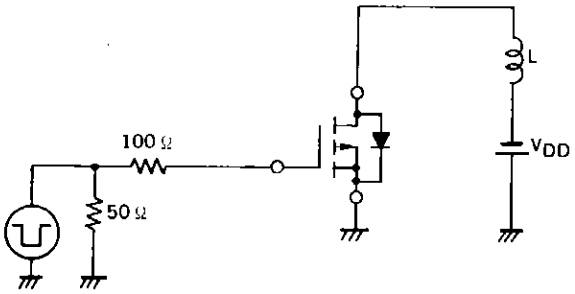
SWITCHING TIME vs. DRAIN CURRENT

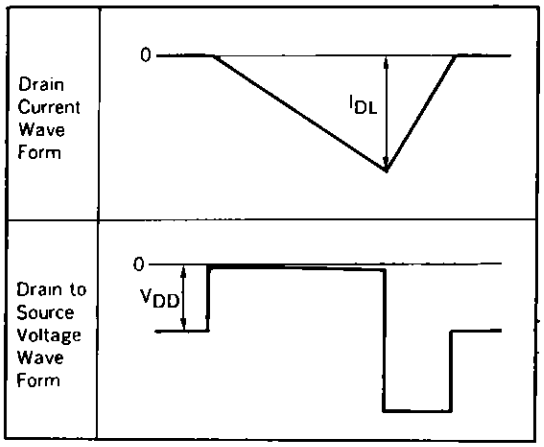


NORMALIZED TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

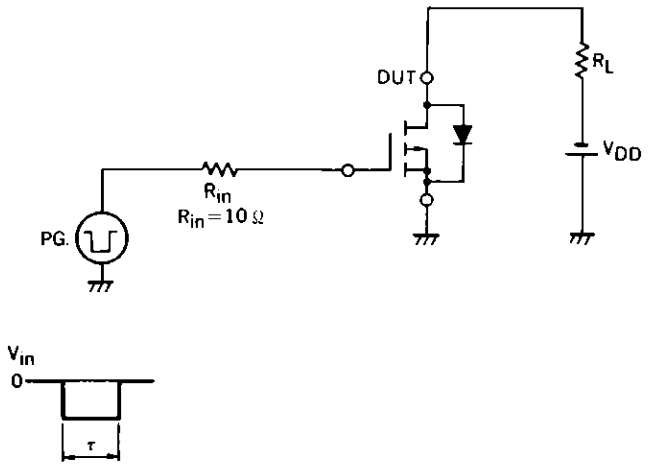


TEST CIRCUIT 1 : UNCLAMPED SUSTAINING ENERGY

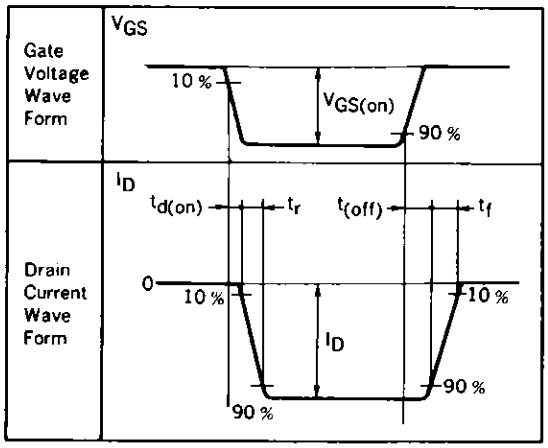




TEST CIRCUIT 2 : SWITCHING CHARACTERISTICS



τ = 1 μs
Duty Cycle ≦ 1 %



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