2SJ601-ZK

P-Channel Power MOS FET

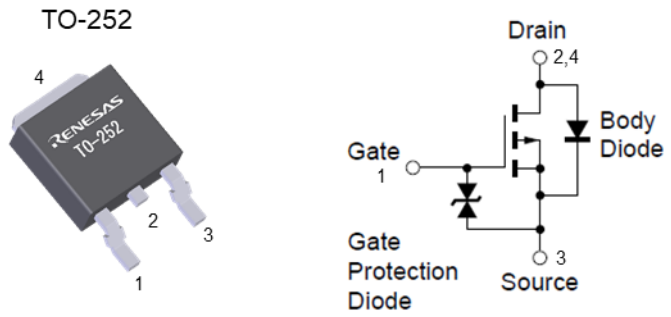
-60V, -36A, 31mΩ

R07DS1591EJ0200
Rev.2.00
Feb.3.2025

Features

- Low on-state resistance
  RDS(on)1 = 31 mΩ MAX. (VGS = –10 V, ID = –18 A)
  RDS(on)2 = 46 mΩ MAX. (VGS = –4.0 V, ID = –18 A)
- Low Ciss: Ciss = 3300 pF TYP.
- Built-in gate protection diode
- Applications : For switching

Outline



Absolute Maximum Ratings

(T_j=25°C unless otherwise notice.)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DSS}	-60	V
Gate to Source Voltage	V_{GSS}	∓20	V
Drain Current (DC)	$I_{D(DC)}$ Notes1,2,5	∓36	A
Drain Current (pulse)	$I_{D(pulse)}$ Notes1,3,5	∓120	A
Power Dissipation T_c = 25°C	P_D Notes5	65	W
Power Dissipation T_a = 25°C	P_D Notes5	1.0	W
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	-55 to 150	°C
Single Avalanche Current	I_{AS} Notes4	-36	A
Single Avalanche Energy	E_{AS} Notes4	123	mJ

Thermal Resistance

Item	Symbol	Max	Unit
Junction to Case Thermal Resistance	$R_{th(j-c)}$ Notes5	1.92	°C/W
Junction to Ambient Thermal Resistance	$R_{th(j-a)}$ Notes5	125	°C/W

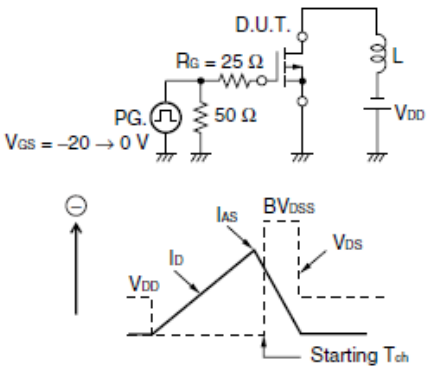
Electrical Characteristics

(T_j=25°C unless otherwise notice.)

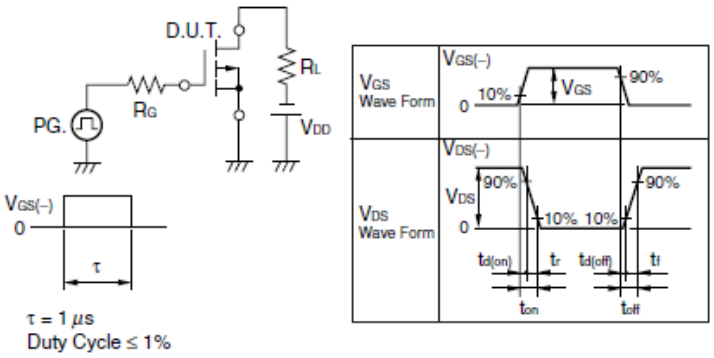
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-10	μA	V_{DS} = -60 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	∓10	μA	V_{GS} = ∓20 V, V_{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	-1.5	-2.0	-2.5	V	V_{DS} = -10 V, I_D = -1 mA
Forward Transfer Admittance	| yfs |	15	30	—	S	V_{GS} = -10 V, I_D = -18 A
Drain to Source On-state Resistance	$R_{DS(on)}$	—	25	31	mΩ	V_{GS} = -10 V, I_D = -18 A
	$R_{DS(on)}$	—	32	46	mΩ	V_{GS} = -4.0 V, I_D = -18 A
Input Capacitance	C_{iss}	—	3300	—	pF	V_{DS} = -10 V
Output Capacitance	C_{oss}	—	580	—	pF	V_{GS} = 0 V
Reverse Transfer Capacitance	C_{rss}	—	230	—	pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$	—	11	—	ns	V_{DD} = -30 V
Rise Time	t_r	—	12	—	ns	I_D = -18 A
Turn-off Delay Time	$t_{d(off)}$	—	80	—	ns	V_{GS} = -10 V
Fall Time	t_f	—	53	—	ns	R_G = 0 Ω
Total Gate Charge	Q_g	—	63	—	nC	V_{DD} = -48 V
Gate to Source Charge	Q_{gs}	—	10	—	nC	V_{GS} = -10 V
Gate to Drain Charge	Q_{gd}	—	16	—	nC	I_D = -36 A
Body Diode Forward Voltage	$V_{F(S-D)}$	—	1.0	—	V	I_F = 36 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	—	52	—	ns	I_F = 36 A, V_{GS} = 0 V
Reverse Recovery Charge	Q_{rr}	—	108	—	nC	di/dt = 100 A/μs

Notes 1. Tc = 25°C
2. Value is limited by overall system design including PCB
3. PW ≤ 10μs
4. L = 100μH , V_{DD} = -30V , V_{GS} = -20 → 0V , R_G = 25Ω
5. Defined by design. Not subject to production test.

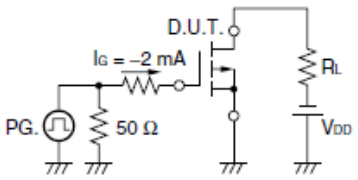
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

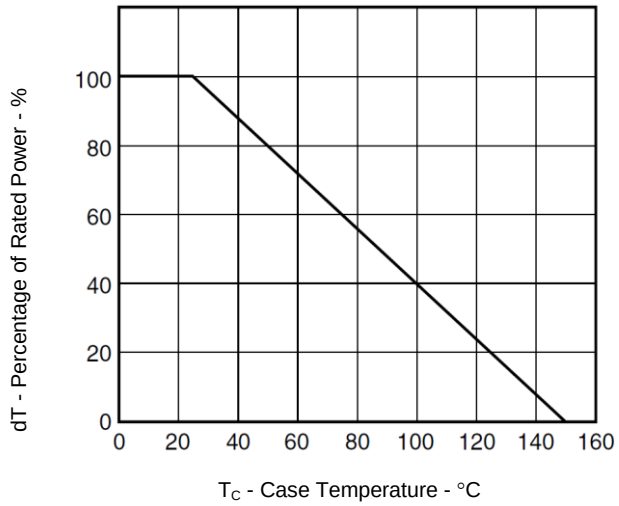


TEST CIRCUIT 3 GATE CHARGE

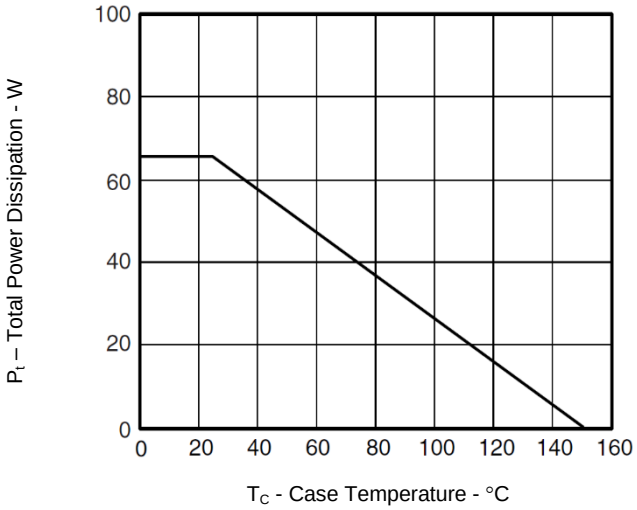


Typical Characteristics

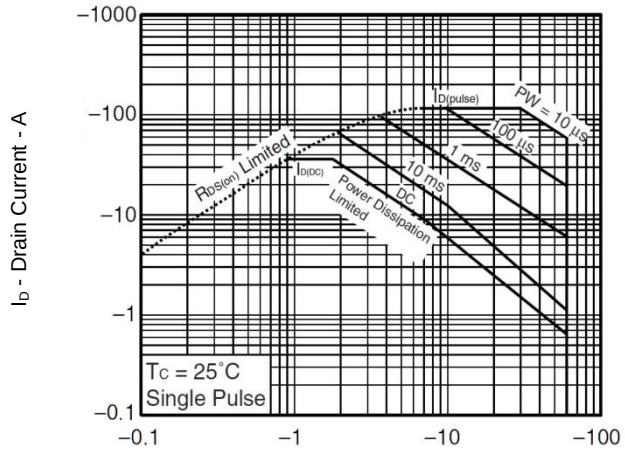
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



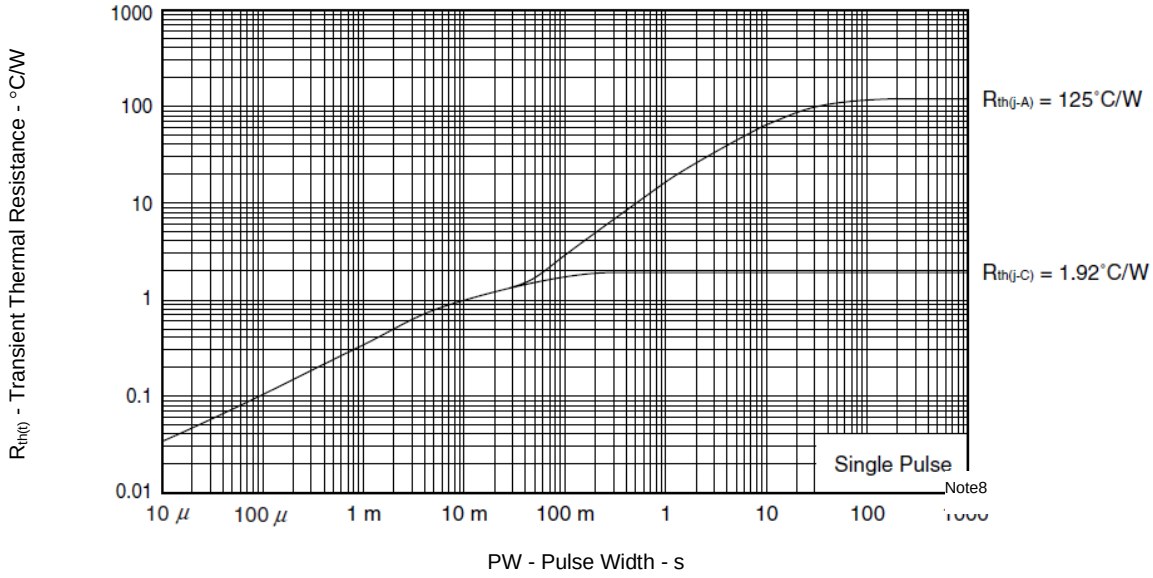
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



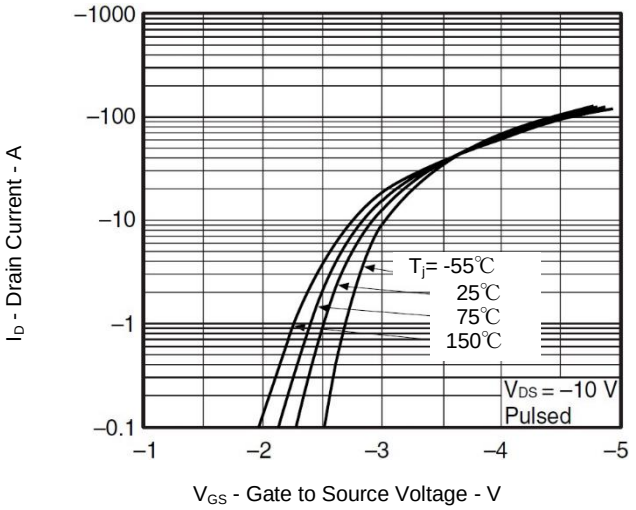
FORWARD BIAS SAFE OPERATING AREA



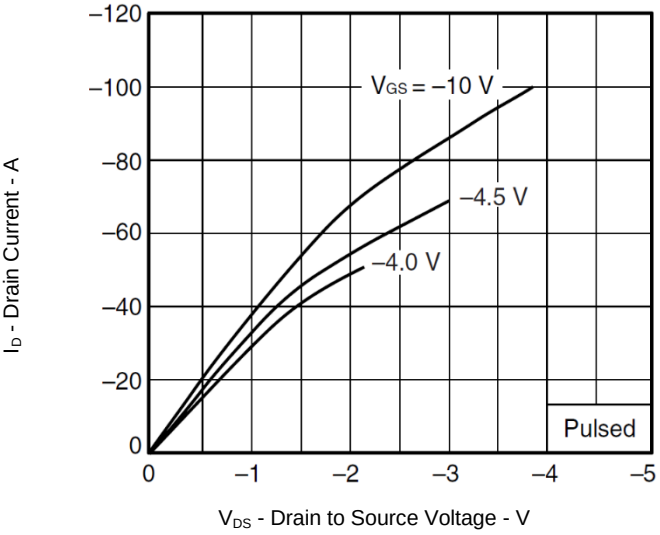
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



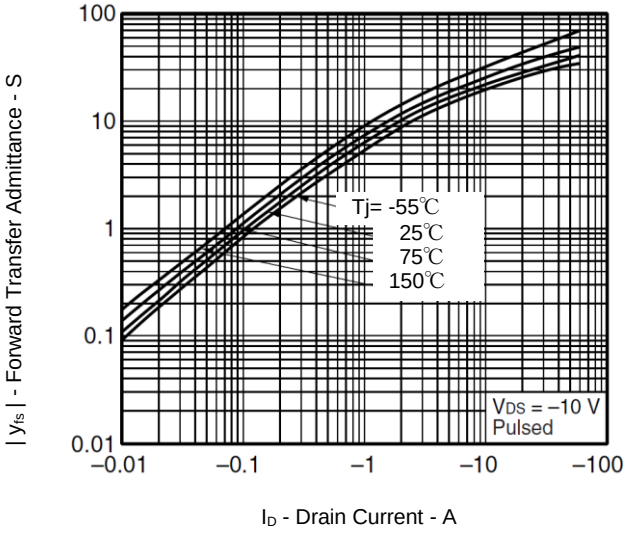
FORWARD TRANSFER CHARACTERISTICS



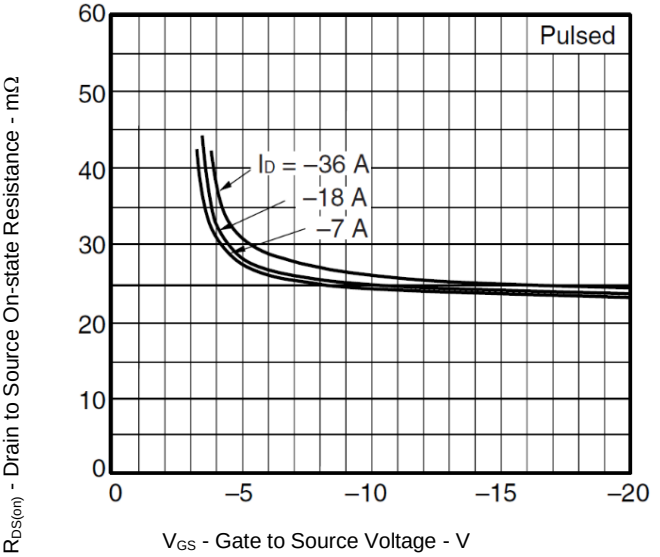
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



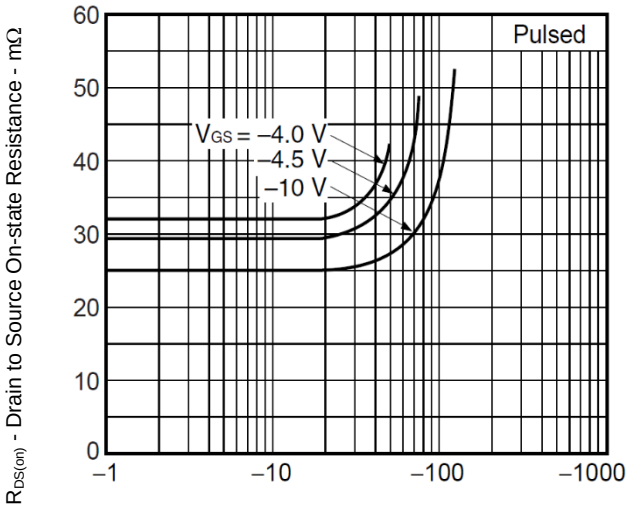
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



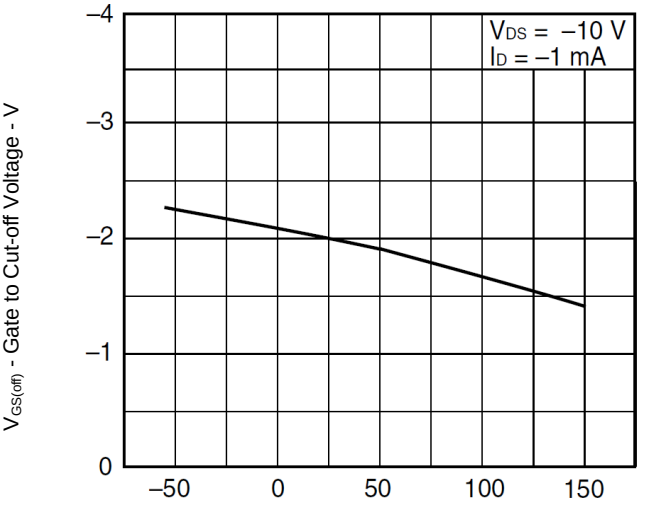
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



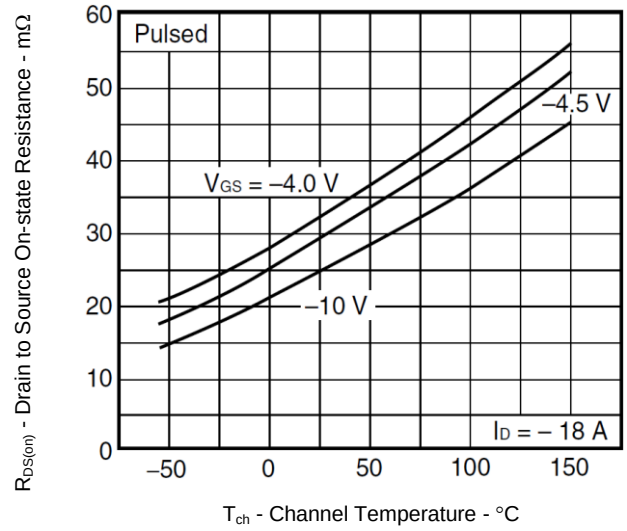
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



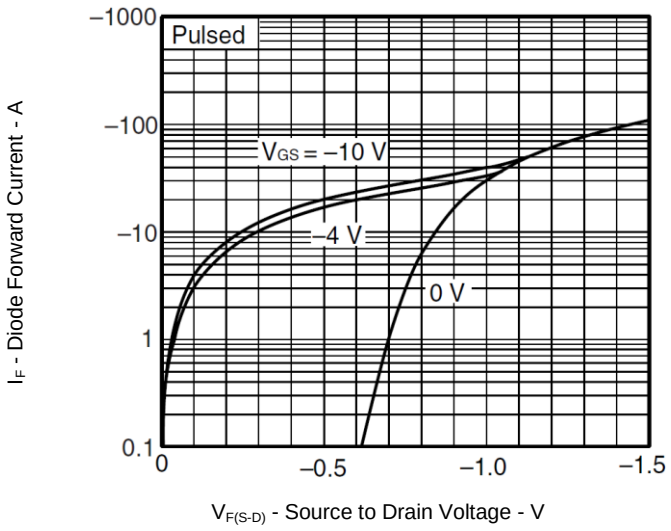
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



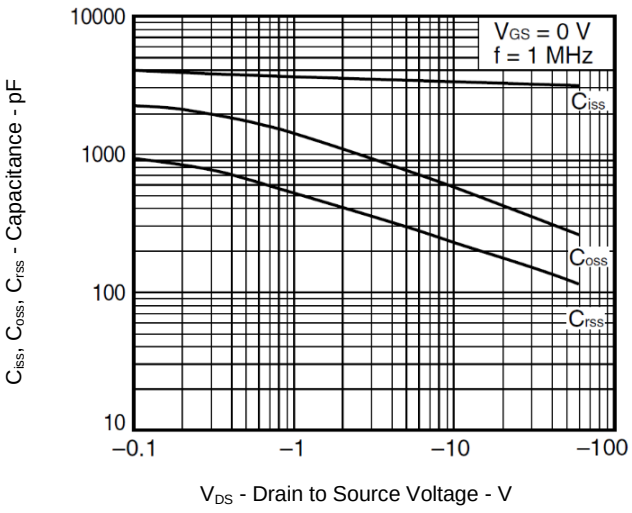
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



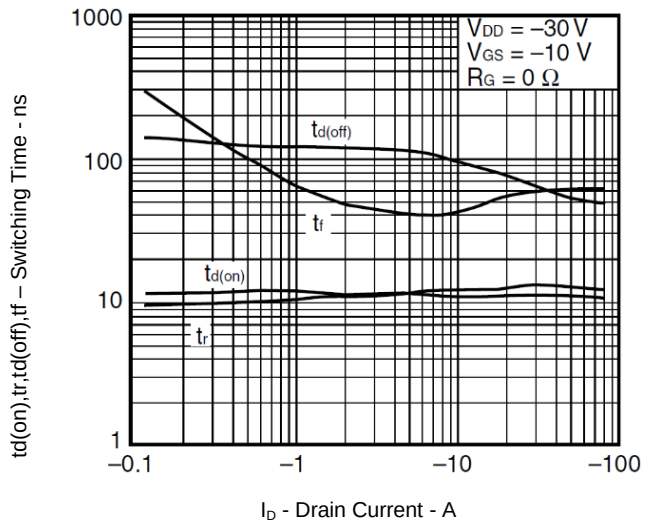
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



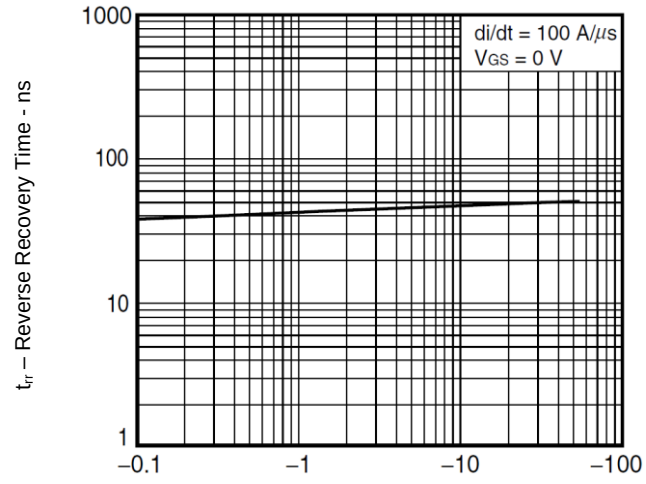
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



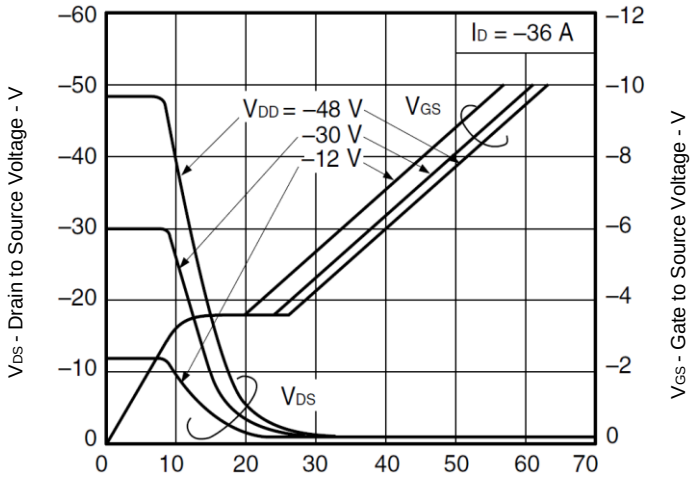
SWITCHING CHARACTERISTICS



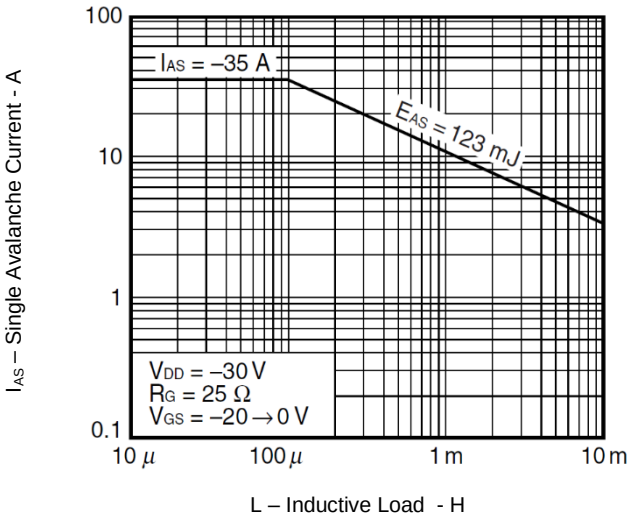
REVERSE RECOVERY TIME vs. DRAIN CURRENT



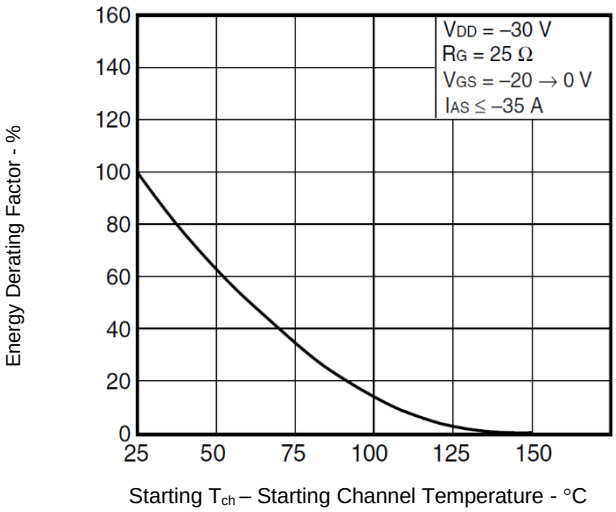
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD

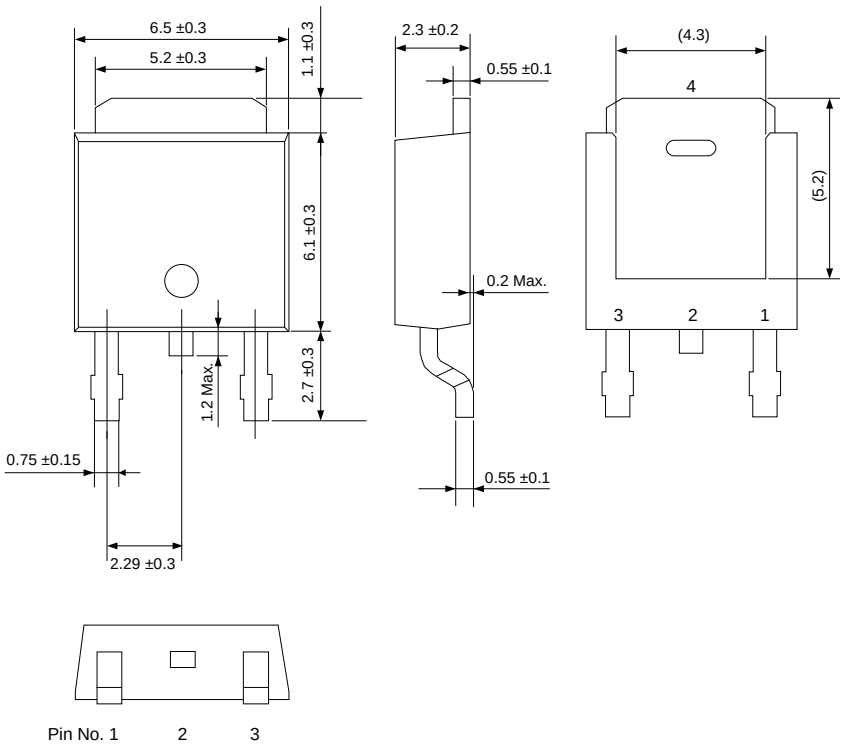


SHINGLE AVALANCHE ENERGY
DERATING FACTOR

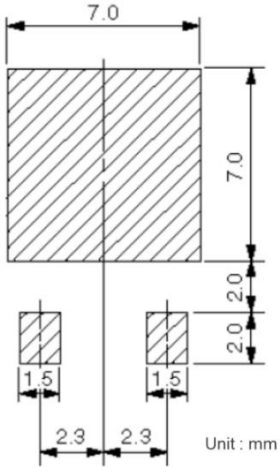


Package Dimensions (Unit : mm)

Package Name	JEITA Package Code	JEDEC Code	RENESAS Code	Previous Code	MASS (Typ) [g]
TO-252	—	TO-252	PRSS0004ZK-A	TO-252A	0.32



Mount Pad



Notice The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Remark : Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Continuous heavy condition (e.g. high temperature/voltage/current or high variation of temperature) may affect reliability even if it is within the absolute maximum ratings. Please consider derating condition for appropriate reliability in reference Renesas Semiconductor Reliability Handbook.

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Revision History

Rev.	Date	Description	
		Page	Summary
-	Aug 2006	-	Previous No. D14646EJ5V0DS00
2.00	Feb 3 , 2025	7	Changed Package Dimensions