Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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MOS FIELD EFFECT TRANSISTOR

2SK4178

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK4178 is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for low voltage high current applications such as DC/DC converter with synchronous rectifier.

FEATURES

• Low on-state resistance

 $R_{DS(on)1} = 9.0 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 10 \text{ V, Ip} = 30 \text{ A)}$

• Low gate to drain charge

 $Q_{GD} = 3.7 \text{ nC TYP.} (V_{DD} = 15 \text{ V}, I_D = 30 \text{ A})$

• 4.5 V drive available

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
2SK4178(1)-S27-AY Note		Tube 75 p/tube	TO-251 (MP-3-b) typ. 0.34 g
2SK4178-ZK-E1-AY Note	Pure Sn (Tin)	Tono 2500 n/mod	TO 252 (MD 27K) to 0.27 c
2SK4178-ZK-E2-AY Note		Tape 2500 p/reel	TO-252 (MP-3ZK) typ. 0.27 g

Note Pb-free (This product does not contain Pb in external electrode).

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Ves = 0 V)	VDSS	30	V
Gate to Source Voltage (V _{DS} = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	<u>±</u> 48	Α
Drain Current (pulse) Note1	D(pulse)	±144	Α
Total Power Dissipation (Tc = 25°C)	P _{T1}	33	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note2	las	23	Α
Single Avalanche Energy Note2	Eas	52.9	mJ

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Starting Tch = 25°C, VdD = 15 V, Rg = 25 Ω , Vgs = 20 \rightarrow 0 V, L = 0.1 mH

(TO-251)



TO-252)



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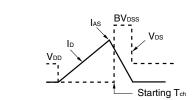
ELECTRICAL CHARACTERISTICS (TA = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 30 V, V _{GS} = 0 V			10	μΑ
Gate Leakage Current	Igss	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.5	2.0	2.5	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = 10 V, I _D = 12 A	7	15		S
Drain to Source On-state Resistance Note	R _{DS(on)1}	V _{GS} = 10 V, I _D = 30 A		6.8	9.0	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 12 A		9.8	15	mΩ
Input Capacitance	Ciss	V _{DS} = 10 V,		1500		pF
Output Capacitance	Coss	V _{GS} = 0 V,		360		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		126		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 30 A,		9		ns
Rise Time	tr	V _{GS} = 10 V,		9.7		ns
Turn-off Delay Time	t _{d(off)}	$R_G = 3 \Omega$		32		ns
Fall Time	tr			7.7		ns
Total Gate Charge	Q _{G1}	V _{DD} = 15 V, V _{GS} = 10 V, I _D = 30 A		24		nC
	Q _{G2}	V _{DD} = 15 V, V _{GS} = 4.5 V, I _D = 30 A		11.5		nC
Gate to Source Charge	Qgs	V _{DD} = 15 V, I _D = 30 A		3.7		nC
Gate to Drain Charge	Q _{GD}			3.7		nC
Gate Resistance	Rg	0 0		1.2		Ω
Body Diode Forward Voltage Note	V _F (S-D)	I _F = 30 A, V _{GS} = 0 V		0.87	1.5	V
Reverse Recovery Time	tin	IF = 30 A, VGS = 0 V,		29		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		23		nC

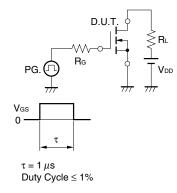
Note Pulsed

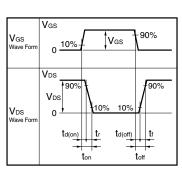
TEST CIRCUIT 1 AVALANCHE CAPABILITY

$\begin{array}{c|c} D.U.T. \\ \hline PG. \\ \hline \end{array} \begin{array}{c} S \\ \hline \end{array} \begin{array}{c} S \\ \hline \end{array} \begin{array}{c} V \\ \end{array} \end{array} \begin{array}{c} V \\ \end{array} \end{array} \begin{array}{c} V \\ \end{array} \begin{array}{c} V \\ \end{array} \begin{array}{c} V \\ \end{array} \begin{array}{c} V \\ \end{array} \end{array} \begin{array}{c} V \\ \end{array} \end{array} \begin{array}{c} V \\ \end{array} \begin{array}{c} V \\ \end{array} \begin{array}{c} V \\ \end{array} \begin{array}{c} V \\ \end{array} \end{array} \begin{array}{c} V \\ \end{array} \begin{array}{c} V \\ \end{array} \begin{array}{c} V \\ \end{array} \end{array} \begin{array}{c} V \\ \end{array} \begin{array}{c} V \\ \end{array} \end{array} \begin{array}{c} V \\ \end{array} \begin{array}{c} V \\ \end{array} \begin{array}{c} V \\ \end{array} \begin{array}{c} V \\ \end{array} \end{array}$

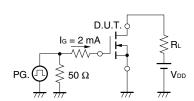


TEST CIRCUIT 2 SWITCHING TIME

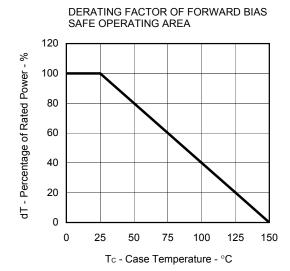


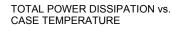


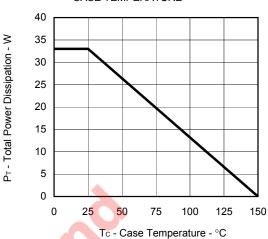
TEST CIRCUIT 3 GATE CHARGE



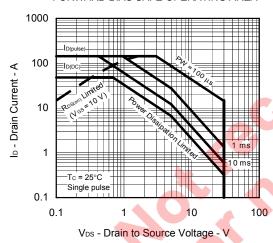
TYPICAL CHARACTERISTICS (T_A = 25°C)



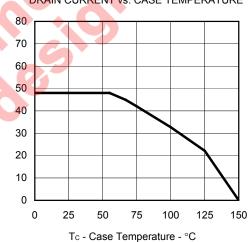




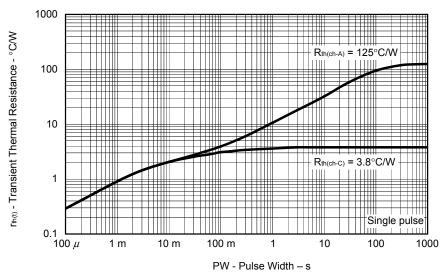
FORWARD BIAS SAFE OPERATING AREA



DRAIN CURRENT vs. CASE TEMPERATURE



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

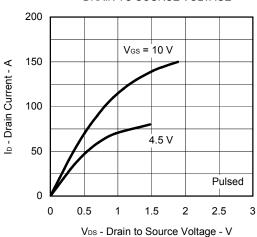


Data Sheet D19080EJ1V0DS

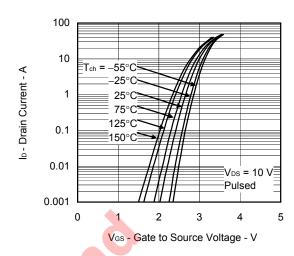
| yrs | - Forward Transfer Admittance - S

Rps(on) - Drain to Source On-state Resistance - mΩ

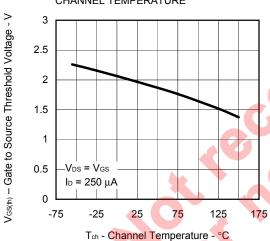
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



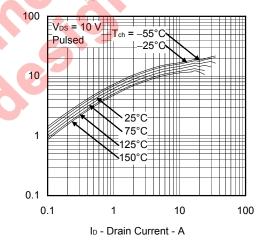
FORWARD TRANSFER CHARACTERISTICS



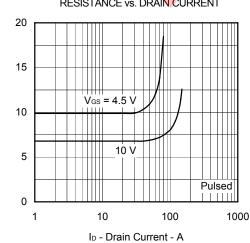
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



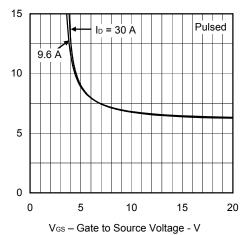
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



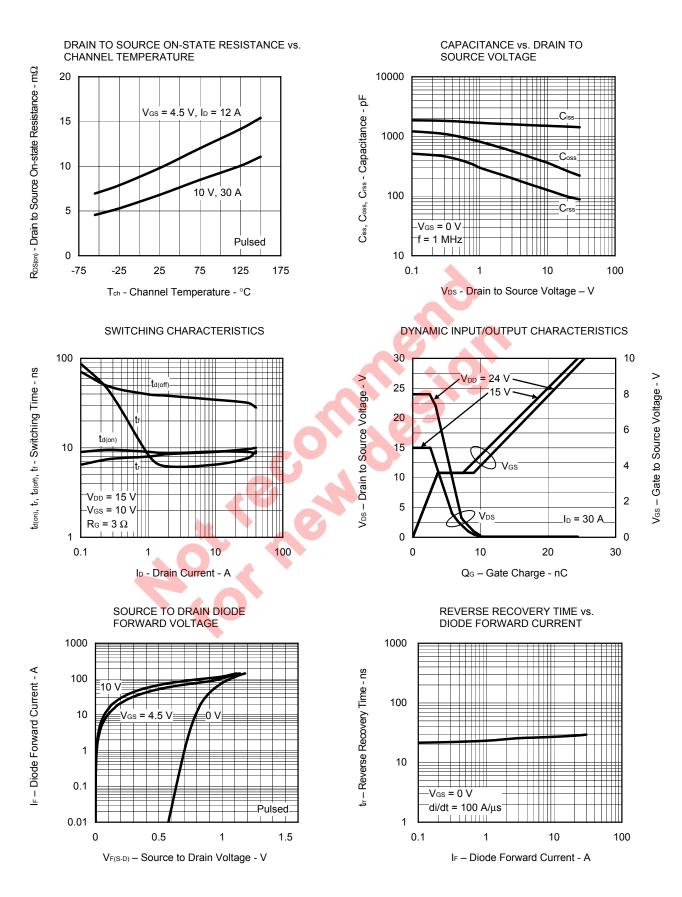
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



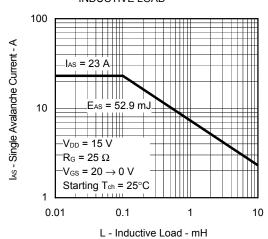
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



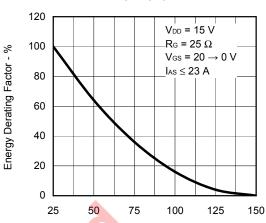
RDS(on) - Drain to Source On-state Resistance - m\Omega



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD

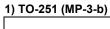


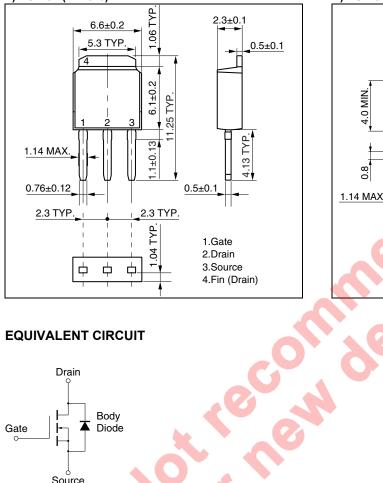
SINGLE AVALANCHE ENERGY DERATING FACTOR



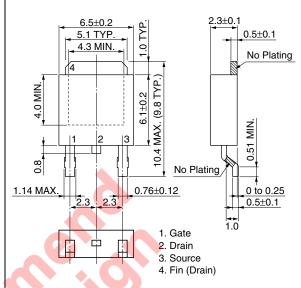
Starting T_{ch} - Starting Channel Temperature - °C

PACKAGE DRAWINGS (Unit: mm)

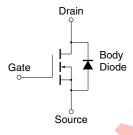




2) TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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