PECL INPUT OSCAR™ USER CONFIGURABLE CLOCK ICS525-03

Description

The ICS525-03 are the most flexible way to generate a high-quality, high-accuracy, high-frequency clock output from a PECL input. The name OSCaR stands for OSCillator Replacement, as they are designed to replace crystal oscillators in almost any electronic system. The user can configure the device to produce nearly any output frequency from any input frequency by grounding or floating the select pins. Neither microcontroller, software, nor device programmer are needed to set the frequency. Using Phase-Locked Loop (PLL) techniques, the device accepts a PECL clock to produce output clocks up to 250 MHz, keeping them frequency locked together. Resistors are for PECL outputs only.

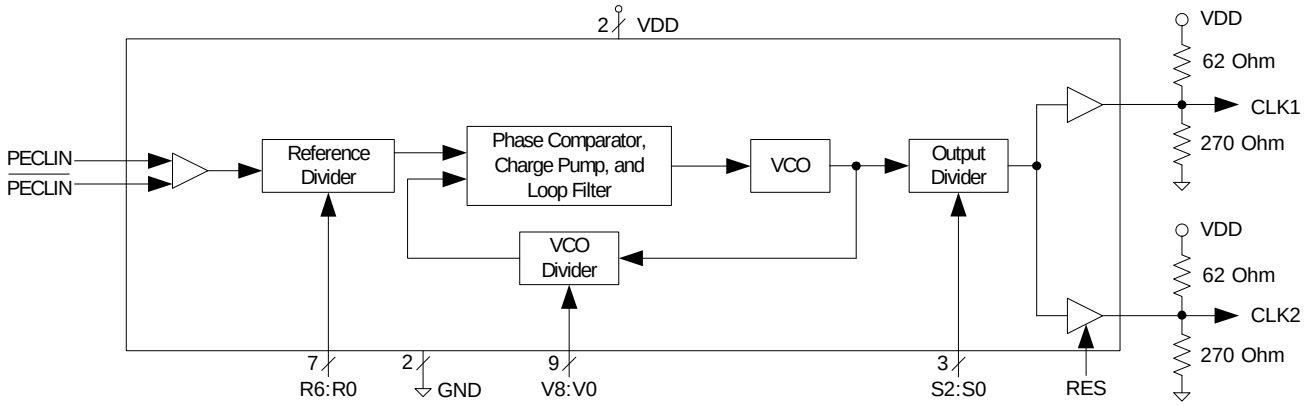
For simple multipliers to produce common frequencies, refer to the LOCO™ family of parts, which are smaller and more cost effective.

This product is intended for clock generation. It has low output jitter (variation in the output period), but input to output skew and jitter are not defined nor guaranteed.

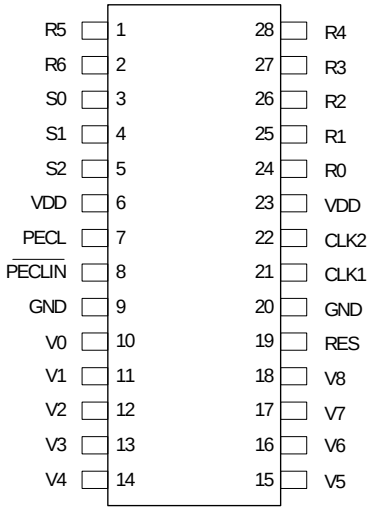
Features

- Packaged as 28-pin SSOP (150 mil body)
- Highly accurate frequency generation
- User determines the output frequency by setting all internal dividers
- Eliminates need for custom oscillators
- No software needed
- Pull-ups on all select inputs
- PECL input clock frequency of 0.5 to 250 MHz
- Output clock frequencies up to 250 MHz
- Very low jitter
- Operating voltage of 3.0 V or 5.5 V
- 25 mA drive capability at TTL levels
- Ideal for oscillator replacement
- Industrial temperature
- Pb (lead) free package
- Advanced, low-power CMOS process

Block Diagram



Pin Assignment



28-pin SSOP

RES Value Table

RES	CLK1	CLK2	Pre-divide (P)
0	CMOS	CMOS	2
1.1 kΩ Resistor to VDD	PECL	PECL	1

Output Divider and Maximum Output Frequency Table

S2	S1	S0	CLK	Max. Output Frequency (MHz)			
pin 5	pin 4	pin 3	Output Divider (OD)	VDD = 5 V		VDD = 3.3 V	
				RES = 0	RES = 1.1 kΩ	RES = 0	RES = 1.1 kΩ
0	0	0	6	67	34	40	20
0	0	1	2	200	100	120	60
0	1	0	8	50	25	30	15
0	1	1	4	100	50	60	30
1	0	0	5	80	40	48	24
1	0	1	7	57	29	34	17
1	1	0	1	250	200	200	125
1	1	1	3	133	80	80	40

Note: 0 = connect directly to ground; 1 = connect directly to VDD.

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1, 2, 24-28	R5, R6, R0-R4	I(PU)	Reference divider word input pins determined by user. Forms a binary number from 0 to 127.
3, 4, 5	S0, S1, S2	I(PU)	Select pins for output divider determined by user. See table above.
6, 23	VDD	Power	Connect to VDD.
7	PECLIN	Input	PECL input.
8	PECLIN	Input	Complementary PECL input.
9, 20	GND	Power	Connect to ground.
10 - 18	V0 - V8	I(PU)	VCO divider word input pins determined by user. Forms a binary number from 0 to 511.
19	RES	Input	Select eithe PECL or CMOS outputs. See table above.
21	CLK1	Output	Output clock. Either PECL or CMOS determined by RES.
22	CLK2	Output	Output clock. Either PECL or CMOS determined by RES.

KEY: I(PU) = Input with internal pull-up resistor.

Output Clock Selection

If RES is connected directly to ground, CLK1 and CLK2 are low skew, CMOS outputs clocks. They are not complementary. If RES is connected to VDD through a 1.1 kΩ resistor, then CLK1 and CLK2 become complementary PECL outputs which require the external resistor network shown in the the block diagram. Refer to Application Note MAN09 for additional information.

External Components/Crystal Selection

Decoupling Capacitors

The ICS525-03 requries two 0.01µF decoupling capacitors to be connected between VDD and GND, one on each side of the chip. The capacitor must be connected close to the device to minimize lead inductance. No external power supply filtering is required for this device.

External Resistors

If PECL outputs are desired, RES should be tied to VDD with a 1.1 kΩ resistor. Each output needs a resistive network of 62Ω and 270Ω per the block diagram on page 1. Application note MAN09 gives more information about resistor selection.

Determining (setting) the Output Frequency

Users have full control in setting the desired output frequency over the range shown in the table on page 2. To replace a standard oscillator, users should connect the divider select input pins directly to ground (or VDD, although this is not required because of internal pull-ups) during Printed Circuit Board layout. The ICS525-03 will automatically produce the correct clock when all components are soldered. It is also possible to connect the inputs to parallel I/O ports to switch frequencies. By choosing divides carefully, the number of inputs which need to be changed can be minimized. Observe the restrictions on allowed values of VDW and RDW.

The output of the ICS525-03 can be determined by the following simple equation:

$$\text{CLK Frequency} = \text{Input Frequency} \times P \times \frac{(VDW + 8)}{(RDW + 2) \bullet OD}$$

Where:

Reference Divider Word (RDW) = 0 to 127

VCO Divider Word (VDW) = 0 to 511

Output Divider (OD) = values on page 2

Pre-divide (P) = values on page 2 under RES Value Table

Also, the following operating ranges should be observed:

$$10\ \text{MHz} < \text{Input frequency} \times \frac{(VDW+8)}{(RDW+2)} < 350\ \text{MHz at 5.0 V or } < 250\ \text{MHz at 3.3 V}$$

$$200\ \text{kHz} < \frac{\text{Input Frequency}}{(RDW+2)}$$

(See table on page 2 for full details of maximum output)

The dividers are expressed as integers, so that if a 66.66 MHz PECL output is desired from a 14.31818 PECL input, the Reference Divider Word (RDW) should be 59 and the VCO Divider Word (VDW) should be 276, with an Output Divider (OD) of 1. To select PECL outputs, the RES pin should be tied to VDD with a 1.1kΩ resistor.

In this example, R6:R0 is 100010100, and S2:S0 is 110. Since all of these inputs have pull-up reistors, it is only necessary to ground the zero pins, namely V7, V6, V5, V3, V1, V0, R6, R2 and S0.

To determine the best combination of VCO, reference, and output divide, use the ICS525 Calculator on our web site. The online form is easy to use and quickly shows you up to three options for these settings. Alternately, you may send an e-mail to cmd-support@idt.com.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS525-03. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature, Industrial	-40 to +85° C
Storage Temperature	-65° C to 150° C
Junction Temperature	125° C
Soldering Temperature	260° C (max. of 10 seconds)

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		5.5	V
Operating Supply Current	IDD	60 MHz out, no load		15		mA
Operating Supply Current, LVPECL mode	IDD	With termination resistors		35		mA
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Peak-to-peak Input Voltage		PECLIN, $\overline{\text{PECLIN}}$	0.3		1	V
Common Mode Range		PECLIN, $\overline{\text{PECLIN}}$	VDD-1.4		VDD-0.6	
Output High Voltage	V_{OH}	I_{OH} = -25 mA, CMOS out	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 25 mA, CMOS out			0.4	V
Short Circuit Current		CMOS out		±70		mA
Input Capacitance	C_{IN}	V, R, S select pins		4		pF
On-chip Pull-up Resistor	R_{PU}	V, R, S select pins		270		kΩ

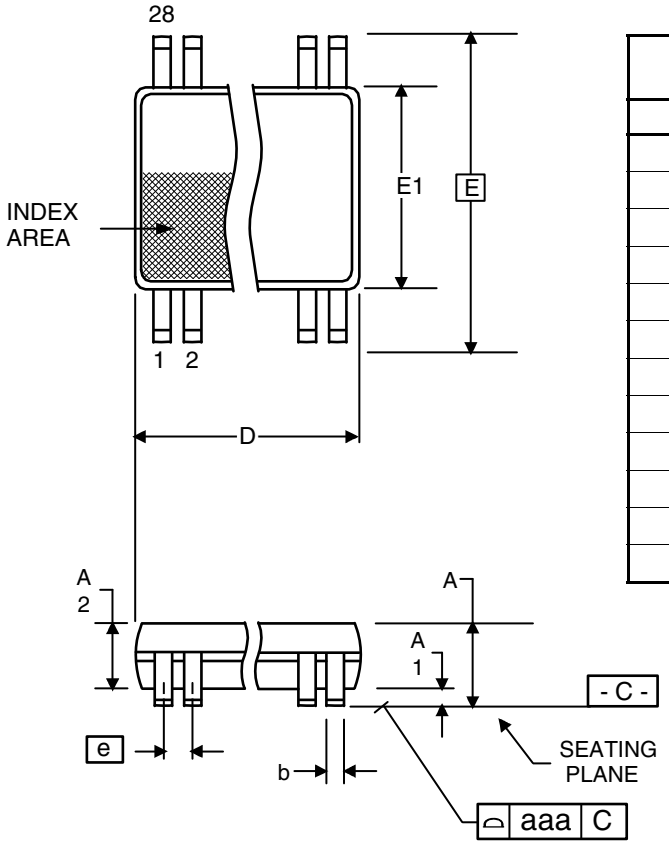
AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F_{IN}	Clock input	0.5		250	MHz
Output Frequency, VDD=4.5 to 5 V	F_{OUT}	OD = 1	1		250	MHz
Output Frequency, VDD=3.0 to 3.6 V	F_{OUT}	OD = 1	1		200	MHz
Output Clock Rise Time, CMOS clock		0.8 to 2.0 V		1		ns
Output Clock Fall Time, CMOS clock		2.0 to 0.8 V		1		ns
Output Clock Duty Cycle, even output dividers		at VDD/2	45		55	%
Output Clock Duty Cycle, odd output dividers		at VDD/2	40		60	%
Absolute Clock Period Jitter	t_{ja}	Deviation from mean		±350		ps
One Sigma Clock Period Jitter	t_{js}	One Sigma		125		ps

Package Outline and Package Dimensions (28-pin SSOP, 150 mil Body)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.053	.069
A1	0.10	0.25	.0040	.010
A2	--	1.50	--	.059
b	0.20	0.30	.008	.012
C	0.18	0.25	.007	.010
D	9.80	10.00	.386	.394
E	5.80	6.20	.228	.244
E1	3.80	4.00	.150	.157
e	0.635 Basic		0.025 Basic	
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

*Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
525R-03ILF	ICS525R-03ILF	Tubes	28-pin SSOP	-40 to +85° C
525R-03ILFT	ICS525R-03ILF	Tape and Reel	28-pin SSOP	-40 to +85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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