# FAST CMOS OCTAL D REGISTERS (3-STATE)

**IDT54/74FCT574T/AT/CT**

## FEATURES:

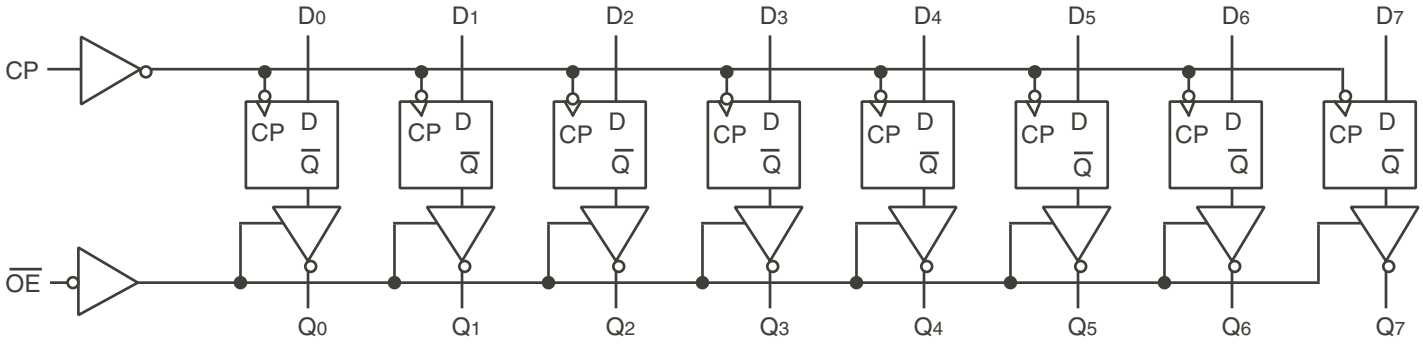
- **Std., A, and C grades**
- **Low input and output leakage ≤1µA (max.)**
- **CMOS power levels**
- **True TTL input and output compatibility:**
  - *$V_{OH}$ = 3.3V (typ.)*
  - *$V_{OL}$ = 0.3V (typ.)*
- **High Drive outputs (-15mA $I_{OH}$, 48mA $I_{OL}$)**
- **Meets or exceeds JEDEC standard 18 specifications**
- **Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)**
- **Power off disable outputs permit "live insertion"**
- **Available in the following packages:**
  - *Industrial: SOIC, QSOP*
  - *Military: CERDIP, LCC*

## DESCRIPTION:

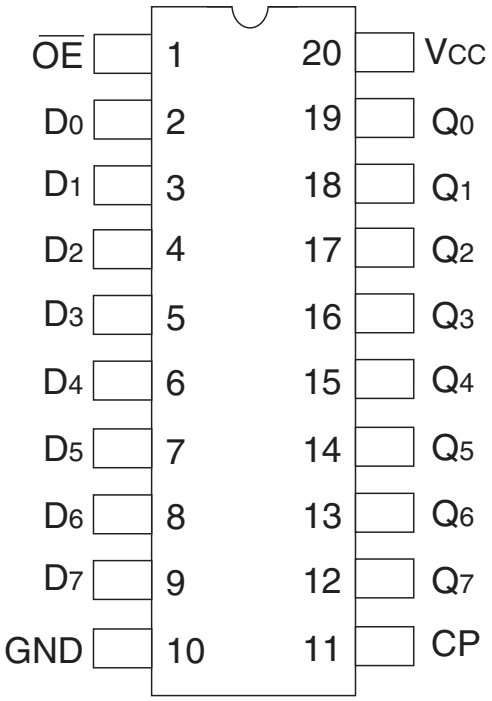
The FCT574T is an 8-bit register built using an advanced dual metal CMOS technology. These registers consist of eight D-type flip-flops with a buffered common clock and buffered 3-state output control. When the output enable ($\overline{OE}$) input is low, the eight outputs are enabled. When the $\overline{OE}$ input is high, the outputs are in the high-impedance state.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the Q outputs on the low-to-high transition of the clock input.

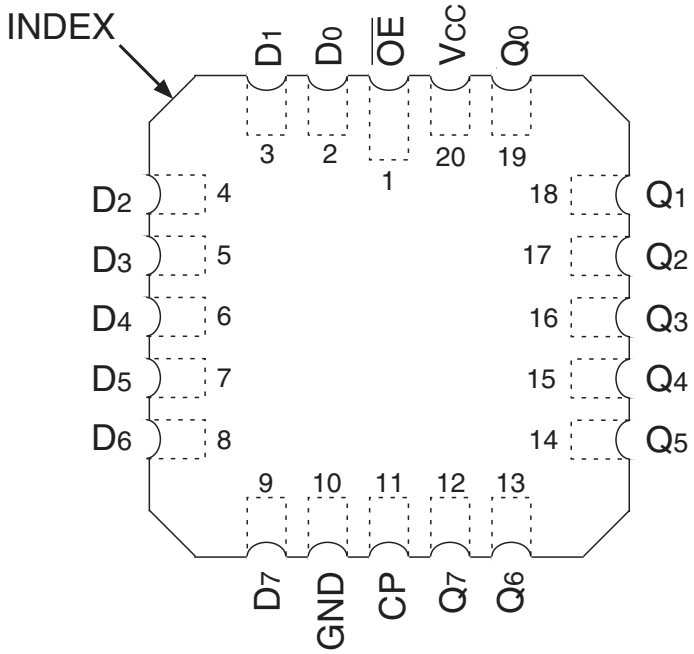
## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION




**CERDIP/ SOIC/ TSSOP**
**TOP VIEW**




**LCC**
**TOP VIEW**

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Description | Max | Unit |
|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | –0.5 to +7 | V |
| $V_{TERM}$(3) | Terminal Voltage with Respect to GND | –0.5 to $V_{CC}$+0.5 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $I_{OUT}$ | DC Output Current | –60 to +120 | mA |

**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Output and I/O terminals only.

## CAPACITANCE ($T_A$ = +25°C, F = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 6 | 10 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 8 | 12 | pF |

**NOTE:**
1. This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

| Pin Names | Description |
|---|---|
| Dx | D flip-flop data inputs |
| CP | Clock Pulse for the register. Enters data on LOW-to-HIGH transition. |
| Qx | 3-State Outputs (TRUE) |
| $\overline{Q}$x | 3-State Outputs (INVERTED) |
| $\overline{OE}$ | Active LOW 3-State Output Enable Input |

## FUNCTION TABLE(1)

| Function | Inputs | | | Outputs | Internal |
|---|---|---|---|---|---|
| | $\overline{OE}$ | CP | Dx | Qx | $\overline{Q}$x |
| High-Z | H | L | X | Z | NC |
| | H | H | X | Z | NC |
| Load Register | L | ↑ | L | L | H |
| | L | ↑ | H | H | L |
| | H | ↑ | L | Z | H |
| | H | ↑ | H | Z | L |

**NOTE:**
1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High Impedance
   NC = No Change
   ↑ = LOW-to-HIGH transition

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: $T_A$ = –40°C to +85°C, $V_{CC}$ = 5.0V ±5%; Military: $T_A$ = –55°C to +125°C, $V_{CC}$ = 5.0V ±10%

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level | Guaranteed Logic HIGH Level | | 2 | — | — | V |
| $V_{IL}$ | Input LOW Level | Guaranteed Logic LOW Level | | — | — | 0.8 | V |
| $I_{IH}$ | Input HIGH Current[4] | $V_{CC}$ = Max. | $V_I$ = 2.7V | — | — | ±1 | µA |
| $I_{IL}$ | Input LOW Current[4] | $V_{CC}$ = Max. | $V_I$ = 0.5V | — | — | ±1 | µA |
| $I_{OZH}$ | High Impedance Output Current | $V_{CC}$ = Max | $V_O$ = 2.7V | — | — | ±1 | µA |
| $I_{OZL}$ | (3-State output pins)[4] | | $V_O$ = 0.5V | — | — | ±1 | |
| $I_I$ | Input HIGH Current[4] | $V_{CC}$ = Max., $V_I$ = $V_{CC}$ (Max.) | | — | — | ±1 | µA |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = Min, $I_{IN}$ = -18mA | | — | –0.7 | –1.2 | V |
| $V_H$ | Input Hysteresis | — | | — | 200 | — | mV |
| $I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$ = Max., $V_{IN}$ = GND or $V_{CC}$ | | — | 0.01 | 1 | mA |

## OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –6mA MIL<br>$I_{OH}$ = –8mA IND | 2.4 | 3.3 | — | V |
| | | | $I_{OH}$ = –12mA MIL<br>$I_{OH}$ = –15mA IND | 2 | 3 | — | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 32mA MIL<br>$I_{OL}$ = 48mA IND | — | 0.3 | 0.5 | V |
| $I_{OS}$ | Short Circuit Current | $V_{CC}$ = Max., $V_O$ = GND[3] | | –60 | –120 | –225 | mA |

**NOTES:**
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. The test limit for this parameter is ±5µA at $T_A$ = –55°C.

## POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $\Delta I_{CC}$ | Quiescent Power Supply Current<br>TTL Inputs HIGH | $V_{CC}$ = Max.<br>$V_{IN}$ = 3.4V[3] | | — | 0.5 | 2 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current[4] | $V_{CC}$ = Max.<br>Outputs Open<br>$\overline{OE}$ = GND<br>One Input Toggling<br>50% Duty Cycle | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 0.15 | 0.25 | mA/<br>MHz |
| $I_C$ | Total Power Supply Current[6] | $V_{CC}$ = Max.<br>Outputs Open<br>$f_{CP}$ = 10MHz<br>50% Duty Cycle<br>$\overline{OE}$ = GND<br>fi = 5MHz<br>One Bit Toggling | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 1.5 | 3.5 | mA |
| | | | $V_{IN}$ = 3.4V<br>$V_{IN}$ = GND | — | 2 | 5.5 | |
| | | $V_{CC}$ = Max.<br>Outputs Open<br>$f_{CP}$ = 10MHz<br>50% Duty Cycle<br>$\overline{OE}$ = GND<br>Eight Bits Toggling<br>fi = 2.5MHz | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 3.8 | 7.3[5] | mA |
| | | | $V_{IN}$ = 3.4V<br>$V_{IN}$ = GND | — | 6 | 16.3[5] | |

**NOTES:**
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient.
3. Per TTL driven input; ($V_{IN}$ = 3.4V). All other inputs at $V_{CC}$ or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of $\Delta I_{CC}$ formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   $I_{CC}$ = Quiescent Current
   $\Delta I_{CC}$ = Power Supply Current for a TTL High Input ($V_{IN}$ = 3.4V)
   $D_H$ = Duty Cycle for TTL Inputs High
   $N_T$ = Number of TTL Inputs at $D_H$
   $I_{CCD}$ = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   $f_{CP}$ = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   $f_i$ = Output Frequency
   $N_i$ = Number of Outputs at $f_i$

All currents are in milliamps and all frequencies are in megahertz.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE - INDUSTRIAL

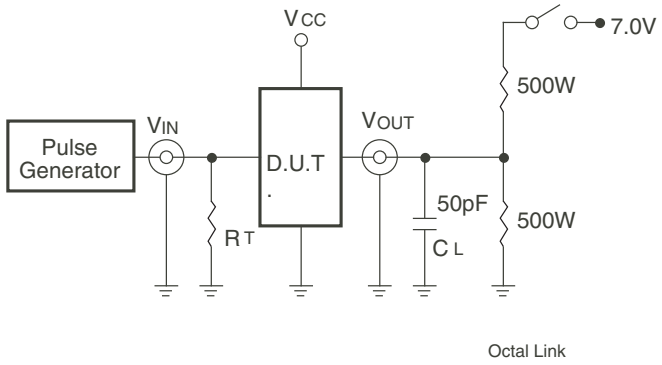
| Symbol | Parameter | Condition[1] | FCT574AT | | FCT574CT | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min.[2] | Max. | Min.[2] | Max. | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>CP to Qx | $C_L$ = 50pF<br>$R_L$ = 500Ω | 2 | 6.5 | 2 | 5.2 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time | | 1.5 | 6.5 | 1.5 | 5.5 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time | | 1.5 | 5.5 | 1.5 | 5 | ns |
| $t_{SU}$ | Set-up Time, HIGH or LOW<br>Dx to CP | | 2 | — | 2 | — | ns |
| $t_H$ | Hold Time, HIGH or LOW<br>Dx to CP | | 1.5 | — | 1.5 | — | ns |
| $t_W$ | CP Pulse Width HIGH or LOW[3] | | 5 | — | 5 | — | ns |

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE - MILITARY

| Symbol | Parameter | Condition[1] | FCT574T | | FCT574AT | | FCT574CT | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>CP to Qx | $C_L$ = 50pF<br>$R_L$ = 500Ω | 2 | 11 | 2 | 7.2 | 2 | 6.2 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time | | 1.5 | 14 | 1.5 | 7.5 | 1.5 | 6.2 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time | | 1.5 | 8 | 1.5 | 6.5 | 1.5 | 5.7 | ns |
| $t_{SU}$ | Set-up Time, HIGH or LOW<br>Dx to CP | | 2 | — | 2 | — | 2 | — | ns |
| $t_H$ | Hold Time, HIGH or LOW<br>Dx to CP | | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| $t_W$ | CP Pulse Width HIGH or LOW[3] | | 7 | — | 6 | — | 6 | — | ns |

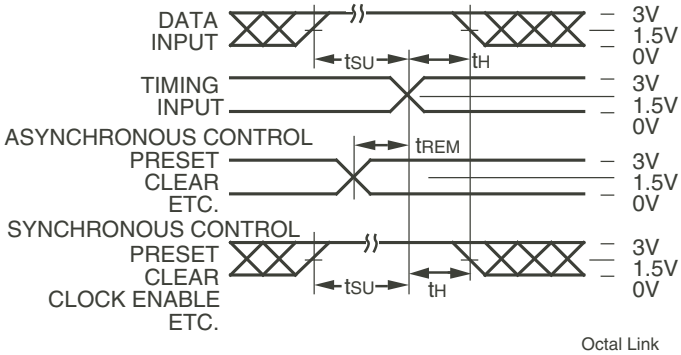
**NOTES:**
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This limit is guaranteed but not tested.

## TEST CIRCUITS AND WAVEFORMS



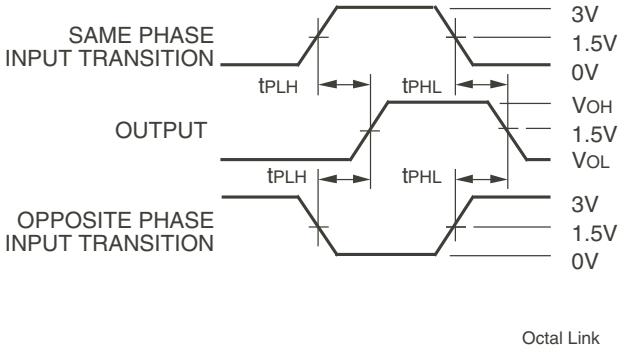

Octal Link

***Test Circuits for All Outputs***




Octal Link

***Set-Up, Hold, and Release Times***




Octal Link

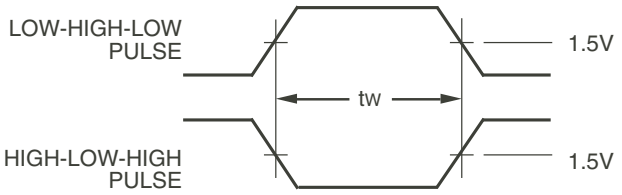
***Propagation Delay***

## SWITCH POSITION

| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | Closed |
| All Other Tests | Open |

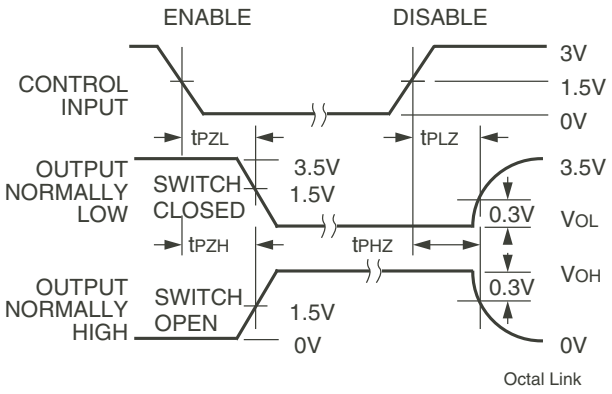
**DEFINITIONS:**

$C_L$ = Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.




***Pulse Width***

Octal Link



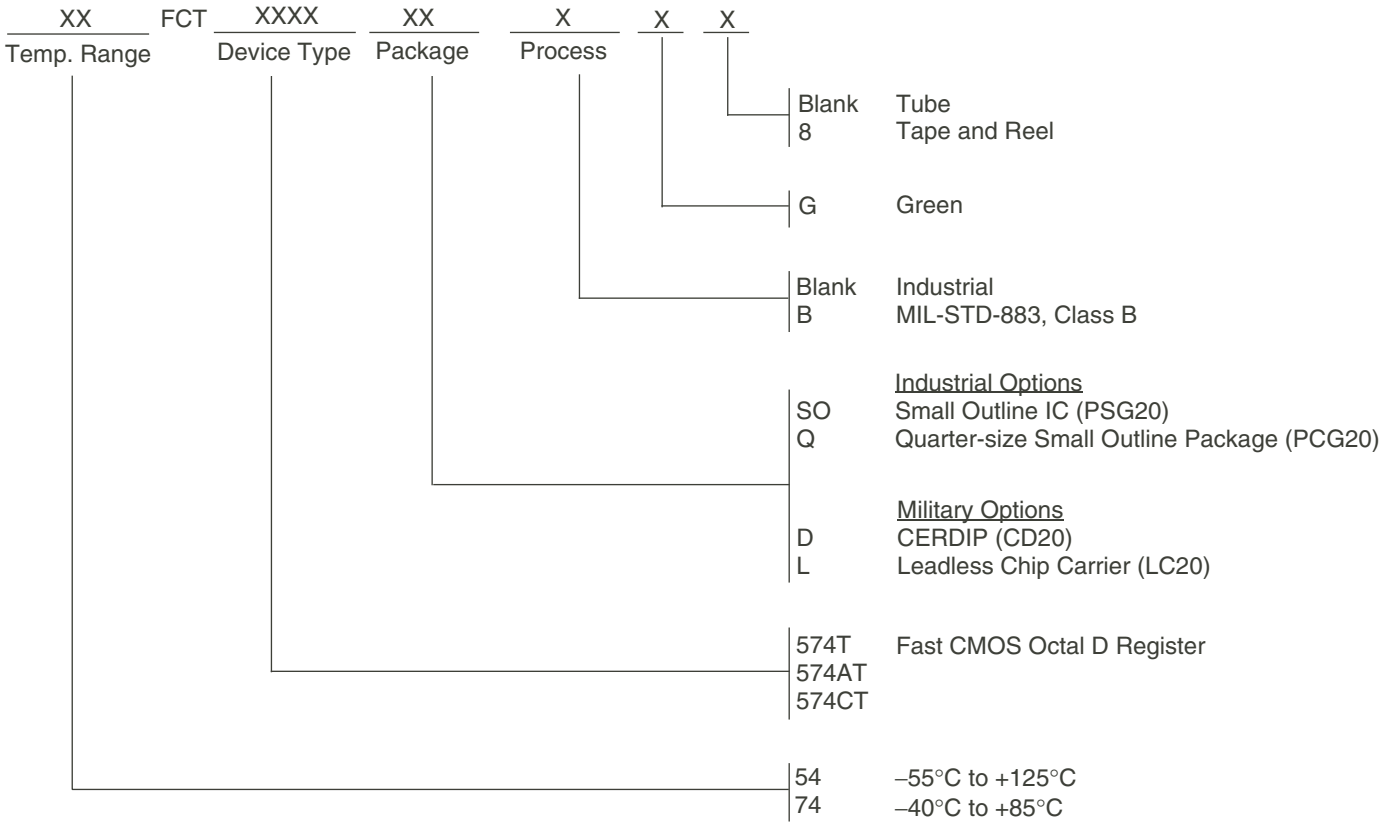

Octal Link

***Enable and Disable Times***

**NOTES:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns.

## ORDERING INFORMATION




## Datasheet Document History

| | | |
|---|---|---|
| 10/10/2009 | Pg. 7 | Updated the ordering information by removing the "IDT" notation and non RoHS part. |
| 11/17/2016 | Pg. 7 | Updated the ordering information by adding detailed package information and Tape & Reel. |

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)


### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com


### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.