

Description

The 5L35023 is a member of the VersaClock® 3S programmable clock generator family with 1.8V operation voltage, and is designed for industrial, consumer, and PCI Express applications. The device features a 3 PLL architecture design; each PLL is individually programmable and allowing up to 6 unique frequency outputs.

The 5L35023 has built-in features such as Proactive Power Saving (PPS), Performance-Power Balancing (PPB), Overshoot Reduction Technology (ORT) and extreme low power DCO. An internal OTP memory allows the user to store the configuration in the device without programming after power-up, then program the 5L35023 again through the I²C interface.

The device has programmable VCO and PLL source selection, allowing power-performance optimization based on the application requirements.

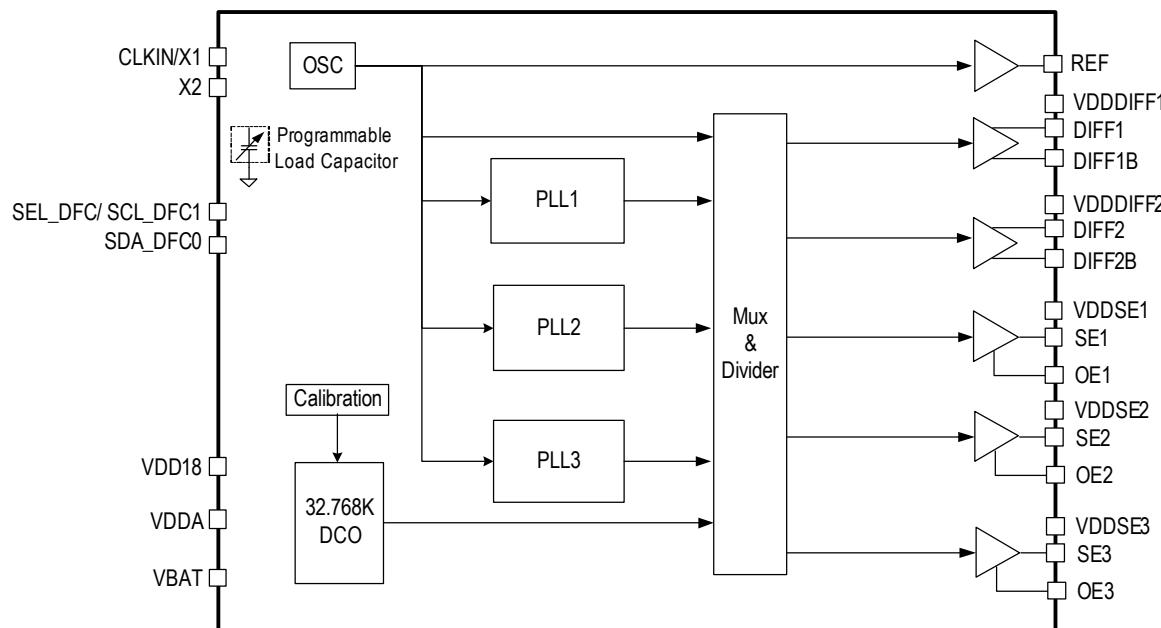
Typical Applications

- Embedded computing devices
- Consumer application crystal oscillator replacements
- SmartDevice, Handheld, and Consumer applications

Key Specifications

- PCIe Gen1/2/3 compliant
- Typical 1.5ps rms jitter integer range: 12kHz–20MHz
- Typical ultra-power-down current 50µA
- < 2µA RTC clock in Suspend Mode operation

Block Diagram



Features

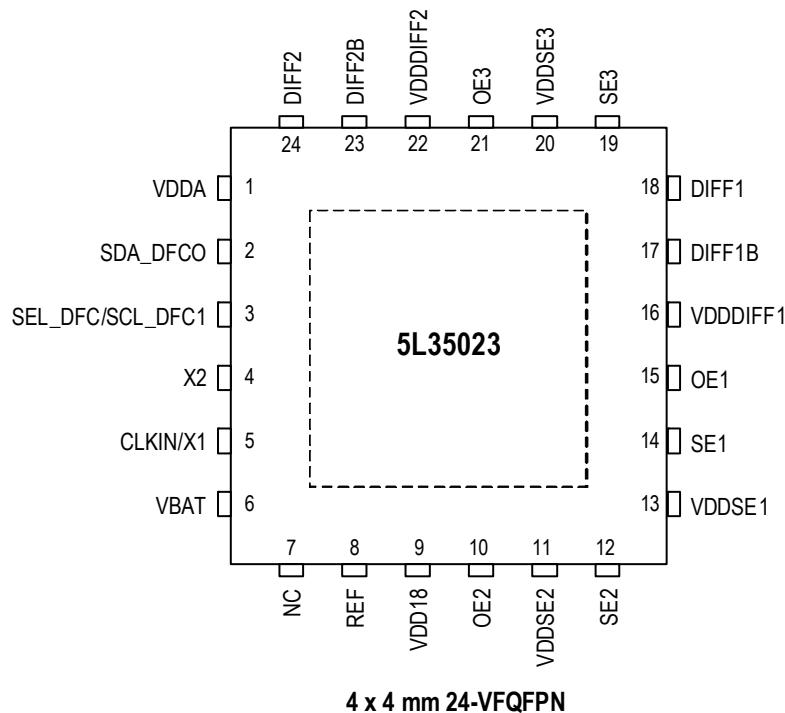
- Configurable OE pin function as OE, PD#, PPS or DFC control function
- Configurable PLL bandwidth; minimizes jitter peaking
- PPS: Proactive Power Saving features save power during the end device power down mode
- PPB: Performance Power Balancing feature allows minimum power consumption based on required performance
- DFC: Dynamic Frequency Control feature allows user to dynamically switch between and up to 4 different frequencies smoothly
- Spread spectrum clock to lower system EMI
- I²C interface
- Suspend Mode, featuring RTC clock only when system goes into low-power operation modes

Output Features

- 2 DIFF outputs with configurable LPHSCL, LVCMOS output pairs: 1MHz–125MHz
- 3 LVCMOS outputs: 1MHz–125MHz
- LVPECL, LVDS, CML and SSTL logic can be easily supported with the LP-HCSL outputs. See application note [AN-891](#) for alternate terminations
- Maximum of 8 LVCMOS outputs
- Low-power 32.768kHz clock supported for all SE1–SE3

Pin Assignments

Figure 1. Pin Assignments for 4 x 4 mm 24-VFQFPN Package – Top View



Pin Descriptions

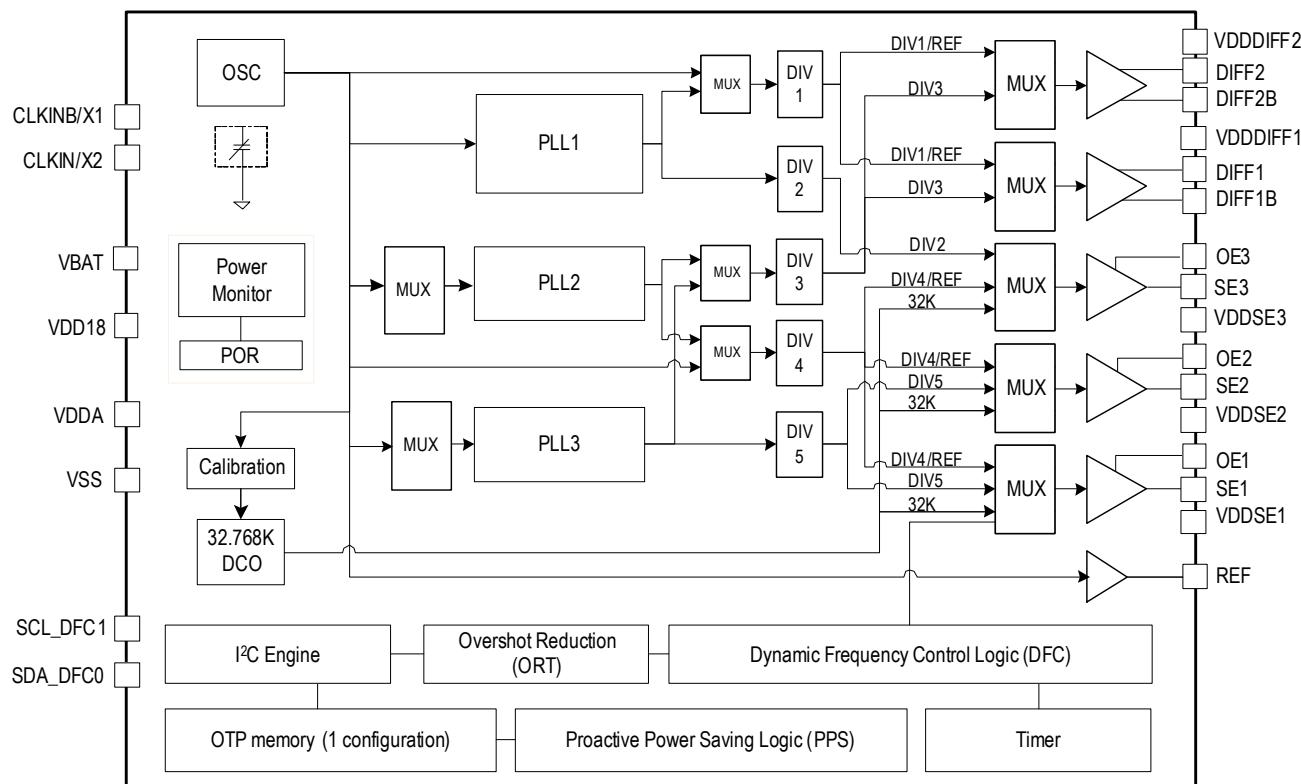
Table 1. Pin Descriptions

| Number | Name | Type | Description |
|--------|----------------------|--------|--|
| 1 | V _{DDA} | Power | V _{DD} 1.8V. |
| 2 | SDA_DFC0 | I/O | I ² C DATA pin, the pin can be DFC0 function by pin 3 SEL_DFC power on latch status. |
| 3 | SEL_DFC/ SCL_DFC1 | Input | I ² C CLK pin, SEL_DFC is a latch input pin during the power-up. High on power-on: I ² C mode as SCLK function. Low on power-on: pin 3 SCL and pin 2 SDA as DFC function control pins. |
| 4 | X2 | I/O | Crystal oscillator interface output. |
| 5 | CLKIN/X1 | Input | Crystal oscillator interface input or single-ended clock input pin (CLKIN). |
| 6 | V _{BAT} | Power | Power supply pin for 32.768kHz DCO; usually connect to coin cell battery, 1.8V. Unused V _{BAT} can be connected to V _{DD18} . |
| 7 | NC | — | No connection. |
| 8 | REF | Output | 1.8V reference clock output. |
| 9 | V _{DD18} | Power | V _{DD} 1.8V. |
| 10 | OE2 | Input | Output enable control 2, multi-function pin. Refer to OE function table. |
| 11 | V _{DDSE2} | Power | Output power supply. Connect to 1.8V. Sets output voltage levels for SE2. |
| 12 | SE2 | Output | Output clock SE2. |
| 13 | V _{DDSE1} | Power | Output power supply. Connect to 1.8V. Sets output voltage levels for SE1. |

Table 1. Pin Descriptions (Cont.)

| Number | Name | Type | Description |
|--------|----------------------|--------|---|
| 14 | SE1 | Output | Output clock SE1. |
| 15 | OE1 | Input | OE1 function selected from OTP pre-program register bits. OE1 pull to 6.5V when burn OTP registers. Refer to OE function table for details. |
| 16 | V _{DDDIFF1} | Power | Output power supply. Connect to 1.8V. Sets output voltage levels for DIFF1. |
| 17 | DIFF1B | Output | Differential clock output 1_Complement; can be OTP pre-programmed to LVCMS/LPHCSL output type. |
| 18 | DIFF1 | Output | Differential clock output 1_True; can be OTP pre-programmed to LVCMS/LPHCSL output type. |
| 19 | SE3 | Output | Output clock SE3. |
| 20 | V _{DDSE3} | Power | Output power supply. Connect to 1.8V. Sets output voltage levels for SE3. |
| 21 | OE3 | Input | Output enable control 3, multi-function pin. Refer to OE Pin Function table. |
| 22 | V _{DDDIFF2} | Power | Output power supply. Connect to 1.8V. Sets output voltage levels for DIFF2. |
| 23 | DIFF2B | Output | Differential clock output 2_Complement; can be OTP pre-programmed to LVCMS/LPHCSL output type. |
| 24 | DIFF2 | Output | Differential clock output 2_True; can be OTP pre-programmed to LVCMS/LPHCSL output type. |
| | EPAD | Power | Connect to ground pad. |

Detailed Block Diagram



Power Group

Table 2. Power Group

| Power Supply | SE | DIFF | DIV | MUX | PLL | DCO | REF | Xtal |
|---------------|------------------|-------|--------|---------|------|-----|-----|------|
| V_{DDSE1} | SE1 ¹ | | | | | | | |
| V_{DDSE2} | SE2 ¹ | | | | | | | |
| V_{DDSE3} | SE3 ¹ | | | | | | | |
| $V_{DDDIFF1}$ | | DIFF1 | DIV3/4 | MUXPLL2 | PLL2 | | | |
| $V_{DDDIFF2}$ | | DIFF2 | DIV1 | MUXPLL1 | | | | |
| V_{DD18} | | | DIV5 | | PLL3 | DCO | REF | Xtal |
| V_{BAT} | | | | | | DCO | | Xtal |
| V_{DDA} | | | DIV2 | | PLL1 | | | |

¹ V_{DDSEx} for non-32kHz outputs should be OFF when V_{DDA}/V_{DD18} turns OFF; VBAT mode only supports 32.768kHz outputs from SE1–3.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 5L35023 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3. Absolute Maximum Ratings

| Item | Rating |
|--|--|
| Supply Voltage, V_{DDA} , V_{DD18} , V_{DDSE} , V_{DDDIFF} | $V_{DD} + 5\%$ maximum |
| Supply Voltage, V_{BAT} | $V_{DD} + 5\%$ maximum |
| Inputs | |
| XIN/CLKIN | 0V to 1.8V voltage swing for both LVCMOS or DIFF CLK |
| Other Inputs | -0.5V to V_{DD18} or V_{DDSE} |
| Outputs, V_{DDSE} (LVCMOS) | -0.5V to V_{DDSE} or $V_{DDDIFF} + 0.5V$ |
| Outputs, IO (SDA) | 10mA |
| Package Thermal Impedance, Θ_{JA} | 42°C/W (0mps) |
| Package Thermal Impedance, Θ_{JC} | 41.8°C/W (0mps) |
| Storage Temperature, T_{STG} | -65°C to 150°C |
| ESD Human Body Model | 2000V |
| Junction Temperature | 125°C |

Recommended Operating Conditions

Table 4. Recommended Operating Conditions

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|-----------------|---|---------|---------|---------|------|
| V_{DDSEX} | Power supply voltage for supporting 1.8V outputs. | 1.71 | 1.8 | 1.89 | V |
| V_{DD18} | Power supply voltage for core logic functions. | 1.71 | 1.8 | 1.89 | V |
| V_{DDA} | Analog power supply voltage. Use filtered analog power supply if available. | 1.71 | 1.8 | 1.89 | V |
| V_{BAT} | Battery power supply voltage. | 1.71 | 1.8 | 1.89 | V |
| T_A | Operating temperature, ambient. | -40 | | 85 | °C |
| C_{LOAD_OUT} | Maximum load capacitance (LVC MOS only). | | 5 | | pF |
| F_{IN} | External reference crystal. | 8 | | 40 | MHz |
| | External reference clock CLKIN, CLKINB. | 1 | | 125 | |
| t_{PU} | Power-up time for all V_{DDs} to reach minimum specified voltage (power ramps must be monotonic). | 0.05 | | 3 | ms |

Crystal Characteristics

Table 5. Crystal Characteristics

| Parameter | Minimum | Typical | Maximum | Unit |
|--------------------------------------|-------------|---------|---------|------|
| Mode of Oscillation | Fundamental | | | |
| Frequency | 8 | | 40 | MHz |
| Frequency when 32.768kHz DCO is used | 8 | 25 | 39 | MHz |
| Equivalent Series Resistance (ESR) | | 10 | 100 | Ω |
| Shunt Capacitance | | 2 | 7 | pF |
| Load Capacitance (C_L) | 6 | 8 | 10 | pF |
| Maximum Crystal Drive Level | | 30 | 100 | μW |

Electrical Characteristics

Supply voltage: all $V_{DD} \pm 5\%$, unless stated otherwise

Table 6. Electrical Characteristics – Current Consumption ^{1,2}

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|------------------------------|---------------------------------|---|---------|---------|---------|---------|
| I_{DDCORE} | Core Supply Current | $V_{DD} = V_{DDSE} = V_{DD18} = 1.8V$; XTAL = 25MHz, PLL2/3 off, no output, PLLs disabled. | | 3.4 | 4.8 | mA |
| I_{DD_PLL1} ³ | PLL1 Supply Current | $V_{DD} = V_{DDSE} = V_{DD18} = 1.8V$; XTAL = 25MHz, PLL2/3 off, no output, PLL1 = 600MHz. | | 12.1 | 15.3 | mA |
| I_{DD_PLL2} ³ | PLL2 Supply Current | $V_{DD} = V_{DDSE} = V_{DD18} = 1.8V$; XTAL = 25MHz, PLL1/3 off, no output, PLL2 = 60MHz. | | 0.5 | 0.8 | mA |
| I_{DD_PLL3} ³ | PLL3 Supply Current | $V_{DD} = V_{DDSE} = V_{DD18} = 1.8V$; XTAL = 25MHz, PLL1/2 off, no output, PLL3 = 480MHz. | | 2.5 | 3.2 | mA |
| I_{DDOx} | Output Buffer Supply Current | LPHCSL, 125MHz, 1.8V V_{DDDIFF} , no load (DIFF1,2). | | 3.4 | 4.1 | mA |
| | | LPHCSL, 100MHz, 1.8V V_{DDDIFF} , no load (DIFF1,2). | | 2.9 | 3.5 | mA |
| | | LVCMS, 8MHz, 1.8V, V_{DDSE} ^{1,2} (SE1). | | 0.5 | 0.6 | mA |
| | | LVCMS, 160MHz, 1.8V V_{DDSE} ^{1,2} (SE1). | | 2.7 | 3.4 | mA |
| I_{DDPD} ³ | Power Down Current–LPHCSL | I^2C functional during power-down, just 32kHz running (if any); DIFF outputs in LPHCSL mode are high/low. | | 2.6 | 3.4 | mA |
| I_{DDPD} ^{3,6} | Power Down Current–LVCMS | I^2C functional during power-down, just 32kHz running (if any); DIFF outputs in LVCMS mode are high/low or low/low. | | 0.5 | 1 | mA |
| I_{DDUPD} ⁴ | Ultra Power Down Current–LPHCSL | I^2C functional during power-down, just 32kHz running (if any); DIFF outputs in LPHCSL mode are low/low. | | 33 | 65 | μA |
| I_{DDUPD} ⁴ | Ultra Power Down Current–LVCMS | I^2C functional during power-down, just 32kHz running (if any) – DIFF outputs in LVCMS mode are low/low. | | 33 | 65 | μA |
| $I_{DDSUSPEND}$ ⁵ | Suspend Mode Current–32kHz x 1 | I^2C off in Suspend Mode. One 32kHz output running. | | 1.4 | 2.1 | μA |
| $I_{DDSUSPEND}$ ⁵ | Suspend Mode Current–32kHz x 2 | I^2C off in Suspend Mode. Two 32kHz outputs running. | | 3.2 | 7.9 | μA |
| $I_{DDSUSPEND}$ ⁵ | Suspend Mode Current–32kHz x 3 | I^2C off in Suspend Mode. Three 32kHz outputs running. | | 3.7 | 8.6 | μA |

¹ All output currents measured with 0.5 inch transmission line and 0pF load.

² Single CMOS driver active.

³ Power-down can be controlled by PD (OE1 input pin) and/or I^2C bit.

⁴ Ultra power-down must be controlled by PD (OE1 input pin).

⁵ Suspend Mode requires all V_{DD} to GND except V_{DDSEN} (as desired) and V_{DD18} .

⁶ DIFF outputs in LVCMS mode can power-down to be high/low or low/low, depending on register 0x22[1:0].

Table 7. Electrical Characteristics – Input Parameters

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|-------------|--|---|------------------------|---------|------------------------|------------|
| V_{IH} | Input High Voltage | Single-ended inputs–OE pins. | $0.65 \times V_{DDSE}$ | | $V_{DDSE} + 0.3$ | V |
| V_{IL} | Input Low Voltage | Single-ended inputs–OE pins. | GND - 0.3 | | $0.35 \times V_{DDSE}$ | V |
| V_{IH} | Input High Voltage–SEL_DFC | Single-ended latched input. | $0.65 \times V_{DDSE}$ | | $V_{DDSE} + 0.3$ | V |
| V_{IL} | Input Low Voltage–SEL_DFC | Single-ended latched input. | GND - 0.3 | | $0.35 \times V_{DDSE}$ | V |
| V_{SWING} | Input Amplitude–CLKIN | Single-ended input swing. | 600 | | V_{DD} | mV |
| I_{IL} | Input Leakage Low Current | $V_{IN} = GND$. | -20 | | 20 | μA |
| I_{IH} | Input Leakage High Current | $V_{IN} = 1.89V$. | -20 | | 20 | μA |
| d_{TIN} | Input Duty Cycle | Measurement from differential waveform. | 45 | | 55 | % |
| C_{IN} | Input Capacitance (CLKIN, CLKINB, OE, SDA, SCL, DFC1:0). | | | 3 | 7 | pF |
| R_{PDR} | Pull-down Resistor–OE pin | | | 550 | | k Ω |
| R_{OUT} | LVC MOS Output Driver Impedance ($V_{DDSE} = 1.8V$) | | | 17 | | Ω |

Table 8. Electrical Characteristics – LVC MOS

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|------------|------------------------|---|-----------------------|---------|------------------------|---------|
| V_{OH} | Output High Voltage | $I_{OH} = -8mA$. | $0.7 \times V_{DDSE}$ | | V_{DDSE} | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 8mA$. | | | $0.25 \times V_{DDSE}$ | V |
| I_{OZDD} | Output Leakage Current | Tri-state outputs, $V_{DDSE} = 1.89V$. | | | 3 | μA |
| $t_{R/F}$ | Output Rise/Fall Time | Single-ended LVC MOS output clock rise and fall time, 20% to 80% of $V_{DDSE} 1.8V$. | | 1.0 | | ns |
| t_{ODC} | Output Duty Cycle | LVC MOS (measured at $V_{DDO}/2$). | 45 | | 55 | % |
| | Output Duty Cycle–REF | Reference clock output or SE1–3 fan out clock measured at $V_{DDO}/2$. | 40 | | 60 | % |

Table 9. Electrical Characteristics – LPHCSL Differential Outputs

| Symbol | Parameter | Minimum | Typical | Maximum | Unit | Notes |
|----------------|--------------------|---------|---------|---------|------|-----------|
| dV/dt | Slew Rate | 1 | 2.5 | 4 | V/ns | 1,2,3,8 |
| $\Delta dV/dt$ | Slew Rate Mismatch | | | 20 | % | 1,2,3,8,9 |
| V_{MAX} | Maximum Voltage | | | 1150 | mV | 1,6 |
| V_{MIN} | Minimum Voltage | -300 | | | mV | 1,6 |
| V_{SWING} | Voltage Swing | 300 | | | mV | 1,2,6 |

Table 9. Electrical Characteristics – LPHCSL Differential Outputs (Cont.)

| Symbol | Parameter | Minimum | Typical | Maximum | Unit | Notes |
|--------------------|----------------------------|---------|---------|---------|------|-------|
| V_{CROSS} | Crossing Voltage Value | 250 | 400 | 550 | mV | 1,4,6 |
| ΔV_{CROSS} | Crossing Voltage Variation | | | 140 | mV | 1,5,9 |
| Jitter-Cy/Cy | Cycle to Cycle Jitter | | | 160 | ps | 1,2 |
| Jitter-STJ | Short Term Period Jitter | | | 300 | ps | 1,2 |
| t_{DC} | Duty Cycle | 45 | | 55 | % | 1,2 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Measured from differential waveform.

³ Slew rate is measured through the V_{SWING} voltage range centered around differential 0V. This results in a ± 150 mV window around differential 0V.

⁴ V_{CROSS} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁵ The total variation of all V_{CROSS} measurements in any particular system. Note that this is a subset of V_{CROSS} min/max (V_{CROSS} absolute) allowed. The intent is to limit V_{CROSS} induced modulation by setting ΔV_{CROSS} to be smaller than V_{CROSS} absolute.

⁶ Measured from single-ended waveform.

⁷ Measured with scope averaging off, using statistics function. Variation is the difference between minimum and maximum.

⁸ Scope average on.

⁹ 100MHz, spread off and 0.5% spread.

General AC Electrical Characteristics

$V_{DD} = 1.8V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$; spread spectrum = off

Table 10. AC Electrical Characteristics

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|--------------|-----------------------------|---|---------|---------|---------|------|
| f_{IN}^1 | Input Frequency | Input frequency limit (XIN). | 8 | | 40 | MHz |
| | | Input frequency limit (LVCMOS to X1). | 1 | | 125 | MHz |
| f_{OUT} | Output Frequency | Single-ended clock output limit (LVCMOS). | 1 | | 125 | MHz |
| | | Differential clock output frequency (LPHCSL). | 1 | | 125 | MHz |
| f_{VCO1} | VCO Frequency Range of PLL1 | VCO operating frequency range. | 300 | | 700 | MHz |
| f_{VCO2} | VCO Frequency Range of PLL2 | VCO operating frequency range. | 30 | | 130 | MHz |
| f_{VCO3} | VCO Frequency Range of PLL3 | VCO operating frequency range. | 300 | | 800 | MHz |
| t_J | Clock Jitter | Cycle-to-cycle jitter (peak-to-peak), multiple output frequencies switching, differential outputs (1.8V nominal output voltage). SE1 = 25MHz. SE2 = 100MHz. SE3 = 125MHz. DIFF1/2 = 100MHz. | | 50 | | ps |
| | | RMS phase jitter (12kHz to 20MHz integration range) differential output, 1.8V nominal output voltage. 25MHz crystal. SE1=12.5MHz-REF/2. SE2=133.333MHz-PLL3. SE3=120MHz-PLL1. DIFF1/2=100MHz-PLL1. REF=25M. | | 1.5 | | ps |
| t_{SKEW} | Output Skew | Skew between the same frequencies, with outputs using the same driver format. | | 75 | | ps |
| t_{LOCK}^2 | Lock Time | PLL/DCO lock time. | | | 10 | ms |

¹ Practical lower frequency is determined by loop filter settings.

² Includes loading the configuration bits from OTP to PLL registers. It does not include OTP programming/write time.

³ Actual PLL lock time depends on the loop configuration.

PCI Express Jitter Specifications

$V_{DDDIFF} = 1.8V \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

Table 11. PCI Express Jitter Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Industry Specification | Unit | Notes |
|-----------------------------------|---------------------------|--|---------|---------|---------|------------------------|------|-------|
| t_J (PCIe Gen1) | Phase Jitter Peak-to-Peak | $f = 100\text{MHz}/125\text{MHz}$, 25MHz crystal input. Evaluation band: 0Hz – Nyquist (clock frequency/2). | | 27 | | 86 | ps | 1,4 |
| $t_{REFCLK_HF_RMS}$ (PCIe Gen2) | Phase Jitter RMS | $f = 100\text{MHz}/125\text{MHz}$, 25MHz crystal input. High band: 1.5MHz – Nyquist (clock frequency/2). | | 1.9 | | 3.10 | ps | 2,4 |
| $t_{REFCLK_LF_RMS}$ (PCIe Gen2) | Phase Jitter RMS | $f = 100\text{MHz}/125\text{MHz}$, 25MHz crystal input. Low band: 10kHz – 1.5MHz. | | 0.9 | | 3.0 | ps | 2,4 |
| t_{REFCLK_RMS} (PCIe Gen3) | Phase Jitter RMS | $f = 100\text{MHz}/125\text{MHz}$, 25MHz crystal input. Evaluation band: 0Hz – Nyquist (clock frequency/2). | | 0.5 | | 1.0 | ps | 3,4 |

Note: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

¹ Peak-to-peak jitter after applying system transfer function for the common clock architecture. Maximum limit for PCI Express Gen1.

² RMS jitter after applying the two evaluation bands to the two transfer functions defined in the common clock architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Gen2 is 3.1ps RMS for $t_{REFCLK_HF_RMS}$ (high band) and 3.0ps RMS for $t_{REFCLK_LF_RMS}$ (low band).

³ RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the PCI_Express_Base_r3.0 10 Nov. 2010 specification, and is subject to change pending the final release version of the specification.

⁴ This parameter is guaranteed by characterization. Not tested in production.

I²C Bus Characteristics

Table 12. I²C Bus DC Characteristics

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|-----------|-----------------------|-------------------------|------------------------|---------|-----------------------|---------------|
| V_{IH} | Input High Level | | $0.7 \times V_{DD18}$ | | | V |
| V_{IL} | Input Low Level | | | | $0.3 \times V_{DD18}$ | V |
| V_{HYS} | Hysteresis of Inputs | | $0.05 \times V_{DD18}$ | | | V |
| I_{IN} | Input Leakage Current | | | | ± 1 | μA |
| V_{OL} | Output Low Voltage | $I_{OL} = 3\text{mA}$. | | | 0.4 | V |

Table 13. I²C Bus AC Characteristics

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|----------------|--|------------|-----------------------|---------|---------|------|
| F_{SCLK} | Serial Clock Frequency (SCL) | | | 100 | 400 | kHz |
| t_{BUF} | Bus Free Time between STOP and START | | 1.3 | | | μs |
| $t_{SU:START}$ | Setup Time, START | | 0.6 | | | μs |
| $t_{HD:START}$ | Hold Time, START | | 0.6 | | | μs |
| $t_{SU:DATA}$ | Setup Time, Data Input (SDA) | | 100 | | | ns |
| $t_{HD:DATA}$ | Hold Time, Data Input (SDA) ¹ | | 0 | | | μs |
| t_{OVD} | Output Data Valid from Clock | | | | 0.9 | μs |
| C_B | Capacitive Load for Each Bus Line | | | | 400 | pF |
| t_R | Rise Time, Data and Clock (SDA, SCL) | | $20 + 0.1 \times C_B$ | | 300 | ns |
| t_F | Fall Time, Data and Clock (SDA, SCL) | | $20 + 0.1 \times C_B$ | | 300 | ns |
| t_{HIGH} | High Time, Clock (SCL) | | 0.6 | | | μs |
| t_{LOW} | Low Time, Clock (SCL) | | 1.3 | | | μs |
| $t_{SU:STOP}$ | Setup Time, STOP | | 0.6 | | | μs |

¹ A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Glossary of Features

Table 14. Glossary of Features

| Term | Function Description | Apply to |
|------------------|---|-----------|
| DFC | Dynamic Frequency Control; from selected PLL to support four VCO frequencies; means two different output frequencies by assigned H/W pin state changes. | PLL2 |
| ORT | Overshot Reduction; when the DFC dynamic frequency change is functional, the VCO changes frequencies smoothly to target frequency without overshoot or undershoot. | PLL2 |
| OE | Output enable function; each output can be controlled by assigned OE pin and the dedicated OE pin can be OTP programmable as global Power Down function (PD#) or Output Enable (OE) or Proactive Power Saving function (PPS) or RESET pin function. | OE1–3 |
| SS | Spread spectrum clock. | PLL1/PLL2 |
| Slew Rate | LVCMOS outputs with slew rate control – slow and fast. | LVCMOS |
| PPS | Proactive Power Saving; utilize OE pin as monitor pin for end device X2 clock status. See <i>PPS Function</i> description for details. | SE1–3 |

Device Features and Functions

Performance Power Balancing

VersaClock 3S features Performance Power Balancing with three individual programmable PLL designs and provides a balance between performance and power consumption.

The device can operate within single-digit mA low-power operation or support high-performance requirements such as PCIe Gen 3 with additional power.

In order to satisfy system trade-off, outputs have the option to route from different PLL/input sources.

Table 15. Power Saving Modes Summary

| Power Mode | External Condition | Internal Operating Condition | Core Current Consumption |
|------------------|---------------------------|--|--------------------------|
| Power-down Mode | V_{DD} all connected. | All off, I ² C still active. | 2mA |
| Ultra-power-down | V_{DD} all connected. | All off. | 50 μ A |
| Suspend Mode | Only V_{BAT} connected. | All off, only DCO on with RTC (32.768kHz) output only. | 2 μ A |

Table 16. Output Source

| Source | Outputs | | | | | |
|-----------|----------|-----------|-----------|-----------|-------|-------|
| | REF | SE1 | SE2 | SE3 | DIFF1 | DIFF2 |
| Xtal REF | Xtal REF | Xtal REF | Xtal REF | Xtal REF | | |
| 32.768kHz | | 32.768kHz | 32.768kHz | 32.768kHz | | |
| PLL1 | | | | PLL1 | PLL1 | PLL1 |
| PLL2 | | PLL2 | PLL2 | PLL2 | PLL2 | PLL2 |
| PLL3 | | PLL3 | PLL3 | | PLL3 | PLL3 |

Table 17. SE1 Output

| SE1 | B36<4> | B36<3> | B31<1> | B29<3> |
|-----------------------|--------|--------|--------|--------|
| From 32kHz | 0 | 1 | 0 | 0 |
| From PLL3 + Divider 5 | 1 | 0 | 0 | 0 |
| From PLL2 + Divider 4 | 1 | 1 | 1 | 0 |
| From REF + Divider 4 | 1 | 1 | 0 | 1 |

Table 18. SE2 Output

| SE2 | B31<7> | B31<6> | B36<0> | B31<1> | B29<3> |
|-----------------------|--------|--------|--------|--------|--------|
| From 32kHz | 0 | 0 | 0 | 0 | 0 |
| From PLL3 + Divider 5 | 1 | 0 | 0 | 0 | 0 |
| From PLL2 + Divider 4 | 1 | 1 | 1 | 1 | 0 |
| From REF + Divider 4 | 1 | 1 | 1 | 0 | 1 |

Table 19. SE3 Output

| SE3 | B33<7> | B33<6> | B7<5> | B29<3> | B36<1> | B31<1> |
|-----------------------|--------|--------|-------|--------|--------|--------|
| From 32kHz | 0 | 0 | 0 | 0 | 0 | 0 |
| From PLL1 + Divider 2 | 1 | 0 | 1 | 0 | 0 | 0 |
| From PLL2 + Divider 4 | 1 | 1 | 0 | 0 | 1 | 1 |
| From REF + Divider 4 | 1 | 1 | 0 | 1 | 1 | 0 |

Table 20. DIFF1 Output

| DIFF1 | B34<7> | B0<3> |
|-------------------------|--------|-------|
| From PLL1 + Divider 1 | 0 | 0 |
| From PLL2/3 + Divider 3 | 1 | 0 |
| From REF + Divider 1 | 0 | 1 |

Table 21. DIFF2 Output

| DIFF2 | B35<7> | B0<3> |
|-------------------------|--------|-------|
| From PLL1 + Divider 1 | 0 | 0 |
| From PLL2/3 + Divider 3 | 1 | 0 |
| From REF + Divider 1 | 0 | 1 |

DFC – Dynamic Frequency Control

- OTP programmable—4 different feedback fractional dividers (4 VCO frequencies) that apply to PLL2.
- ORT (over shoot reduction) function will be applied automatically during the VCO frequency change.
- Smooth frequency incremental or decremental from current VCO to targeted VCO base on DFC hardware pins selection.

Figure 2. DFC Function Block Diagram

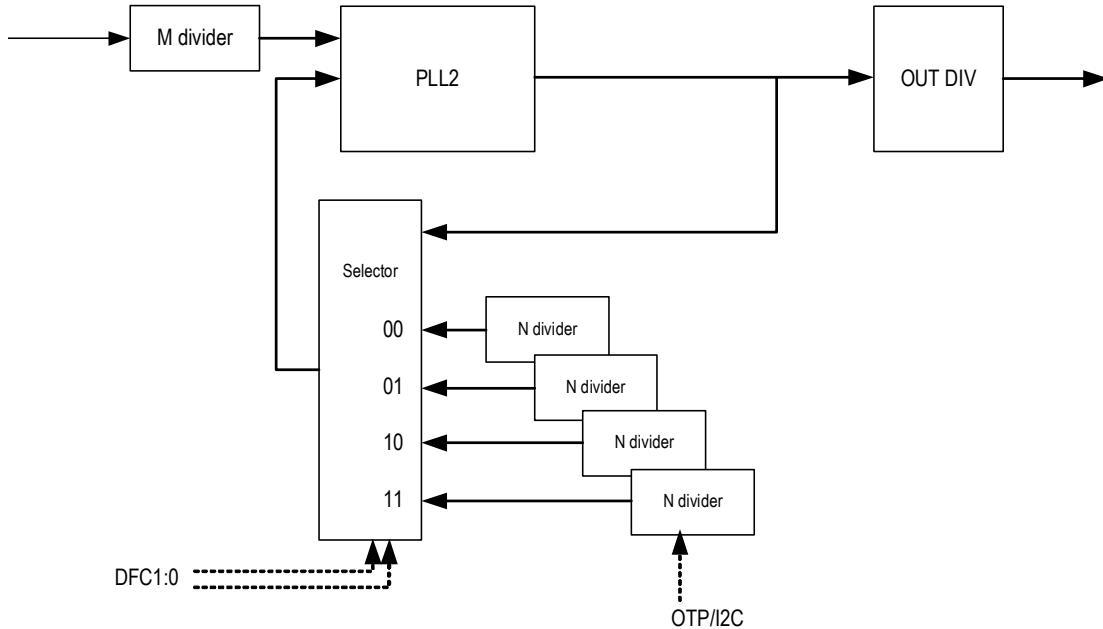


Table 22. DFC Function Priority

| DFC_EN bit (W32[4]) | OE1_fun_sel (W30[6:5]) | OE3_fun_sel (W30[3:2]) | SCL_DFC1 | DFC[1:0] | Notes |
|---------------------|------------------------|------------------------|----------|----------------------|---|
| 0 | x | x | x | 0 | DFC disable |
| 1 | 11 (DFC) | 00–10 (DFC) | x | [0,OE1] | One pin DFC–OE1 |
| 1 | 11 (DFC) | 11 (DFC) | x | [OE3,OE1] | Two pin DFC–OE3, OE1 |
| 1 | 00–10 | 11 | x | Not permitted | Not supported |
| 1 | 00–10 | 00–10 | 0 | [SCL_DFC1, SDA_DFC0] | I ² C pin as DFC control pins mode |
| 1 | 00–10 | 00–10 | 1 | W30[1:0] | I ² C control DFC mode |

DFC Function Programming

- Register B63b3:2 selects DFC00–DFC11 configuration.
- Bytes 16–19 are the registers for PLL2 VCO setting, based on B63b3:2 configuration selection, the data write to B16–19 will be stored in selected configuration OTP memory.
- Refer to *DFC Function Priority* table. Select proper control pin(s) to activate DFC function.
- Note the DFC function can also be controlled by I²C access.

PPS – Proactive Power Saving Function

PPS (Proactive Power Saving) is an IDT patented unique design for the clock generator that proactively detects end device power down state and then switches output clocks between normal operation clock frequency and low power mode 32kHz clock that only consumes $< 2\mu\text{A}$ current. The system could save power when the device goes into power down or sleep mode. The PPS function diagram is shown as below.

Figure 3. PPS Function Block Diagram

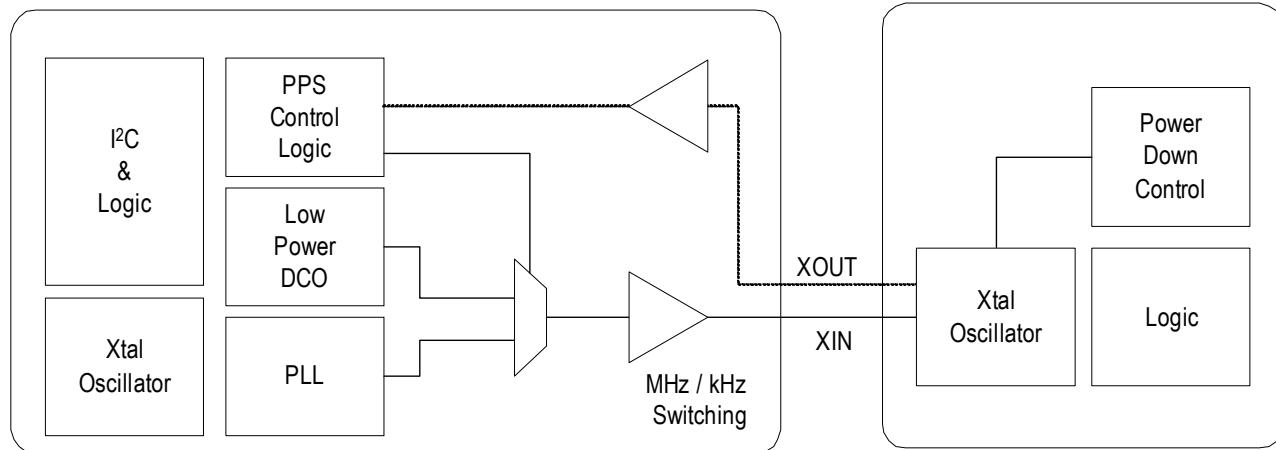
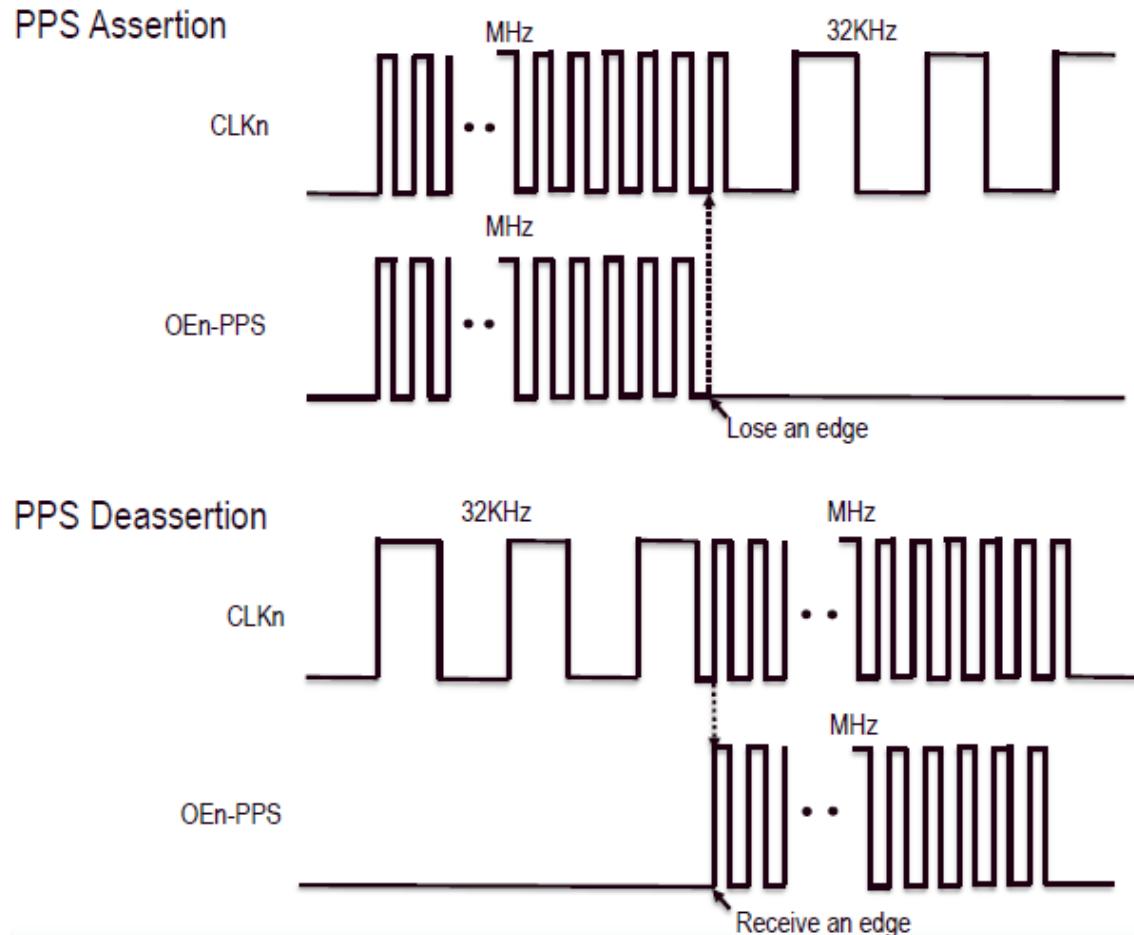


Figure 4. PPS Assertion/Deassertion Timing Chart



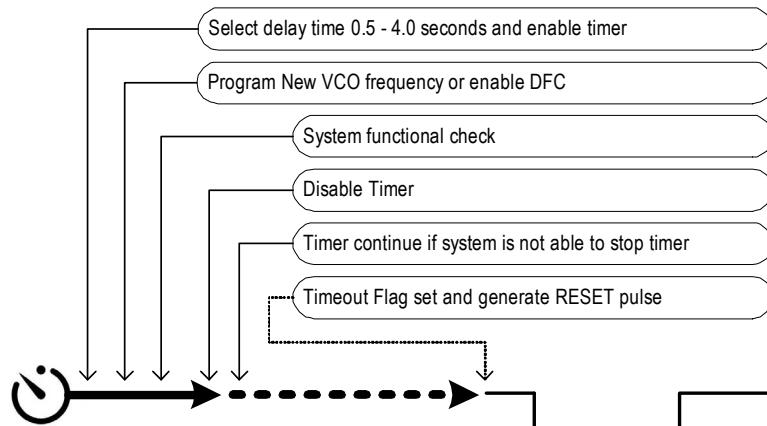
PPS Function Programming

1. Refer to the *OE Pin Functions* table to have the proper PPS function selected for OE pin(s). Note that the register default is set to Output enable (OE) function for OE pins.
2. Have proper setup to Byte 30 and 32 for OE1–OE3 function selection; for PPS function, select 10 to control register bits.

Timer Function Description

1. The timer function can be used together with the DFC (Dynamic Frequency Control) function or with another PLL frequency programming.
2. The timer provides 4 different delay times by two bits selection: 0.5 seconds, 1 seconds, 2 seconds, 4 seconds.
3. The timeout flag will be set when timer times out and the flag can be cleared by writing 0 to timer enable bit.
4. When timer times out, RESET pin can generate a 250ms pulse signal if RESET control bit is enabled.
5. When timer times out, DFC stage will switch back to DFC00 setting if DFC function is enabled and DFC function will be disabled after RESET.

Figure 5. Timer Functions



OE Pin Function

OE pins in the 5L35023 have multiple functions. The OE pins can be configured as output enable control (OE) or chip power-down control (PD#) or Proactive Power Saving function (PPS). Furthermore, the OE pins can be configured as single or two-pin Dynamic Frequency Control (DFC), or the RESET out function that is associated with the Timer function.

Table 23. OE Pin Functions

| Function | Pin | | |
|------------------------------|---------------|---------------|---------------|
| | OE1 | OE2 | OE3 |
| SE Output Enable/Disable | SE1 (default) | SE2 (default) | SE3 (default) |
| DIFF Output Enable/Disable | — | DIFF1/DIFF2 | — |
| Global Power Down (PD#) | PD# | — | — |
| Proactive Power Saving Input | SE1_PPS | SE2_PPS | SE3_PPS |
| DOC Control (Only PLL2) | DFC0 | — | DFC1 |
| RESET OUT | — | RESET OUT | — |

Table 24. OE Pin Function Summary

| OE Pin | Description |
|------------------|--|
| OE1: SE1 | OE1 only control SE1 enable/disable; other outputs are not affected by this pin status. |
| OE2: SE2 | OE2 only control SE2 enable/disable; other outputs are not affected by this pin status. |
| OE3: SE3 | OE3 only control SE3 enable/disable; other outputs are not affected by this pin status. |
| OE2: DIFF1/DIFF2 | OE2 control differential outputs 1 and 2 only; other SE outputs are not affected by this pin status. |
| OE1: PD# | OE1 control chip global power down (PD#) except 32.768kHz on OE1 (when 32kHz is enabled). When the PD# pin is active low, the chip goes to lowest power down mode and all outputs are disabled except 32kHz output and only keep 32kHz/Xtal calibration. |
| OE1: SE1_PPS | Configure OE1 as SE1_PPS (Proactive Power Saving) function pin. |
| OE2: SE2_PPS | Configure OE2 as SE2_PPS (Proactive Power Saving) function pin. |
| OE3: SE3_PPS | Configure OE3 as SE3_PPS (Proactive Power Saving) function pin. |
| OE1: DFC0 | Configure OE1 as DFC0 control pin 0. |
| OE3/DFC1 | Configure OE3 as DFC1 control pin 1. |

Table 25. PD# Priority

| PD# | I2C_OE_EN_bit | SE1/2/3, DIFF1/DIFF2 | Output | Notes |
|-----|---------------|----------------------|---------|----------------|
| 0 | x | x | stop | 32kHz free run |
| 1 | 0 | x | stop | |
| 1 | 1 | 0 | stop | |
| 1 | 1 | 1 | running | |

Crystal Input (X1/X2)

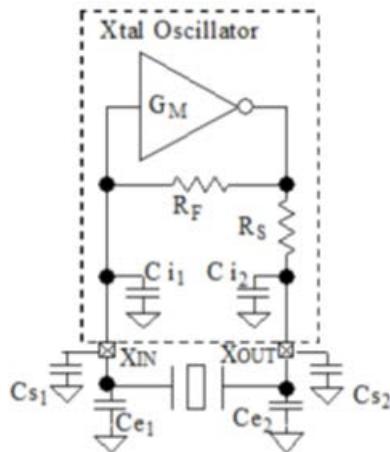
The crystal oscillators should be fundamental mode quartz crystals; overtone crystals are not suitable. Crystal frequency should be specified for parallel resonance with 40MHz maximum.

A crystal manufacturer will calibrate its crystals to the nominal frequency with a certain load capacitance value. When the oscillator load capacitance matches the crystal load capacitance, the oscillation frequency will be accurate as 0 PPM. When the oscillator load capacitance is lower than the crystal load capacitance, the oscillation frequency will be higher than nominal. In order to get an accurate oscillation frequency, the matching the oscillator load capacitance with the crystal load capacitance is required.

To set the oscillator load capacitance, 5L35023 has built-in two programmable tuning capacitors inside the chip, one at XIN and one at XOUT. They can be adjusted independently. The value of each capacitor is composed of a fixed capacitance amount plus a variable capacitance amount set with the XTAL[7:0] register. Adjustment of the crystal tuning capacitors allows for maximum flexibility to accommodate crystals from various manufacturers. The range of tuning capacitor values available are in accordance with the following table.

Table 26. Programmable Tuning Caps

| Parameter | Bits | Range | Minimum (pF) | Maximum (pF) |
|------------|-------|---------------------|--------------|--------------|
| Xtal [7:0] | 4 × 2 | +1 / +2 / +4 / +8pF | 0 | 15pF |



$$XTAL[3:0] = XTAL[7:4] = 2 \times XTAL C_L - 8pF \quad (\text{Eq.1})$$

Equation 1 and the table of XTAL[7:0] tuning capacitor characteristics show that the parallel tuning capacitance can be set between 0pF to 15pF with a resolution of 1pF.

For a crystal $C_L = 8pF$, where C_L is the parallel capacity specified by the crystal vendor that sets the crystal frequency to the nominal value. Under the assumptions that the stray capacity between the crystal leads on the circuit board is zero and that no external tuning caps are placed on the crystal leads, then the internal parallel tuning capacity is equal to the load capacity presented to the crystal by the device.

The internal load capacitors are true parallel-plate capacitors for ultra-linear performance. Parallel-plate capacitors were chosen to reduce the frequency shift that occurs when non-linear load capacitance interacts with load, bias, supply, and temperature changes. External non-linear crystal load capacitors should not be used for applications that are sensitive to absolute frequency requirements.

The 5L35023 supports spread spectrum clocks from PLL1 and PLL2; the PLL1 built-in with analog spread spectrum and PLL2 has digital spread spectrum.

Spread Spectrum

The 5L35023 supports spread spectrum clocks from PLL1 and PLL2; the PLL1 built-in with analog spread spectrum and PLL2 has digital spread spectrum.

Table 27. Spread Spectrum Generation Specifications

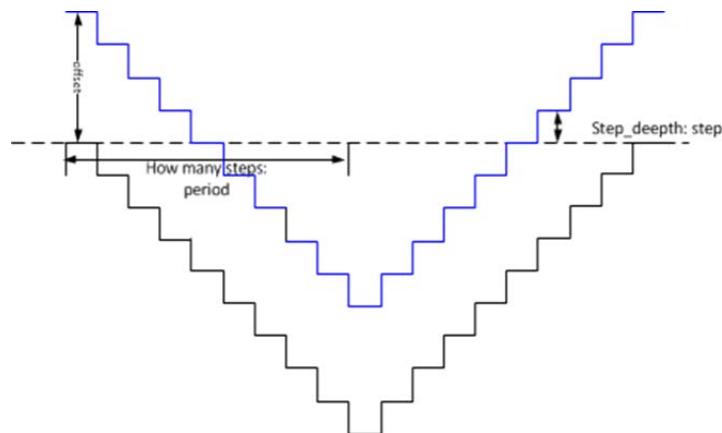
| Symbol | Parameter | Description | Minimum | Typical | Maximum | Unit |
|---------------------|------------------|--|---------|--------------|---------|--------------------|
| f_{OUT} | Output Frequency | Output frequency range. | 1 | | 125 | MHz |
| f_{MOD} | Mod Frequency | Modulation frequency. | | 30 to 63 | | kHz |
| f_{SPREAD} | Spread Value | Amount of spread value (programmable)–down spread. | | -0.5% to -2% | | % f_{OUT} |
| %tolerance | Spread% Value | Variation of spread range. | | 15 | | % |

Figure 6. Digital Spread Spectrum

$$N = \frac{F_{VCO}}{2 * F_{OUT}}$$

$$\text{period} = \frac{F_{PFD}}{2 * F_{SS}}$$

$$\text{step} = \frac{N * \text{SSamount}}{\text{period}}$$



Down spread or Spread off

$$N = F_{VCO}/F_{PFD}$$

Center Spread

$$N = N_{Soff} + N * \text{SSamount}/2$$

N: include integer and fraction

F_{VCO}: VCOs frequency

F_{PFD}: PLLs pfd frequency

F_{SS}: spread modulation rate

SSamount: spread percentage

The black line is for the down spread; N will decrease to make the center frequency is lower than spread off.

The blue line is for the center spread; there is an offset put on divider ratio to make the center frequency keep same as spread off.

Example: 0.5% down spread at 32kHz modulation rate.

Suspend Mode with RTC Clock Only

VersaClock 3S can operate on the following two modes:

- Full-power mode:
 - Full chip active with the most functionality and all V_{DD}s are connected to power supply.
- Low-power Suspend Mode:
 - Device power-up with below sequence:
 1. V_{BAT} and all other V_{DD}s are powered up. V_{BAT} ramp must be earlier or same time as other V_{DD}s.
 2. After full power up is completed, the device can go into Suspend Mode triggered by V_{BAT} is powered and rest of the V_{DD}s ramped down (ramp down time slower than 3ms).

In Suspend Mode, device will operate with a 2uA core power with only V_{BAT} powered up. Producing 32kHz outputs on SEx outputs (it can be multiple copies). Operating at this state helps system in power-down, or sleep mode without losing date-time information at a very low power budget. When system waking up, device will go back to full power mode automatically and produce outputs upon user configuration.

When there is core power present (V_{DD18} and V_{DDA}), the device will switch DCO supply to core power to save battery.

ORT-VCO Overshoot Reduction Technology

The 5L35023 supports the VCO overshoot reduction technology (ORT) to prevent an output clock frequency spike when the device is changing frequency on the fly or doing DFC (Dynamic Frequency Control) function. The VCO frequency changes are under control instead of free-run to targeted frequency.

PLL Features and Descriptions

Table 28. Output 1 Divider

| Output Divider bits <1:0> | Output Divider bits <3:2> | | | |
|---------------------------|---------------------------|----|----|----|
| | 00 | 01 | 10 | 11 |
| 00 | 1 | 2 | 4 | 8 |
| 01 | 4 | 8 | 16 | 32 |
| 10 | 5 | 10 | 20 | 40 |
| 11 | 6 | 12 | 24 | 48 |

Table 29. Output 2, 4, and 5 Divider

| Output Divider bits <1:0> | Output Divider bits <3:2> | | | |
|---------------------------|---------------------------|----|----|----|
| | 00 | 01 | 10 | 11 |
| 00 | 1 | 2 | 4 | 5 |
| 01 | 3 | 6 | 12 | 15 |
| 10 | 5 | 10 | 20 | 25 |
| 11 | 10 | 20 | 40 | 50 |

Table 30. Output 3 Divider

| Output Divider bits <1:0> | Output Divider bits <3:2> | | | |
|---------------------------|---------------------------|----|----|----|
| | 00 | 01 | 10 | 11 |
| 00 | 1 | 2 | 4 | 8 |
| 01 | 3 | 6 | 12 | 24 |
| 10 | 5 | 10 | 20 | 40 |
| 11 | 10 | 20 | 40 | 80 |

Applications

Input Clock Recommendations

CLKINB/X1 and CLKIN/X2

If used as crystal inputs, each set of pins must be connected to a crystal. If using these pins as X1/X2 see Xtal section, if using as CLKINB/CLKIN, see [Crystal Input \(X1/X2\)](#) and [Input-Driving the XIN/CLKIN or CLKIN](#) sections. If overdriving, set byte 0 bit 1 to enable.

Recommendations for Unused Input and Output Pins

LVC MOS Control Pins

LVC MOS control pins have internal pull-downs outlined in [Table 31](#). Additional resistance is not required but may be added for additional protection. A $10\text{k}\Omega$ resistor can be used.

LVC MOS Outputs

Any LVC MOS output can be left floating if unused. There should be no trace attached. The output buffer should be disabled by setting 0x22[0] to 0.

Differential Outputs

All unused differential outputs can be left floating. Renesas recommends that no trace be attached and that the outputs be disabled through 0x1D[3] and 0x1D[4]. Both sides of the differential output pair should be treated the same, either left floating or terminated.

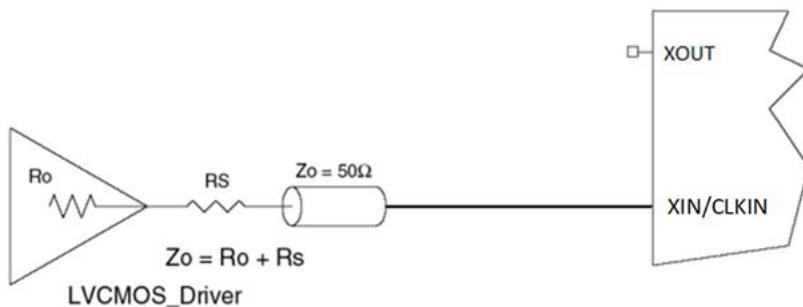
Input-Driving the XIN/CLKIN or CLKIN

In some cases, it is encouraged to have CLKINB/X1 driven by a clock input for reasons like better SNR, multiple input select with device CLKIN, etc. The CLKINB/X1 pin requires an input amplitude outlined in the [Driving XIN/CLKIN with a CMOS Driver](#).

Driving XIN/CLKIN with a CMOS Driver

The CLKINB/X1 input can be overdriven by an LVC MOS driver or by one side of a differential driver through an AC coupling capacitor. The CLKIN/X2 pin must be left floating.

Figure 7. LVC MOS Driver to XTAL Input Interface



If using an input of 3.3V or 2.5V or 1.8V to drive the part, a voltage divider configuration like this is needed:

Figure 8. LVCMS Driver to XTAL Input Interface

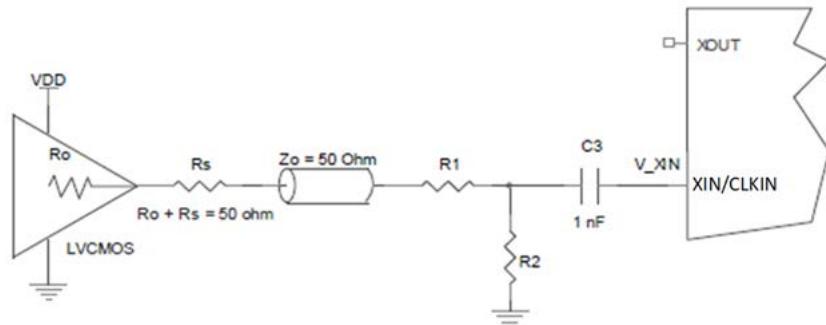


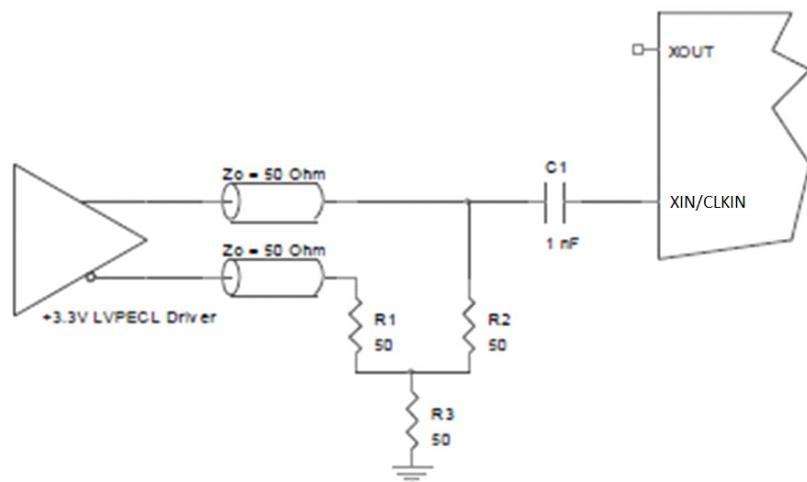
Table 31. Nominal Voltage Divider Values for Overdriving XIN with Single-ended Driver

| LVCMS Driver V _{DD} | R _o +R _s | R1 | R2 | V _{XIN} | R _o +R ₁ +R ₂ |
|---------------------------------|--------------------------------|-----|-----|------------------|--|
| 3.3 | 50.0 | 130 | 75 | 0.97 | 255 |
| 2.5 | 50.0 | 100 | 100 | 1.00 | 250 |
| 1.8 | 50.0 | 62 | 130 | 0.97 | 242 |

Driving XIN with an LVPECL Driver

Figure x. shows an example of the interface diagram for a +3.3V LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the CLKINB/X1 input. It is recommended that all components in the schematics be placed in the layout; though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input. If the driver is 2.5V LVPECL, the only change necessary is to use the appropriate value of R3.

Figure 9. Overdriving XIN with an LVPECL Driver



CLKIN is able to accept both LVDS and LVPECL input signals as it is internally AC coupled. However, occasionally, it is desired to have CLKIN to take CMOS levels. This is achieved by using the same configuration as shown in [Figure 8](#), without the C3 capacitor.

Output Clock Test Conditions

Figure 10. LVC MOS Output Test Conditions

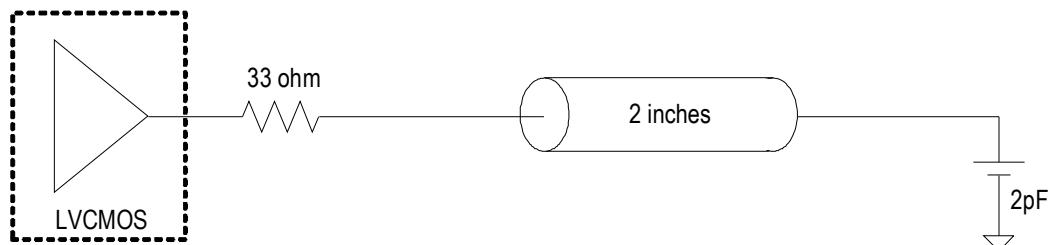
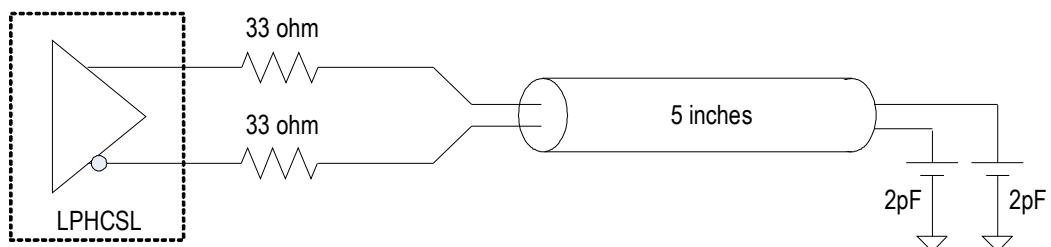


Figure 11. LP-HCSL Output Test Conditions



General I²C Mode Operations

The device acts as a slave device on the I²C bus using one of the four I²C addresses (0xD0, 0xD2, 0xD4, or 0xD6) to allow multiple devices to be used in the system. The interface accepts byte-oriented block write and block read operations. Two address bytes specify the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP bit is received, at which point, all data received in the block write will be written simultaneously.

For full electrical I²C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-down resistors have a size of 100kΩ typical.

Figure 12. I²C Slave Read and Write Cycle Sequencing

Current Read



Sequential Read



Sequential Write



from master to slave
 from slave to master

S = start
Sr = repeated start
A = acknowledge
Abar = none acknowledge
P = stop

Byte 0: General Control

| Byte 00h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|----------------|-----------------------------------|------|------------------------------------|-----------------------|-----|
| Bit 7 | OTP_Burned | OTP memory programming indication | R/W | OTP memory non-programmed | OTP memory programmed | 0 |
| Bit 6 | I2C_addr[1] | I2C address select bit 1 | R/W | 00: D0 / 01: D2 10: D4 / 11: D6 | 0 | 0 |
| Bit 5 | I2C_addr[0] | I2C address select bit 0 | R/W | | 11: D6 | 0 |
| Bit 4 | PLL1_SSEN | PLL1 Spread Spectrum enable | R/W | disable | enable | 0 |
| Bit 3 | DIV1_src_sel | Divider 1 source clock select | R/W | PLL1 | Xtal | 0 |
| Bit 2 | PLL3_refin_sel | PLL3 source selection | R/W | Xtal | Seed (DIV2) | 0 |
| Bit 1 | Reserved | | | | | 0 |
| Bit 0 | OTP_protect | OTP memory protection | R/W | read/write | write locked | 0 |

Byte 1: Dash Code ID (optional)

| Byte 01h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|----------------|------------------|------|---|---|-----|
| Bit 7 | DashCode ID[7] | Dash code ID | R/W | — | — | 0 |
| Bit 6 | DashCode ID[6] | Dash code ID | R/W | — | — | 0 |
| Bit 5 | DashCode ID[5] | Dash code ID | R/W | — | — | 0 |
| Bit 4 | DashCode ID[4] | Dash code ID | R/W | — | — | 0 |
| Bit 3 | DashCode ID[3] | Dash code ID | R/W | — | — | 0 |
| Bit 2 | DashCode ID[2] | Dash code ID | R/W | — | — | 0 |
| Bit 1 | DashCode ID[1] | Dash code ID | R/W | — | — | 0 |
| Bit 0 | DashCode ID[0] | Dash code ID | R/W | — | — | 0 |

Byte 2: Crystal Cap Setting

| Byte 02h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|-------------|-----------------------------|------|------------------------------|---|-----|
| Bit 7 | Xtal_Cap[7] | Xtal cap load trimming bits | R/W | x1 x2 x4 x8 total 15pf | 0 | 0 |
| Bit 6 | Xtal_Cap[6] | Xtal cap load trimming bits | R/W | | 0 | 0 |
| Bit 5 | Xtal_Cap[5] | Xtal cap load trimming bits | R/W | | 0 | 0 |
| Bit 4 | Xtal_Cap[4] | Xtal cap load trimming bits | R/W | | 1 | 1 |
| Bit 3 | Xtal_Cap[3] | Xtal cap load trimming bits | R/W | | 0 | 0 |
| Bit 2 | Xtal_Cap[2] | Xtal cap load trimming bits | R/W | | 0 | 0 |
| Bit 1 | Xtal_Cap[1] | Xtal cap load trimming bits | R/W | | 0 | 0 |
| Bit 0 | Xtal_Cap[0] | Xtal cap load trimming bits | R/W | | 1 | 1 |

Byte 3: PLL3 M Divider

| Byte 03h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|---------------|--------------------------------|------|----------------|---------------------|-----|
| Bit 7 | PLL3_MDIV1 | PLL3 source clock divider | R/W | disable M DIV1 | bypadd divider (/1) | 0 |
| Bit 6 | PLL3_MDIV2 | PLL3 source clock divider | R/W | disable M DIV2 | bypadd divider (/2) | 0 |
| Bit 5 | PLL3_M_DIV[5] | PLL3 reference integer divider | R/W | 3-64 | default 25 | 0 |
| Bit 4 | PLL3_M_DIV[4] | PLL3 reference integer divider | R/W | — | — | 1 |
| Bit 3 | PLL3_M_DIV[3] | PLL3 reference integer divider | R/W | — | — | 1 |
| Bit 2 | PLL3_M_DIV[2] | PLL3 reference integer divider | R/W | — | — | 0 |
| Bit 1 | PLL3_M_DIV[1] | PLL3 reference integer divider | R/W | — | — | 0 |
| Bit 0 | PLL3_M_DIV[0] | PLL3 reference integer divider | R/W | — | — | 1 |

Byte 4: PLL3 N Divider

| Byte 04h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|---------------|--|------|--|---|-----|
| Bit 7 | PLL3_N_DIV[7] | PLL3 VCO feedback integer divider bit7 | R/W | 12-2048, default VCO setting is 480MHz | 1 | |
| Bit 6 | PLL3_N_DIV[6] | PLL3 VCO feedback integer divider bit6 | R/W | | 1 | |
| Bit 5 | PLL3_N_DIV[5] | PLL3 VCO feedback integer divider bit5 | R/W | | 1 | |
| Bit 4 | PLL3_N_DIV[4] | PLL3 VCO feedback integer divider bit4 | R/W | | 0 | |
| Bit 3 | PLL3_N_DIV[3] | PLL3 VCO feedback integer divider bit3 | R/W | | 0 | |
| Bit 2 | PLL3_N_DIV[2] | PLL3 VCO feedback integer divider bit2 | R/W | | 0 | |
| Bit 1 | PLL3_N_DIV[1] | PLL3 VCO feedback integer divider bit1 | R/W | | 0 | |
| Bit 0 | PLL3_N_DIV[0] | PLL3 VCO feedback integer divider bit0 | R/W | | 0 | |

Byte 5: PLL3 Loop Filter Setting and N Divider 10:8

| Byte 05h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|----------------|---|------|--|--------------------|-----|
| Bit 7 | PLL3_R100K | PLL3 Loop filter resister 100kohm | R/W | bypass | plus 100kohm | 0 |
| Bit 6 | PLL3_R50K | PLL3 Loop filter resister 50kohm | R/W | bypass | plus 50kohm | 0 |
| Bit 5 | PLL3_R25K | PLL3 Loop filter resister 25kohm | R/W | bypass | plus 25kohm | 0 |
| Bit 4 | PLL3_R12.5K | PLL3 Loop filter resister 12.5kohm | R/W | bypass | plus 12.5kohm | 1 |
| Bit 3 | PLL3_R6K | PLL3 Loop filter resister 6kohm | R/W | bypass | only 6kohm applied | 0 |
| Bit 2 | PLL3_N_DIV[10] | PLL3 VCO feedback integer divider bit10 | R/W | 12-2048, default VCO setting is 480MHz | 0 | |
| Bit 1 | PLL3_N_DIV[9] | PLL3 VCO feedback integer divider bit9 | R/W | | 0 | |
| Bit 0 | PLL3_N_DIV[8] | PLL3 VCO feedback integer divider bit8 | R/W | | 1 | |

Byte 6: PLL3 Charge Pump Control

| Byte 06h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|-----------------|---|------|------|------|-----|
| Bit 7 | OUTDIV 3 Source | Output divider 3 source clock selection | R/W | PLL2 | PLL3 | 0 |
| Bit 6 | PLL3_CP_8X | PLL3 charge pump control | R/W | — | x8 | 1 |
| Bit 5 | PLL3_CP_4X | PLL3 charge pump control | R/W | — | x4 | 1 |
| Bit 4 | PLL3_CP_2X | PLL3 charge pump control | R/W | — | x2 | 0 |
| Bit 3 | PLL3_CP_1X | PLL3 charge pump control | R/W | — | x1 | 1 |
| Bit 2 | PLL3_CP_24 | PLL3 charge pump control | R/W | — | /24 | 1 |
| Bit 1 | PLL3_CP_3 | PLL3 charge pump control | R/W | — | /3 | 0 |
| Bit 0 | PLL3_SIREF | PLL3 SiRef current selection | R/W | 10µA | 20µA | 0 |

Formula: $(i_{\text{Ref}} (10\mu\text{A}) \times (1 + \text{SIREF}) \times (1 \times 1X + 2 \times 2X + 4 \times 4X + 8 \times 8X + 16 \times 16X)) / ((24 \times /24) + (3 \times /3))$

Byte 7: PLL1 Control and OUTDIV5 Divider

| Byte 07h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|-------------------|-------------------------------|------|---------|--------|-----|
| Bit 7 | PLL1_MDIV_Doubler | PLL1 reference clock doubler | R/W | disable | enable | 0 |
| Bit 6 | PLL1_SIREF | PLL1 SiRef current selection | R/W | 10.8µA | 21.6µA | 0 |
| Bit 5 | PLL1_EN_CH2 | PLL1 output Channel 2 control | R/W | disable | enable | 1 |
| Bit 4 | PLL1_EN_3rdpole | PLL1 3rd Pole control | R/W | disable | enable | 0 |
| Bit 3 | OUTDIV5[3] | Output divider5 control bit 3 | R/W | — | — | 0 |
| Bit 2 | OUTDIV5[2] | Output divider5 control bit 2 | R/W | — | — | 0 |
| Bit 1 | OUTDIV5[1] | Output divider5 control bit 1 | R/W | — | — | 1 |
| Bit 0 | OUTDIV5[0] | Output divider5 control bit 0 | R/W | — | — | 1 |

Byte 8: PLL1 M Divider

| Byte 08h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|---------------|--|------|---------------------|---------------------|-----|
| Bit 7 | PLL1_MDIV1 | PLL3 VCO reference clock divider 1 | R/W | disable M DIV1 | bypass divider (/1) | 0 |
| Bit 6 | PLL1_MDIV2 | PLL3 VCO reference clock divider 2 | R/W | disable M DIV2 | bypass divider (/2) | 0 |
| Bit 5 | PLL1_M_DIV[5] | PLL1 reference clock divider control bit 5 | R/W | 3–64, default is 25 | | 0 |
| Bit 4 | PLL1_M_DIV[4] | PLL1 reference clock divider control bit 4 | R/W | | | 1 |
| Bit 3 | PLL1_M_DIV[3] | PLL1 reference clock divider control bit 3 | R/W | | | 1 |
| Bit 2 | PLL1_M_DIV[2] | PLL1 reference clock divider control bit 2 | R/W | | | 0 |
| Bit 1 | PLL1_M_DIV[1] | PLL1 reference clock divider control bit 1 | R/W | | | 0 |
| Bit 0 | PLL1_M_DIV[0] | PLL1 reference clock divider control bit 0 | R/W | | | 1 |

Byte 9: PLL1 VCO N Divider

| Byte 09h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|---------------|---|------|-------------------------|---|-----|
| Bit 7 | PLL1_N_DIV[7] | PLL1 VCO feedback divider control bit 7 | R/W | 12–2048, default is 600 | 0 | 0 |
| Bit 6 | PLL1_N_DIV[6] | PLL1 VCO feedback divider control bit 6 | R/W | | 1 | 1 |
| Bit 5 | PLL1_N_DIV[5] | PLL1 VCO feedback divider control bit 5 | R/W | | 0 | 0 |
| Bit 4 | PLL1_N_DIV[4] | PLL1 VCO feedback divider control bit 4 | R/W | | 1 | 1 |
| Bit 3 | PLL1_N_DIV[3] | PLL1 VCO feedback divider control bit 3 | R/W | | 1 | 1 |
| Bit 2 | PLL1_N_DIV[2] | PLL1 VCO feedback divider control bit 2 | R/W | | 0 | 0 |
| Bit 1 | PLL1_N_DIV[1] | PLL1 VCO feedback divider control bit 1 | R/W | | 0 | 0 |
| Bit 0 | PLL1_N_DIV[0] | PLL1 VCO feedback divider control bit 0 | R/W | | 0 | 0 |

Byte 10: PLL Loop Filter and N Divider

| Byte 0Ah | Name | Control Function | Type | 0 | 1 | PWD |
|----------|----------------|---|------|-------------------------|----------------------|-----|
| Bit 7 | PLL1_R100K | PLL1 Loop filter resister 100kohm | R/W | bypass | plus 100kohm | 1 |
| Bit 6 | PLL1_R50K | PLL1 Loop filter resister 50kohm | R/W | bypass | plus 50kohm | 0 |
| Bit 5 | PLL1_R25K | PLL1 Loop filter resister 25kohm | R/W | bypass | plus 25kohm | 1 |
| Bit 4 | PLL1_R12.5K | PLL1 Loop filter resister 12.5kohm | R/W | bypass | plus 12.5kohm | 1 |
| Bit 3 | PLL1_R1.0K | PLL1 Loop filter resister 1kohm | R/W | bypass | only 1.0kohm applied | 0 |
| Bit 2 | PLL1_N_DIV[10] | PLL1 VCO feedback integer divider bit10 | R/W | 12–2048, default is 600 | 0 | 0 |
| Bit 1 | PLL1_N_DIV[9] | PLL1 VCO feedback integer divider bit9 | R/W | | 1 | 1 |
| Bit 0 | PLL1_N_DIV[8] | PLL1 VCO feedback integer divider bit8 | R/W | | 0 | 0 |

Byte 11: PLL1 Charge Pump

| Byte 0Bh | Name | Control Function | Type | 0 | 1 | PWD |
|----------|-------------|--------------------------|------|---|-----|-----|
| Bit 7 | PLL1_CP_32X | PLL1 charge pump control | R/W | — | x32 | 0 |
| Bit 6 | PLL1_CP_16X | PLL1 charge pump control | R/W | — | x16 | 0 |
| Bit 5 | PLL1_CP_8X | PLL1 charge pump control | R/W | — | x8 | 0 |
| Bit 4 | PLL1_CP_4X | PLL1 charge pump control | R/W | — | x4 | 0 |
| Bit 3 | PLL1_CP_2X | PLL1 charge pump control | R/W | — | x2 | 0 |
| Bit 2 | PLL1_CP_1X | PLL1 charge pump control | R/W | — | x1 | 1 |
| Bit 1 | PLL1_CP_24 | PLL1 charge pump control | R/W | — | /24 | 1 |
| Bit 0 | PLL1_CP_3 | PLL1 charge pump control | R/W | — | /3 | 0 |

Byte 12: PLL1 Spread Spectrum Control

| Byte 0Ch | Name | Control Function | Type | 0 | 1 | PWD |
|----------|-------------------|---|------|---|---|-----|
| Bit 7 | PLL1_SS_REFDIV23 | PLL1 Spread Spectrum control - Ref divider 23 | R/W | — | — | 0 |
| Bit 6 | PLL1_SS_REFDIV[6] | PLL1 Spread Spectrum control - Ref divider 6 | R/W | — | — | 0 |
| Bit 5 | PLL1_SS_REFDIV[5] | PLL1 Spread Spectrum control - Ref divider 5 | R/W | — | — | 0 |
| Bit 4 | PLL1_SS_REFDIV[4] | PLL1 Spread Spectrum control - Ref divider 4 | R/W | — | — | 0 |
| Bit 3 | PLL1_SS_REFDIV[3] | PLL1 Spread Spectrum control - Ref divider 3 | R/W | — | — | 0 |
| Bit 2 | PLL1_SS_REFDIV[2] | PLL1 Spread Spectrum control - Ref divider 2 | R/W | — | — | 0 |
| Bit 1 | PLL1_SS_REFDIV[1] | PLL1 Spread Spectrum control - Ref divider 1 | R/W | — | — | 0 |
| Bit 0 | PLL1_SS_REFDIV[0] | PLL1 Spread Spectrum control - Ref divider 0 | R/W | — | — | 0 |

Byte 13: PLL1 Spread Spectrum Control

| Byte 0Dh | Name | Control Function | Type | 0 | 1 | PWD |
|----------|-------------------|--|------|---|---|-----|
| Bit 7 | PLL1_SS_FBDIV[15] | PLL1 Spread Spectrum - feedback divider 15 | R/W | — | — | 0 |
| Bit 6 | PLL1_SS_FBDIV[14] | PLL1 Spread Spectrum - feedback divider 14 | R/W | — | — | 0 |
| Bit 5 | PLL1_SS_FBDIV[13] | PLL1 Spread Spectrum - feedback divider 13 | R/W | — | — | 0 |
| Bit 4 | PLL1_SS_FBDIV[12] | PLL1 Spread Spectrum - feedback divider 12 | R/W | — | — | 0 |
| Bit 3 | PLL1_SS_FBDIV[11] | PLL1 Spread Spectrum - feedback divider 11 | R/W | — | — | 0 |
| Bit 2 | PLL1_SS_FBDIV[10] | PLL1 Spread Spectrum - feedback divider 10 | R/W | — | — | 0 |
| Bit 1 | PLL1_SS_FBDIV[9] | PLL1 Spread Spectrum - feedback divider 9 | R/W | — | — | 0 |
| Bit 0 | PLL1_SS_FBDIV[8] | PLL1 Spread Spectrum - feedback divider 8 | R/W | — | — | 0 |

Byte 14: PLL1 Spread Spectrum Control

| Byte 0Eh | Name | Control Function | Type | 0 | 1 | PWD |
|----------|------------------|---|------|---|---|-----|
| Bit 7 | PLL1_SS_FBDIV[7] | PLL1 Spread Spectrum - feedback divider 7 | R/W | — | — | 0 |
| Bit 6 | PLL1_SS_FBDIV[6] | PLL1 Spread Spectrum - feedback divider 6 | R/W | — | — | 0 |
| Bit 5 | PLL1_SS_FBDIV[5] | PLL1 Spread Spectrum - feedback divider 5 | R/W | — | — | 0 |
| Bit 4 | PLL1_SS_FBDIV[4] | PLL1 Spread Spectrum - feedback divider 4 | R/W | — | — | 0 |
| Bit 3 | PLL1_SS_FBDIV[3] | PLL1 Spread Spectrum - feedback divider 3 | R/W | — | — | 0 |
| Bit 2 | PLL1_SS_FBDIV[2] | PLL1 Spread Spectrum - feedback divider 2 | R/W | — | — | 0 |
| Bit 1 | PLL1_SS_FBDIV[1] | PLL1 Spread Spectrum - feedback divider 1 | R/W | — | — | 0 |
| Bit 0 | PLL1_SS_FBDIV[0] | PLL1 Spread Spectrum - feedback divider 0 | R/W | — | — | 0 |

Byte 15: Output Divider1 Control

| Byte 0Fh | Name | Control Function | Type | 0 | 1 | PWD |
|----------|------------|-------------------------------|------|---|---|-----|
| Bit 7 | OUTDIV1[3] | Output divider1 control bit 3 | R/W | — | — | 0 |
| Bit 6 | OUTDIV1[2] | Output divider1 control bit 2 | R/W | — | — | 0 |
| Bit 5 | OUTDIV1[1] | Output divider1 control bit 1 | R/W | — | — | 1 |
| Bit 4 | OUTDIV1[0] | Output divider1 control bit 0 | R/W | — | — | 1 |
| Bit 3 | OUTDIV2[3] | Output divider2 control bit 3 | R/W | — | — | 0 |
| Bit 2 | OUTDIV2[2] | Output divider2 control bit 2 | R/W | — | — | 0 |
| Bit 1 | OUTDIV2[1] | Output divider2 control bit 1 | R/W | — | — | 1 |
| Bit 0 | OUTDIV2[0] | Output divider2 control bit 0 | R/W | — | — | 1 |

Byte 16: PLL2 Integer Feedback Divide

| Byte 10h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|-----------------|----------------------------------|------|---|---|-----|
| Bit 7 | | Reserved | | — | — | 0 |
| Bit 6 | | Reserved | | — | — | 0 |
| Bit 5 | | Reserved | | — | — | 0 |
| Bit 4 | | Reserved | | — | — | 0 |
| Bit 3 | | Reserved | | — | — | 0 |
| Bit 2 | PLL2_FB_INT[10] | PLL2 feedback integer divider 10 | R/W | — | — | 0 |
| Bit 1 | PLL2_FB_INT[9] | PLL2 feedback integer divider 9 | R/W | — | — | 0 |
| Bit 0 | PLL2_FB_INT[8] | PLL2 feedback integer divider 8 | R/W | — | — | 0 |

Byte 17: PLL2 Integer Feedback Divider

| Byte 11h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|--------------------|---------------------------------|------|---|---|-----|
| Bit 7 | PLL2_FB_INT_DIV[7] | PLL2 feedback integer divider 7 | R/W | — | — | 0 |
| Bit 6 | PLL2_FB_INT_DIV[6] | PLL2 feedback integer divider 6 | R/W | — | — | 0 |
| Bit 5 | PLL2_FB_INT_DIV[5] | PLL2 feedback integer divider 5 | R/W | — | — | 1 |
| Bit 4 | PLL2_FB_INT_DIV[4] | PLL2 feedback integer divider 4 | R/W | — | — | 1 |
| Bit 3 | PLL2_FB_INT_DIV[3] | PLL2 feedback integer divider 3 | R/W | — | — | 1 |
| Bit 2 | PLL2_FB_INT_DIV[2] | PLL2 feedback integer divider 2 | R/W | — | — | 1 |
| Bit 1 | PLL2_FB_INT_DIV[1] | PLL2 feedback integer divider 1 | R/W | — | — | 0 |
| Bit 0 | PLL2_FB_INT_DIV[0] | PLL2 feedback integer divider 0 | R/W | — | — | 0 |

Byte 18: PLL2 Fractional Feedback Divider

| Byte 12h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|---------------------|-------------------------------------|------|---|---|-----|
| Bit 7 | PLL2_FB_FRC_DIV[15] | PLL2 feedback fractional divider 15 | R/W | — | — | 0 |
| Bit 6 | PLL2_FB_FRC_DIV[14] | PLL2 feedback fractional divider 14 | R/W | — | — | 0 |
| Bit 5 | PLL2_FB_FRC_DIV[13] | PLL2 feedback fractional divider 13 | R/W | — | — | 0 |
| Bit 4 | PLL2_FB_FRC_DIV[12] | PLL2 feedback fractional divider 12 | R/W | — | — | 0 |
| Bit 3 | PLL2_FB_FRC_DIV[11] | PLL2 feedback fractional divider 11 | R/W | — | — | 0 |
| Bit 2 | PLL2_FB_FRC_DIV[10] | PLL2 feedback fractional divider 10 | R/W | — | — | 0 |
| Bit 1 | PLL2_FB_FRC_DIV[9] | PLL2 feedback fractional divider 9 | R/W | — | — | 0 |
| Bit 0 | PLL2_FB_FRC_DIV[8] | PLL2 feedback fractional divider 8 | R/W | — | — | 0 |

Byte 19: PLL2 Fractional Feedback Divider

| Byte 13h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|--------------------|------------------------------------|------|---|---|-----|
| Bit 7 | PLL2_FB_FRC_DIV[7] | PLL2 feedback fractional divider 7 | R/W | — | — | 0 |
| Bit 6 | PLL2_FB_FRC_DIV[6] | PLL2 feedback fractional divider 6 | R/W | — | — | 0 |
| Bit 5 | PLL2_FB_FRC_DIV[5] | PLL2 feedback fractional divider 5 | R/W | — | — | 0 |
| Bit 4 | PLL2_FB_FRC_DIV[4] | PLL2 feedback fractional divider 4 | R/W | — | — | 0 |
| Bit 3 | PLL2_FB_FRC_DIV[3] | PLL2 feedback fractional divider 3 | R/W | — | — | 0 |
| Bit 2 | PLL2_FB_FRC_DIV[2] | PLL2 feedback fractional divider 2 | R/W | — | — | 0 |
| Bit 1 | PLL2_FB_FRC_DIV[1] | PLL2 feedback fractional divider 1 | R/W | — | — | 0 |
| Bit 0 | PLL2_FB_FRC_DIV[0] | PLL2 feedback fractional divider 0 | R/W | — | — | 0 |

Byte 20: PLL2 Spread Spectrum Control

| Byte 14h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|--------------|-------------------------------------|------|---|---|-----|
| Bit 7 | PLL2_STEP[7] | PLL2 spread step size control bit 7 | R/W | — | — | 0 |
| Bit 6 | PLL2_STEP[6] | PLL2 spread step size control bit 6 | R/W | — | — | 0 |
| Bit 5 | PLL2_STEP[5] | PLL2 spread step size control bit 5 | R/W | — | — | 0 |
| Bit 4 | PLL2_STEP[4] | PLL2 spread step size control bit 4 | R/W | — | — | 0 |
| Bit 3 | PLL2_STEP[3] | PLL2 spread step size control bit 3 | R/W | — | — | 0 |
| Bit 2 | PLL2_STEP[2] | PLL2 spread step size control bit 2 | R/W | — | — | 0 |
| Bit 1 | PLL2_STEP[1] | PLL2 spread step size control bit 1 | R/W | — | — | 0 |
| Bit 0 | PLL2_STEP[0] | PLL2 spread step size control bit 0 | R/W | — | — | 0 |

Byte 21: PLL2 Spread Spectrum Control

| Byte 15h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|--------------------|---|------|---|---|-----|
| Bit 7 | PLL2_STEP_DELTA[7] | PLL2 spread step size control delta bit 7 | R/W | — | — | 0 |
| Bit 6 | PLL2_STEP_DELTA[6] | PLL2 spread step size control delta bit 6 | R/W | — | — | 0 |
| Bit 5 | PLL2_STEP_DELTA[5] | PLL2 spread step size control delta bit 5 | R/W | — | — | 0 |
| Bit 4 | PLL2_STEP_DELTA[4] | PLL2 spread step size control delta bit 4 | R/W | — | — | 0 |
| Bit 3 | PLL2_STEP_DELTA[3] | PLL2 spread step size control delta bit 3 | R/W | — | — | 0 |
| Bit 2 | PLL2_STEP_DELTA[2] | PLL2 spread step size control delta bit 2 | R/W | — | — | 0 |
| Bit 1 | PLL2_STEP_DELTA[1] | PLL2 spread step size control delta bit 1 | R/W | — | — | 0 |
| Bit 0 | PLL2_STEP_DELTA[0] | PLL2 spread step size control delta bit 0 | R/W | — | — | 0 |

Byte 22: PLL2 Spread Spectrum Control

| Byte 16h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|---------------|--------------------------------------|------|---|---|-----|
| Bit 7 | PLL2_STEP[15] | PLL2 spread step size control bit 15 | R/W | — | — | 0 |
| Bit 6 | PLL2_STEP[14] | PLL2 spread step size control bit 14 | R/W | — | — | 0 |
| Bit 5 | PLL2_STEP[13] | PLL2 spread step size control bit 13 | R/W | — | — | 0 |
| Bit 4 | PLL2_STEP[12] | PLL2 spread step size control bit 12 | R/W | — | — | 0 |
| Bit 3 | PLL2_STEP[11] | PLL2 spread step size control bit 11 | R/W | — | — | 0 |
| Bit 2 | PLL2_STEP[10] | PLL2 spread step size control bit 10 | R/W | — | — | 0 |
| Bit 1 | PLL2_STEP[9] | PLL2 spread step size control bit 9 | R/W | — | — | 0 |
| Bit 0 | PLL2_STEP[8] | PLL2 spread step size control bit 8 | R/W | — | — | 0 |

Byte 23: PLL2 Period Control

| Byte 17h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|----------------|---------------------------|------|---|---|-----|
| Bit 7 | PLL2_PERIOD[7] | PLL2 period control bit 7 | R/W | — | — | 0 |
| Bit 6 | PLL2_PERIOD[6] | PLL2 period control bit 6 | R/W | — | — | 0 |
| Bit 5 | PLL2_PERIOD[5] | PLL2 period control bit 5 | R/W | — | — | 0 |
| Bit 4 | PLL2_PERIOD[4] | PLL2 period control bit 4 | R/W | — | — | 0 |
| Bit 3 | PLL2_PERIOD[3] | PLL2 period control bit 3 | R/W | — | — | 0 |
| Bit 2 | PLL2_PERIOD[2] | PLL2 period control bit 2 | R/W | — | — | 0 |
| Bit 1 | PLL2_PERIOD[1] | PLL2 period control bit 1 | R/W | — | — | 0 |
| Bit 0 | PLL2_PERIOD[0] | PLL2 period control bit 0 | R/W | — | — | 0 |

Byte 24: PLL2 Control Register

| Byte 18h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|----------------|------------------------------------|------|---------|--------------------|-----|
| Bit 7 | PLL2_PERIOD[9] | PLL2 period control bit 9 | R/W | — | — | 0 |
| Bit 6 | PLL2_PERIOD[8] | PLL2 period control bit 8 | R/W | — | — | 0 |
| Bit 5 | PLL2_SSEN | PLL2 spread spectrum enable | R/W | disable | enable | 0 |
| Bit 4 | PLL2_R100K | PLL2 Loop filter resister 100kohm | — | bypass | plus 100kohm | 0 |
| Bit 3 | PLL2_R50K | PLL2 Loop filter resister 50kohm | — | bypass | plus 50kohm | 1 |
| Bit 2 | PLL2_R25K | PLL2 Loop filter resister 25kohm | — | bypass | plus 25kohm | 1 |
| Bit 1 | PLL2_R12.5K | PLL2 Loop filter resister 12.5kohm | — | bypass | plus 12.5kohm | 1 |
| Bit 0 | PLL2_R6K | PLL2 Loop filter resister 6kohm | — | bypass | only 6kohm applied | 0 |

Byte 25: PLL2 Charge Pump Control

| Byte 19h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|-------------|------------------------------|------|------|------|-----|
| Bit 7 | PLL2_CP_16X | PLL2 charge pump control | R/W | — | x16 | 0 |
| Bit 6 | PLL2_CP_8X | PLL2 charge pump control | R/W | — | x8 | 0 |
| Bit 5 | PLL2_CP_4X | PLL2 charge pump control | R/W | — | x4 | 0 |
| Bit 4 | PLL2_CP_2X | PLL2 charge pump control | R/W | — | x2 | 1 |
| Bit 3 | PLL2_CP_1X | PLL2 charge pump control | R/W | — | x1 | 0 |
| Bit 2 | PLL2_CP_24 | PLL2 charge pump control | R/W | — | /24 | 1 |
| Bit 1 | PLL2_CP_3 | PLL2 charge pump control | R/W | — | /3 | 0 |
| Bit 0 | PLL2_SIREF | PLL2 SiRef current selection | R/W | 10µA | 20µA | 0 |

Byte 26: PLL2 M Divider Setting

| Byte 1Ah | Name | Control Function | Type | 0 | 1 | PWD |
|----------|-------------------|--------------------------------------|------|---------------------|---------------------|-----|
| Bit 7 | PLL2_MDIV_Doubler | PLL2 reference divider - doubler | R/W | disable | enable | 0 |
| Bit 6 | PLL2_MDIV1 | PLL2 reference divider 1 | R/W | disable M DIV1 | bypadd divider (/1) | 0 |
| Bit 5 | PLL2_MDIV2 | PLL2 reference divider 2 | R/W | disable M DIV2 | bypadd divider (/2) | 0 |
| Bit 4 | PLL2_MDIV[4] | PLL2 reference divider control bit 4 | R/W | 3–64, default is 25 | 3–64, default is 25 | 1 |
| Bit 3 | PLL2_MDIV[3] | PLL2 reference divider control bit 3 | R/W | | | 1 |
| Bit 2 | PLL2_MDIV[2] | PLL2 reference divider control bit 2 | R/W | | | 0 |
| Bit 1 | PLL2_MDIV[1] | PLL2 reference divider control bit 1 | R/W | | | 0 |
| Bit 0 | PLL2_MDIV[0] | PLL2 reference divider control bit 0 | R/W | | | 1 |

Byte 27: Output Divider 4

| Byte 1Bh | Name | Control Function | Type | 0 | 1 | PWD |
|----------|------------|-----------------------------|------|---|---|-----|
| Bit 7 | OUTDIV3[3] | Out divider 3 control bit 3 | R/W | — | — | 0 |
| Bit 6 | OUTDIV3[2] | Out divider 3 control bit 2 | R/W | — | — | 1 |
| Bit 5 | OUTDIV3[1] | Out divider 3 control bit 1 | R/W | — | — | 0 |
| Bit 4 | OUTDIV3[0] | Out divider 3 control bit 0 | R/W | — | — | 0 |
| Bit 3 | OUTDIV4[3] | Out divider 4 control bit 3 | R/W | — | — | 0 |
| Bit 2 | OUTDIV4[2] | Out divider 4 control bit 2 | R/W | — | — | 0 |
| Bit 1 | OUTDIV4[1] | Out divider 4 control bit 1 | R/W | — | — | 1 |
| Bit 0 | OUTDIV4[0] | Out divider 4 control bit 0 | R/W | — | — | 1 |

Byte 28: PLL Operation Control Register

| Byte 1Ch | Name | Control Function | Type | 0 | 1 | PWD |
|----------|----------------|--|------|-------------|-----------------------|-----|
| Bit 7 | PLL2_HRS_EN | PLL2 spread high resolution selection enable | R/W | normal | enable (shift 4 bits) | 0 |
| Bit 6 | PLL2_refin_sel | PLL2 reference clock source select | R/W | Xtal | DIV2 | 0 |
| Bit 5 | PLL3_PDB | PLL3 Power Down | R/W | Power Down | running | 1 |
| Bit 4 | PLL3_LCKBYPSSB | PLL3 lock bypass | R/W | bypass lock | lock | 1 |
| Bit 3 | PLL2_PDB | PLL2 Power Down | R/W | Power Down | running | 1 |
| Bit 2 | PLL2_LCKBYPSSB | PLL2 lock bypass | R/W | bypass lock | lock | 1 |
| Bit 1 | PLL1_PDB | PLL1 Power Down | R/W | Power Down | running | 1 |
| Bit 0 | PLL1_LCKBYPSSB | PLL1 lock bypass | R/W | bypass lock | lock | 1 |

Byte 29: Output Control

| Byte 1Dh | Name | Control Function | Type | 0 | 1 | PWD |
|----------|----------------|---|------|----------------|------------|-----|
| Bit 7 | DIFF1_SEL | Differential clock 1 output OE2 control | | not controlled | controlled | 0 |
| Bit 6 | DIFF2_SEL | Differential clock 2 output OE2 control | | not controlled | controlled | 0 |
| Bit 5 | DIFF1_EN | Differential clock 1 output enable | R/W | disable | enable | 1 |
| Bit 4 | DIFF2_EN | Differential clock 2 output enable | R/W | disable | enable | 1 |
| Bit 3 | OUTDIV4_Source | Output divider 4 source clock selection | R/W | PLL2 | Xtal | 0 |
| Bit 2 | SE1_SLEW | SE 1 slew rate control | R/W | normal | strong | 0 |
| Bit 1 | VDD1_SEL[1] | VDD1 level control bit 1 | R/W | 11: 1.8V | | 0 |
| Bit 0 | VDD1_SEL[0] | VDD1 level control bit 0 | R/W | | | 0 |

Byte 30: OE and DFC Control

| Byte 1Eh | Name | Control Function | Type | 0 | 1 | PWD |
|----------|----------------|----------------------------------|------|--------------------|-------------|-----|
| Bit 7 | SE1_EN | SE1 output enable control | R/W | disable | enable | 1 |
| Bit 6 | OE1_fun_sel[1] | OE1 pin function selection bit 1 | R/W | 11:DFC0 01: PD# | 10: SE1_PPS | 0 |
| Bit 5 | OE1_fun_sel[0] | OE1 pin function selection bit 0 | R/W | | 00: SE1_OE | 0 |
| Bit 4 | SE3_EN | SE3 output enable | R/W | disable | enable | 1 |
| Bit 3 | OE3_fun_sel[1] | OE3 pin function selection bit 1 | R/W | 11: DFC1 01:xx | 10: SE3_PPS | 0 |
| Bit 2 | OE3_fun_sel[0] | OE3 pin function selection bit 0 | R/W | | 00: SE3_OE | 0 |
| Bit 1 | DFC_SW_Sel[1] | DFC frequency select bit 1 | R/W | 00: N0 01: N1 | 10: N2 | 0 |
| Bit 0 | DFC_SW_Sel[0] | DFC frequency select bit 0 | R/W | | 11: N3 | 0 |

Byte 31: Control Register

| Byte 1Fh | Name | Control Function | Type | 0 | 1 | PWD |
|----------|-----------------|-------------------------------|------|-------------|--------------------------|-----|
| Bit 7 | SE2_Freerun_32K | SE2 32K Freerun | - | freerun 32K | B31 bit 0 control source | 1 |
| Bit 6 | VDD2_SEL[1] | VDD2 level control bit 1 | R/W | 11: 1.8V | | 0 |
| Bit 5 | VDD2_SEL[0] | VDD2 level control bit 0 | R/W | | | 0 |
| Bit 4 | SE2_SLEW | SE 2 slew rate control | R/W | normal | strong | 0 |
| Bit 3 | PLL2_3rd_EN_CFG | PLL2 3rd order control | - | 1st order | 3rd order | 0 |
| Bit 2 | PLL2_EN_CH2 | PLL2 channel 2 enable control | R/W | disable | enable | 1 |
| Bit 1 | PLL2_EN_3rdpole | PLL2 3rd Pole control | R/W | disable | enable | 0 |
| Bit 0 | SE2_CLKSEL1 | SE2 source clock selection | - | DIV5 | DIV4 | 0 |

Byte 32: Control Register

| Byte 20h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|----------------|----------------------------------|------|-----------------------------|-------------|-----|
| Bit 7 | SE2_EN | SE2 output enable | R/W | disable | enable | 1 |
| Bit 6 | OE2_fun_sel[1] | OE2 pin function selection bit 1 | R/W | 11: RESET 01: DIFF1/2 OE | 10: SE2_PPS | 0 |
| Bit 5 | OE2_fun_sel[0] | OE2 pin function selection bit 0 | R/W | | 00: SE2_OE | 0 |
| Bit 4 | DFC_EN | DFC function control | R/W | disable | enable | 0 |
| Bit 3 | WD_EN | WatchDog timer control | R/W | disable | enable | 0 |
| Bit 2 | Timer_sel<1> | Watchdog timer select bit 1 | R/W | 00: 250ms 10: 2s | 01: 500ms | 0 |
| Bit 1 | Timer_sel<0> | Watchdog timer select bit 0 | R/W | | 11: 4s | 0 |
| Bit 0 | Alarm_Flag | Alarm Status (Read Only) | R | No alarm | Alarmed | 0 |

Byte 33: SE3 and DIFF1 Control Register

| Byte 21h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|------------------|--|------|------------------|----------------------------------|-----|
| Bit 7 | SE3_Freerun_32K | SE3 32K free run | R/W | freerun 32K | DIV2 or DIV4 selected by B33bit6 | 1 |
| Bit 6 | SE3_CLKSEL1 | SE3 source clock selection | R/W | DIV2 | DIV4 | 0 |
| Bit 5 | VDD3_SEL[1] | VDD3 level control bit 1 | R/W | 11: 1.8V | | 0 |
| Bit 4 | VDD3_SEL[0] | VDD3 level control bit 0 | R/W | | | 0 |
| Bit 3 | SE3_SLEW | SE 3 slew rate control | R/W | normal | strong | 0 |
| Bit 2 | DIFF_PDBHiZEN | Differential output high-Z at power down | R/W | TBD | output tri-state, bias off | 0 |
| Bit 1 | DIFF1_CMOS2_FLIP | Differential 1/2 LVCMOS output control | R/W | DIFF1_B inverted | DIFF1_B non-inverted | 0 |
| Bit 0 | DIFF2_CMOS2_FLIP | Differential 1/2 LVCMOS output control | R/W | DIFF2_B inverted | DIFF2_B non-inverted | 0 |

Byte 34: DIFF1 Control Register

| Byte 22h | Name | Control Function | Type | 0 | 1 | PWD | | |
|----------|----------------------|---|------|---|--------|-----|--|--|
| Bit 7 | DIFF1_CLK_SEL | Differential clock 1 source selection | R/W | DIV1 | DIV3 | 1 | | |
| Bit 6 | Reserved | | | | | 1 | | |
| Bit 5 | DIFF1_OUTPUT_TYPE[1] | Differential clock 1 type select bit 1 | R/W | 00: LVMOS 01: Reserved 10: Reserved 11: LPHCSL | | 1 | | |
| Bit 4 | DIFF1_OUTPUT_TYPE[0] | Differential clock 1 type select bit 0 | R/W | | | 1 | | |
| Bit 3 | Reserved | | | | | 0 | | |
| Bit 2 | Reserved | | | | | 1 | | |
| Bit 1 | DIFF1_CMOS_SLEW | Differential clock 1 LVCMOS slew rate control | R/W | normal | strong | 0 | | |
| Bit 0 | D1FF1_CMOS2_EN | Differential clock 1 LVCMOS output_B control | R/W | disable | enable | 0 | | |

Byte 35: DIFF2 Control Register

| Byte 23h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|----------------------|---|------|--------------|--------------|-----|
| Bit 7 | DIFF2_CLK_SEL | Differential clock 2 source selection | R/W | DIV1 | DIV3 | 0 |
| Bit 6 | | Reserved | | | | 1 |
| Bit 5 | DIFF2_OUTPUT_TYPE[1] | Differential clock 2 type select bit 1 | R/W | 00: LVMOS | 01: Reserved | 1 |
| Bit 4 | DIFF2_OUTPUT_TYPE[0] | Differential clock 2 type select bit 0 | | 10: Reserved | 11: LPHCSL | 1 |
| Bit 3 | | Reserved | | | | 0 |
| Bit 2 | | Reserved | | | | 0 |
| Bit 1 | DIFF2_CMOS_SLEW | Differential clock 2 LVCMOS slew rate control | R/W | normal | strong | 0 |
| Bit 0 | DIFF2_CMOS2_EN | Differential clock 2 LVCMOS output_B control | R/W | disable | enable | 0 |

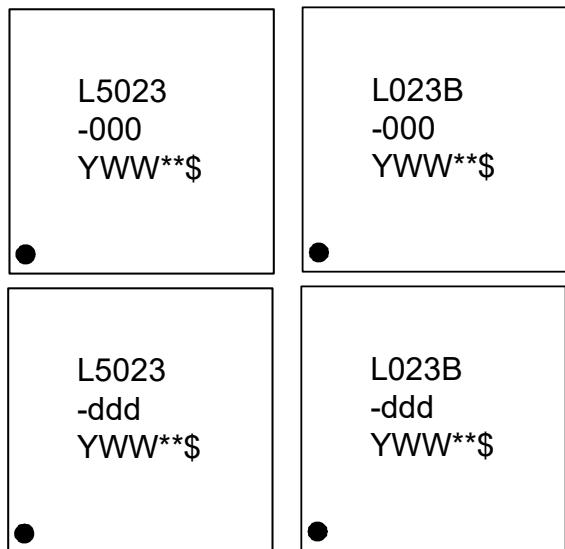
Byte 36: SE1 and DIV4 control

| Byte 24h | Name | Control Function | Type | 0 | 1 | PWD |
|----------|------------------------|----------------------------------|------|--------------|-----------------|-----|
| Bit 7 | I2C_PDB | chip power down control bit | R/W | power down | normal | 1 |
| Bit 6 | Ref_free_run | Reference clock output (SE2/SE3) | R/W | stop | freerun | 0 |
| Bit 5 | free_run_output_config | SE clocks free run control | R/W | SE2 free run | SE2/3 free run | 0 |
| Bit 4 | SE1_Freerun_32K | SE1 clock output default | R/W | 32k freerun | B36bit3 control | 0 |
| Bit 3 | SE1_CLKSEL1 | SEL1 output select | R/W | DIV5 | DIV4 | 1 |
| Bit 2 | REF_EN | REF output enable | R/W | disable | enable | 1 |
| Bit 1 | DIV4_CH3_EN | DIV4 channel 3 output control | R/W | disable | enable | 0 |
| Bit 0 | DIV4_CH2_EN | DIV4 channel 2 output control | R/W | disable | enable | 0 |

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

Marking Diagrams



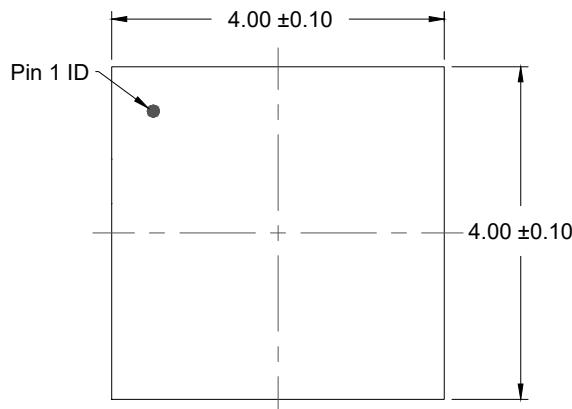
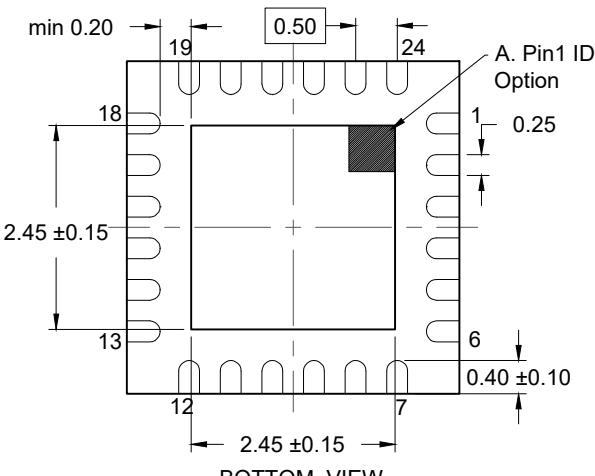
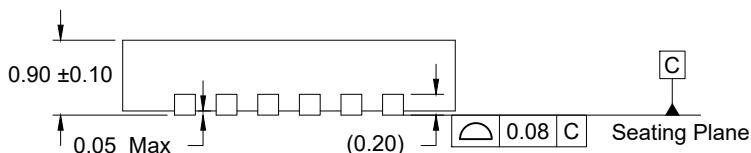
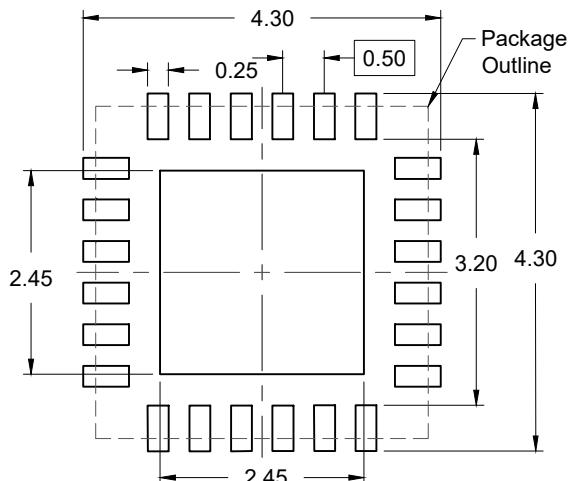
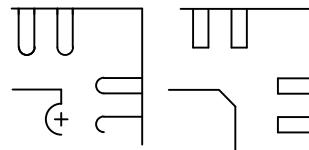
- Line 1 is the truncated part number.
- "-000" denotes un-programmed part. Configuration left blank for user customization.
- "-ddd" denotes the dash code.
- "YWW" is the last digit of the year and week that the part was assembled.
- "**" denotes sequential lot number.
- "\$" denotes mark code.

Ordering Information

| Orderable Part Number | Package | Carrier Type | Temperature Range |
|-----------------------|---------------------------------|---------------|-------------------|
| 5L35023-000NLGI | 4 x 4 mm, 0.5mm pitch 24-VFQFPN | Trays | -40° to +85°C |
| 5L35023-000NLGI8 | 4 x 4 mm, 0.5mm pitch 24-VFQFPN | Tape and Reel | -40° to +85°C |
| 5L35023-dddNLGI | 4 x 4 mm, 0.5mm pitch 24-VFQFPN | Trays | -40° to +85°C |
| 5L35023-dddNLGI8 | 4 x 4 mm, 0.5mm pitch 24-VFQFPN | Tape and Reel | -40° to +85°C |
| 5L35023B-000NLGI | 4 x 4 mm, 0.5mm pitch 24-VFQFPN | Trays | -40° to +85°C |
| 5L35023B-000NLGI8 | 4 x 4 mm, 0.5mm pitch 24-VFQFPN | Tape and Reel | -40° to +85°C |
| 5L35023B-dddNLGI | 4 x 4 mm, 0.5mm pitch 24-VFQFPN | Trays | -40° to +85°C |
| 5L35023B-dddNLGI8 | 4 x 4 mm, 0.5mm pitch 24-VFQFPN | Tape and Reel | -40° to +85°C |

Revision History

| Revision Date | Description of Change |
|--------------------|--|
| December 15, 2025 | Added Applications section. |
| November 20, 2025 | Updated description for pin 6 in Pin Descriptions . |
| October 23, 2025 | <ul style="list-style-type: none">▪ Updated register tables; Byte 27, Byte 31, Byte 36.▪ Changed f_{VCO1} VCO Frequency Range of PLL1 maximum to 700MHz from 600MHz in Table 10. |
| July 16, 2025 | Updated capacitor values and equation in section Crystal Input (X1/X2) . |
| September 25, 2024 | Updated Byte 1Fh Bit 7 Name and Control Function to SE2_Freerun_32K in the Byte 31: Control Register table. Also updated columns 0 and 1 for Bit 7. |
| November 30, 2022 | Updated POD links in Ordering Information . |
| October 4, 2019 | Removed comment "VBAT power ramp-up should be same or earlier time than other VDD power rail." from Power Group table. |
| September 26, 2019 | <ul style="list-style-type: none">▪ Updated Supply Voltage values in Absolute Maximum Ratings table.▪ Added F_{IN} parameter/values to Recommended Operating Conditions table.▪ Updated f_{VCO3} VCO Frequency Range of PLL3 in AC Timing Electrical Characteristics table.▪ Updated VMAX values in Electrical Characteristics - LPHCSL Differential Outputs table.▪ Updated PPS Assertion/Deassertion Timing diagram.▪ Added "B" revision orderable part numbers and marking diagrams. |
| November 29, 2017 | Updated I ² C section. |
| July 13, 2017 | Corrected typo in block diagram. |
| June 29, 2017 | Initial release. |


TOP VIEW

BOTTOM VIEW

SIDE VIEW

RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)


A. PIN1 ID OPTION DETAILS

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ± 0.05 mm for the non-toleranced dimensions.
4. Numbers in () are for references only.
5. Pin#1 ID is identified by either chamfer or notch.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.