

Description

The 5P49V6967 is a programmable clock generator intended for high-performance consumer, networking, industrial, computing, and data-communications applications. This is Renesas' sixth generation of programmable clock technology (VersaClock 6E).

The frequencies are generated from a single reference clock. The reference clock can originate from one of the two redundant clock inputs. A glitchless manual switchover function allows one of the redundant clocks to be selected during normal operation.

Two select pins allow up to four different configurations to be programmed and may be used for different operating modes.

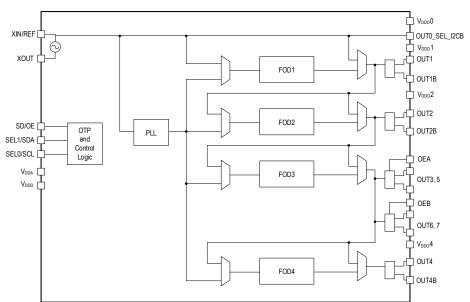
Typical Applications

- Ethernet switch/router
- PCI Express 1.0/2.0/3.0/4.0 spread spectrum on
- PCI Express 1.0/2.0/3.0/4.0/5.0 spread spectrum off
- Broadcast video/audio timing
- Multi-function printer
- Processor and FPGA clocking
- Any-frequency clock conversion
- MSAN/DSLAM/PON
- Fiber Channel, SAN
- Telecom line cards
- Datacenter

Features

- Flexible 1.8V, 2.5V, 3.3V power rails
- High-performance, low phase noise PLL, < 0.5ps RMS typical phase jitter on outputs
- Four banks of internal OTP memory
 - In-system or factory programmable
- I²C serial programming interface
 - 0xD0 or 0xD4 I²C address options allow multiple devices configured in the same system.
- Reference LVCMOS output clock
- Three Universal configurable outputs (OUT1, 2, 4):
 - Differential (LVPECL, LVDS, or HCSL) 1kHz to 350MHz
 - Two single-ended (in-phase or 180 degrees out of phase)
 1kHz to 200MHz
 - I/O VDDs can be mixed and matched, supporting 1.8V (LVDS and LVCMOS), 2.5V, or 3.3V
 - Independent spread spectrum on each output pair
- Four additional LPHCSL outputs (OUT 3, 5, 6, 7)
 - 1.8V low power supply
 - 1kHz to 200MHz
- Programmable output enable or power-down mode
- Available in 5 × 5 mm 40-VFQFPN package
- -40° to +85°C industrial temperature operation

Block Diagram





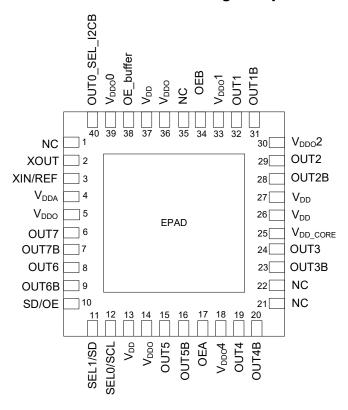
Contents

Absol Therr Reco Electr	Descriptions olute Maximum Ratings rmal Characteristics ommended Operating Conditions	6
Therr Reco Electr	rmal Characteristics	6
Reco Electi		
Electi	ommended Operating Conditions	^
Toot	trical Characteristics	7
resti	t Loads	14
	r Performance Characteristics	
PCI E	Express Jitter Performance and Specification	16
Featu	tures and Functional Blocks	18
10.1	Clock Inputs	18
10.2	Pevice Startup and Power-on-Reset	18
10.3	Internal Crystal Oscillator (XIN/REF)	19
	10.3.1 Choosing Crystals	19
	10.3.2 Tuning the Crystal Load Capacitor	19
10.4	Programmable Loop Filter	21
10.5	Fractional Output Dividers (FOD)	21
	10.5.1 Individual Spread Spectrum Modulation	21
	10.5.2 Bypass Mode	21
	10.5.3 Cascaded Mode	21
	10.5.4 Dividers Alignment	21
	10.5.5 Programmable Skew	22
10.6	Output Drivers	22
10.7	SD/OE Pin Function	22
10.8	I ² C Operation	23
Typic	cal Application Circuit	24
11.1	Recommendations for Unused Input and Output Pins	24
	11.1.1 XIN/REF and XOUT	24
	11.1.2 LVCMOS Outputs	24
	11.1.3 Differential Outputs	24
11.2	! Input – Driving the XIN/REF	24
	11.2.1 Driving XIN/REF with a CMOS Driver	24
	11.2.2 Driving XIN with a LVPECL Driver	25
11.3	Output – Single-ended or Differential Clock Terminations	26
	11.3.1 LVDS Termination	26
	11.3.2 LVPECL Termination	27
	11.3.3 HCSL Termination	28
	11.3.4 LVCMOS Termination	28
Pack	kage Outline Drawings	29
Marki	king Diagram	29
Orde	eringInformation	29

	10.7 10.8 Typi 11.1 11.2 11.3	10.6 Output Drivers

1. Pin Assignments

Figure 1. Pin Assignments for 5×5 mm 40-VFQFPN Package – Top View



40-pin VFQFPN

2. Pin Descriptions

Table 1. Pin Descriptions

Number	Na	ame	Туре	Description	
1	NC	Input	-	Do not connect	
2	XOUT	Input	-	Crystal Oscillator interface output.	
3	XIN/REF	Input	-	Crystal Oscillator interface input, or single-ended LVCMOS clock input. Input voltage needs to be below 1.2V. Refer to the <i>Output Drivers</i> section for more details.	
4	VDDA	Power	-	Analog functions power supply pin. Connect to 1.8V.	
5	VDDO	Power	-	Connect to 1.8V. Power pin for outputs 3, 5–7.	
6	OUT7	Output	-	Output clock 7. Low-Power HCSL (LP-HCSL) output.	
7	OUT7B	Output	-	Complementary output clock 7. Low-power HCSL (LP-HCSL) output.	
8	OUT6	Output	-	Output clock 6. Low-power HCSL (LP-HCSL) output.	
9	OUT6B	Output	-	Complementary output clock 6. Low-power HCSL (LP-HCSL) output.	



Number	Na	ıme	Туре	Description
10	SD/OE	Input	Internal Pull-down	Enables/disables the outputs (OE) or powers down the chip (SD). The SH bit controls the configuration of the SD/OE pin. The SH bit needs to be high for SD/OE pin to be configured as SD. The SP bit (0x02) controls the polarity of the signal to be either active HIGH or LOW only when pin is configured as OE (Default is active LOW.) Weak internal pull-down resistor. When configured as SD, the device is shut down, differential outputs are driven high/low, and the single-ended LVCMOS outputs are driven low. When configured as OE, and outputs are disabled, the outputs can be selected to be tri-stated or driven high/low.
11	SEL1/SDA	Input	Internal Pull-down	Configuration select pin, or I ² C SDA input as selected by OUT0_SEL_I2CB.
12	SEL0/SCL	Input	Internal Pull-down	Configuration select pin, or I ² C SCL input as selected by OUT0_SEL_I2CB.
13	VDD	Power	-	Connect to 1.8V.
14	VDDO	Power	-	Connect to 1.8V. Power pin for outputs 3, 5–7.
15	OUT5	Output	-	Output clock 5. Low-power HCSL (LP-HCSL) output.
16	OUT5B	Output	-	Complementary output clock 5. Low-power HCSL (LP-HCSL) output.
17	OEA	Input	Internal Pull-down	Active-low Output Enable pin for outputs 3 and 5. 0 = Enable outputs; 1 = Disable outputs. This pin has internal pull-down.
18	VDDO4	Power	-	Connect to 1.8V to 3.3V. VDD supply for OUT4.
19	OUT4	Output	-	Output clock 4. Refer to the Output Drivers section for more details.
20	OUT4B	Output	-	Complementary Output Clock 4. Refer to the <i>Output Drivers</i> section for more details.
21	NC	_	-	Do not connect.
22	NC	_	-	Do not connect.
23	OUT3B	Output	-	Complementary Output Clock 3. Refer to the <i>Output Drivers</i> section for more details.
24	OUT3	Output	-	Output Clock 3. Refer to the Output Drivers section for more details.
25	VDD_Core	Power	-	Connect to 1.8V
26	VDD	Power	-	Connect to 1.8V
27	VDD	Power	-	Connect to 1.8V
28	OUT2B	Output	-	Complementary output clock 2. Refer to the <i>Output Drivers</i> section for more details.
29	OUT2	Output	-	Output Clock 2. Refer to the Output Drivers section for more details.
30	VDDO2	Power	-	Connect to 1.8V to 3.3V. VDD supply for OUT2.
31	OUT1B	Output	-	Complementary output clock 1. Refer to the <i>Output Drivers</i> section for more details.
32	OUT1	Output	-	Output Clock 1. Refer to the Output Drivers section for more details.



Number	Na	ame	Туре	Description
33	VDDO1	Power	-	Connect to 1.8V to 3.3V. VDD supply for OUT1.
34	OEB	Input	Internal Pull-down	Active-low Output Enable pin for outputs 6 and 7. 0 = Enable outputs; 1 = Disable outputs. This pin has internal pull-down.
35	NC	_	-	Do not connect.
36	VDDO	Power	-	Connect to 1.8V. Power pin for outputs 3, 5–7.
37	VDD	Power	-	Connect to 1.8V.
38	OE_buffer		Internal Pull-up	Active High Output enable for outputs 3, 5–7. 0 = Disable outputs; 1 = Enable outputs. This pin has internal pull-up.
39	VDD00	Power	-	Power supply pin for OUT0_SEL_I2CB. Connect to 1.8 to 3.3V. Sets the output voltage levels for OUT0.
40	OUT0_SE _I2CB	Output	Internal Pull-down	Latched input/LVCMOS output. At power up, the voltage at the pin OUT0_SEL_I2CB is latched by the device and used to select the state of pins 11 and 12. If a weak pull-up (10Kohms) is placed on OUT0_SEL_I2CB, pins 11 and 12 will be configured as hardware select pins, SEL1 and SEL0. If a weak pull-down (10Kohms) is placed on OUT0_SEL_I2CB or it is left floating, pins 11 and 12 will act as the SDA and SCL pins of an I2C interface. After power up, the pin acts as a LVCMOS reference output.
EPAD	GND	GND	-	Connect to ground pad.



3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the device at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Supply Voltage	VDDA, VDDD, VDDO	-0.5	3.6	V
	XIN/REF	-0.5	1.2	
Input Voltage	SD/OE, SEL1/SDA, SEL0/SCL	-0.5	3.465	V
	CLKIN, CLKINB	-0.5	1.2	
I ² C Loading Current	-	-	10	mA
Storage Temperature	T _{STG}	-65	150	°C
Junction Temperature	TJ	-	125	°C
Human Body Model (Tested per JS-001-2017)	ESD	-	2000	٧
Charged Device Model (AECQ100)	ESD	-	750	V
Latch-Up (AECQ100)	-	100	100	mA

4. Thermal Characteristics

Table 3. Thermal Characteristics

Symbol	Parameter	Value	Unit
θја	Theta JA. Junction to air thermal impedance (0mps)	41.08	°C/W
θЈВ	Theta JB. Junction to board thermal impedance (0mps)	13.76	°C/W
θјс	Theta JC. Junction to case thermal impedance (0mps)	28.45	°C/W

5. Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
	Power supply voltage for supporting 1.8V outputs.	1.71	1.8	1.89	V
V_{DDDx}	Power supply voltage for supporting 2.5V outputs.	2.375	2.5	2.625	V
	Power supply voltage for supporting 3.3V outputs.	3.135	3.3	3.465	V



V _{DDD}	Power supply voltage for core logic functions.	1.71	-	3.465	V
V_{DDA}	Analog power supply voltage. Use filtered analog power supply.	1.71	-	3.465	V
T _{PU}	Power ramp time for all V _{DD} s to reach 90% of V _{DD} .	0.05	-	50	ms
T _A	Operating temperature, ambient.	-40	-	85	°C
CL	Maximum load capacitance (3.3V LVCMOS only).	-	-	15	pF

6. Electrical Characteristics

Table 5. Current Consumption Characteristics

 V_{DDA} , V_{DDD} , V_{DDO0} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +85°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
IDDCORE [a]	Core Supply Current	100MHz on all outputs, 25MHz REFCLK.	-	33	42	mA
I _{DDOX}	Output Buffer Supply	LVPECL, 350MHz, 3.3V V _{DDOx} ^[b]	-	45	58	mA
	Current	LVPECL, 350MHz, 2.5V V _{DDOx} ^[b]	-	36	47	mA
		LVDS, 350MHz, 3.3V V _{DDOx} [b]	-	26	32	mA
		LVDS, 350MHz, 2.5V V _{DDOx} [b]	-	25	30	mA
		LVDS, 350MHz, 1.8V V _{DDOx} [b]	-	22	27	mA
		HCSL, 250MHz, 3.3V V _{DDOx} [b]	-	39	48	mA
		HCSL, 250MHz, 2.5V V _{DDOx} [b]	-	37	46	mA
		LVCMOS, 50MHz, 3.3V, V _{DDOx} [b],[c]	-	22	27	mA
		LVCMOS, 50MHz, 2.5V, V _{DDOx} [b],[c]	-	20	24	mA
		LVCMOS, 50MHz, 1.8V, V _{DDOx} [b],[c]	-	17	21	mA
		LVCMOS, 200MHz, 3.3V V _{DDOx} [b],[c]	-	43	56	mA
		LVCMOS, 200MHz, 2.5V V _{DDOx} [b],[c]	-	33	43	mA
		LVCMOS, 200MHz, 1.8V V _{DDOx} [b],[c]	-	24	31	mA
I _{DDPD}	Power Down Current	SD asserted, I ² C programming.	-	10	12	mA

[[]a] $I_{DDCORE} = I_{DDA} + I_{DDD}$.

[[]b] Measured into a 5" 50Ω trace. See Test Loads section for more details.

[[]c] Single CMOS driver active.



Table 6. AC Timing Characteristics

 V_{DDA} , V_{DDD} , V_{DDO0} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +85°C, unless stated otherwise.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
F _{IN} [a]	Input Frequency	Input frequency limit (Crystal)	8	-	40	MHz
		Input frequency limit (Single-ended over XIN)	1	-	200	IVITZ
F _{OUT} [b]	Output Frequency	Single-ended clock output limit (LVCMOS), individual FOD mode.	1	-	200	
		Differential clock output (LVPECL/LVDS/HCSL), individual FOD mode.	1	-	350	
		Single-ended clock output limit (LVCMOS), cascaded FOD mode, output 2, 4.	0.001	-	200	MHz
		Differential clock output limit (LVPECL/LVDS/HCSL), cascaded FOD mode, output 2, 4.	0.001	-	350	
		Differential clock output (LP-HCSL output 3, 5, 6, 7)	0.001	-	200	
fVCO	VCO Operating Frequency Range		2500	-	2900	MHz
T _{DC} [c]	Output Duty Cycle	Measured at $V_{DD}/2$, all outputs except reference output, V_{DDOX} = 2.5V or 3.3V.	45	50	55	%
		Measured at $V_{DD}/2$, all outputs except reference output, $V_{DDOX} = 1.8V$	40	50	60	%
		Measured at $V_{DD}/2$, reference output OUT0 (5MHz–150.1MHz) with 50% duty cycle input.	40	50	60	%
		Measured at V _{DD} /2, reference output OUT0 (150.1MHz–200MHz) with 50% duty cycle input.	30	50	70	%
Tskew	Output Skew	Skew between the same frequencies, with outputs using the same driver format and phase delay set to 0ns.	-	75	-	ps
T _{STARTUP} [d] [e]	Startup Time	Measured after all $V_{DD}s$ have raised above 90% of their target value. $\[mathbb{M}\]$	-	-	30	ms
		PLL lock time from shutdown mode.	-	3	4	ms

[[]a] Practical lower frequency is determined by loop filter settings.

[[]b] A slew rate of 2.75V/ns or greater should be selected for output frequencies of 100MHz or higher.

[[]c] Duty cycle is only guaranteed at maximum slew rate settings.

[[]d] Actual PLL lock time depends on the loop configuration.

[[]e] Includes loading the configuration bits from EPROM to PLL registers. It does not include EPROM programming/write time.

[[]f] Power-up with temperature calibration enabled, please contact Renesas if shorter lock-time is required in system.



Table 7. Input Characteristics

 V_{DDA} , V_{DDD} , V_{DDO0} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +85°C, unless stated otherwise.

Symbol	Parameter	Pins	Minimum	Typical	Maximum	Unit
C _{IN}	Input Capacitance	SD/OE,SEL1/SDA, SEL0/SCL	-	3	7	pF
R _{PD}	Pull-down Resistor	SD/OE,SEL1/SDA, SEL0/SCL, OUT0_SEL_I2CB	100	-	300	kΩ
V _{IH}	Input High Voltage	SD/OE	0.7 x V _{DDD}	-	V _{DDD} + 0.3	V
V_{IL}	Input Low Voltage	SD/OE	GND - 0.3	-	0.3 x V _{DDD}	V
VIH	Input High Voltage	OUT0_SEL_I2CB	0.65 x V _{DDO0}	-	V _{DDO0} + 0.3	V
VIL	Input Low Voltage	OUT0_SEL_I2CB	GND - 0.3	-	0.4	٧
V _{IH}	Input High Voltage	XIN/REF	0.8	-	1.2	V
VIL	Input Low Voltage	XIN/REF	GND - 0.3	-	0.4	V
T _R /T _F	Input Rise/Fall Time	SD/OE, SEL1/SDA, SEL0/SCL	-	-	300	ns



Table 8. Electrical Characteristics – CMOS Outputs

 V_{DDA} , V_{DDD} , V_{DDO0} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +85°C, unless stated otherwise.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
Vон	Output High Voltage	IOH = -15mA (3.3V), -12mA (2.5V).	0.7 x V _{DDO}	-	V_{DDO}	V
V _{OH}	Output High Voltage	IOH = -8mA (1.8V)	0.7 x V _{DDO}	-	V _{DDO}	V
Vol	Output Low Voltage	IOH = 15mA (3.3V), 12mA (2.5V), 8mA (1.8V)	-	-	0.45	V
Rout	Output Driver Impedance	CMOS Output Driver	-	17	-	Ω
Tsr	Slew Rate, SLEW[1:0] = 00	Single-ended 3.3V LVCMOS output clock	1.0	2.2	-	
	Slew Rate, SLEW[1:0] = 01	rise and fall time, 20% to 80% of VDDO (output load = 5pF) V _{DDOX} = 3.3V	1.2	2.3	-	
	Slew Rate, SLEW[1:0] = 10	1.3	2.4	-		
	Slew Rate, SLEW[1:0] = 11		1.7	2.7	-	
	Slew Rate, SLEW[1:0] = 00	Single-ended 2.5V LVCMOS output clock	0.6	1.3	-	
	Slew Rate, SLEW[1:0] = 01		0.7	1.4	-	\
	Slew Rate, SLEW[1:0] = 10	rise and fall time, 20% to 80% of VDDO (output load = 5pF) VDDOX = 2.5V	0.6	1.4	-	V/ns
	Slew Rate, SLEW[1:0] = 11		1.0	1.7	-	
	Slew Rate, SLEW[1:0] = 00	Single-ended 1.8V LVCMOS output clock	0.3	0.7	-	
	Slew Rate, SLEW[1:0] = 01	rise and fall time, 20% to 80% of VDDO (output load = 5pF) VDD = 1.8V.	0.4	0.8	-	
	Slew Rate, SLEW[1:0] = 10	(output load – opi) vbb – 1.0v.	0.4	0.9	-	
	Slew Rate, SLEW[1:0] = 11		0.7	1.2	-	
lozdd	Output Leakage Current (OUT1–4)	Tri-state outputs	-	-	5	μA
	Output Leakage Current (OUT0)	Tri-state outputs	-	-	30	μA



Table 9. Electrical Characteristics – LVDS Outputs

 V_{DDA} , V_{DDD} , V_{DDO0} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +85°C, unless stated otherwise.

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V _{OT} (+)	Differential Output Voltage for the TRUE Binary State	247	-	454	mV
V _{OT} (-)	Differential Output Voltage for the FALSE Binary State	-454	ı	-247	mV
ΔV_{OT}	Change in V _{OT} between Complimentary Output States	-	1	50	mV
V _{OS}	Output Common Mode Voltage (Offset Voltage) at 3.3V ±5%, 2.5V ±5%	1.125	1.25	1.375	٧
	Output Common Mode Voltage (Offset Voltage) at 1.8V ±5%	0.8	0.875	0.96	V
ΔV_{OS}	Change in V _{OS} between Complimentary Output States	-	-	50	mV
Ios	Outputs Short Circuit Current, V _{OUT} + or V _{OUT} - = 0V or V _{DDO}	-	9	24	mA
I _{OSD}	Differential Outputs Short Circuit Current, V _{OUT} + = V _{OUT} -	-	6	12	mA
T _R	LVDS rise time 20–80%	-	300	-	ps
T _F	LVDS fall time 80–20%	-	300	-	ps

Table 10. Electrical Characteristics – LVPECL Outputs

 V_{DDA} , V_{DDD} , V_{DDO0} = 3.3V ±5%, 2.5V ±5%, T_A = -40°C to +85°C, unless stated otherwise.

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V _{OH}	Output Voltage High, terminated through 50Ω tied to V_{DD} - $2V$	V _{DDO} - 1.19	-	V _{DDO} - 0.69	V
V _{OL}	Output Voltage Low, terminated through 50Ω tied to V_{DD} - $2V$	V _{DDO} - 1.94	-	V _{DDO} - 1.4	V
V _{SWING}	Peak-to-Peak Differential Output Voltage Swing	1.1	-	2	V
T _R	LVPECL rise time 20–80%	-	400	-	ns
T _F	LVPECL fall time 80–20%	-	400	-	ns



Table 11. Electrical Characteristics – HCSL Outputs[a]

 V_{DDA} , V_{DDD} , $V_{DD00} = 3.3V \pm 5\%$, $2.5V \pm 5\%$, $T_A = -40$ °C to +85°C, unless stated otherwise.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
dV/dt	Slew Rate	Scope averaging on [b] [c]	1	-	4	V/ns
ΔdV/dt	Slew Rate Matching	Scope averaging on [b] [c]	-	-	20	%
V_{MAX}	Maximum Voltage	Measurement on single-ended signal	-	1	1150	mV
V _{MIN}	Minimum Voltage	using absolute value (scope averaging off)	-300	-	-	mV
V _{SWING}	Voltage Swing	Scope averaging off [b] [f]	300	-	-	mV
V _{CROSS}	Crossing Voltage Value	Scope averaging off [d] [f]	250	-	550	mV
ΔV _{CROSS}	Crossing Voltage Variation	Scope averaging off [e]	-	-	140	mV

[[]a] Guaranteed by design and characterization. Not 100% tested in production.

Table 12. Spread-Spectrum Generation Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
fssout	Spread Frequency	Output frequency range for spread spectrum 5		-	300	MHz
f _{MOD}	Mod Frequency	Modulation frequency.		30 to 63		
f	Sproad Value	Amount of spread value (programmable)-center spread.	±0.1% to ±2.5%		5%	%f _{OUT}
f _{SPREAD} Spread Value		Amount of spread value (programmable)-down spread.		-0.2% to -5°	%	/º¹OUT

[[]b] Measured from differential waveform.

[[]c] Slew rate is measured through the VSWING voltage range centered on differential 0V. This results in a ±150mV window around differential 0V.

[[]d] VCROSS is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e., Clock rising and Clock# falling).

[[]e] The total variation of all VCROSS measurements in any particular system. Note that this is a subset of VCROSS min/max (VCROSS absolute) allowed. The intent is to limit VCROSS induced modulation by setting ΔVCROSS to be smaller than VCROSS absolute.

[[]f] Measured from single-ended waveform.



Table 13. I²C Bus (SCL/SDA) DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V _{IH}	Input High Level	For SEL1/SDA pin and SEL0/SCL pin.	0.7 x V _{DDD}	-	-	V
V _{IL}	Input Low Level	For SEL1/SDA pin and SEL0/SCL pin.	-	-	0.3 x V _{DDD}	V
V _{HYS}	Hysteresis of Inputs		0.05 x V _{DDD}	-	-	V
I _{IN}	Input Leakage Current		-1	-	36	μA
V _{OL}	Output Low Voltage	I _{OL} = 3mA.	-	-	0.45	V

Table 14. I²C Bus (SCL/SDA) AC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
F _{SCLK}	Serial Clock Frequency (SCL)	10	-	400	kHz
t _{BUF}	Bus Free Time between Stop and Start	1.3	-	-	μs
t _{SU:STA}	Setup Time, Start	0.6	-	-	μs
t _{HD:STA}	Hold Time, Start	0.6	-	-	μs
t _{SU:DAT}	Setup Time, Data Input (SDA)	0.1	-	-	μs
t _{HD:DAT}	Hold Time, Data Input (SDA) ¹	0	-	-	μs
t _{OVD}	Output Data Valid from Clock	-	-	0.9	μs
C _B	Capacitive Load for Each Bus Line	-	-	400	pF
t _R	Rise Time, Data and Clock (SDA, SCL)	20 + 0.1 x C _B	-	300	ns
t _F	Fall Time, Data and Clock (SDA, SCL)	20 + 0.1 x C _B	-	300	ns
t _{HIGH}	High Time, Clock (SCL)	0.6	-	-	μs
t _{LOW}	Low Time, Clock (SCL)	1.3	-	-	μs
t _{SU:STO}	Setup Time, Stop	0.6	-	-	μs

[[]a] A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[[]b] I²C inputs are 3.3V tolerant.

7. Test Loads

Figure 2. LVCMOS Test Load

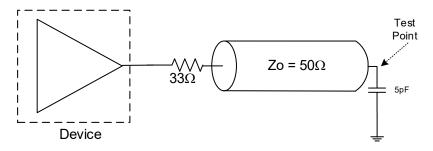


Figure 3. HCSL/LPHCSL Test Load

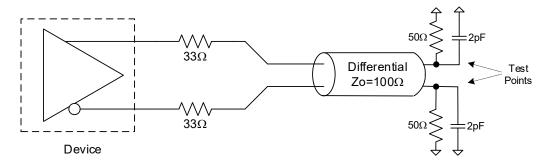


Figure 4. LVDS Test Load

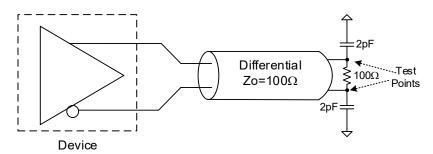
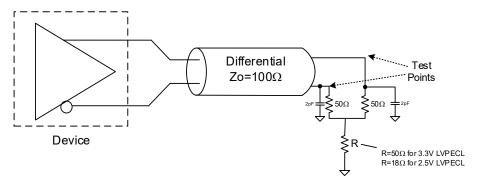
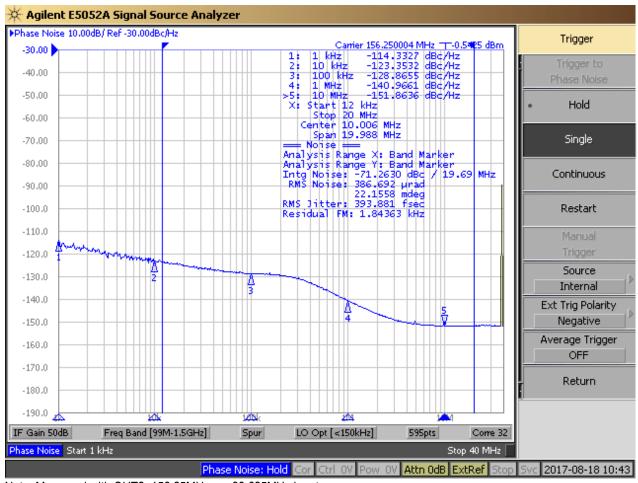


Figure 5. LVPECL Test Load



8. Jitter Performance Characteristics

Figure 6. Typical Phase Jitter Plot at 156.25MHz



Note: Measured with OUT2=156.25MHz on, 39.625MHz input.

Table 15. Jitter Performance[a] [b]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
J _{CY-CY}	Cycle to Cycle Jitter	LVCMOS 3.3V ±5%,-40°C to 90°C	-	12	30	ps
		All differential outputs 3.3V ±5%, -40°C to 90°C	-	25	35	ps
J _{pk-pk}	Period Jitter	LVCMOS 3.3V ±5%, -40°C to 90°C	-	15	40	ps
		All differential outputs 3.3V ±5%, -40°C to 90°C	-	24	35	ps
J _{RMS}	RMS Phase Jitter	LVCMOS 3.3V ±5%, -40°C to 90°C	-	0.3	-	ps
	(12kHz-20MHz)	All differential outputs 3.3V ±5%, -40°C to 90°C	-	0.6	-	ps

[[]a] Measured with 25MHz crystal input

[[]b] Configured with OUT0 = 25MHz_LVCMOS OUT1 = 100MHz HCSL OUT2 = 125MHz LVDS OUT3 = 156.25MHz_LVPECL



9. PCI Express Jitter Performance and Specification

Table 16. PCI Express Jitter Performance (Spread Spectrum = OFF)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Limit	Unit	Notes
	tjphPCleG1-CC	PCle Gen1 (2.5 GT/s) SSC = OFF	-	4	-	86	ps (p-p)	1, 2
	4	PCIe Gen2 Lo Band (5.0 GT/s) SSC = OFF	-	0.05	-	3	ps (RMS)	1, 2
PCle Phase Jitter (Common Clocked	t _{jphPCleG2-CC}	PCle Gen2 Hi Band (5.0 GT/s) SSC = OFF	-	0.22	-	3.1	ps (RMS)	1, 2
Architectures)	t _{jphPCleG3-CC}	PCle Gen3 (8.0 GT/s) SSC = OFF	-	0.12	-	1	ps (RMS)	1, 2
	t _{jphPCleG4-CC}	PCIe Gen4 (16.0 GT/s) SSC = OFF	-	0.12	-	0.5	ps (RMS)	1, 2, 3, 4
	t _{jphPCleG5-CC}	PCIe Gen5 (32.0 GT/s) SSC = OFF	-	0.05	-	0.15	ps (RMS)	1, 2, 3, 5
	tjphPCleG1-SRNS	PCle Gen1 (2.5 GT/s) SSC = OFF	-	3	-	n/a	ps (p-p)	1, 2, 6
	tjphPCleG2-SRNS	PCle Gen2 (5.0 GT/s) SSC = OFF	-	0.26	-	n/a	ps (RMS)	1, 2, 6
PCIe Phase Jitter (SRNS Architectures)	t _{jphPCleG3-SRNS}	PCle Gen3 (8.0 GT/s) SSC = OFF	-	0.07	-	n/a	ps (RMS)	1, 2, 6
	tjphPCleG4-SRNS	PCIe Gen4 (16.0 GT/s) SSC = OFF	-	0.07	-	n/a	ps (RMS)	1, 2, 6
	t _{jphPCleG5-SRNS}	PCle Gen5 (32.0 GT/s) SSC = OFF	-	0.07	-	n/a	ps (RMS)	1, 2, 6

¹ The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 7.0, Revision 1.0. See the Test Loads section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table.

- 3 SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
- ⁴ Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
- ⁵ Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
- 6 While the PCI Express Base Specification 5.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, it does not provide specification limits, hence the n/a in the Limit column. SRIS values are informative only. In general, a clock operating in an SRIS system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by √2.

² Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results the RTO result must be used.

Table 17. PCI Express Jitter Performance (Spread Spectrum = ON)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Limit	Unit	Notes
	t _{jphPCleG1-CC}	PCle Gen1 (2.5 GT/s) SSC = ≤ -0.5%	-	16	-	86	ps (p-p)	1, 2
	t	PCIe Gen2 Lo Band (5.0 GT/s) SSC = \leq -0.5%	-	0.02	-	3	ps (RMS)	1, 2
PCIe Phase Jitter (Common Clocked	tjphPCleG2-CC	PCIe Gen2 Hi Band (5.0 GT/s) SSC = \leq -0.5%	-	0.92	-	3.1	ps (RMS)	1, 2
Architectures)	tjphPCleG3-CC	PCIe Gen3 (8.0 GT/s) SSC = ≤ -0.5%	-	0.37	-	1	ps (RMS)	1, 2
	tjphPCleG4-CC	PCle Gen4 (16.0 GT/s) SSC = <u><</u> -0.5%	-	0.37	-	0.5	ps (RMS)	1, 2, 3, 4
	t _{jphPCleG5-CC}	PCle Gen5 (32.0 GT/s) SSC = ≤ -0.5%	-	N/A	-	0.15	ps (RMS)	1, 2, 3, 5
	t _{jphPCleG1-SRIS}	PCle Gen1 (2.5 GT/s) SSC = ≤ -0.3%	-	14	-	n/a	ps (p-p)	1, 2, 6
	t _{jphPCleG2-SRIS}	PCle Gen2 (5.0 GT/s) SSC = ≤ -0.3%	-	1.4	-	n/a	ps (RMS)	1, 2, 6
PCIe Phase Jitter (SRIS Architectures)	t _{jphPCleG3-SRIS}	PCIe Gen3 (8.0 GT/s) SSC = <u><</u> -0.3%	-	0.42	-	n/a	ps (RMS)	1, 2, 6
	tjphPCleG4-SRIS	PCle Gen4 (16.0 GT/s) SSC = ≤ -0.3%	-	0.36	-	n/a	ps (RMS)	1, 2, 6
	t _{jphPCleG5-SRIS}	PCle Gen5 (32.0 GT/s) SSC = ≤ -0.3%	-	N/A	-	n/a	ps (RMS)	1, 2, 6

¹ The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 7.0, Revision 1.0. See the Test Loads section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table.

- 3 SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
- ⁴ Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
- ⁵ Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
- 6 While the PCI Express Base Specification 5.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, it does not provide specification limits, hence the n/a in the Limit column. SRIS values are informative only. In general, a clock operating in an SRIS system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by √2.

² Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results the RTO result must be used.

10. Features and Functional Blocks

10.1 Clock Inputs

There is one differential clock input that support LVDS, HCSL, LVPECL logic levels without external terminations. The CLKIN pin can accept CMOS signals up to 1.2V. For more information on driving CLKIN with a CMOS signal, see section Input – Driving the XIN/REF. The two clock inputs can be left floating when unused.

When using the CLKIN pins the en clkin register must be set. For more details, see the Register Descriptions and Programming Guide.

The crystal oscillator is enabled by default but can be disabled when unused. For more details, see the <u>Register Descriptions and Programming Guide</u>.

10.2 Device Startup and Power-on-Reset

The 5P49V6975A has an internal power-up reset (POR) circuit. All VDDs must be connected to the desired supply voltage to trigger a POR.

The user can define specific default configurations through internal One-Time-Programmable (OTP) memory -- either the user or factory can program the default configuration. Contact Renesas if a specific factory-programmed default configuration is required, or refer to the VersaClock 6E Programming Guide.

The device will identity which of the two modes to operate in by the state of the OUT0_SEL_I2CB pin at POR. Both modes' default configurations can be programmed as follows:

- Software Mode (I²C): OUT0_SEL_I2CB is low at POR.
 The I²C interface will be open to users for in-system programming, overriding device default configurations at any time.
- 2. Hardware Select Mode: OUT0_SEL_I2CB is high at POR.

The device has been programmed to load OTP at power-up (REG0[7] = 1). The device will load internal registers according to *Table 18*. *Power-Up Behavior*.

Internal OTP memory can support up to four configurations, which selectable by the SEL0/SEL1 pins.

At POR, logic levels at SEL0 and SEL1 pins must be settled, which results in the selected configuration to be loaded at power up.

After the first 10ms of operation, the levels of the SELx pins can be changed, either to low or to the same level as VDDD/VDDA. The SELx pins must be driven with a digital signal of < 300ns rise/fall time and only a single pin can be changed at a time. After a pin level change, the device must not be interrupted for at least 1ms so that the new values have time to load and take effect.

Table 18. Power-Up Behavior

OUT0_SEL_I2CB at POR	SEL1	SEL0	I ² C Access	REG0:7	Config
1	0	0	No	0	0
1	0	1	No	0	1
1	1	0	No	0	2
1	1	1	No	0	3
0	Х	X	Yes	1	I ² C defaults
0	Х	Х	Yes	0	0

10.3 Internal Crystal Oscillator (XIN/REF)

10.3.1 Choosing Crystals

A crystal manufacturer will calibrate its crystals to the nominal frequency with a certain load capacitance value. When the oscillator load capacitance matches the crystal load capacitance, the oscillation frequency will be accurate. When the oscillator load capacitance is lower than the crystal load capacitance, the oscillation frequency will be higher than nominal and vice versa. Therefore, for an accurate oscillation frequency you must match the oscillator load capacitance with the crystal load capacitance.

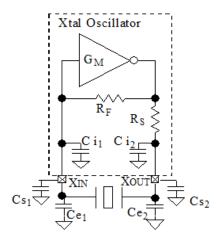
10.3.2 Tuning the Crystal Load Capacitor

Cs1 and Cs2 are stray capacitances at each crystal pin and typical values are between 1pF and 3pF (see Figure 7).

Ce1 and Ce2 are additional external capacitors. Increasing the load capacitance reduces the oscillator gain, so it is recommended to consult the manufacturer when adding Ce1 and/or Ce2 to avoid crystal startup issues.

Ci1 and Ci2 are integrated programmable load capacitors, one at XIN and one at XOUT.

Figure 7. Tuning the Crystal Load Capacitor



The value of each capacitor is composed of a fixed capacitance amount plus a variable capacitance amount set with the XTAL[5:0] register. Ci1 and Ci2 are commonly programmed to be the same value. Adjustment of the crystal tuning capacitors allows maximum flexibility to accommodate crystals from various manufacturers. The range of tuning capacitor values available are in accordance with the following table. Ci1/Ci2 starts at 0pF with the setting 000000b and can be increased up to 13.83pF with the setting 111111b. The step per bit is 0.43pF.

Table 19. XTAL[5:0] Tuning Capacitor

Parameter	Bits	Step (pF)	Min (pF)	Max (pF)
XTAL	6	0.43	0	13.83

You can write the following equation for this capacitance:

The final load capacitance of the crystal:

$$C_L = C_{XIN} \times C_{XOUT} / (C_{XIN} + C_{XOUT})$$

It is recommended to set the same value at each crystal pin meaning:

$$C_{XIN} = C_{XOUT}$$



Example: The crystal load capacitance is specified as 8pF, the stray capacitance at each crystal pin is Cs = 1.5pF, and the package stray capacitance is Ce = 7pF. Assuming equal capacitance value at XIN and XOUT = 6.92pF, the equation is as follows:

$$C_L = (6.92pF + 7.5pF + 1.5pF) / 2 = 7.9pF$$

XTAL[5:0] = 10000

Table 20. Recommended Crystal Characteristics

Parameter	Minimum	Typical	Maximum	Unit
Mode of Oscillation		Fundamental		
Frequency	8	25	40	MHz
Equivalent Series Resistance (ESR)	-	10	100	Ω
Shunt Capacitance	-	•	7	pF
Load Capacitance (C _L) at < = 25MHz	6	8	12	pF
Load Capacitance (C _L) > 25MHz to 40MHz	6	-	8	pF
Maximum Crystal Drive Level	-	-	100	μW

10.4 Programmable Loop Filter

The device PLL loop bandwidth operating range depends on the input reference frequency (Fref).

Table 21. Loop Filter Settings

Input Reference Frequency (MHz)	Loop Bandwidth Minimum (kHz)	Loop Bandwidth Maximum (kHz)
1	40	126
350	300	1000

10.5 Fractional Output Dividers (FOD)

The 5P49V6975A has four fractional output dividers (FOD). Each FOD is comprised of a 12-bit integer counter and a 24-bit fractional counter. The output divider can operate in integer divide only mode for improved performance or use the fractional counters to generate a clock frequency accurate to 50ppb.

FODs support the following features.

10.5.1 Individual Spread Spectrum Modulation

The output clock frequencies can be modulated to spread energy across a broader range of frequencies, thereby lowering system EMI. Each divider has individual spread ability. Spread modulation independent of output frequency, a triangle wave modulation between 30 and 63kHz.

Spread spectrum can be applied to any output clock, clock frequency, or spread amount from $\pm 0.25\%$ to $\pm 2.5\%$ center-spread and -0.5% to -5% down-spread.

10.5.2 Bypass Mode

Bypass mode (divide by 1) allows the output to behave as a buffered copy from the input or another FOD.

10.5.3 Cascaded Mode

As shown in the block diagram on page 1, FODs can be cascaded for lower output frequency.

For example, if OUT1 is configured to run at 12.288MHz and needs another 48kHz output, the user can cascade FOD2 by taking input from OUT1, with a divide ratio of 256. As a result, OUT 2 runs at 48kHz while in alignment with 12.288MHz on OUT1.

10.5.4 Dividers Alignment

Each output divider block has a synchronizing pulse to provide startup alignment between outputs dividers. This allows alignment of outputs for low skew performance.

When the 5P49V6975A is in hardware select mode, outputs are automatically aligned at POR. The same synchronization reset is also triggered when switching between configurations with the SEL0/1 pins. This ensures that the outputs remain aligned in every configuration.

When the 5P49V6975A is using software mode, I²C is used to reprogram an output divider during operation, and therefore, alignment can be lost. Alignment can be restored by manually triggering a reset through I²C.

The outputs are aligned on the falling edges of each output by default. Rising edge alignment can also be achieved by using the programmable skew feature to delay the faster clock by 180 degrees. The programmable skew feature also allows for fine tuning of the alignment.



10.5.5 Programmable Skew

The 5P49V6975A can skew outputs by quadrature values. The skew on each output can be adjusted from 0 to 360 degrees. Skew is adjusted in units equal to 1/32 of the VCO period. As a result, for 100MHz output and a 2800MHz VCO, the user can select how many 11.161ps units to be added to the skew (resulting in units of 0.402 degrees). For example, 0, 0.402, 0.804, 1.206, 1.408, and so on. The granularity of the skew adjustment is always dependent on the VCO period and the output period.

10.6 Output Drivers

Device output drivers can individually support the following features:

- 2.5V or 3.3V voltage level for HCSL/LVPECL operation
- 1.8V, 2.5V, or 3.3V voltage levels for CMOS/LVDS operation
- CMOS supports four operating modes:
 - CMOSD: OUTx and OUTxB 180 degrees out of phase
 - CMOSX2: OUTx and OUTxB phase-aligned
 - CMOS1: only OUTx pin is on
 - CMOS2: only OUTxB pin is on

When a given output is configured to CMOSD or CMOSX2, then all previously described configuration and control apply equally to both pins.

Independent output enable/disabled by register bits. When disabled, an output can be either in a logic 1 state or Hi-Z.

The following options are used to disable outputs:

- Output turned off by I²C
- Output turned off by SD/OE pin
- Output unused, which means it is turned off regardless of OE pin status

10.7 SD/OE Pin Function

The SD/OE pin can be programmed as follows:

- OE output enable (low active)
- OE output enable (high active)
- Global shutdown (low active)
- Global shutdown (high active)

Output behavior when disabled is also programmable. The user can select the output driver behavior when it is off as follows:

- OUTx pin high, OUTxB pin low (controlled by SD/OE pin)
- OUTx/OUTxB Hi-Z (controlled by SD/OE pin)
- OUTx pin high, OUTxB pin low (configured through I²C)
- OUTx/OUTxB Hi-Z (configured by I²C)

The user can disable the output with either I²C or SD/OE pin. For more information, see the VersaClock 6E Programming Guide.



10.8 I²C Operation

The 5P49V6975A acts as a slave device on the I²C bus using one of the two I²C addresses (0xD0 or 0xD4) to allow multiple devices to be used in the system. The interface accepts byte-oriented block write and block read operations.

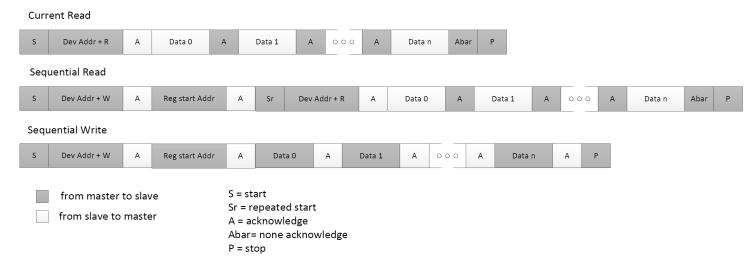
Address bytes (2 bytes) specify the register address of the byte position of the first register to write or read.

Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first).

Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP bit is received, at which point, all data received in the block write will be written simultaneously.

For full electrical I2C compliance, use external pull-up resistors for SDATA and SCLK.

Figure 8. I2C R/W Sequence



11. Typical Application Circuit

For more information on application and reference circuit designs, refer to the 5P49V6967 and 5P49V6968 Evaluation Board Manual.

11.1 Recommendations for Unused Input and Output Pins

11.1.1 XIN/REF and XOUT

If used as crystal inputs, each set of pins must be connected to a crystal. If using these pins as XIN/REF, see the section Input – Driving the XIN/REF for important information.

11.1.2 LVCMOS Outputs

Any LVCMOS output can be left floating if unused. There should be no trace attached. The output buffer should be set to high-impedance state to avoid unnecessary noise generation.

11.1.3 Differential Outputs

All unused differential outputs can be left floating. Renesas recommends that no trace be attached and that the outputs be set to high impedance. Both sides of the differential output pair should be treated the same, either left floating or terminated

11.2 Input – Driving the XIN/REF

11.2.1 Driving XIN/REF with a CMOS Driver

In some instances, it is preferable to have XIN/REF driven by a clock input -- for reasons such as better SNR, multiple input select with device CLKIN, etc. The XIN/REF pin can take an input when its amplitude is between 500mV and 1.2V, and the slew rate more than 0.2V/ns. The XIN/REF input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XOUT pin can be left floating.

When driving the XIN with a CMOS or differential signal, set the load capacitor to 0.

Figure 9. Overdriving XIN with a CMOS Driver

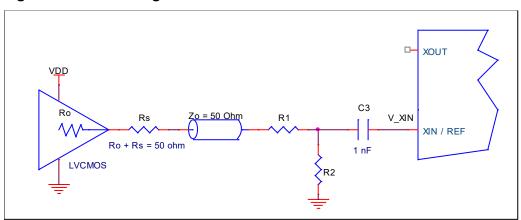


Table 22. Nominal Voltage Divider Values for Overdriving XIN with Single-ended Driver

LVCMOS Diver V _{DD}	Ro + Rs	R1	R2	V_XIN (peak)	Ro+Rs+R1+R2
3.3	50.0	130	75	0.97	255



Ī	2.5	50.0	100	100	1.00	250
	1.8	50.0	62	130	0.97	242

11.2.2 Driving XIN with a LVPECL Driver

Figure 10 shows an example of the interface diagram for a 3.3V LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XIN/REF input. It is recommended that all components in the schematic be placed in the layout; though some components may not be used, they can be used for debugging purposes. The datasheet specifications are characterized and guaranteed using a quartz crystal as the input. If the driver is 2.5V LVPECL, the only required change is to use the appropriate R3 value.

Figure 10. Overdriving XIN with a LVPECL Driver

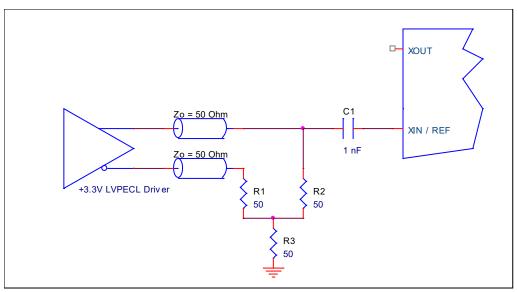


Table 23 shows resistor values that ensure the maximum drive level for the XIN port is not exceeded for all combinations of 5% tolerance on the driver V_{DD} , V_{DDO0} , and 5% resistor tolerances. The resistor values can be adjusted to reduce the loading for a slower and weaker LVCMOS driver by increasing the impedance of the R1–R2 divider. To better assist with this assessment, the total load (Ro+Rs+R1+R2) on the driver is included in the table.

Table 23. Nominal Voltage Divider Values for Overdriving XIN with Single-ended Driver

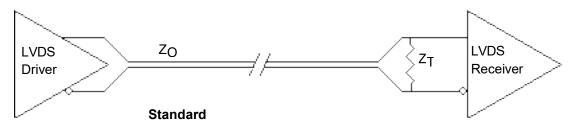
LVCMOS Diver V _{DD}	Ro + Rs	R1	R2	Vrx (peak)	Ro+Rs+R1+R2
3.3	50.0	130	75	0.97	255
2.5	50.0	100	100	1.00	250
1.8	50.0	62	130	0.97	242

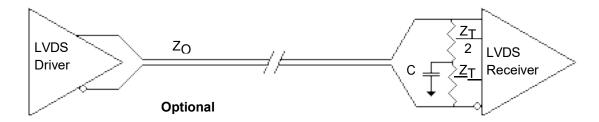
11.3 Output - Single-ended or Differential Clock Terminations

11.3.1 LVDS Termination

For a general LVDS interface, the recommended value for the termination impedance (ZT) is between 90Ω and 132Ω . The actual value should be selected to match the differential impedance (Zo) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω . Differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. The standard termination schematic as shown in figure *Standard Termination* or the termination of figure *Optional Termination* can be used, which uses a center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the Renesas LVDS output.

Figure 11. Standard and Optional Terminations





11.3.2 LVPECL Termination

The clock layout topology shown below are typical terminations for LVPECL outputs. The differential outputs generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50 Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. For VDDO = 2.5V, the VDDO − 2V is very close to ground level. The R3 in 2.5V LVPECL Output Termination can be eliminated and the termination is shown in 2.5V LVPECL Output Termination (2).

Figure 12. 3.3V LVPECL Output Termination

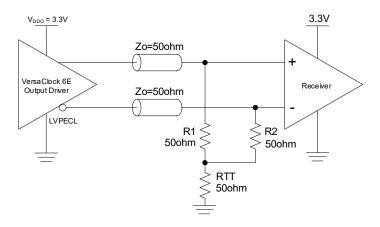


Figure 14. 2.5V LVPECL Output Termination

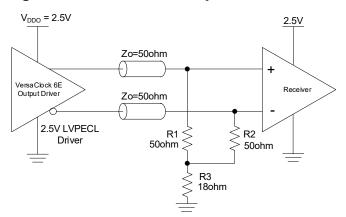


Figure 13. 3.3V LVPECL Output Termination (2)

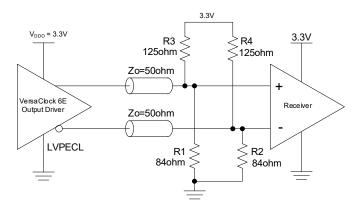


Figure 15. 2.5V LVPECL Output Termination (2)

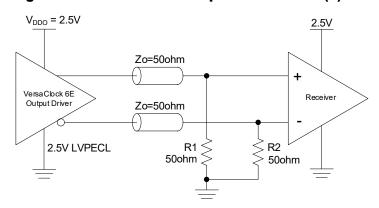
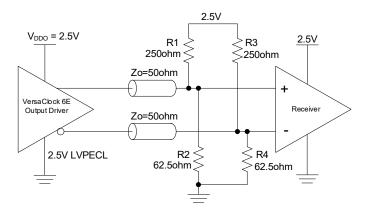


Figure 16. 2.5V LVPECL Output Termination (3)



11.3.3 HCSL Termination

HCSL termination scheme applies to both 3.3V and 2.5V VDDO.

Figure 17. HCSL Receiver Terminated

VersaClock 6E
Output Driver

33

Zo=50ohm

Receiver

VersaClock 6E
Output Driver

33

VersaClock 6E
Output Driver

33

Accepton Acceptor

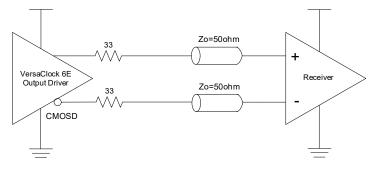
Figure 18. HCSL Source Terminated

11.3.4 LVCMOS Termination

Each output pair can be configured as a standalone CMOS or dual-CMOS output driver. An example of CMOSD driver termination is shown in the following figure:

- CMOS1 Single CMOS active on OUTx pin
- CMOS2 Single CMOS active on OUTxB pin
- CMOSD Dual CMOS outputs active on both OUTx and OUTxB pins, 180 degrees out of phase
- CMOSX2 Dual CMOS outputs active on both OUTx and OUTxB pins, in-phase.

Figure 19. LVCMOS Termination



12. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

13. Marking Diagram



- Lines 1 and 2 indicate the part number.
- Line 3:
 - "YYWW" is the last digit of the year and week that the part was assembled.
 - # denotes the sequential lot number.
 - "\$" denotes the mark code.

14. Ordering Information

Part Number [a][b]	Package	Carrier Type	Temperature Range
5P49V6967AdddNDGI	5 × 5 mm <u>40-VFQFPN</u>	Tray	-40° to +85°C
5P49V6967AdddNDGI8	5 × 5 mm <u>40-VFQFPN</u>	Tape and Reel	-40° to +85°C
5P49V6967A000NDGI	5 × 5 mm <u>40-VFQFPN</u>	Tray	-40° to +85°C
5P49V6967A000NDGI8	5 × 5 mm <u>40-VFQFPN</u>	Tape and Reel	-40° to +85°C

[[]a] "ddd" denotes factory programmed configurations based on required settings. Please contact factory for factory programming.

[[]b] "000" denotes un-programmed parts for user customization.



15. Revision History

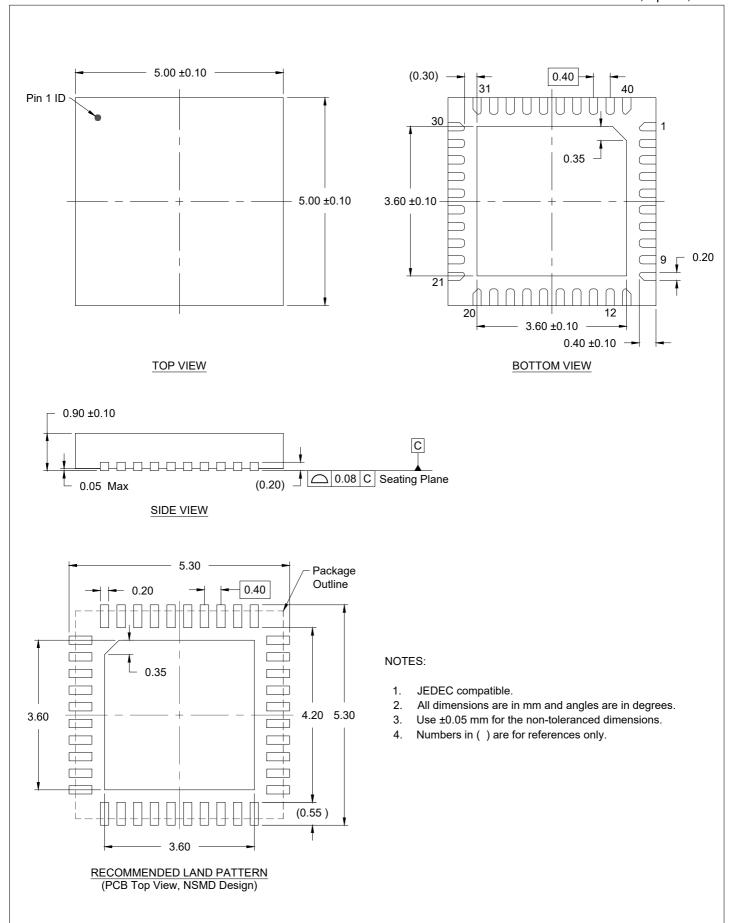
Revision Date	Description of Change
November 24, 2025	Updated Absolute Maximum Ratings table.
November 4, 2025	 Added section Clock Inputs. Added section Recommendations for Unused Input and Output Pins. Updated section Typical Application Circuit.
July 15, 2025	Updated capacitor values, equation and example in section 10.3.2.
April 17, 2024	Updated 1.8V V _{OH} to 0.7 × V _{DDO} from 0.5 × V _{DDO} in Table 8.
January 25, 2022	Updated descriptive text in Output – Single-ended or Differential Clock Terminations, LVDS Termination section.
July 7, 2021	 Updated the descriptive text in the LVDS Termination section. Updated the Package Outline Drawings section.
August 20, 2020	Updated slew rate terminology in section Driving XIN/REF with a CMOS Driver.
October 8, 2019	 Updated Absolute Maximum Ratings table. Updated PCI Express Jitter Performance tables (Table 16 and Table 17). Updated Electrical Characteristics tables (Table 8, Table 10 and Table 13).
June 19, 2019	 PCIe specification updated. Added recommended power ramp time. Expanded spread spectrum value range. I2C tolerant voltage footnote changed to 3.3V. LVDS Termination section allows AC-coupling for LVDS signals
August 30, 2018	Updated schematics for Driving XIN/REF with a CMOS Driver and Driving XIN with an LVPECL Driver sections.
July 5, 2018	Removed all references to CLKIN.
March 16, 2018	 Updated absolute maximum ratings for supply voltage to 3.6V. Updated typical and maximum values in Current Consumption table. Minor updates to AC Timing Characteristics, CMOS Outputs, and LVDS Outputs tables.
December 12, 2017	Initial release.

Package Outline Drawing



PSC-4292-03 NDG40P3

40-QFN 5.0 x 5.0 x 0.9 mm Body, 0.40 mm Pitch Rev.04, Apr 23, 2025



IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.