

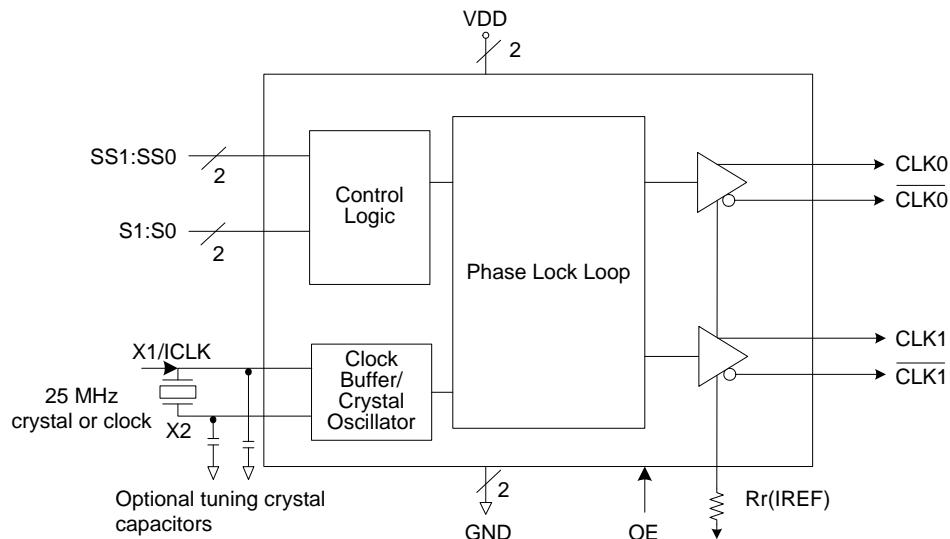
Description

The IDT5V41129 is a spread spectrum clock generator that supports PCI-Express Gen1 and Ethernet requirements. The device is used for PC or embedded systems to substantially reduce electromagnetic interference (EMI). The device provides two differential (HCSL) spread spectrum outputs. The spread type and amount are configured via select pin. Using IDT's patented Phase-Locked Loop (PLL) techniques, the device takes a 25 MHz crystal input and produces two pairs of differential outputs at 25 MHz, 100 MHz, 125 MHz or 200 MHz clock frequencies for HCSL, and 25 MHz or 100 MHz for LVDS.

Features

- Packaged in 16-pin TSSOP
- RoHS 5 (green) or RoHS 6 (green and lead free) compliant packaging
- Supports HCSL or LVDS output levels
- Operating voltage of 3.3 V
- Input frequency of 25 MHz
- Jitter 60 ps (cycle-to-cycle)
- Spread Spectrum capability
- Industrial and commercial temperature ranges
- **For PCIe Gen2 applications, see the 5V41065**
- **For PCIe Gen3 applications, see the 5V41235**

Block Diagram



Pin Assignment

| | | | |
|---------|---|----|--------|
| S0 | 1 | 16 | VDDXD |
| S1 | 2 | 15 | CLK0 |
| SS0 | 3 | 14 | CLK0 |
| X1/ICLK | 4 | 13 | GNDODA |
| X2 | 5 | 12 | VDDODA |
| OE | 6 | 11 | CLK1 |
| GNDXD | 7 | 10 | CLK1 |
| SS1 | 8 | 9 | IREF |

16-pin (173 mil) TSSOP

Output Select Table 1 (MHz)

| S1 | S0 | CLK(1:0), CLK(1:0) |
|----|----|--------------------|
| 0 | 0 | 25M |
| 0 | 1 | 100M |
| 1 | 0 | 125M |
| 1 | 1 | 200M |

Spread Selection Table 2

| SS1 | SS0 | Spread% |
|-----|-----|------------|
| 0 | 0 | No Spread |
| 0 | 1 | Down -0.5 |
| 1 | 0 | Down -0.75 |
| 1 | 1 | No Spread |

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|---|
| 1 | S0 | Input | Select pin 0. See Table1. Internal pull-up resistor. |
| 2 | S1 | Input | Select pin 1. See Table 1. Internal pull-up resistor. |
| 3 | SS0 | Input | Spread Select pin 0. See Table 2. Internal pull-up resistor. |
| 4 | X1/ICLK | Input | Crystal or clock input. Connect to a 25 MHz crystal or single ended clock. |
| 5 | X2 | Output | Crystal connection. Leave unconnected for clock input. |
| 6 | OE | Input | Output enable. Tri-states outputs and device is not shut down. Internal pull-up resistor. |
| 7 | GNDXD | Power | Connect to ground. |
| 8 | SS1 | Input | Spread Select pin 1. See Table 2. Internal pull-up resistor. |
| 9 | IREF | Output | Precision resistor attached to this pin is connected to the internal current reference. |
| 10 | CLK1 | Output | HCSL complimentary clock output 1. |
| 11 | CLK1 | Output | HCSL true clock output 1. |
| 12 | VDDODA | Power | Connect to voltage supply +3.3 V for output driver and analog circuits |
| 13 | GNDODA | Power | Connect to ground. |
| 14 | CLK0 | Output | HCSL complimentary clock output 0. |
| 15 | CLK0 | Output | HCSL true clock output 0. |
| 16 | VDDXD | Power | Connect to voltage supply +3.3 V for crystal oscillator and digital circuit. |

Applications Information

External Components

A minimum number of external components are required for proper operation.

Decoupling Capacitors

Decoupling capacitors of $0.01\ \mu\text{F}$ should be connected between each VDD pin and the ground plane, as close to the VDD pin as possible. Do not share ground vias between components. Route power from power source through the capacitor pad and then into ICS pin.

Crystal

A 25 MHz fundamental mode parallel resonant crystal should be used. This crystal must have less than 300 ppm of error across temperature in order for the IDT5V41129 to meet PCI Express specifications.

Crystal Capacitors

Crystal capacitors are connected from pins X1 to ground and X2 to ground to optimize the accuracy of the output frequency.

C_L = Crystal's load capacitance in pF

Crystal Capacitors (pF) = $(C_L - 8) * 2$

For example, for a crystal with a 16 pF load cap, each external crystal cap would be 16 pF. $(16-8)*2=16$.

Current Source (Iref) Reference Resistor - R_R

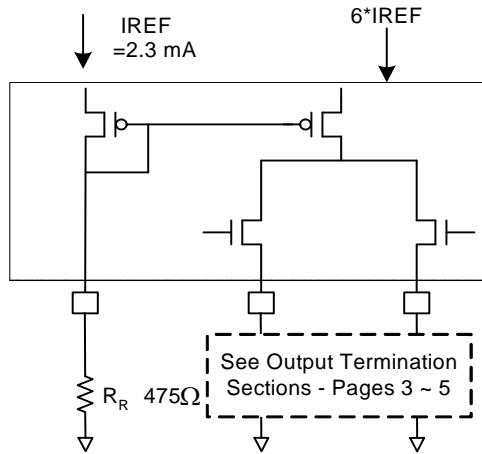
If board target trace impedance (Z) is 50Ω , then $R_R = 475\Omega$ (1%), providing IREF of 2.32 mA. The output current (I_{OH}) is equal to $6*IREF$.

Output Termination

The PCI-Express differential clock outputs of the IDT5V41129 are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the **PCI-Express Layout Guidelines** section.

The IDT5V41129 can also be configured for LVDS compatible voltage levels. See the **LVDS Compatible Layout Guidelines** section.

Output Structures



General PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1. Each $0.01\mu\text{F}$ decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible.
2. No vias should be used between decoupling capacitor and VDD pin.
3. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.
4. An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (any ferrite beads and bulk decoupling capacitors can be mounted on the back). Other signal traces should be routed away from the IDT5V41129. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

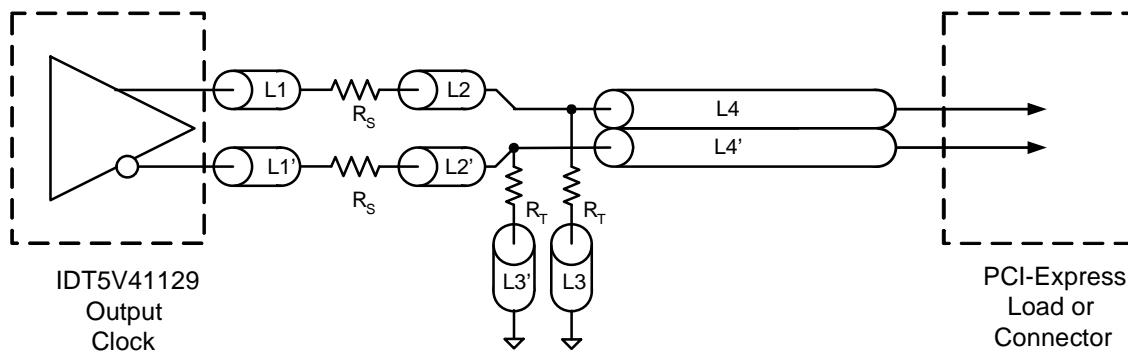
PCI-Express Layout Guidelines

| Common Recommendations for Differential Routing | Dimension or Value | Unit |
|---|--------------------|------|
| L1 length, Route as non-coupled 50 ohm trace. | 0.5 max | inch |
| L2 length, Route as non-coupled 50 ohm trace. | 0.2 max | inch |
| L3 length, Route as non-coupled 50 ohm trace. | 0.2 max | inch |
| R_S | 33 | ohm |
| R_T | 49.9 | ohm |

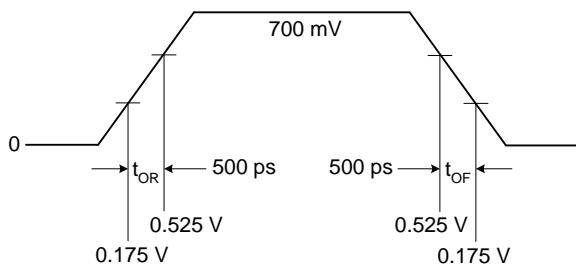
| Differential Routing on a Single PCB | Dimension or Value | Unit |
|---|---------------------|------|
| L4 length, Route as coupled microstrip 100 ohm differential trace. | 2 min to 16 max | inch |
| L4 length, Route as coupled stripline 100 ohm differential trace. | 1.8 min to 14.4 max | inch |

| Differential Routing to a PCI Express Connector | Dimension or Value | Unit |
|---|-----------------------|------|
| L4 length, Route as coupled microstrip 100 ohm differential trace. | 0.25 to 14 max | inch |
| L4 length, Route as coupled stripline 100 ohm differential trace. | 0.225 min to 12.6 max | inch |

PCI-Express Device Routing



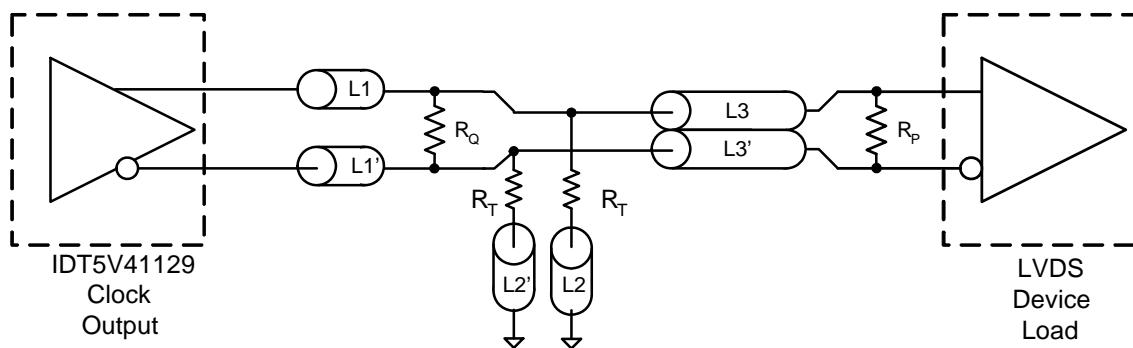
Typical PCI-Express (HCSL) Waveform



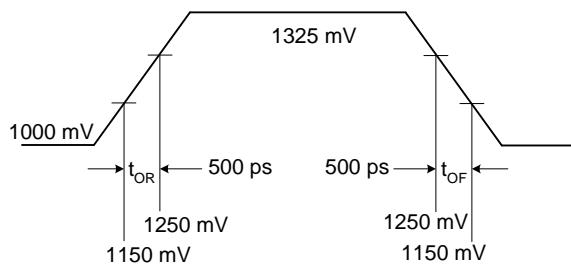
LVDS Compatible Layout Guidelines

| LVDS Recommendations for Differential Routing | Dimension or Value | Unit |
|---|--------------------|------|
| L1 length, Route as non-coupled 50 ohm trace. | 0.5 max | inch |
| L2 length, Route as non-coupled 50 ohm trace. | 0.2 max | inch |
| R_P | 100 | ohm |
| R_Q | 100 | ohm |
| R_T | 150 | ohm |

LVDS Device Routing



Typical LVDS Waveform



Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5V41129. These ratings are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|--|---------------------|
| Supply Voltage, VDDXD, VDDODA | 7 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature (commercial) | 0 to +70°C |
| Ambient Operating Temperature (industrial) | -40 to +85°C |
| Storage Temperature | -65 to +150°C |
| Junction Temperature | 125°C |
| Soldering Temperature | 260°C |
| ESD Protection (Input) | 2000 V min. (HBM) |

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V $\pm 10\%$** , Ambient Temperature -40 to +85°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|------------------------------------|-------------------|----------------------------|---------|------|----------|-------|
| Supply Voltage | V | | 2.97 | 3.3 | 3.63 | V |
| Input High Voltage ¹ | V _{IH} | S0, S1, OE, ICLK, SS0, SS1 | 2.0 | | VDD +0.3 | V |
| Input Low Voltage ¹ | V _{IL} | S0, S1, OE, ICLK, SS0, SS1 | VSS-0.3 | | 0.8 | V |
| Input Leakage Current ² | I _{IL} | 0 < Vin < VDD | -5 | | 5 | μA |
| Operating Supply Current | I _{DD} | 50Ω, 2 pF | | | 78 | mA |
| | I _{DDOE} | OE =Low | | | 44 | mA |
| Input Capacitance | C _{IN} | Input pin capacitance | | | 7 | pF |
| Output Capacitance | C _{OUT} | Output pin capacitance | | | 6 | pF |
| Pin Inductance | L _{PIN} | | | | 5 | nH |
| Output Resistance | R _{OUT} | CLK outputs | 3.0 | | | kΩ |
| Pull-up Resistor | R _{PU} | S0, S1, OE, SS0, SS1 | | 100 | | kΩ |

1. Single edge is monotonic when transitioning through region.

2. Inputs with pull-ups/-downs are not included.

AC Electrical Characteristics - CLK0/CLK1, CLK0/CLK1

Unless stated otherwise, **VDD=3.3 V $\pm 10\%$** , Ambient Temperature -40 to +85°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|--------------|--|------|------|------|-------|
| Input Frequency | | | | 25 | | MHz |
| Output Frequency | | HCSL termination | 25 | | 200 | MHz |
| | | LVDS termination | 25 | | 100 | MHz |
| Output High Voltage ^{1,2} | V_{OH} | HCSL | 660 | 700 | 850 | mV |
| Output Low Voltage ^{1,2} | V_{OL} | HCSL | -150 | 0 | 27 | mV |
| Crossing Point Voltage ^{1,2} | | Absolute | 250 | 350 | 550 | mV |
| Crossing Point Voltage ^{1,2,4} | | Variation over all edges | | | 140 | mV |
| Jitter, Cycle-to-Cycle ^{1,3} | | | | 60 | 100 | ps |
| Frequency Synthesis Error | | All outputs | | 0 | | ppm |
| Modulation Frequency | | Spread spectrum | 30 | 31.5 | 33 | kHz |
| Rise Time ^{1,2} | t_{OR} | From 0.175 V to 0.525 V | 175 | 332 | 700 | ps |
| Fall Time ^{1,2} | t_{OF} | From 0.525 V to 0.175 V | 175 | 344 | 700 | ps |
| Rise/Fall Time Variation ^{1,2} | | | | | 125 | ps |
| Output to Output Skew | | | | | 50 | ps |
| Duty Cycle ^{1,3} | | | 45 | | 55 | % |
| Output Enable Time ⁵ | | All outputs | | 10 | 12 | μs |
| Output Disable Time ⁵ | | All outputs | | 10 | 12 | μs |
| Stabilization Time | t_{STABLE} | From power-up VDD=3.3 V | | 3.0 | 3.5 | ms |
| Spread Spectrum Transition Time | t_{SPREAD} | Stabilization time after spread spectrum changes | | 3.0 | 3.5 | ms |

Note 1: Test setup is $R_L=50$ ohms with 2 pF, $R_r = 475\Omega$ (1%).

Note 2: Measurement taken from a single-ended waveform.

Note 3: Measurement taken from a differential waveform.

Note 4: Measured at the crossing point where instantaneous voltages of both CLK and \overline{CLK} are equal.

Note 5: CLK pins are tri-stated when OE is low asserted. CLK is driven differential when OE is high.

Electrical Characteristics - Differential Phase Jitter

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|---------------|-----------------|------------|-----|-----|-----|----------|-------|
| Jitter, Phase | $t_{jphasePLL}$ | PCIe Gen 1 | - | - | 86 | ps (p-p) | 1, 2 |

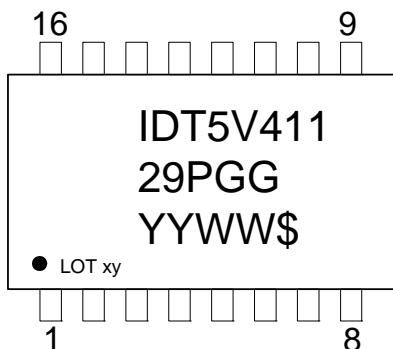
Note 1: Guaranteed by design and characterization, not 100% tested in production.

Note 2: See <http://www.pcisig.com> for complete specs.

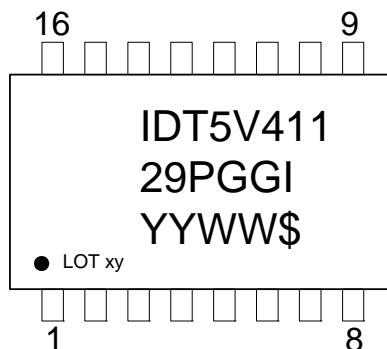
Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 78 | | °C/W |
| | θ_{JA} | 1 m/s air flow | | 70 | | °C/W |
| | θ_{JA} | 3 m/s air flow | | 68 | | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | | | 37 | | °C/W |

Marking Diagram (5V41129PGG)



Marking Diagram (5V41129PGGI)

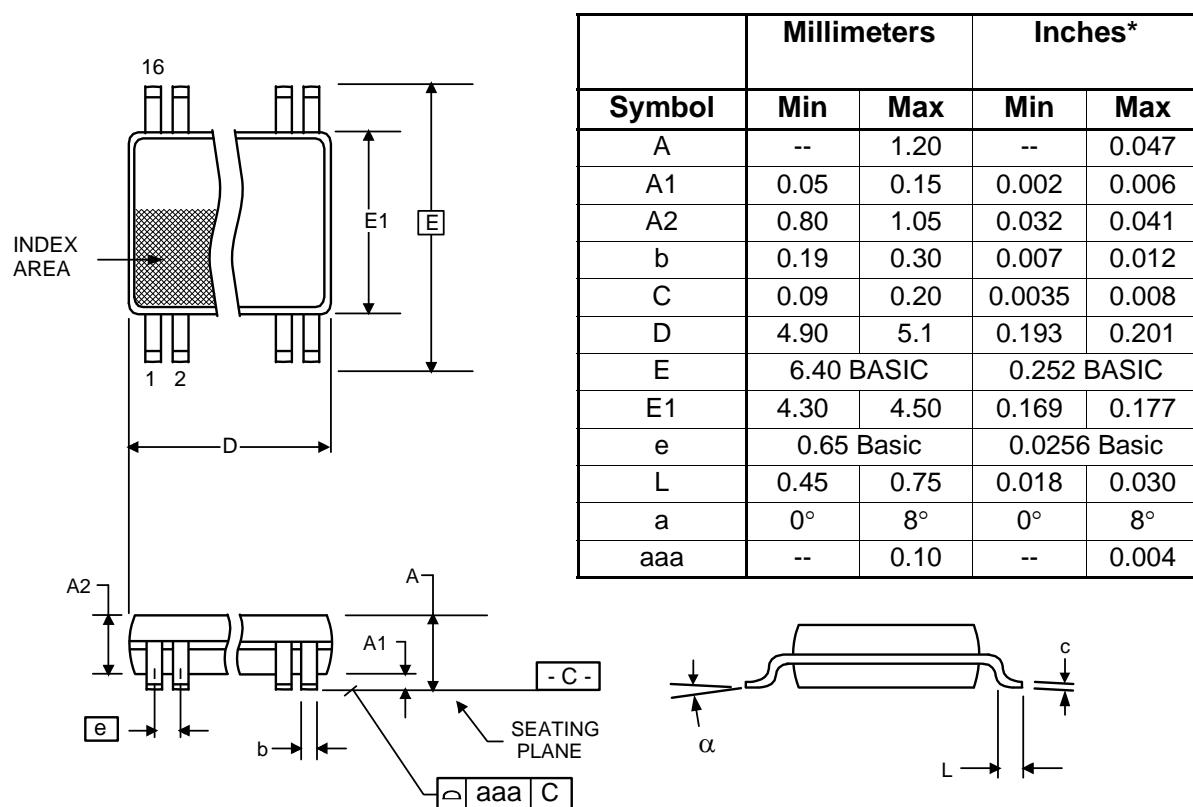


Notes:

1. Line 1 and 2: IDT part number.
2. Line 3: YYWW – Date code; \$ – Assembly location.
3. “G” after the two-letter package code designates RoHS compliant package.
4. “I” at the end of part number indicates industrial temperature range.

Package Outline and Package Dimensions (16-pin TSSOP, 173 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



| Symbol | Millimeters | | Inches* | |
|--------|-------------|------|--------------|-------|
| | Min | Max | Min | Max |
| A | -- | 1.20 | -- | 0.047 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 |
| A2 | 0.80 | 1.05 | 0.032 | 0.041 |
| b | 0.19 | 0.30 | 0.007 | 0.012 |
| C | 0.09 | 0.20 | 0.0035 | 0.008 |
| D | 4.90 | 5.1 | 0.193 | 0.201 |
| E | 6.40 BASIC | | 0.252 BASIC | |
| E1 | 4.30 | 4.50 | 0.169 | 0.177 |
| e | 0.65 Basic | | 0.0256 Basic | |
| L | 0.45 | 0.75 | 0.018 | 0.030 |
| a | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | 0.004 |

Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|------------|--------------------|--------------|---------------|
| 5V41129PGG | see page 8 | Tubes | 16-pin TSSOP | 0 to +70° C |
| 5V41129PGG8 | | Tape and Reel | 16-pin TSSOP | 0 to +70° C |
| 5V41129PGGI | | Tubes | 16-pin TSSOP | -40 to +85° C |
| 5V41129PGGI8 | | Tape and Reel | 16-pin TSSOP | -40 to +85° C |

“G” after the two-letter package code are the Pb-Free configuration and are RoHS compliant.

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Revision History

| Rev. | Date | Originator | Description of Change |
|------|----------|------------|---|
| C | 10/30/12 | D. Chan | Updated device top-side markings per latest ProdBuilder info. |
| D | 02/03/14 | RDW | Typo for part number in Termination drawings. Moved to final. |
| | | | |

IDT5V41129

2 OUTPUT PCI-EXPRESS GEN1 CLOCK SOURCE

PCIE SSCG

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