RENESAS

8-OUTPUT SMALL FORM FACTOR PCIE GEN 1-3 CLOCK GENERATOR — 6P41302

Description

The 6P41302 is an 8-output very low power clock generator for PCIe Gen1-2-3 applications with integrated output terminations providing Zo = 100Ω. The device has 8 output enables for clock management and supports 2 different spread spectrum levels in addition to spread off.

Typical Applications

PCIe Gen1–3 Clock Generator for Freescale designs

Output Features

- 8 0.7V low-power HCSL-compatible (LP-HCSL) DIF pairs with Zo = 100Ω
- 1 1.8V LVCMOS REF output w/Wake-On-LAN (WOL) support

Key Specifications

- DIF cycle-to-cycle jitter < 50ps
- DIF output-to-output skew < 50ps
- DIF phase jitter is PCIe Gen1–3 compliant
- REF phase jitter is < 1.5ps RMS

Features

- Integrated terminations provide 100Ω differential Zo; reduced component count and board space
- 1.8V operation; reduced power consumption
- Outputs can optionally be supplied from any voltage between 1.05V and 1.8V; maximum power savings
- OE# pins; support DIF power management
- LP-HCSL differential clock outputs; reduced power and board space
- Programmable Slew rate for each output; allows tuning for various line lengths
- Programmable output amplitude; allows tuning for various application environments
- DIF outputs blocked until PLL is locked; clean system start-up
- Selectable 0%, -0.25% or -0.5% spread on DIF outputs; reduces EMI
- External 25MHz crystal; supports tight ppm with 0 ppm synthesis error
- Configuration can be accomplished with strapping pins; SMBus interface not required for device control
- 3.3V tolerant SMBus interface works with legacy controllers
- Space saving 6 x 6 mm 48-VFQFPN; minimal board space
- Selectable SMBus addresses; multiple devices can easily share an SMBus segment

Block Diagram
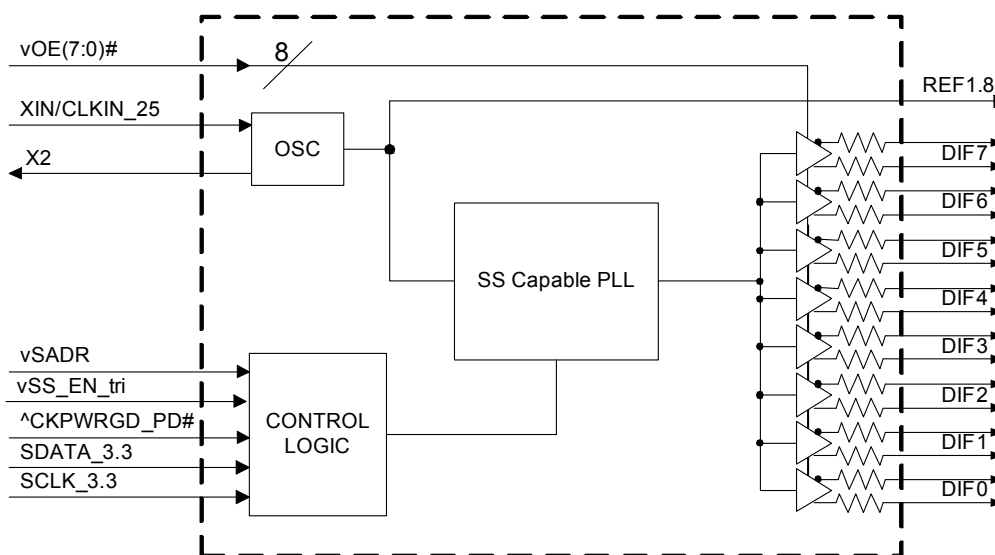
Pin Configuration
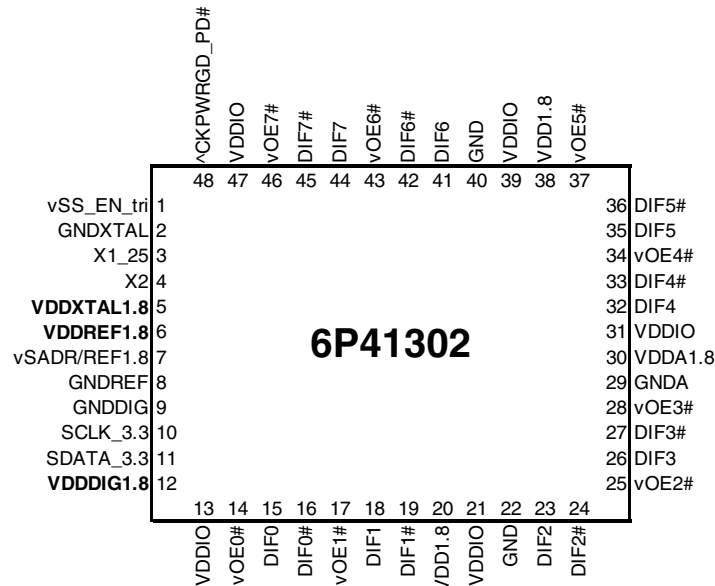
48-VFQFPN, 6 x 6 mm, 0.4mm pitch

vv prefix indicates internal 60kOhm pull-down resistor

v prefix indicates internal 120kOhm pull-down resistor

^ prefix indicates internal 120kOhm pull-up resistor

Pins 5, 6 and 12 are the Suspend voltage rails.

SMBus Address Selection Table

	SADR	Address	+ Read/Write Bit
State of SADR on first application	0	1101000	x
of CKPWRGD_PD#	1	1101010	x

Power Management Table

CKPWRGD_PD#	SMBus OE bit	DIFx			REF
		OEx#	True O/P	Comp. O/P	
0	X	X	Low	Low	Hi-Z[1]
1	1	0	Running	Running	Running
1	0	1	Low	Low	Low

1. REF is Hi-Z until the 1st assertion of CKPWRGD_PD# high. After this, when CKPWRG_PD# is low, REF is Low.

Power Connections

Pin Number			Description
VDD	VDDIO	GND	
5		2	XTAL OSC
6		8	REF Power
12		9	Digital (dirty) Power
20,38	13,21,31,39, 47	22,29,40	DIF outputs
30		29	PLL Analog

Pin Descriptions

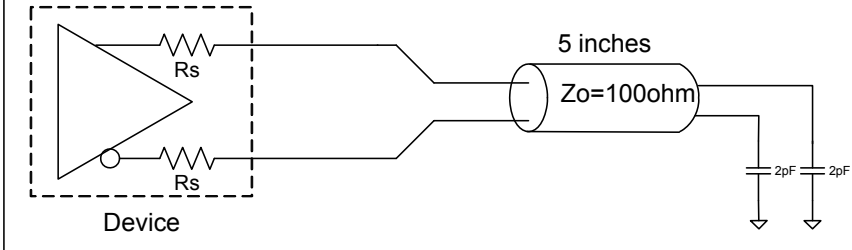| PIN #	PIN NAME	TYPE	DESCRIPTION
1	vSS_EN_tri	LATCHED IN	Latched select input to select spread spectrum amount at initial power up : 1 = -0.5% spread, M = -0.25%, 0 = Spread Off
2	GNDXTAL	GND	GND for XTAL
3	X1_25	IN	Crystal input, Nominally 25.00MHz.
4	X2	OUT	Crystal output.
5	VDDXTAL1.8	PWR	Power supply for XTAL, nominal 1.8V
6	VDDREF1.8	PWR	VDD for REF output. nominal 1.8V.
7	vSADR/REF1.8	LATCHED I/O	Latch to select SMBus Address/1.8V LVCMOS copy of X1/REFIN pin
8	GNDREF	GND	Ground pin for the REF outputs.
9	GNDDIG	GND	Ground pin for digital circuitry
10	SCLK_3.3	IN	Clock pin of SMBus circuitry, 3.3V tolerant.
11	SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
12	VDDDIG1.8	PWR	1.8V digital power (dirty power)
13	VDDIO	PWR	Power supply for differential outputs
14	vOE0#	IN	Active low input for enabling DIF pair 0. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
15	DIF0	OUT	Differential true clock output
16	DIF0#	OUT	Differential Complementary clock output
17	vOE1#	IN	Active low input for enabling DIF pair 1. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
18	DIF1	OUT	Differential true clock output
19	DIF1#	OUT	Differential Complementary clock output
20	VDD1.8	PWR	Power supply, nominal 1.8V
21	VDDIO	PWR	Power supply for differential outputs
22	GND	GND	Ground pin.
23	DIF2	OUT	Differential true clock output
24	DIF2#	OUT	Differential Complementary clock output
25	vOE2#	IN	Active low input for enabling DIF pair 2. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
26	DIF3	OUT	Differential true clock output
27	DIF3#	OUT	Differential Complementary clock output
28	vOE3#	IN	Active low input for enabling DIF pair 3. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
29	GNDA	GND	Ground pin for the PLL core.
30	VDDA1.8	PWR	1.8V power for the PLL core.
31	VDDIO	PWR	Power supply for differential outputs
32	DIF4	OUT	Differential true clock output
33	DIF4#	OUT	Differential Complementary clock output
34	vOE4#	IN	Active low input for enabling DIF pair 4. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
35	DIF5	OUT	Differential true clock output
36	DIF5#	OUT	Differential Complementary clock output
37	vOE5#	IN	Active low input for enabling DIF pair 5. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
38	VDD1.8	PWR	Power supply, nominal 1.8V
39	VDDIO	PWR	Power supply for differential outputs

Pin Descriptions (cont.)

PIN #	PIN NAME	TYPE	DESCRIPTION
40	GND	GND	Ground pin.
41	DIF6	OUT	Differential true clock output
42	DIF6#	OUT	Differential Complementary clock output
43	vOE6#	IN	Active low input for enabling DIF pair 6. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
44	DIF7	OUT	Differential true clock output
45	DIF7#	OUT	Differential Complementary clock output
46	vOE7#	IN	Active low input for enabling DIF pair 7. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
47	VDDIO	PWR	Power supply for differential outputs
48	^CKPWRGD_PD#	IN	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.

Test Loads

Low-Power HCSL Differential Output Test Load

5 inches

Rs

Rs

Zo=100ohm

Device

2pF 2pF

REF Output Test Load

Zo = 50 ohms

33

5pF

REF Output
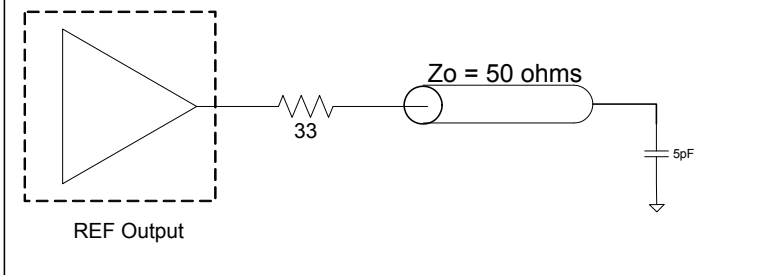
Alternate Terminations

Driving LVDS

3.3V

Rs

Cc

R7a

R7b

Rs

Cc

Zo

LVDS Clock
input

R8a

R8b

Device
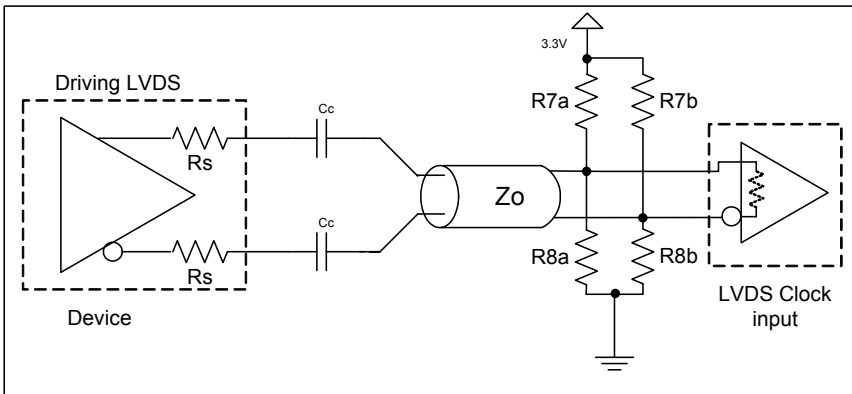
Driving LVDS inputs with the 6P41302

	Value		
	Receiver has	Receiver does not	
Component	termination	have termination	Note
R7a, R7b	10K ohm	140 ohm	
R8a, R8b	5.6K ohm	75 ohm	
Cc	0.1 uF	0.1 uF	
Vcm	1.2 volts	1.2 volts	

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 6P41302. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
1.8V Supply Voltage	VDDxx	Applies to VDD, VDDA and VDDIO	-0.5		2.5	V	1,2
Input Voltage	V_{IN}		-0.5		V_{DD}+0.5V	V	1, 3
Input High Voltage, SMBus	V_{IHSMB}	SMBus clock and data pins			3.6V	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 2.5V.

Electrical Characteristics–Current Consumption

TA = T_{AMB}; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	I_{DDAOP}	VDDA, All outputs active @100MHz		6	9	mA	
	I_{DDOP}	All VDD, except VDDA and VDDIO, All outputs active @100MHz		12	16	mA	
	I_{DDIOOP}	VDDIO, All outputs active @100MHz		28	35	mA	
Wake-on-LAN Current (CKPWRGD_PD# = '0' Byte 3, bit 5 = '1')	I_{DDAPD}	VDDA, DIF outputs off, REF output running		0.4	1	mA	2
	I_{DDPD}	All VDD, except VDDA and VDDIO, DIF outputs off, REF output running		5.3	8	mA	2
	I_{DDIOPD}	VDDIO, DIF outputs off, REF output running		0.04	0.1	mA	2
Powerdown Current (CKPWRGD_PD# = '0' Byte 3, bit 5 = '0')	I_{DDAPD}	VDDA, all outputs off		0.4	1	mA	
	I_{DDPD}	All VDD, except VDDA and VDDIO, all outputs off		0.6	1	mA	
	I_{DDIOPD}	VDDIO, all outputs off		0.0005	0.1	mA	

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] This is the current required to have the REF output running in Wake-on-LAN mode (Byte 3, bit 5 = 1)

Electrical Characteristics–DIF Output Duty Cycle, Jitter, and Skew Characteristics

TA = T_{AMB}; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Duty Cycle	t_{DC}	Measured differentially, PLL Mode	45	50	55	%	1,2
Skew, Output to Output	t_{sk3}	Averaging on, V_T = 50%		43	50	ps	1,2
Jitter, Cycle to cycle	$t_{jcyc-cyc}$			14	50	ps	1,2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

$T_A = T_{AMB}$; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DDxx}	Supply voltage for core, analog and single-ended LVCMOS outputs	1.7	1.8	1.9	V	
Output Supply Voltage	V_{DDIO}	Supply voltage for differential Low Power Outputs	0.9975	1.05-1.8	1.9	V	
Ambient Operating Temperature	T_{AMB}	Commercial range	0	25	70	°C	
		Industrial range	-40	25	85	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus	$0.75\,V_{DD}$		$V_{DD} + 0.3$	V	
Input Mid Voltage	V_{IM}	Single-ended tri-level inputs ('_tri' suffix)	$0.4\,V_{DD}$	$0.5\,V_{DD}$	$0.6\,V_{DD}$	V	
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus	-0.3		$0.25\,V_{DD}$	V	
Output High Voltage	V_{IH}	Single-ended outputs, except SMBus. I_{OH} = -2mA	V_{DD}-0.45			V	
Output Low Voltage	V_{IL}	Single-ended outputs, except SMBus. I_{OL} = -2mA			0.45	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA	
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA	
Input Frequency	F_{in}	XTAL, or X1 input	23	25	27	MHz	
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		0.6	1.8	ms	1,2
SS Modulation Frequency	f_{MOD}	Allowable Frequency (Triangular Modulation)	30	31.6	33	kHz	1
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	1	3	3	clocks	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion		20	300	us	1,3
Tfall	t_F	Fall time of single-ended control inputs			5	ns	2
Trise	t_R	Rise time of single-ended control inputs			5	ns	2
SMBus Input Low Voltage	V_{ILSMB}	V_{DDSMB} = 3.3V, see note 4 for $V_{DDSMB} < 3.3V$			0.6	V	
SMBus Input High Voltage	V_{IHSMB}	V_{DDSMB} = 3.3V, see note 5 for $V_{DDSMB} < 3.3V$	2.1		3.6	V	4
SMBus Output Low Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	
SMBus Sink Current	I_{PULLUP}	@ V_{OL}	4			mA	
Nominal Bus Voltage	V_{DDSMB}		1.7		3.6	V	
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15V) to (Min VIH + 0.15V)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15V) to (Max VIL - 0.15V)			300	ns	1
SMBus Operating Frequency	f_{MAXSMB}	Maximum SMBus operating frequency			400	kHz	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200 mV.

[4] For $V_{DDSMB} < 3.3V$, $V_{IHSMB} >= 0.65 \times V_{DDSMB}$.

Electrical Characteristics–DIF Low Power HCSL Outputs

TA = T$_{AMB;}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	Trf	Scope averaging on fast setting	1.6	2.3	3.5	V/ns	1,2,3
		Scope averaging on slow setting	1.3	1.9	2.9	V/ns	1,2,3
Slew rate matching	ΔTrf	Slew rate matching, Scope averaging on		7	20	%	1,2,4
Voltage High	V$_{HIGH}$	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660	784	850	mV	7
Voltage Low	V$_{LOW}$		-150	-33	150		7
Max Voltage	Vmax	Measurement on single ended signal using absolute value. (Scope averaging off)		816	1150	mV	7
Min Voltage	Vmin		-300	-42			7
Vswing	Vswing	Scope averaging off	300	1634		mV	1,2,7
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250	427	550	mV	1,5,7
Crossing Voltage (var)	Δ-Vcross	Scope averaging off		12	140	mV	1,6,7

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus amplitude settings.

Electrical Characteristics–Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures

T$_{AMB}$ = over the specified operating range. Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	Specification Limit	UNITS	NOTES
t$_{jphPCIeG1-CC}$	Phase Jitter, PLL Mode	PCIe Gen 1	21	25	35	86	ps (p-p)	1, 2, 3
t$_{jphPCIeG2-CC}$		PCIe Gen 2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5-16MHz, 8-16MHz, CDR = 5MHz)	0.9	0.9	1.1	3	ps (rms)	1, 2
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5-16MHz, 8-16MHz, CDR = 5MHz)	1.5	1.6	1.9	3.1	ps (rms)	1, 2
t$_{jphPCIeG3-CC}$		PCIe Gen 3 (PLL BW of 2-4MHz, 2-5MHz, CDR = 10MHz)	0.3	0.37	0.44	1	ps (rms)	1, 2
t$_{jphPCIeG4-CC}$		PCIe Gen 4 (PLL BW of 2-4MHz, 2-5MHz, CDR = 10MHz)	0.3	0.37	0.44	0.5	ps (rms)	1, 2

Notes on PCIe Filtered Phase Jitter Table

[1] Applies to all differential outputs, guaranteed by design and characterization.

[2] Calculated from Intel-supplied Clock Jitter Tool, with spread on and off.

[3] Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1^{-12}.

Electrical Characteristics–REF

TA = T$_{AMB;}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values		0		ppm	1,2
Clock period	T$_{period}$	25MHz output		40		ns	2
Rise/Fall Slew Rate	t$_{rf1}$	Byte 3 = 1F, 20% to 80% of VDDREF	0.6	1	1.6	V/ns	1
Rise/Fall Slew Rate	t$_{rf1}$	Byte 3 = 5F, 20% to 80% of VDDREF	0.9	1.4	2.2	V/ns	1,3
Rise/Fall Slew Rate	t$_{rf1}$	Byte 3 = 9F, 20% to 80% of VDDREF	1.1	1.7	2.7	V/ns	1
Rise/Fall Slew Rate	t$_{rf1}$	Byte 3 = DF, 20% to 80% of VDDREF	1.1	1.8	2.9	V/ns	1
Duty Cycle	d$_{t1X}$	V$_T$ = VDD/2 V	45	49.1	55	%	1,4
Duty Cycle Distortion	d$_{tcd}$	V$_T$ = VDD/2 V	0	2	4	%	1,5
Jitter, cycle to cycle	t$_{jcyc-cyc}$	V$_T$ = VDD/2 V		19.1	250	ps	1,4
Noise floor	t$_{jdBc1k}$	1kHz offset		-129.8	-105	dBc	1,4
Noise floor	t$_{jdBc10k}$	10kHz offset to Nyquist		-143.6	-115	dBc	1,4
Jitter, phase	t$_{jphREF}$	12kHz to 5MHz		0.63	1.5	ps (rms)	1,4

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is trimmed to 25.00MHz.

[3] Default SMBus value.

[4] When driven by a crystal.

[5] When driven by an external oscillator via the X1 pin, X2 should be floating.

Clock Periods–Differential Outputs with Spread Spectrum Disabled

SSC OFF	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
DIF	100.00	9.94900		9.99900	10.00000	10.00100		10.05100	ns	1,2

Clock Periods–Differential Outputs with Spread Spectrum Enabled

SSC ON	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
DIF	99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns	1,2

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is trimmed to 25.00 MHz

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if X$_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N			
			ACK
O		X Byte	
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Note: Read/Write address is latched on SADR pin.

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
			Beginning Byte N
ACK		X Byte	
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: Output Enable Register [1]

Byte 0	Name	Control Function	Type	0	1	Default
Bit 7	DIF OE7	Output Enable	RW	Low/Low	Enabled	1
Bit 6	DIF OE6	Output Enable	RW	Low/Low	Enabled	1
Bit 5	DIF OE5	Output Enable	RW	Low/Low	Enabled	1
Bit 4	DIF OE4	Output Enable	RW	Low/Low	Enabled	1
Bit 3	DIF OE3	Output Enable	RW	Low/Low	Enabled	1
Bit 2	DIF OE2	Output Enable	RW	Low/Low	Enabled	1
Bit 1	DIF OE1	Output Enable	RW	Low/Low	Enabled	1
Bit 0	DIF OE0	Output Enable	RW	Low/Low	Enabled	1

1. A low on these bits will override the OE# pin and force the differential output Low/Low

SMBus Table: SS Readback and Control Register

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	SSENRB1	SS Enable Readback Bit1	R	00' for SS_EN_tri = 0, '01' for SS_EN_tri		Latch
Bit 6	SSENRB1	SS Enable Readback Bit0	R	= 'M', '11 for SS_EN_tri = '1'		Latch
Bit 5	SSEN_SWCNTRL	Enable SW control of SS	RW	Values in B1[7:6] control SS amount	Values in B1[4:3] control SS amount.	0
Bit 4	SSENSW1	SS Enable Software Ctl Bit1	RW[1]	00' = SS Off, '01' = -0.25% SS,		0
Bit 3	SSENSW0	SS Enable Software Ctl Bit0	RW[1]	'10' = Reserved, '11'= -0.5% SS		0
Bit 2	Reserved					1
Bit 1	AMPLITUDE 1	Controls Output Amplitude	RW	00 = 0.6V	01 = 0.7V	1
Bit 0	AMPLITUDE 0		RW	10= 0.8V	11 = 0.9V	0

1. B1[5] must be set to a 1 for these bits to have any effect on the part.

SMBus Table: DIF Slew Rate Control Register

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7	SLEWRATESEL DIF7	Adjust Slew Rate of DIF7	RW	Slow Setting	Fast Setting	1
Bit 6	SLEWRATESEL DIF6	Adjust Slew Rate of DIF6	RW	Slow Setting	Fast Setting	1
Bit 5	SLEWRATESEL DIF5	Adjust Slew Rate of DIF5	RW	Slow Setting	Fast Setting	1
Bit 4	SLEWRATESEL DIF4	Adjust Slew Rate of DIF4	RW	Slow Setting	Fast Setting	1
Bit 3	SLEWRATESEL DIF3	Adjust Slew Rate of DIF3	RW	Slow Setting	Fast Setting	1
Bit 2	SLEWRATESEL DIF2	Adjust Slew Rate of DIF2	RW	Slow Setting	Fast Setting	1
Bit 1	SLEWRATESEL DIF1	Adjust Slew Rate of DIF1	RW	Slow Setting	Fast Setting	1
Bit 0	SLEWRATESEL DIF0	Adjust Slew Rate of DIF0	RW	Slow Setting	Fast Setting	1

SMBus Table: Nominal Vhigh Amplitude Control/ REF Control Register

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7	REF	Slew Rate Control	RW	00 = Slowest	01 = Slow	0
Bit 6			RW	10 = Fast	11 = Faster	1
Bit 5	REF Power Down Function	Wake-on-Lan Enable for REF	RW	REF does not run in Power Down	REF runs in Power Down	0
Bit 4	REF OE	REF Output Enable	RW	Low	Enabled	1
Bit 3	Reserved					1
Bit 2	Reserved					1
Bit 1	Reserved					1
Bit 0	Reserved					1

Byte 4 is Reserved

SMBus Table: Revision and Vendor ID Register

Byte 5	Name	Control Function	Type	0	1	Default
Bit 7	RID3		R			0
Bit 6	RID2	Revision ID	R	A rev = 0001		0
Bit 5	RID1		R			0
Bit 4	RID0		R			1
Bit 3	VID3		R			0
Bit 2	VID2	VENDOR ID	R	0001 = IDT		0
Bit 1	VID1		R			0
Bit 0	VID0		R			1

SMBus Table: Device Type/Device ID

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7	Device Type1	Device Type	R	00 = FGx, 01 = DBx ZDB/FOB,		0
Bit 6	Device Type0		R	10 = DMx, 11= DBx FOB		0
Bit 5	Device ID5		R			0
Bit 4	Device ID4		R			0
Bit 3	Device ID3		R			1
Bit 2	Device ID2	Device ID	R	001000 binary or 08 hex		0
Bit 1	Device ID1		R			0
Bit 0	Device ID0		R			0

SMBus Table: Byte Count Register

Byte 7	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	BC4		RW			0
Bit 3	BC3		RW	Writing to this register will configure how		1
Bit 2	BC2	Byte Count Programming	RW	many bytes will be read back, default is		0
Bit 1	BC1		RW	= 8 bytes.		0
Bit 0	BC0		RW			0

Recommended Crystal Characteristics (3225 package)

PARAMETER	VALUE	UNITS	NOTES
Frequency	25	MHz	1
Resonance Mode	Fundamental	-	1
Frequency Tolerance @ 25°C	±20	PPM Max	1
Frequency Stability, ref @ 25°C Over Operating Temperature Range	±20	PPM Max	1
Temperature Range (commercial)	0~70	°C	1
Temperature Range (industrial)	-40~85	°C	2
Equivalent Series Resistance (ESR)	50	Ω Max	1
Shunt Capacitance (C_O)	7	pF Max	1
Load Capacitance (C_L)	8	pF Max	1
Drive Level	0.3	mW Max	1
Aging per year	±5	PPM Max	1

Notes:

1. FOX 603-25-150.

2. For I-temp, FOX 603-25-261.

Thermal Characteristics

PARAMETER	SYMBOL	CONDITIONS	PKG	TYP.	UNITS	NOTES
Thermal Resistance	θ_{JC}	Junction to Case	NDG48	33	°C/W	1
	θ_{Jb}	Junction to Base		2.1	°C/W	1
	θ_{JA0}	Junction to Air, still air		37	°C/W	1
	θ_{JA1}	Junction to Air, 1 m/s air flow		30	°C/W	1
	θ_{JA3}	Junction to Air, 3 m/s air flow		27	°C/W	1
	θ_{JA5}	Junction to Air, 5 m/s air flow		26	°C/W	1

[1] ePad soldered to board

Marking Diagram

```
┌──────────────────┐
│                  │
│   IDT6P413       │
│   02NDGI         │
│   YYWW$          │
│                  │
│ ● LOT            │
└──────────────────┘
```
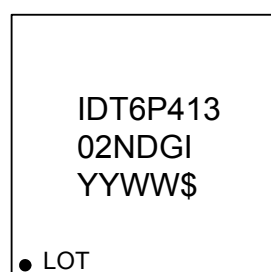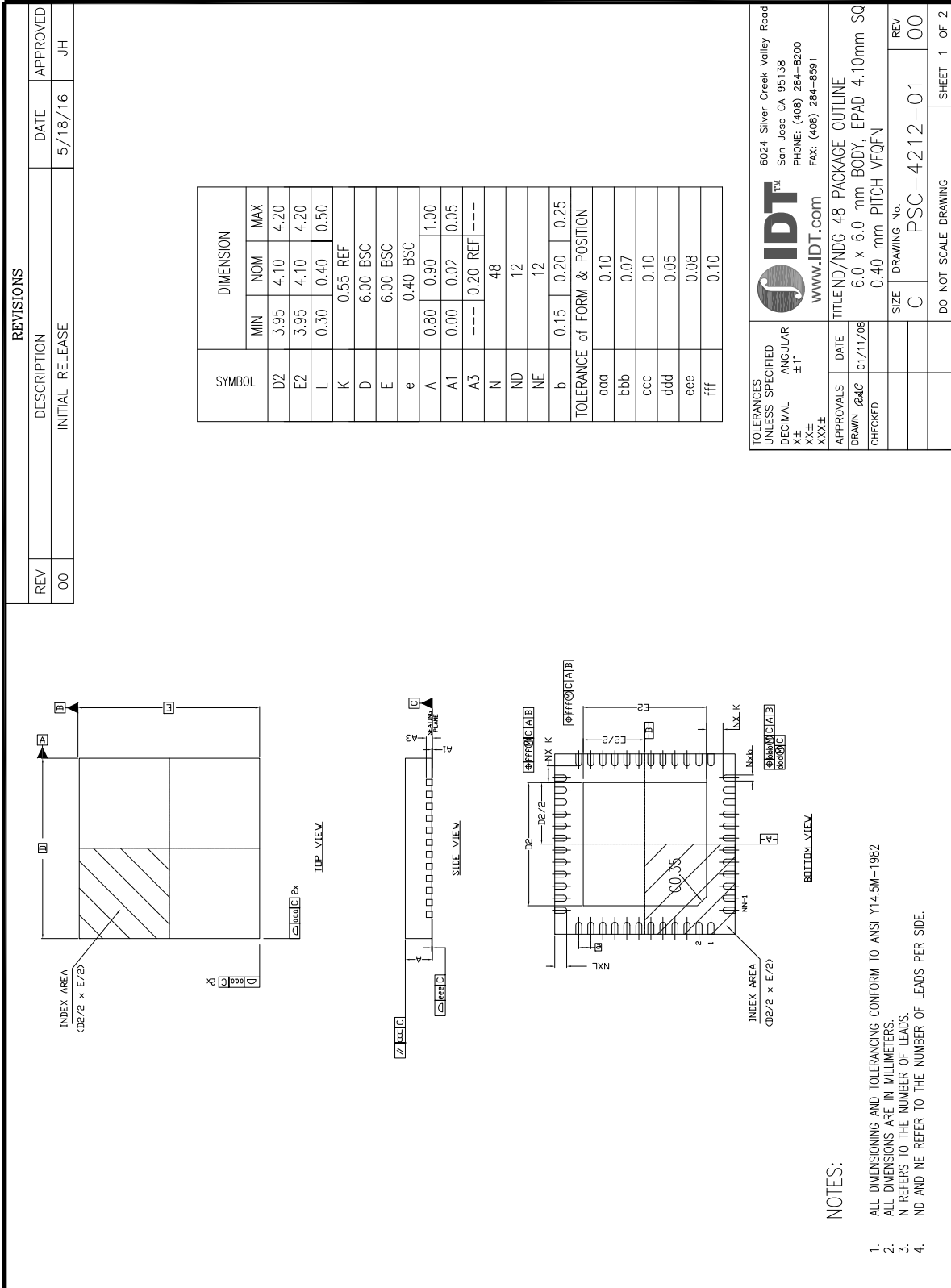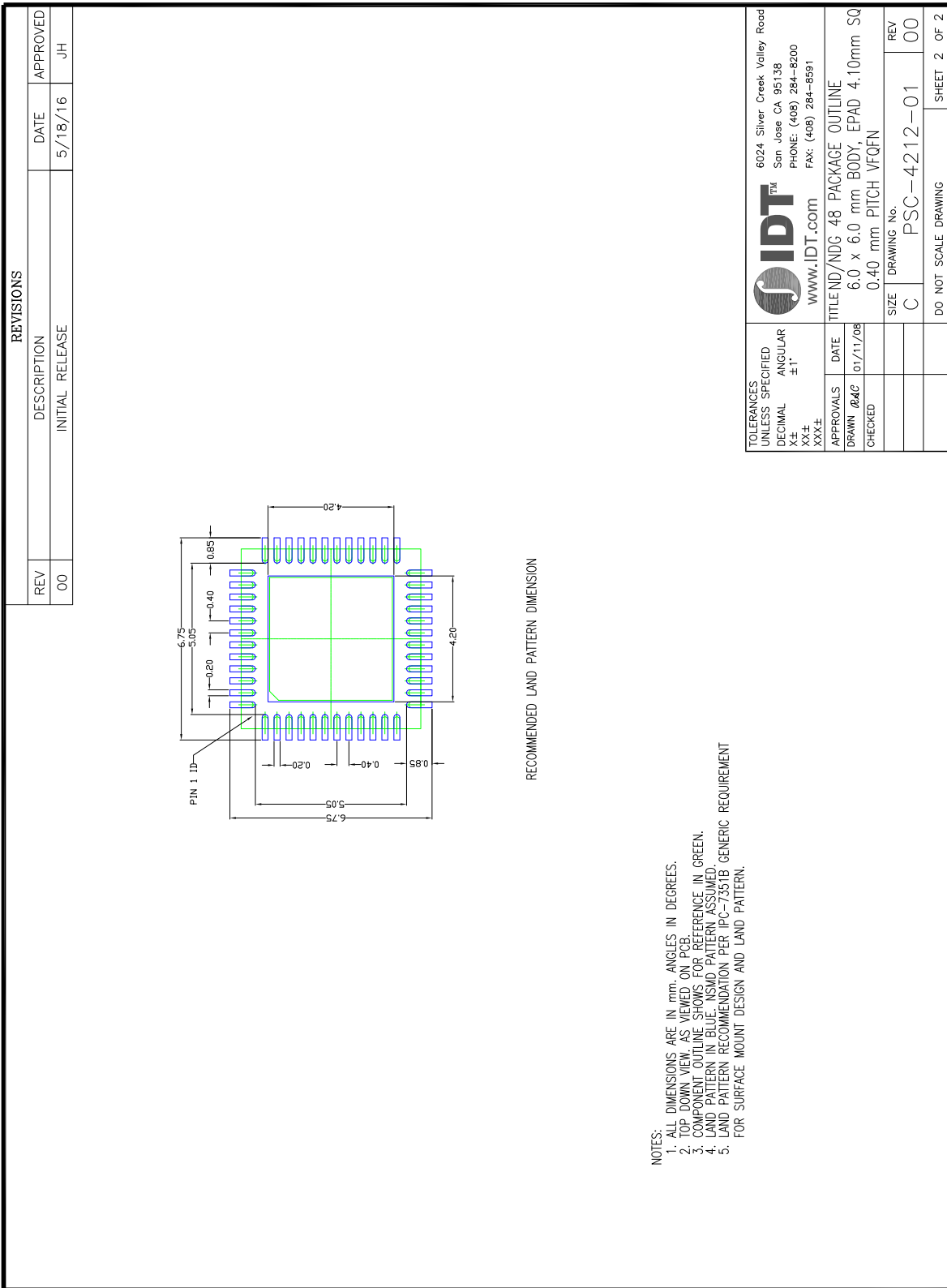
Notes:

2. 'G' denotes RoHS compliant package.

3. 'I' denotes industrial temperature grade.

3. '$' is the mark code.

4. 'YYWW' is the last two digits of the year and week that the part was assembled.

6. 'LOT' is the lot number.

Package Outline Drawings (NDG48P1)

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	5/18/16	JH

SYMBOL	DIMENSION		
	MIN	NOM	MAX
D2	3.95	4.10	4.20
E2	3.95	4.10	4.20
L	0.30	0.40	0.50
K	0.55 REF		
D	6.00 BSC		
E	6.00 BSC		
e	0.40 BSC		
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	---	0.20 REF	---
N	48		
ND	12		
NE	12		
b	0.15	0.20	0.25
TOLERANCE of FORM & POSITION			
aaa	0.10		
bbb	0.07		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
X±   ±1°
XX±
XXX±

APPROVALS	DATE
DRAWN RMC	01/11/08
CHECKED	

6024 Silver Creek Valley Road
San Jose CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-8591
www.IDT.com

TITLE ND/NDG 48 PACKAGE OUTLINE
6.0 x 6.0 mm BODY, EPAD 4.10mm SQ
0.40 mm PITCH VFQFN

SIZE C   DRAWING No. PSC-4212-01   REV 00

DO NOT SCALE DRAWING   SHEET 1 OF 2

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N REFERS TO THE NUMBER OF LEADS.
4. ND AND NE REFER TO THE NUMBER OF LEADS PER SIDE.

Package Outline Drawings (NDG48P1), cont.

RECOMMENDED LAND PATTERN DIMENSION

PIN 1 ID

4.20
0.85
6.75
5.05
0.40
0.20
4.20
0.85
0.40
0.20
5.05
6.75

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
OO	INITIAL RELEASE	5/18/16	JH

TOLERANCES
UNLESS SPECIFIED
DECIMAL ANGULAR
X± ±1°
XX±
XXX±

APPROVALS		DATE
DRAWN	BLC	01/11/08
CHECKED		

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TITLE: ND/NDG 48 PACKAGE OUTLINE
6.0 x 6.0 mm BODY, EPAD 4.10mm SQ
0.40 mm PITCH VFQFN

SIZE	DRAWING No.	REV
C	PSC-4212-01	OO

DO NOT SCALE DRAWING   SHEET 2 OF 2

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
6P41302NDGI	Trays	48-pin VFQFPN	-40 to +85° C
6P41302NDGI8	Tape and Reel	48-pin VFQFPN	-40 to +85° C

"G" after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Revision History

Issue Date	Description	Page #
2/22/2013	Initial release - final	
7/7/2014	1. Updated block diagram to latest format. 2. Removed red highlighting of certain VDD pins. 3. Updated IDD tables to break out Idd Suspend current. Total current did not change. 4. General description updated to latest standard. 5. Byte 6 b(7:6) description updated.	Various
9/29/2014	1. Updated front page text and block diagram. 2. Updated pin out to remove references to VDD Suspend pins. Using the part with collapsible power supplies did not save power and complicated board design. NO pins were changed. 3. Updated SMBus Descriptions 4. Simplified footnote 2 on PPM table. 5. Updated all electrical tables to latest format.	Various
1/24/2018	1. Corrected Byte 5 bit 4 to be '1' instead of '0'	12

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