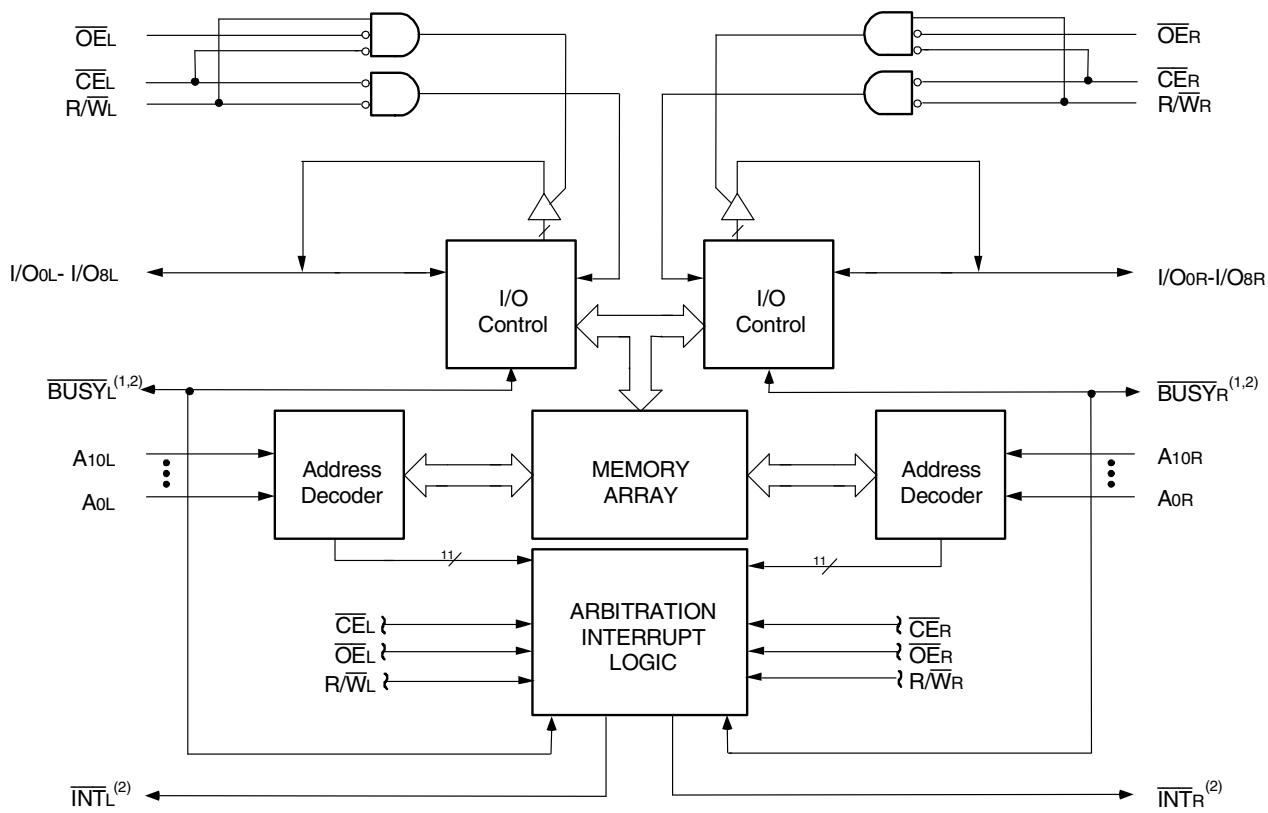


Features

- * High-speed access
 - Commercial: 25ns (max.)
- ♦ Low-power operation
 - IDT70121/70125L
 - Active: 675mW (typ.)
 - Standby: 1mW (typ.)
- ♦ MASTER IDT70121 easily expands data bus width to 18 bits or more using SLAVE IDT70125 chip
- ♦ Fully asynchronous operation from either port
- ♦ On-chip port arbitration logic (IDT70121 only)
- ♦ BUSY output flag on Master; BUSY input on Slave
- ♦ INT flag for port-to-port communication
- ♦ Battery backup operation—2V data retention
- ♦ TTL-compatible, signal 5V ($\pm 10\%$) power supply
- ♦ Available in 52-pin PLCC
- ♦ Green parts available, see ordering information

Functional Block Diagram



2654 drw 01

NOTES:

1. 70121 (MASTER): BUSY is non-tri-stated push-pull output.
70125 (SLAVE): BUSY is input.
2. INT is non-tri-stated push-pull output.

Description

The IDT70121/IDT70125 are high-speed 2K x 9 Dual-Port Static RAMs. The IDT70121 is designed to be used as a stand-alone 9-bit Dual-Port RAM or as a "MASTER" Dual-Port RAM together with the IDT70125 "SLAVE" Dual-Port in 18-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 18-bit-or-wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power-down

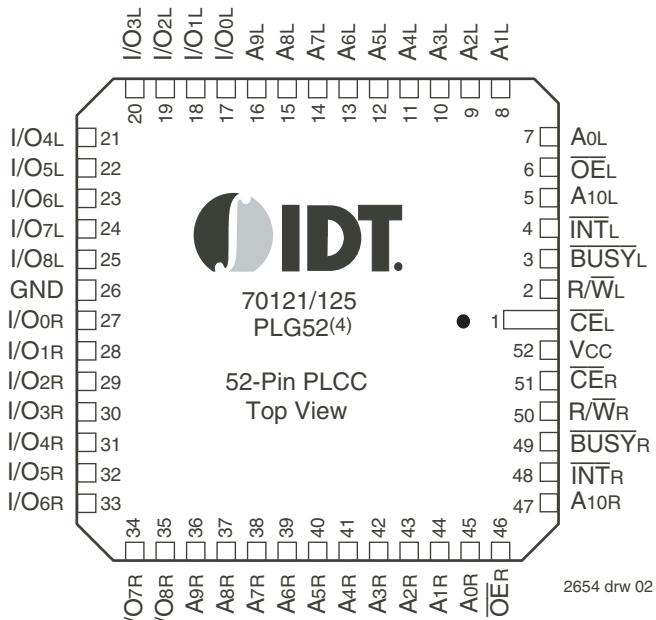
feature, controlled by \overline{CE} , permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT70121/IDT70125 utilizes a 9-bit wide data path to allow for Data/Control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using CMOS high-performance technology, these devices typically operate on only 675mW of power. Low-power (L) versions offer battery backup data retention capability with each port typically consuming 200 μ W from a 2V battery.

The IDT70121/IDT70125 devices are packaged in a 52-pin PLCC.

Pin Configurations^(1,2,3)



NOTES:

1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. Package body is approximately .75 in x .75 in x .17 in.
4. This package code is used to reference the package diagram.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	50	mA

2654 tbl 01

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VTERM must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to $\leq 20\text{mA}$ for the period of $VTERM \geq Vcc + 10\%$.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	6.0 ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

2654 tbl 03

NOTES:

- $V_{IL} \geq -1.5\text{V}$ for pulse width less than 10ns.
- VTERM must not exceed Vcc + 10%.

Capacitance ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter	Conditions ⁽¹⁾	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	9	pF
C _{OUT}	Output Capacitance	V _{OUT} = 3dV	10	pF

2654 tbl 04

NOTE:

- This parameter is determined by device characterization but is not production tested.

Maximum Operating Temperature and Supply Voltage⁽¹⁾

Grade	Ambient Temperature	GND	V _{CC}
Commercial	0°C to +70°C	0V	5.0V \pm 10%
Industrial	-40°C to +85°C	0V	5.0V \pm 10%

2654 tbl 02

NOTES:

- This is the parameter T_A . This is the "instant on" case temperature.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{CC} = 5.0\text{V} \pm 10\%$)

Symbol	Parameter	Test Conditions	70121S 70125S		70121L 70125L		Unit
			Min.	Max.	Min.	Max.	
I _U	Input Leakage Current ⁽¹⁾	V _{CC} = 5.5V, V _{IN} = 0V to V _{CC}	—	10	—	5	µA
I _O	Output Leakage Current	V _{CC} = 5.5V, $\overline{CE} = V_{IH}$, V _{OUT} = 0V to V _{CC}	—	10	—	5	µA
V _{OL}	Output Low Voltage	I _{OL} = +4mA	—	0.4	—	0.4	V
V _{OH}	Output High Voltage	I _{OH} = -4mA	2.4	—	2.4	—	V

2654 tbl 05

NOTE:

- At V_{CC} $\leq 2.0\text{V}$ leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range^(1,4) (VCC = 5V ± 10%)

Symbol	Parameter	Test Condition	Version	70121X25 70125X25 Com'l Only		70121X35 70125X35 Com'l & Ind		Unit
				Typ.	Max.	Typ.	Max.	
ICC	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = VIL$, Outputs Disabled $f = f_{MAX}^{(2)}$	COM'L	S L	135 135	260 220	135 135	250 210
			IND	S L	— —	— —	135 135	275 250
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}^A = \overline{CE}^B = VIH$ $f = f_{MAX}^{(2)}$	COM'L	S L	30 30	65 45	30 30	65 45
			IND	S L	— —	— —	30 30	80 65
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^A = VIL$ and $\overline{CE}^B = VIH^{(5)}$ Active Port Outputs Disabled, $f=f_{MAX}^{(2)}$	COM'L	S L	80 80	175 145	80 80	165 135
			IND	S L	— —	— —	80 80	190 165
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	$\overline{CE}^A = \overline{CE}^B \geq VCC - 0.2V$ $VIN \geq VCC - 0.2V$ or $VIN \leq 0.2V, f = 0^{(3)}$	COM'L	S L	1.0 0.2	15 5	1.0 0.2	15 5
			IND	S L	— —	— —	1.0 0.2	15 5
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^A \leq 0.2V$ and $\overline{CE}^B \geq VCC - 0.2V^{(5)}$ $VIN \geq VCC - 0.2V$ or $VIN \leq 0.2V$ Active Port Outputs Disabled, $f = f_{MAX}^{(2)}$	COM'L	S L	70 70	170 140	70 70	160 130
			IND	S L	— —	— —	70 70	185 160

2654 tbl 06a

Symbol	Parameter	Test Condition	Version	70121X55 70125X55 Com'l Only		Unit	
				Typ.	Max.		
ICC	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = VIL$, Outputs Disabled $f = f_{MAX}^{(2)}$	COM'L	S L	135 135	240 200	mA
			IND	S L	— —	— —	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}^A = \overline{CE}^B = VIH$ $f = f_{MAX}^{(2)}$	COM'L	S L	30 30	65 45	mA
			IND	S L	— —	— —	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^A = VIL$ and $\overline{CE}^B = VIH^{(5)}$ Active Port Outputs Disabled, $f=f_{MAX}^{(2)}$	COM'L	S L	80 80	155 125	mA
			IND	S L	— —	— —	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	$\overline{CE}^A = \overline{CE}^B \geq VCC - 0.2V$ $VIN \geq VCC - 0.2V$ or $VIN \leq 0.2V, f = 0^{(3)}$	COM'L	S L	1.0 0.2	15 5	mA
			IND	S L	— —	— —	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^A \leq 0.2V$ and $\overline{CE}^B \geq VCC - 0.2V^{(5)}$ $VIN \geq VCC - 0.2V$ or $VIN \leq 0.2V$ Active Port Outputs Disabled, $f = f_{MAX}^{(2)}$	COM'L	S L	70 70	150 120	mA
			IND	S L	— —	— —	

2654 tbl 06b

NOTES:

1. 'X' in part numbers indicates power rating (S or L).
2. At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of $1/t_{RC}$, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
3. $f = 0$ means no address or control lines change. Applies only to inputs at CMOS level standby.
4. $VCC=5V$, $TA=+25^\circ C$ for Typ, and is not production tested.
5. Port "A" may be either left or right port. Port "B" is opposite from port "A".

Data Retention Characteristics (L Version Only)

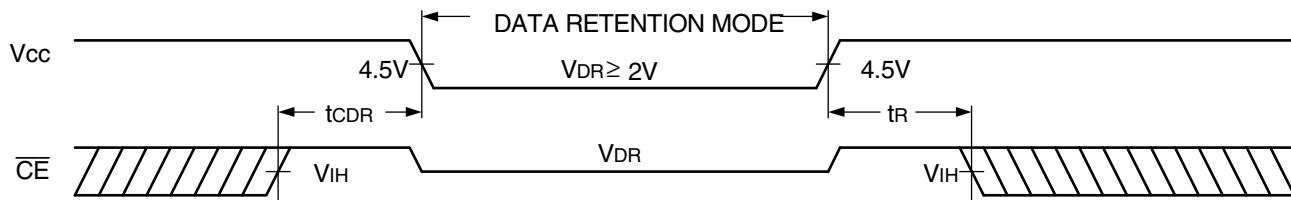
Symbol	Parameter	Test Condition	Min.	Typ. ⁽¹⁾	Max.	Unit	
V _{DR}	V _{CC} for Data Retention		2.0	—	—	V	
I _{CDR}	Data Retention Current	V _{CC} = 2V, $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2$	IND.	—	100	4000	μA
t _{CDR} ⁽³⁾	Chip Deselect to Data Retention Time		COM'L.	—	100	1500	
t _R ⁽³⁾	Operation Recovery Time		t _{RC} ⁽²⁾	—	—	V	

2654 tbl 07

NOTES:

1. V_{CC} = 2V, T_A = +25°C, and are not production tested.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but is not production tested.

Data Retention Waveform



2654 drw 03

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

2654 tbl 08

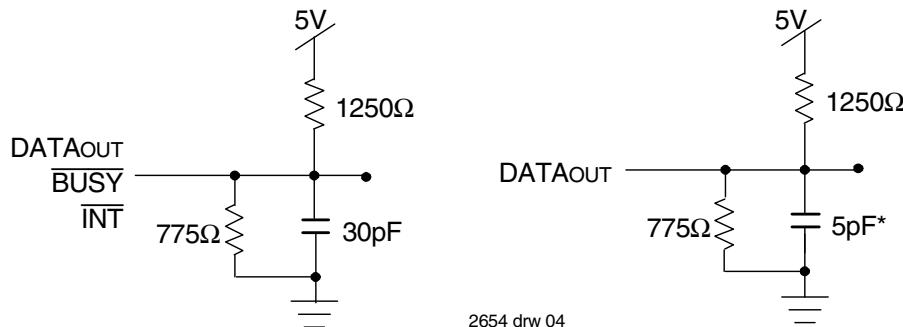


Figure 1. AC Output Test Load

Figure 2. Output Test Load

(For tLz, thz, twz, tow)

*Including scope and jig.

AC Electrical Characteristics Over the
Operating Temperature and Supply Voltage Range⁽³⁾

Symbol	Parameter	70121X25 70125X25 Com'l Only		70121X35 70125X35 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t _{RC}	Read Cycle Time	25	—	35	—	ns
t _{AA}	Address Access Time	—	25	—	35	ns
t _{ACE}	Chip Enable Access Time	—	25	—	35	ns
t _{AOE}	Output Enable Access Time	—	12	—	25	ns
t _{OH}	Output Hold from Address Change	0	—	0	—	ns
t _{LZ}	Output Low-Z Time ^(1,2)	0	—	0	—	ns
t _{HZ}	Output High-Z Time ^(1,2)	—	10	—	15	ns
t _{PU}	Chip Enable to Power Up Time ⁽²⁾	0	—	0	—	ns
t _{PD}	Chip Disable to Power Down Time ⁽²⁾	—	50	—	50	ns

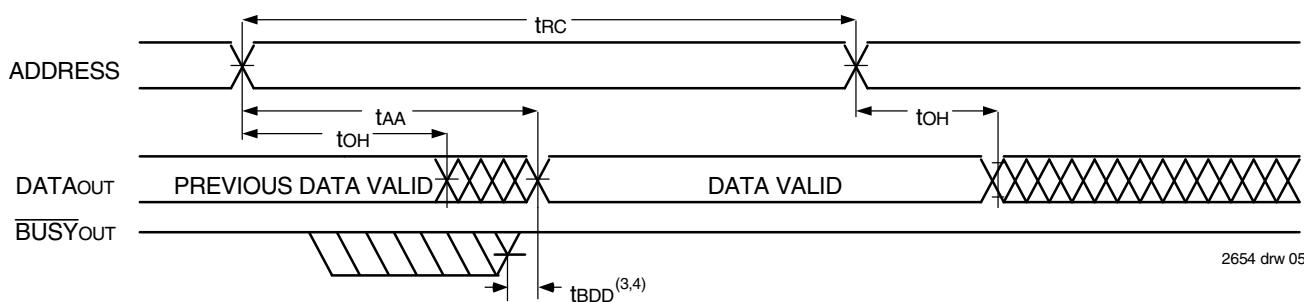
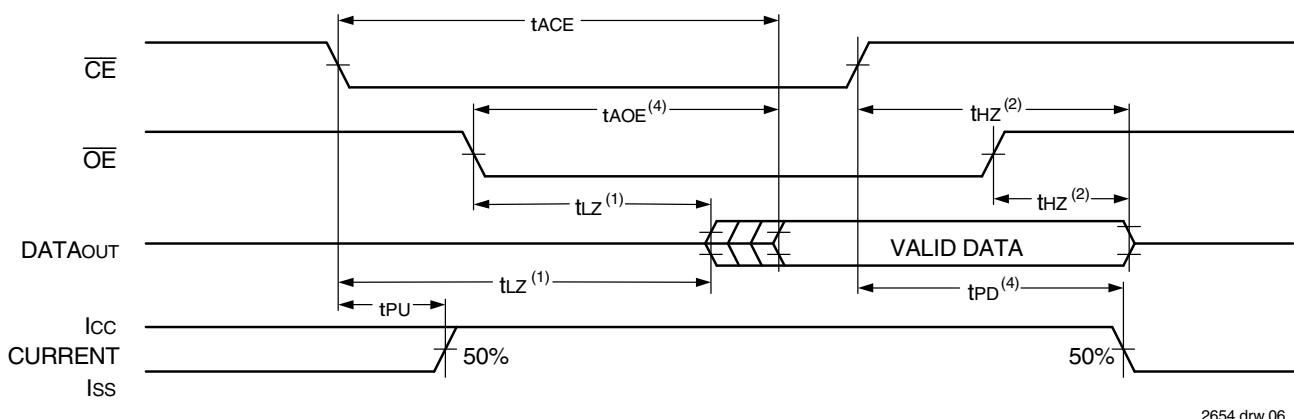
2654tbl09a

Symbol	Parameter	70121X55 70125X55 Com'l Only		Unit
		Min.	Max.	
READ CYCLE				
t _{RC}	Read Cycle Time	55	—	ns
t _{AA}	Address Access Time	—	55	ns
t _{ACE}	Chip Enable Access Time	—	55	ns
t _{AOE}	Output Enable Access Time	—	35	ns
t _{OH}	Output Hold from Address Change	0	—	ns
t _{LZ}	Output Low-Z Time ^(1,2)	0	—	ns
t _{HZ}	Output High-Z Time ^(1,2)	—	30	ns
t _{PU}	Chip Enable to Power Up Time ⁽²⁾	0	—	ns
t _{PD}	Chip Disable to Power Down Time ⁽²⁾	—	50	ns

2654tbl09b

NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter guaranteed by device characterization, but is not production tested.
3. 'X' in part numbers indicates power rating (S or L).

Timing Waveform of Read Cycle No. 1, Either Side^(1,2,4)Timing Waveform of Read Cycle No. 2, Either Side⁽⁵⁾

NOTES:

1. Timing depends on which signal is asserted last, \overline{OE} or \overline{CE} .
2. Timing depends on which signal is de-asserted first, \overline{OE} or \overline{CE} .
3. tBDD delay is required only in a case where the opposite port is completing a write operation to the same address location. For simultaneous read operations \overline{BUSY} has no relationship to valid output data.
4. Start of valid data depends on which timing becomes effective last, tAOE, tACE, tAA, or tBDD.
5. $R/W = V_{IH}$, $\overline{CE} = V_{IL}$, and $\overline{OE} = V_{IL}$, and the address is valid prior to other coincidental with \overline{CE} transition LOW.

AC Electrical Characteristics Over the
Operating Temperature and Supply Voltage Range⁽⁴⁾

Symbol	Parameter	70121X25 70125X25 Com'l Only		70121X35 70125X35 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE						
t _{WC}	Write Cycle Time ⁽⁴⁾	25	—	35	—	ns
t _{EW}	Chip Enable to End-of-Write	20	—	30	—	ns
t _{AW}	Address Valid to End-of-Write	20	—	30	—	ns
t _{AS}	Address Set-up Time	0	—	0	—	ns
t _{WP}	Write Pulse Width ⁽⁶⁾	20	—	30	—	ns
t _{WR}	Write Recovery Time	0	—	0	—	ns
t _{DW}	Data Valid to End-of-Write	12	—	20	—	ns
t _{HZ}	Output High-Z Time ^(1,2,3)	—	10	—	15	ns
t _{DH}	Data Hold Time ⁽⁵⁾	0	—	0	—	ns
t _{WZ}	Write Enable to Output in High-Z ^(1,3)	—	10	—	15	ns
t _{OW}	Output Active from End-of-Write ^(1,2,3,5)	0	—	0	—	ns

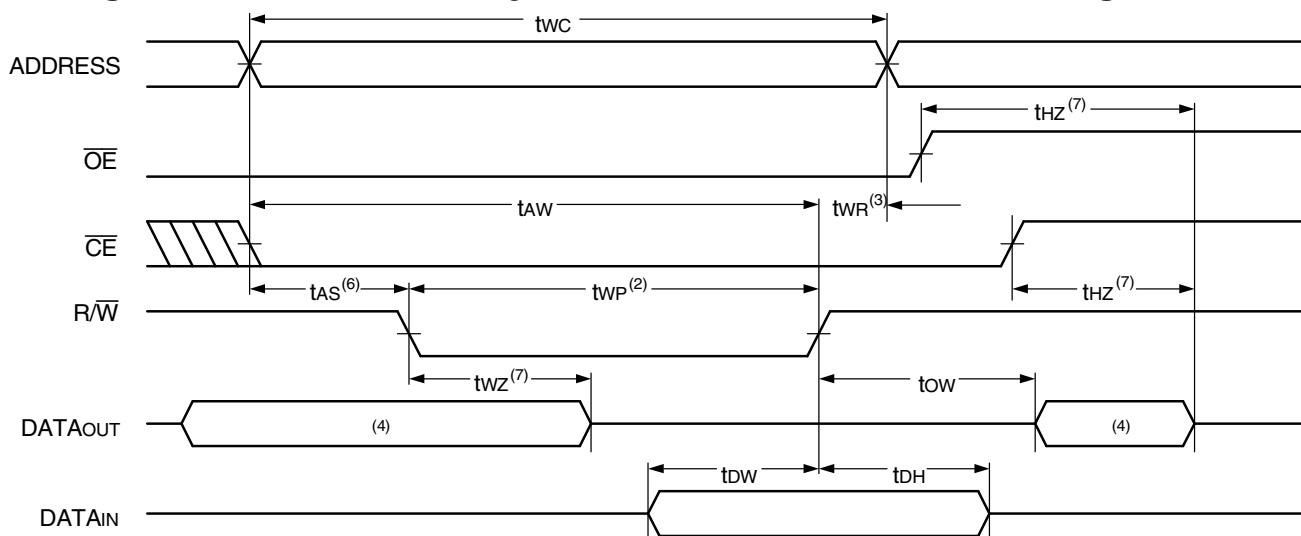
2654 tbl 10a

Symbol	Parameter	70121X55 70125X55 Com'l Only		Unit
		Min.	Max.	
WRITE CYCLE				
t _{WC}	Write Cycle Time ⁽⁴⁾	55	—	ns
t _{EW}	Chip Enable to End-of-Write	40	—	ns
t _{AW}	Address Valid to End-of-Write	40	—	ns
t _{AS}	Address Set-up Time	0	—	ns
t _{WP}	Write Pulse Width ⁽⁶⁾	40	—	ns
t _{WR}	Write Recovery Time	0	—	ns
t _{DW}	Data Valid to End-of-Write	20	—	ns
t _{HZ}	Output High-Z Time ^(1,2,3)	—	30	ns
t _{DH}	Data Hold Time ⁽⁵⁾	0	—	ns
t _{WZ}	Write Enable to Output in High-Z ^(1,3)	—	30	ns
t _{OW}	Output Active from End-of-Write ^(1,2,3,5)	0	—	ns

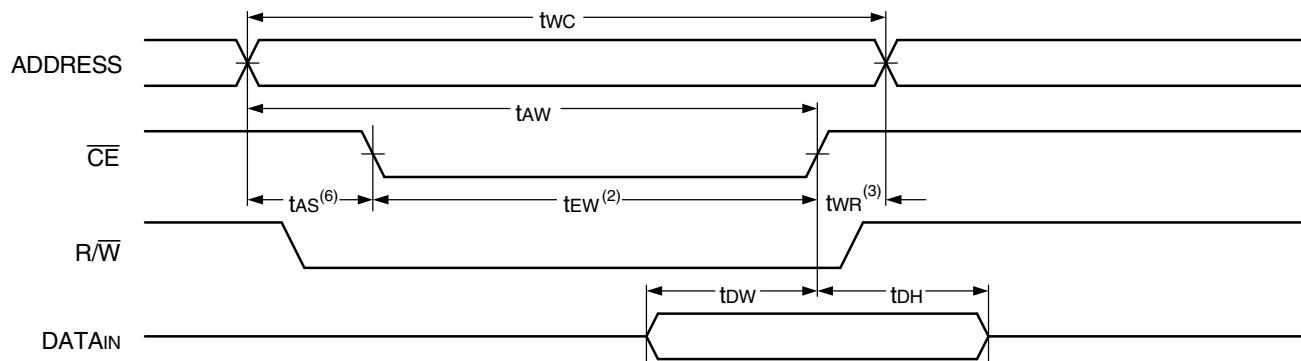
2654 tbl 10b

NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter guaranteed by device characterization, but is not production tested.
3. For MASTER/SLAVE combination, t_{WC} = t_{BAA} + t_{WP}, since R/W = V_{IL} must occur after t_{BAA}.
4. 'X' in part numbers indicates power rating (S or L).
5. The specified t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
6. If \overline{OE} is LOW during a R/W controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{OW}. If \overline{OE} is HIGH during a R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

Timing Waveform of Write Cycle No. 1, **R/W** Controlled Timing^(1,5,8)

2654 drw 07

Timing Waveform of Write Cycle No. 2, **CE** Controlled Timing^(1,5)

2654 drw 08

NOTES:

1. R/W or CE must be HIGH during all address transitions.
2. A write occurs during the overlap (tew or twp) of a CE = VIL and a R/W = VIL
3. tWR is measured from the earlier of CE or R/W going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the CE LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal (CE or R/W) is asserted last.
7. This parameter is determined by device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
8. If OE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of twp or (tew + tdw) to allow the I/O drivers to turn off data to be placed on the bus for the required tow. If OE is HIGH during a R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽⁶⁾

Symbol	Parameter	70121X25 70125X25 Com'l Only		70121X35 70125X35 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	
BUSY TIMING (For MASTER IDT70121)						
t _{BAA}	BUSY Access Time from Address	—	20	—	20	ns
t _{BDA}	BUSY Disable Time from Address	—	20	—	20	ns
t _{BAC}	BUSY Access Time from Chip Enable	—	20	—	20	ns
t _{BDC}	BUSY Disable Time from Chip Enable	—	20	—	20	ns
t _{WDD}	Write Pulse to Data Delay ⁽¹⁾		50		60	
t _{DDD}	Write Data Valid to Read Data Delay ⁽¹⁾		35		45	
t _{APS}	Arbitration Priority Set-up Time ⁽²⁾	5	—	5	—	ns
t _{BDD}	BUSY Disable to Valid Data ⁽³⁾	—	30	—	30	ns
t _{WH}	Write Hold After <u>BUSY</u> ⁽⁵⁾	15	—	20	—	ns
BUSY INPUT TIMING (For SLAVE IDT70125)						
t _{WB}	Write to <u>BUSY</u> Input ⁽⁴⁾	0	—	0	—	ns
t _{WH}	Write Hold After <u>BUSY</u> ⁽⁵⁾	15	—	20	—	ns
t _{WDD}	Write Pulse to Data Delay ⁽¹⁾	—	50	—	60	ns
t _{DDD}	Write Data Valid to Read Data Delay ⁽¹⁾	—	35	—	45	ns

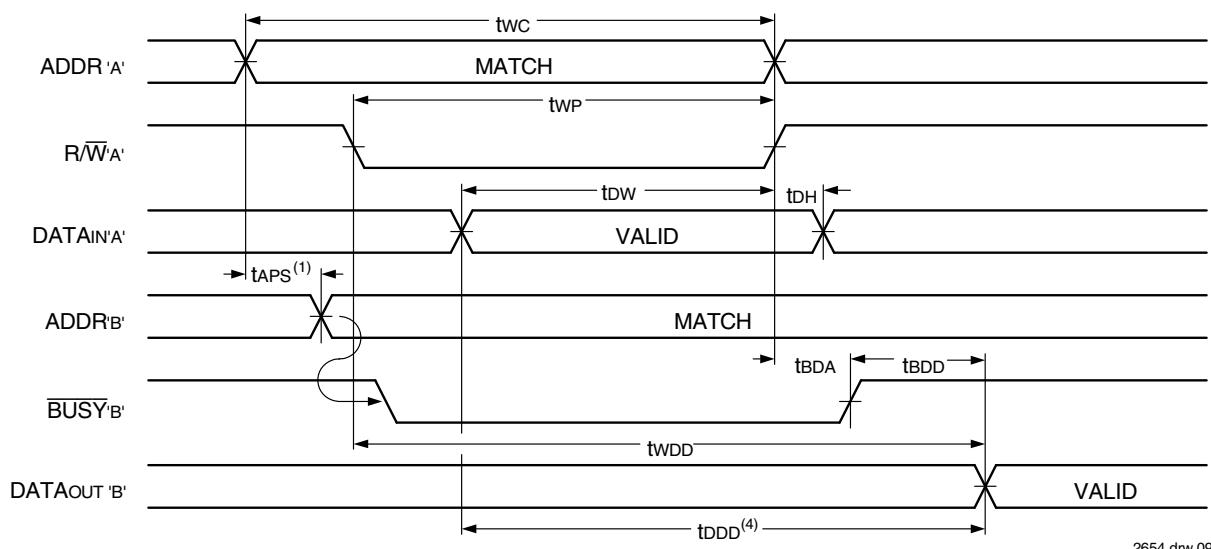
2654 tbl 11a

Symbol	Parameter	70121X55 70125X55 Com'l Only		Unit
		Min.	Max.	
BUSY TIMING (For MASTER IDT 70121)				
t _{BAA}	BUSY Access Time from Address	—	30	ns
t _{BDA}	BUSY Disable Time from Address	—	30	ns
t _{BAC}	BUSY Access Time from Chip Enable	—	30	ns
t _{BDC}	BUSY Disable Time from Chip Enable	—	30	ns
t _{WDD}	Write Pulse to Data Delay ⁽¹⁾		80	
t _{DDD}	Write Data Valid to Read Data Delay ⁽¹⁾		65	
t _{APS}	Arbitration Priority Set-up Time ⁽²⁾	5	—	ns
t _{BDD}	BUSY Disable to Valid Data ⁽³⁾	—	45	ns
t _{WH}	Write Hold After <u>BUSY</u> ⁽⁵⁾	20	—	ns
BUSY INPUT TIMING (For SLAVE IDT 70125)				
t _{WB}	Write to <u>BUSY</u> Input ⁽⁴⁾	0	—	ns
t _{WH}	Write Hold After <u>BUSY</u> ⁽⁵⁾	20	—	ns
t _{WDD}	Write Pulse to Data Delay ⁽¹⁾	—	80	ns
t _{DDD}	Write Data Valid to Read Data Delay ⁽¹⁾	—	65	ns

2654 tbl 11b

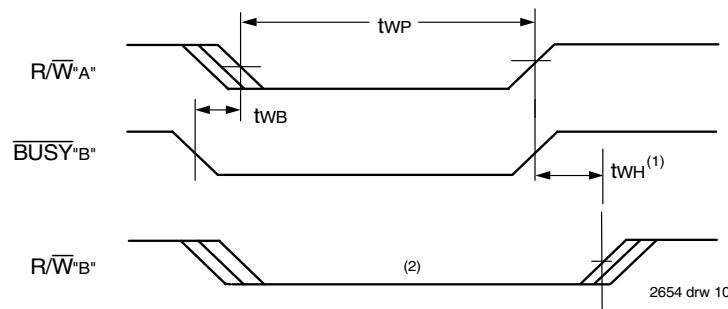
NOTES:

1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and BUSY".
2. To ensure that the earlier of the two ports wins.
3. t_{BDD} is a calculated parameter and is the greater of 0, t_{WDD} - t_{WP} (actual) or t_{DDD} - t_{DW} (actual).
4. To ensure that a write cycle is inhibited on port 'B' during contention on port 'A'..
5. To ensure that a write cycle is completed on port 'B' after contention on port 'A'.
6. 'X' in part numbers indicates power rating (S or L).

Timing Waveform of Write with Port-to-Port Read and **BUSY**^(1,2,3)

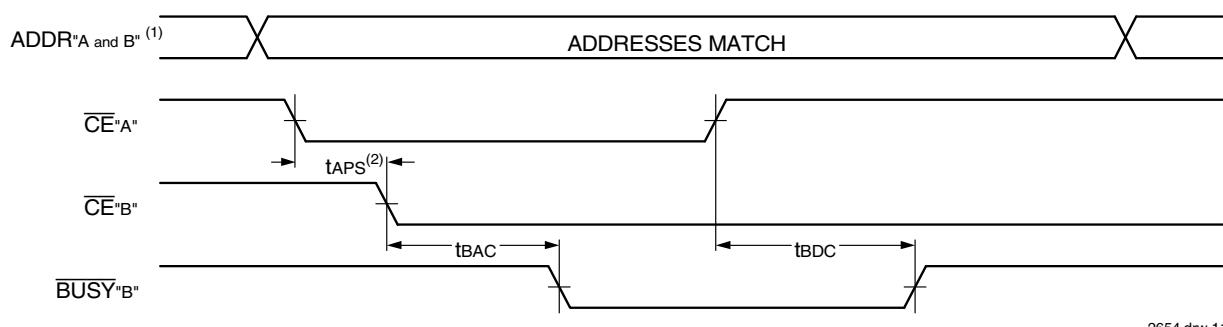
NOTES:

1. To ensure that the earlier of the two ports wins, tAPS is ignored for Slave (IDT70125).
2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
3. $OE = V_{IL}$ for the reading port.
4. All timing is the same for the left and right ports. Port "A" may be either the left or right port. Port "B" is opposite from port "A".

Timing Waveform of Write with **BUSY**⁽³⁾

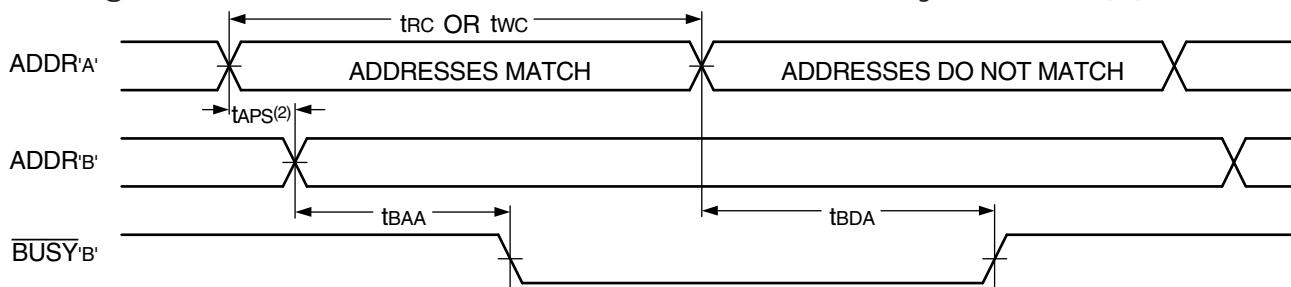
NOTES:

1. twh must be met for both **BUSY** input (slave) and output (master).
2. **BUSY** is asserted on port 'B' blocking R/W'B', until **BUSY**'B' goes HIGH.
3. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

Timing Waveform of **BUSY** Arbitration Controlled by **CE** Timing⁽¹⁾

NOTES:

1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. If tAPS is not satisfied, the **BUSY** will be asserted on one side or the other, but there is no guarantee on which side **BUSY** will be asserted (70121 only).

Timing Waveform of **BUSY** Arbitration Controlled by Address(1)

2654 drw 12

NOTES:

1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. If t_{APS} is not satisfied, the \overline{BUSY} will be asserted on one side or the other, but there is no guarantee on which side \overline{BUSY} will be asserted (70121 only).

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽¹⁾

Symbol	Parameter	70121X25 70125X25 Com'l Only		70121X35 70125X35 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	
INTERRUPT TIMING						
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	25	—	35	ns
t_{INR}	Interrupt Reset Time	—	25	—	35	ns

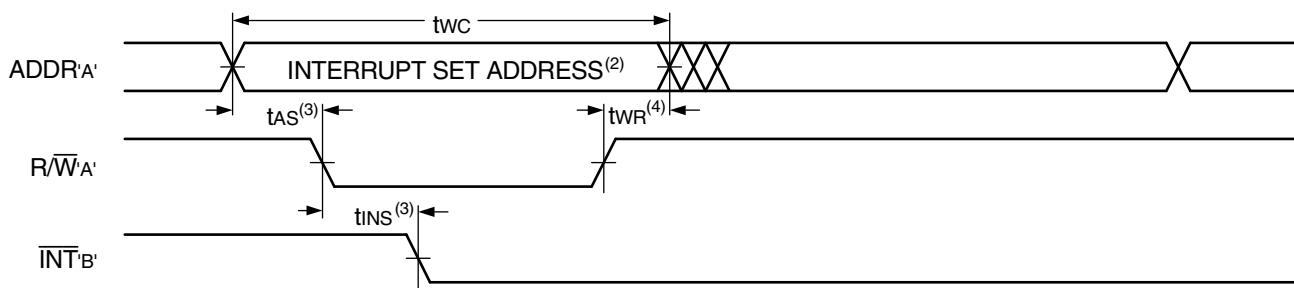
2654 tbl 12a

Symbol	Parameter	70121X55 70125X55 Com'l Only		Unit
		Min.	Max.	
INTERRUPT TIMING				
t_{AS}	Address Set-up Time	0	—	ns
t_{WR}	Write Recovery Time	0	—	ns
t_{INS}	Interrupt Set Time	—	45	ns
t_{INR}	Interrupt Reset Time	—	45	ns

2654 tbl 12b

NOTES:

1. 'X' in part numbers indicates power rating (S or L).

Timing Waveform of Interrupt Mode⁽¹⁾

2654 drw 13

NOTES:

1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. See Interrupt Truth Table.
3. Timing depends on which enable signal (\overline{CE} or $\overline{R/W}$) is asserted last.
4. Timing depends on which enable signal (\overline{CE} or $\overline{R/W}$) is de-asserted first.

Truth Tables

Truth Table I. Non-Contention Read/Write Control⁽⁴⁾

Left or Right Port ⁽¹⁾				Function
$\overline{R/W}$	\overline{CE}	\overline{OE}	D0-8	
X	H	X	Z	Port Disable and in Power-Down Mode, lsB2 or lsB4
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L = H$, Power-Down Mode, lsB1 or lsB3
L	L	X	DATAIN	Data on Port Written Into Memory ⁽²⁾
H	L	L	DATAout	Data in Memory Output on Port ⁽³⁾
H	L	H	Z	High-Impedance Outputs

2654 tbl 13

NOTES:

1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$.
2. If $\overline{BUSY} = L$, data is not written.
3. If $\overline{BUSY} = L$, data may not be valid, see twdd and tdd timing.
4. 'H' = V_{IH} , 'L' = V_{IL} , 'X' = DON'T CARE, 'Z' = HIGH IMPEDANCE

Truth Table II. Interrupt Flag^(1,4)

Left Port					Right Port					Function
$\overline{R/W}_L$	\overline{CE}_L	\overline{OE}_L	$A_{10L}-A_{0L}$	\overline{INT}_L	$\overline{R/W}_R$	\overline{CE}_R	\overline{OE}_R	$A_{10R}-A_{0R}$	\overline{INT}_R	
L	L	X	7FF	X	X	X	X	X	X	$L^{(2)}$ Set Right \overline{INT}_R Flag
X	X	X	X	X	X	L	L	7FF	H ⁽³⁾	Reset Right \overline{INT}_R Flag
X	X	X	X	$L^{(3)}$	L	L	X	7FE	X	Set Left \overline{INT}_L Flag
X	L	L	7FE	$H^{(2)}$	X	X	X	X	X	Reset Left \overline{INT}_L Flag

2654tbl 14

NOTES:

1. Assumes $\overline{BUSYL} = \overline{BUSYR} = V_{IH}$.
2. If $\overline{BUSYL} = V_{IL}$, then No Change.
3. If $\overline{BUSYR} = V_{IL}$, then No Change.
4. 'H' = HIGH, 'L' = LOW, 'X' = DON'T CARE

Functional Description

The IDT70121/125 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70121/125 has an automatic power down feature controlled by \overline{CE} . The \overline{CE} controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected (\overline{CE} HIGH). When a port is enabled, access to the entire memory array is permitted.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag (\overline{INTL}) is asserted when the right port writes to memory location 7FE (HEX), where a write is defined as the $\overline{CE} = R/W = VIL$ per Truth Table II. The left port clears the interrupt by access address location 7FE access when $\overline{CE}_R = \overline{OE}_R = VIL$, R/W is a "don't care". Likewise, the right port interrupt flag (\overline{INTR}) is asserted when the left port writes to memory location 7FF (HEX) and to clear the interrupt flag (\overline{INTR}), the right port must access the memory location 7FF. The message (9 bits) at 7FE or 7FF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 7FE and 7FF are not used as mail boxes, but as part of the random access memory. Refer to Table II for the interrupt operation.

Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The \overline{BUSY} pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a \overline{BUSY} indication, the write signal is gated internally to prevent the write from proceeding.

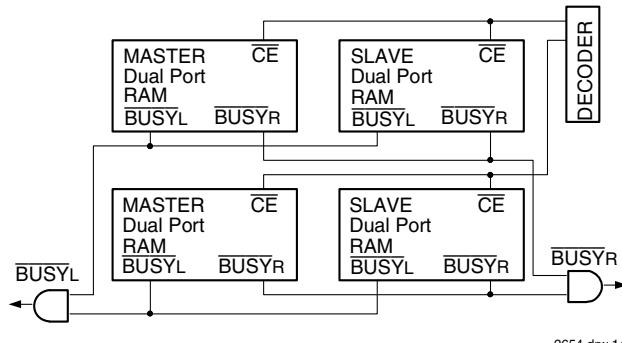
The use of \overline{BUSY} logic is not required or desirable for all applications. In some cases it may be useful to logically OR the \overline{BUSY} outputs together and use any \overline{BUSY} indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of \overline{BUSY} logic is not desirable, the \overline{BUSY} logic can be disabled by using the IDT70125 (SLAVE). In the IDT70125, the \overline{BUSY} pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the \overline{BUSY} pins HIGH. Once in slave mode the \overline{BUSY} pin operates solely as a write inhibit input pin. If desired, unintended write operations can be prevented to a port by tying the \overline{BUSY} pin for that port LOW.

The \overline{BUSY} outputs on the IDT70121/125 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the \overline{BUSY} indication for the resulting array requires the use of an external AND gate.

Width Expansion with Busy Logic Master/Slave Arrays

When expanding an IDT70121/125 RAM array in width while using \overline{BUSY} logic, one master part is used to decide which side of the RAM array will receive a \overline{BUSY} indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master use the \overline{BUSY} signal as a write inhibit signal. Thus on the IDT70121 RAM the \overline{BUSY} pin is an output of the part, and the \overline{BUSY} pin is an input of the IDT70125 as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating \overline{BUSY} on one side of the array and another master indicating \overline{BUSY} on one other side of the array. This would inhibit the write operations from one port for part of a word and



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Figure 3. Busy and chip enable routing for both width and depth expansion with 70121 (Master) and 70125 (Slave) RAMs.

inhibit the write operations from the other port for the other part of the word.

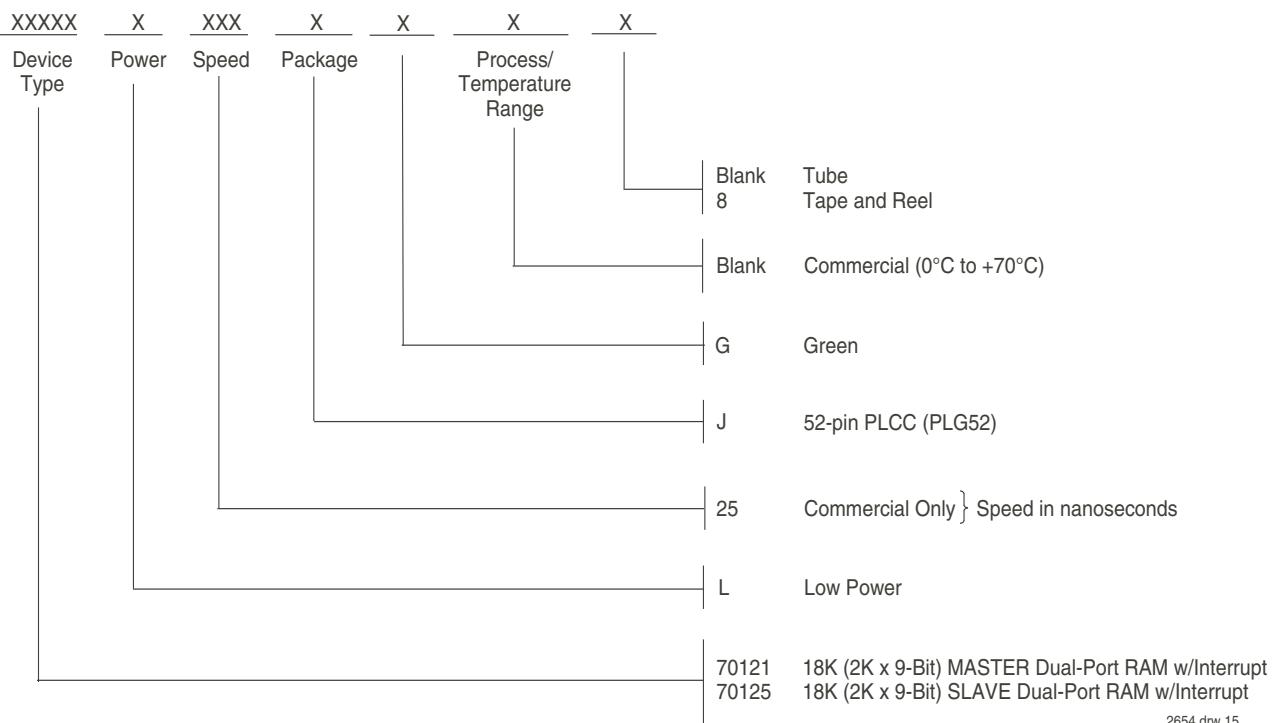
The \overline{BUSY} arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a \overline{BUSY} flag to be output from the master before the actual write pulse can be initiated with either the R/W signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

70121L/70125L

High-Speed 2K x 9 Dual-Port Static RAM with Busy & Interrupt

Commercial Temperature Range

Ordering Information



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NOTES:

LEAD FINISH (SnPb) parts are Obsolete. Product Discontinuation Notice - PDN# SP-17-02.

Note that information regarding recently obsoleted parts are included in this datasheet for customer convenience.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
25	70121L25JG	PLG52	PLCC	C
	70121L25JG8	PLG52	PLCC	C

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
25	70125L25JG	PLG52	PLCC	C
	70125L25JG8	PLG52	PLCC	C

Datasheet Document History

01/06/99:	Initiated datasheet document history Converted to new format Cosmetic and typographical corrections	
	Pages 2 and 3 Added additional notes to pin configurations Changed drawing format	
06/03/99:	Page 1 Corrected DSC number	
05/28/04:	Page 3 Changed storage temperature parameter from -55 to +125 to -65 to +150 Clarified TA parameter footnote	
	Page 4 DC Electrical parameters—changed test condition wording from "open" to "disabled"	
	Page 9 Changed ±500mV to 0mV in notes	
	Page 2 Added date revision for pin configuration	
	Page 4, 6, 8,10&12 Added Industrial temp to column headings for 35ns speed to DC and AC Electrical Characteristics	
	Page 4 Removed Industrial temp from 25, 45 & 55ns speeds from DC Electrical Characteristics	
	Page 3, 4, 6, 8,10&12 Removed Industrial temp footnote from all tables	
	Page 10 Corrected error in AC <u>BUSY</u> timing tables changing 71V33 to 70121 and changing 71V43 to 70125	
	Page 15 Added Industrial temp offering to 35ns ordering information	
	Page 1 & 15 Replaced old TM logo with new TM logo	
	Page 6 Footnote reference 5 removed from AC Electrical Characteristics READ table	
	Page 1 Changed wording of footnote 1 from " <u>INT</u> is totem-pole output" to " <u>INT</u> is non-tr-stated push-pull output"	
	Page 5 Updated AC Test Conditions Input Rise/Fall Times from 5ns to 3ns	
04/05/06:	Page 1 Added green availability to features	
	Page 15 Added green indicator to ordering information	
10/21/08:	Page 15 Removed "IDT" from orderable part number	
08/05/14:	Page 1 Added green availability to Features	
	Page 15 Added green indicator to Ordering Information	
	Page 2 &15 The package code for the J52-1 changed to J52 to match standard package code	
	Page 15 Added Tape and Reel to Ordering Information	
08/27/14:	Page 1 Removed 45ns commercial speed grade from Features High-speed access information	
	Page 1-16 Removed 45ns commercial speed grade throughout the datasheet to correct a discrepancy in IDT's product catalog	
	Page 4 Specifically including the DC Chars table	
	Page 6,8,10&12 Specifically including the AC Chars tables	
	Page 15 Removed 45ns commercial speed grade from the Ordering Information	
10/10/17:	Product Discontinuation Notice - PDN# SP-17-02 Last time buy expires June 15, 2018	
09/16/19:	Page 1 & 15 Deleted obsolete Commercial speed grades 35/55ns and Industrial speed grade 35ns	
	Page 2 Rotated PLG52 PLCC pin configuration to accurately reflect pin 1 orientation	
	Page 15 Added Orderable Part Information table	

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