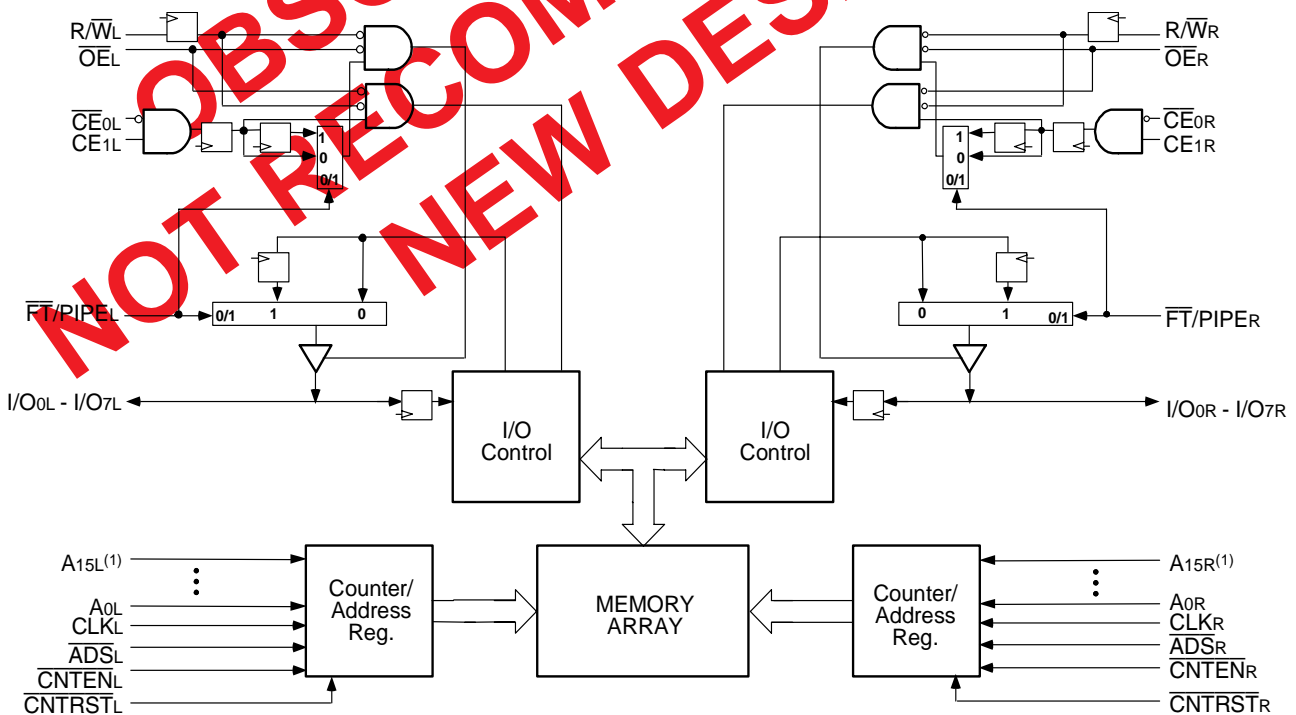


LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

Features:

- ◆ True Dual-Ported memory cells which allow simultaneous access of the same memory location
- ◆ High-speed clock to data access
 - Commercial: 9/12/15ns (max.)
 - Industrial: 12ns (max.)
- ◆ Low-power operation
 - IDT709089/79S
Active: 950mW (typ.)
Standby: 5mW (typ.)
 - IDT709089/79L
Active: 950mW (typ.)
Standby: 1mW (typ.)
- ◆ Flow-Through or Pipelined output mode on either port via the $\overline{\text{FT}}/\text{PIPE}$ pin
- ◆ Counter enable and reset features
- ◆ Dual chip enables allow for depth expansion without additional logic
- ◆ Full synchronous operation on both ports
 - 4ns setup to clock and 1ns hold on all control, data, and address inputs
 - Data input, address, and control registers
 - Fast 9ns clock to data out in the Pipelined output mode
 - Self-timed write allows fast cycle time
 - 15ns cycle time, 66.7MHz operation in the Pipelined output mode
- ◆ TTL-compatible, single 5V ($\pm 10\%$) power supply
- ◆ Industrial temperature range (-40°C to $+85^{\circ}\text{C}$) is available for selected speeds
- ◆ Available in 100-pin Thin Quad Flatpack (TQFP) package
- ◆ Green parts available, see ordering information

Functional Block Diagram



3242 drw 01

NOTE:

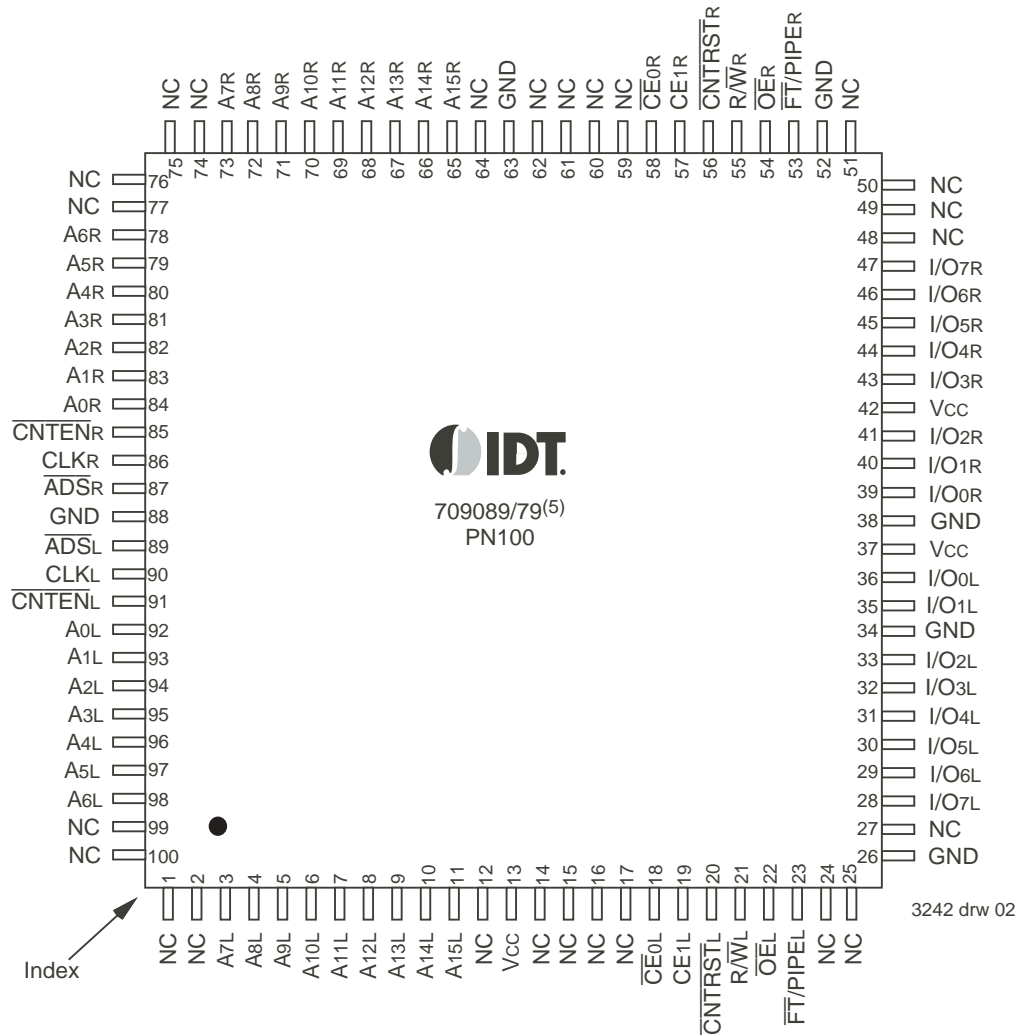
1. A15x is a NC for IDT709079.

Description:

The IDT709089/79 is a high-speed 64/32K x 8 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times.

With an input data register, the IDT709089/79 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{CE0}$ and $CE1$, permits the on-chip circuitry of each port to enter a very low standby power mode. Fabricated using CMOS high-performance technology, these devices typically operate on only 950mW of power.

Pin Configuration^(1,2,3)



NOTES:

1. A15x is a NC for IDT709079.
2. All Vcc pins must be connected to power supply.
3. All GND pins must be connected to ground supply.
4. Package body is approximately 14mm x 14mm x 1.4mm.
5. This package code is used to reference the package diagram.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}, CE_{1L}$	$\overline{CE}_{0R}, CE_{1R}$	Chip Enables
R/\overline{W}_L	R/\overline{W}_R	Read/Write Enable
\overline{OE}_L	\overline{OE}_R	Output Enable
$A_{0L} - A_{15L}^{(1)}$	$A_{0R} - A_{15R}^{(1)}$	Address
$I/O_{0L} - I/O_{7L}$	$I/O_{0R} - I/O_{7R}$	Data Input/Output
CLK_L	CLK_R	Clock
\overline{ADS}_L	\overline{ADS}_R	Address Strobe
\overline{CNTEN}_L	\overline{CNTEN}_R	Counter Enable
\overline{CNTRST}_L	\overline{CNTRST}_R	Counter Reset
$\overline{FT}/PIPE_L$	$\overline{FT}/PIPE_R$	Flow-Through/Pipeline
VCC		Power
GND		Ground

NOTE:

1. A15x is a NC for IDT709079.

3242 tbl 01

Truth Table I—
Read/Write and Enable Control^(1,2,3)

\overline{OE}	CLK	\overline{CE}_0	CE1	R/\overline{W}	I/O ₀₋₇	Mode
X	↑	H	X	X	High-Z	Deselected
X	↑	X	L	X	High-Z	Deselected
X	↑	L	H	L	D _{IN}	Write
L	↑	L	H	H	D _{OUT}	Read
H	X	L	H	X	High-Z	Outputs Disabled

3242 tbl 02

NOTES:

1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. \overline{ADS} , \overline{CNTEN} , \overline{CNTRST} = X.
3. \overline{OE} is an asynchronous input signal.

Truth Table II—Address Counter Control^(1,2)

External Address	Previous Internal Address	Internal Address Used	CLK	\overline{ADS}	\overline{CNTEN}	\overline{CNTRST}	I/O ⁽³⁾	MODE
A _n	X	A _n	↑	L ⁽⁴⁾	X	H	D _{I/O} (n)	External Address Used
X	A _n	A _n + 1	↑	H	L ⁽⁵⁾	H	D _{I/O} (n+1)	Counter Enabled—Internal Address generation
X	A _n + 1	A _n + 1	↑	H	H	H	D _{I/O} (n+1)	External Address Blocked—Counter disabled (A _n + 1 reused)
X	X	A ₀	↑	X	X	L ⁽⁴⁾	D _{I/O} (0)	Counter Reset to Address 0

5640 tbl 03

NOTES:

1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. \overline{CE}_0 and \overline{OE} = V_{IL}; CE₁ and R/\overline{W} = V_{IH}.
3. Outputs configured in Flow-Through Output mode; if outputs are in Pipelined mode the data out will be delayed by one cycle.
4. \overline{ADS} is independent of all other signals including \overline{CE}_0 and CE₁.
5. The address counter advances if \overline{CNTEN} = V_{IL} on the rising edge of CLK, regardless of all other signals including \overline{CE}_0 and CE₁.

Recommended Operating Temperature and Supply Voltage⁽¹⁾

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

3242 tbl 04

NOTES:

1. This is the parameter TA. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0 ⁽¹⁾	V
VIL	Input Low Voltage	-0.5 ⁽²⁾	—	0.8	V

3242 tbl 05

NOTES:

1. VTERM must not exceed Vcc + 10%.
2. VIL ≥ -1.5V for pulse width less than 10ns.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-65 to +150	°C
TJN	Junction Temperature	+150	°C
IOUT	DC Output Current	50	mA

3242 tbl 06

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 10%.
3. Ambient Temperature Under DC Bias. No AC Conditions. Chip Deselected.

Capacitance⁽¹⁾

(TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	9	pF
COU ⁽³⁾	Output Capacitance	VOU = 3dV	10	pF

3242 tbl 07

NOTES:

1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. COU also references CIO.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Vcc = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	709089/79S/L		Unit
			Min.	Max.	
II	Input Leakage Current ⁽¹⁾	Vcc = 5.5V, VIN = 0V to Vcc	—	10	μA
IO	Output Leakage Current	CE0 = VIH or CE1 = VIL, VOUT = 0V to Vcc	—	10	μA
VOL	Output Low Voltage	IOL = +4mA	—	0.4	V
VOH	Output High Voltage	IOH = -4mA	2.4	—	V

3242 tbl 08

NOTE:

1. At Vcc ≤ 2.0V input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽⁶⁾ (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Version	709089/79X9 Com'l Only		709089/79X12 Com'l & Ind		709089/79X15 Com'l Only		Unit	
				Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.		
I _{CC}	Dynamic Operating Current (Both Ports Active)	\overline{CE}_L and $\overline{CE}_R = V_{IL}$ Outputs Disabled $f = f_{MAX}^{(1)}$	COM'L	S	210	390	200	345	190	325	mA
				L	210	350	200	305	190	285	
I _{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L	S	50	135	50	110	50	110	mA
				L	50	115	50	90	50	90	
I _{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^*A = V_{IL}$ and $\overline{CE}^*B = V_{IH}^{(3)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	140	270	130	230	120	220	mA
				L	140	240	130	200	120	190	
I _{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports \overline{CE}_R and $\overline{CE}_L \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(2)}$	COM'L	S	1.0	15	1.0	15	1.0	15	mA
				L	0.2	5	0.2	5	0.2	5	
I _{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^*A < 0.2V$ and $\overline{CE}^*B \geq V_{CC} - 0.2V^{(5)}$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	130	245	120	205	110	195	mA
				L	130	225	120	185	110	175	
			IND	S	—	—	120	220	—	—	
				L	—	—	120	200	—	—	

3242 tbl 09

NOTES:

- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of $1/t_{CYC}$, using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$ means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{CC} = 5V$, $T_A = 25^\circ C$ for Typ, and are not production tested. $I_{CC DC}(f=0) = 150mA$ (Typ).
- $\overline{CE}_X = V_{IL}$ means $\overline{CE}_{0X} = V_{IL}$ and $CE_{1X} = V_{IH}$
 $\overline{CE}_X = V_{IH}$ means $\overline{CE}_{0X} = V_{IH}$ or $CE_{1X} = V_{IL}$
 $\overline{CE}_X \leq 0.2V$ means $\overline{CE}_{0X} \leq 0.2V$ and $CE_{1X} \geq V_{CC} - 0.2V$
 $\overline{CE}_X \geq V_{CC} - 0.2V$ means $\overline{CE}_{0X} \geq V_{CC} - 0.2V$ or $CE_{1X} \leq 0.2V$
 "X" represents "L" for left port or "R" for right port.
- 'X' in part numbers indicate power (S or L).

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1,2 and 3

3242 tbl 10

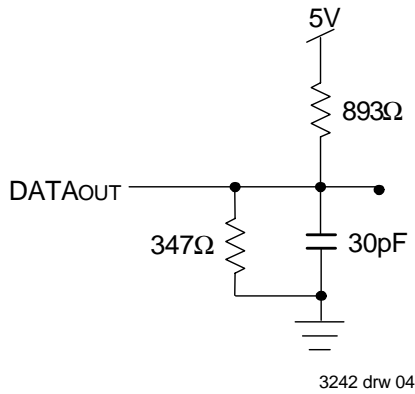


Figure 1. AC Output Test load.

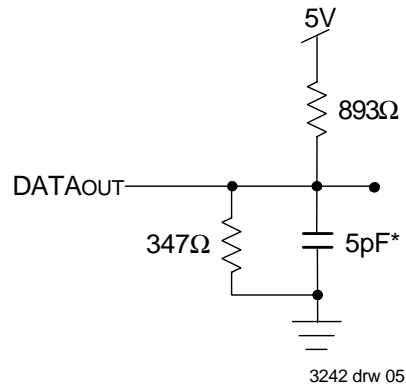


Figure 2. Output Test Load
(For tckLZ, tckHZ, toLZ, and toHZ).
*Including scope and jig.

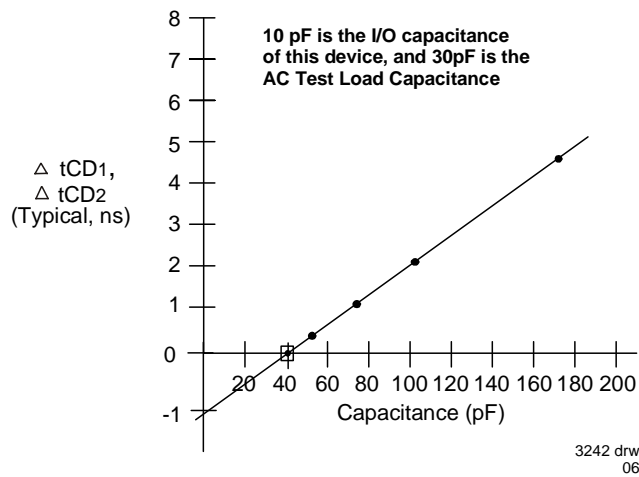


Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)^(3,4) ($V_{CC} = 5V \pm 10\%$)

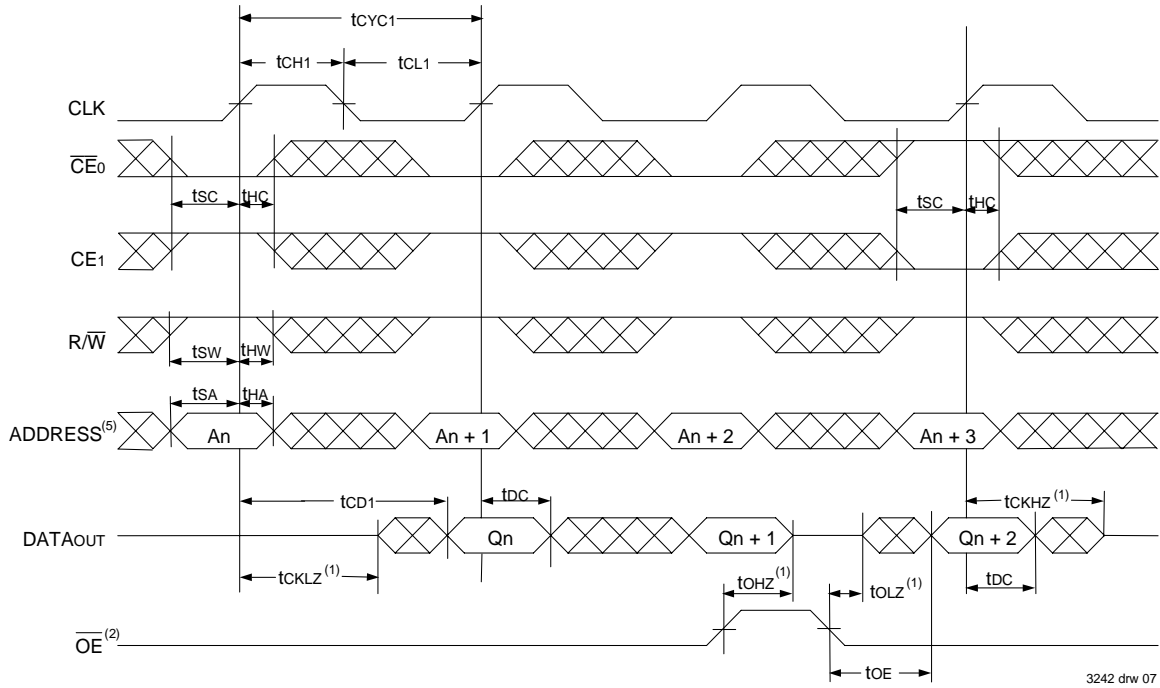
Symbol	Parameter	709089/79X9 Com'1 Only		709089/79X12 Com'1 & Ind		709089/79X15 Com'1 Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{CYC1}	Clock Cycle Time (Flow-Through) ⁽²⁾	25	—	30	—	35	—	ns
t _{CYC2}	Clock Cycle Time (Pipelined) ⁽²⁾	15	—	20	—	25	—	ns
t _{CH1}	Clock High Time (Flow-Through) ⁽²⁾	12	—	12	—	12	—	ns
t _{CL1}	Clock Low Time (Flow-Through) ⁽²⁾	12	—	12	—	12	—	ns
t _{CH2}	Clock High Time (Pipelined) ⁽²⁾	6	—	8	—	10	—	ns
t _{CL2}	Clock Low Time (Pipelined) ⁽²⁾	6	—	8	—	10	—	ns
t _R	Clock Rise Time	—	3	—	3	—	3	ns
t _F	Clock Fall Time	—	3	—	3	—	3	ns
t _{SA}	Address Setup Time	4	—	4	—	4	—	ns
t _{HA}	Address Hold Time	1	—	1	—	1	—	ns
t _{SC}	Chip Enable Setup Time	4	—	4	—	4	—	ns
t _{HC}	Chip Enable Hold Time	1	—	1	—	1	—	ns
t _{SW}	R/W Setup Time	4	—	4	—	4	—	ns
t _{HW}	R/W Hold Time	1	—	1	—	1	—	ns
t _{SD}	Input Data Setup Time	4	—	4	—	4	—	ns
t _{HD}	Input Data Hold Time	1	—	1	—	1	—	ns
t _{SAD}	\overline{ADS} Setup Time	4	—	4	—	4	—	ns
t _{HAD}	\overline{ADS} Hold Time	1	—	1	—	1	—	ns
t _{SCN}	\overline{CNTEN} Setup Time	4	—	4	—	4	—	ns
t _{HCN}	\overline{CNTEN} Hold Time	1	—	1	—	1	—	ns
t _{SRST}	\overline{CNRST} Setup Time	4	—	4	—	4	—	ns
t _{HRST}	\overline{CNRST} Hold Time	1	—	1	—	1	—	ns
t _{OE}	Output Enable to Data Valid	—	9	—	12	—	15	ns
t _{OLZ}	Output Enable to Output Low-Z ⁽¹⁾	2	—	2	—	2	—	ns
t _{OHZ}	Output Enable to Output High-Z ⁽¹⁾	1	7	1	7	1	7	ns
t _{CD1}	Clock to Data Valid (Flow-Through) ⁽²⁾	—	20	—	25	—	30	ns
t _{CD2}	Clock to Data Valid (Pipelined) ⁽²⁾	—	9	—	12	—	15	ns
t _{DC}	Data Output Hold After Clock High	2	—	2	—	2	—	ns
t _{CKHZ}	Clock High to Output High-Z ⁽¹⁾	2	9	2	9	2	9	ns
t _{CKLZ}	Clock High to Output Low-Z ⁽¹⁾	2	—	2	—	2	—	ns
Port-to-Port Delay								
t _{CWDD}	Write Port Clock High to Read Data Delay	—	35	—	40	—	50	ns
t _{CCS}	Clock-to-Clock Setup Time	—	15	—	15	—	20	ns

NOTES:

- Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
- The Pipelined output parameters (t_{CYC2}, t_{CD2}) apply to either or both left and right ports when $\overline{FT}/PIPE = V_{IH}$. Flow-through parameters (t_{CYC1}, t_{CD1}) apply when $\overline{FT}/PIPE = V_{IL}$ for that port.
- All input signals are synchronous with respect to the clock except for the asynchronous Output Enable (\overline{OE}) and $\overline{FT}/PIPE$. $\overline{FT}/PIPE$ should be treated as a DC signal, i.e. steady state during operation.
- 'X' in part number indicates power rating (S or L).

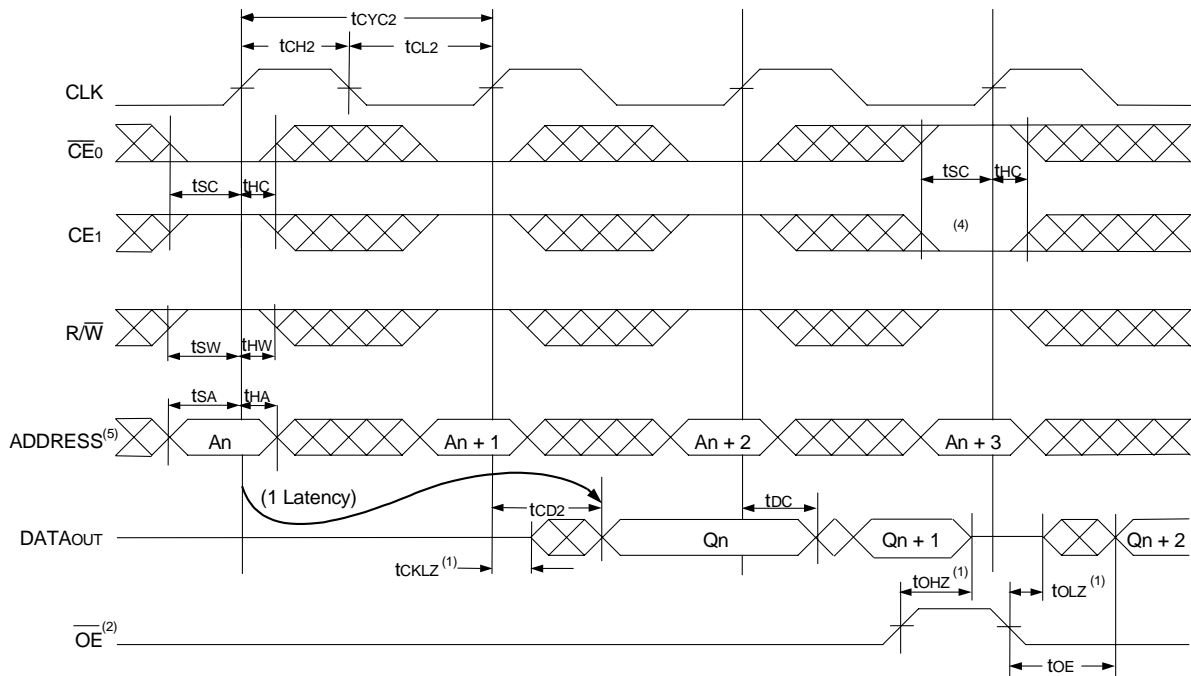
3242 tbl 11

Timing Waveform of Read Cycle for Flow-Through Output ($\overline{\text{FT}}/\text{PIPE} \text{ "X" } = \text{V}_{\text{IL}}$)^(3,6)



3242 drw 07

Timing Waveform of Read Cycle for Pipelined Output ($\overline{\text{FT}}/\text{PIPE} \text{ "X" } = \text{V}_{\text{IH}}$)^(3,6)

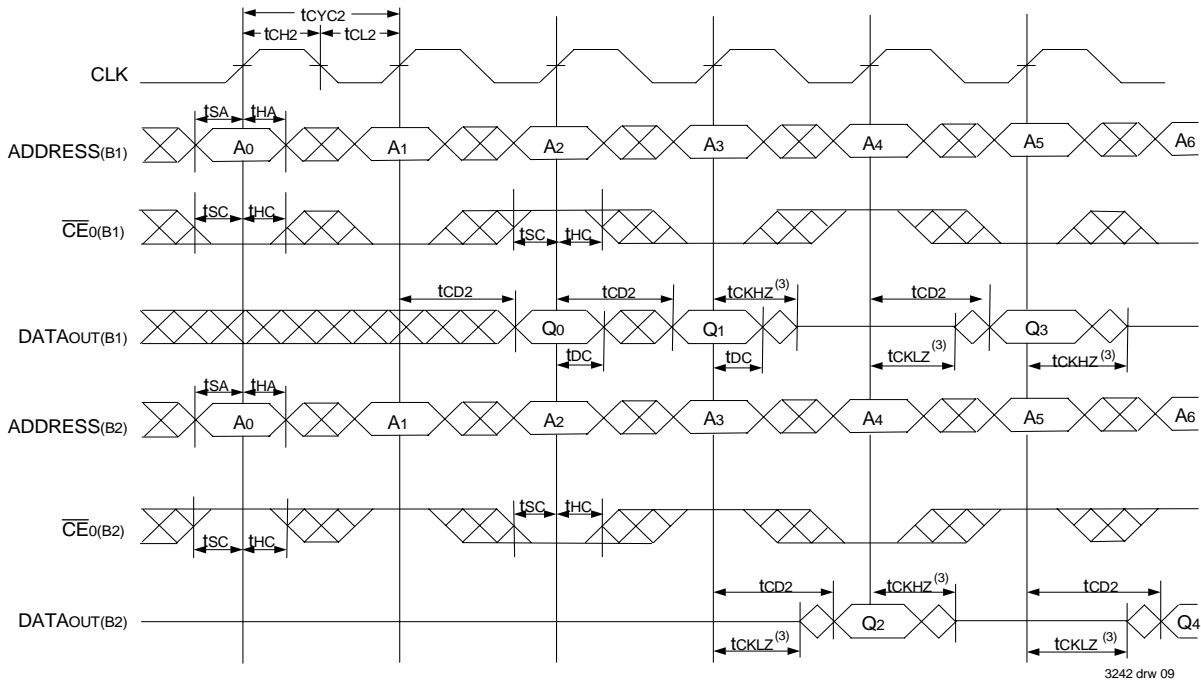


3242 drw 08

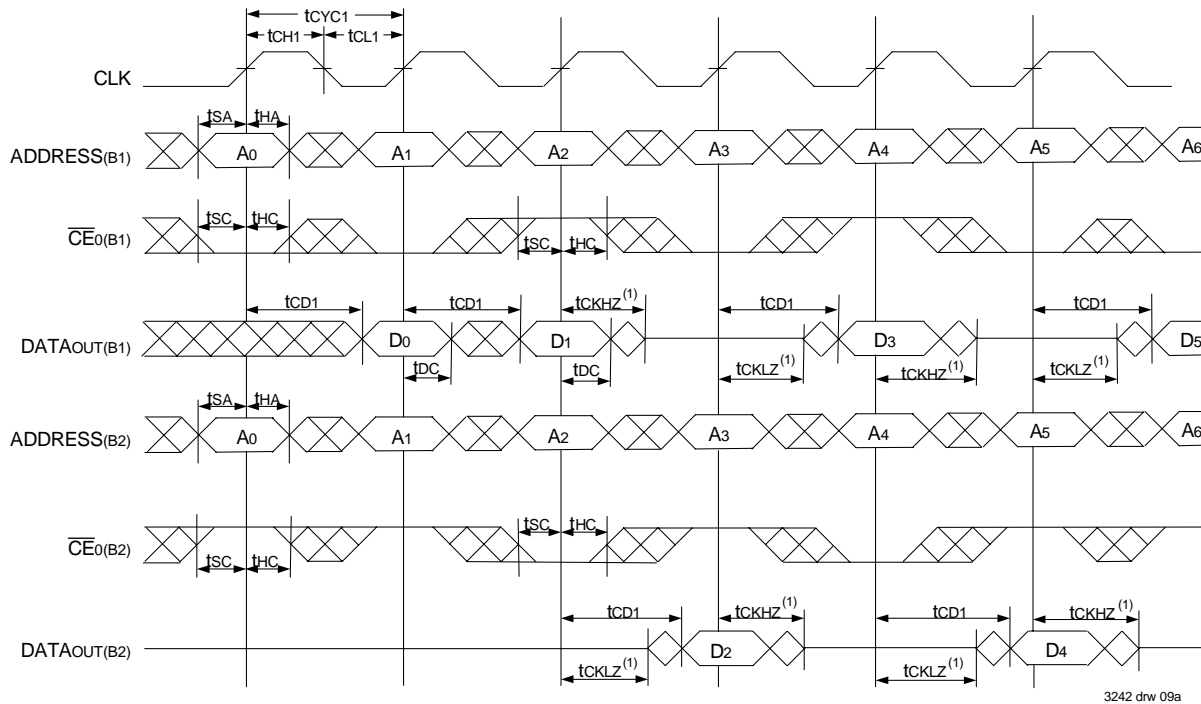
NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $\overline{\text{OE}}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
3. $\overline{\text{ADS}} = \text{V}_{\text{IL}}$ and $\overline{\text{CNTRST}} = \text{V}_{\text{IH}}$.
4. The output is disabled (High-Impedance state) by $\overline{\text{CE}}_0 = \text{V}_{\text{IH}}$ or $\text{CE}_1 = \text{V}_{\text{IL}}$ following the next rising edge of clock. Refer to Truth Table 1.
5. Addresses do not have to be accessed sequentially since $\overline{\text{ADS}} = \text{V}_{\text{IL}}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
6. "x" denotes Left or Right port. The diagram is with respect to that port.

Timing Waveform of a Bank Select Pipelined Read^(1,2)



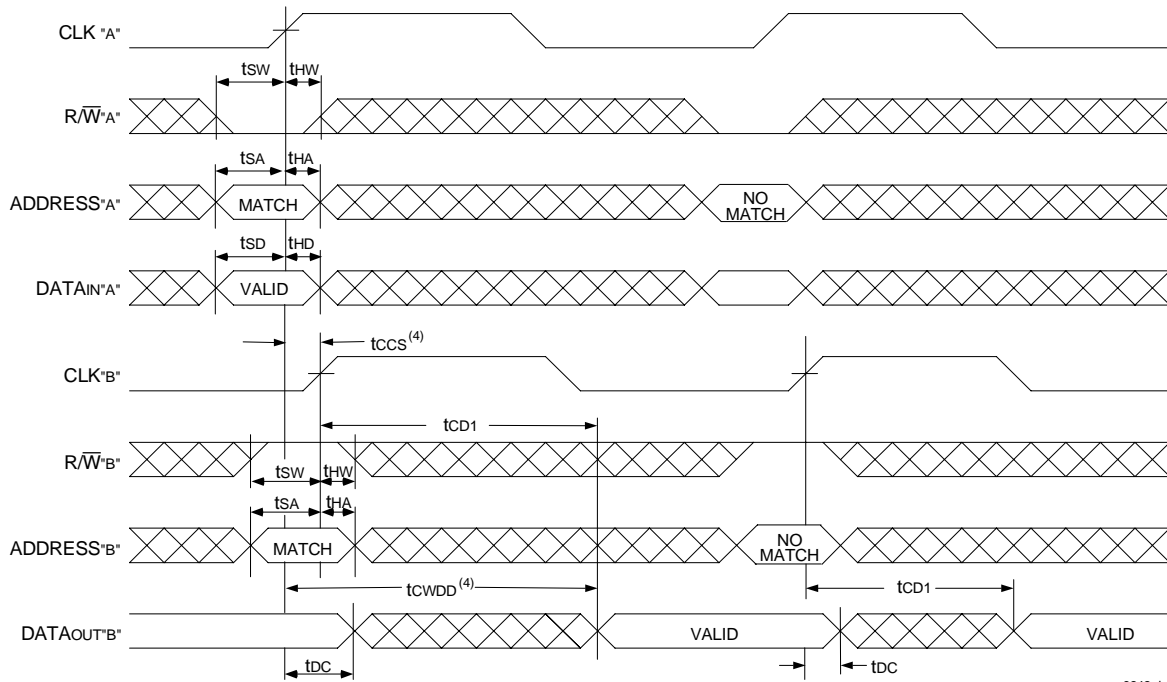
Timing Waveform of a Bank Select Flow-Through Read^(6,7)



NOTES:

1. B1 Represents Bank #1; B2 Represents Bank #2. Each Bank consists of one IDT709089/79 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. \overline{OE} and $\overline{ADS} = V_{IL}$; $CE_1(B1)$, $CE_1(B2)$, R/\overline{W} and $\overline{CNTRST} = V_{IH}$.
3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4. \overline{CE}_0 and $\overline{ADS} = V_{IL}$; CE_1 and $\overline{CNTRST} = V_{IH}$.
5. $\overline{OE} = V_{IL}$ for the Right Port, which is being read from. $\overline{OE} = V_{IH}$ for the Left Port, which is being written to.
6. If $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for tc_{WDD} .
If $t_{CCS} >$ maximum specified, then data from right port READ is not valid until $t_{CCS} + t_{CD1}$. tc_{WDD} does not apply in this case.
7. All timing is the same for both Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite of Port "A".

Timing Waveform with Port-to-Port Flow-Through Read^(1,2,3,5)

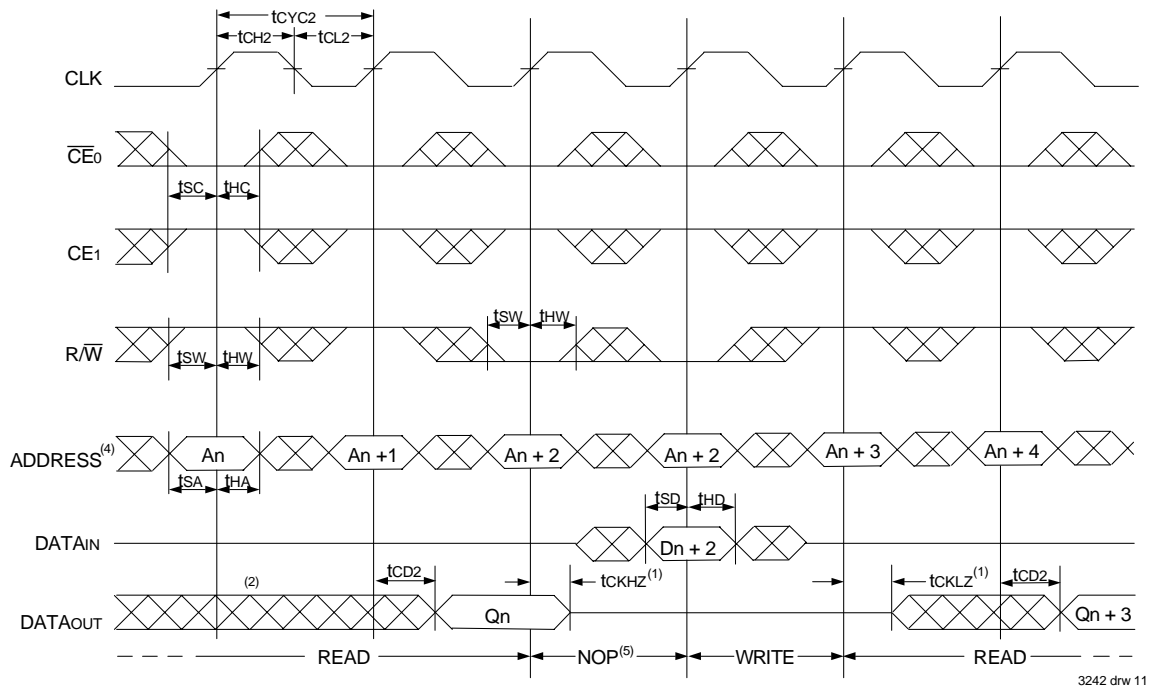


3242 drw 10

NOTES:

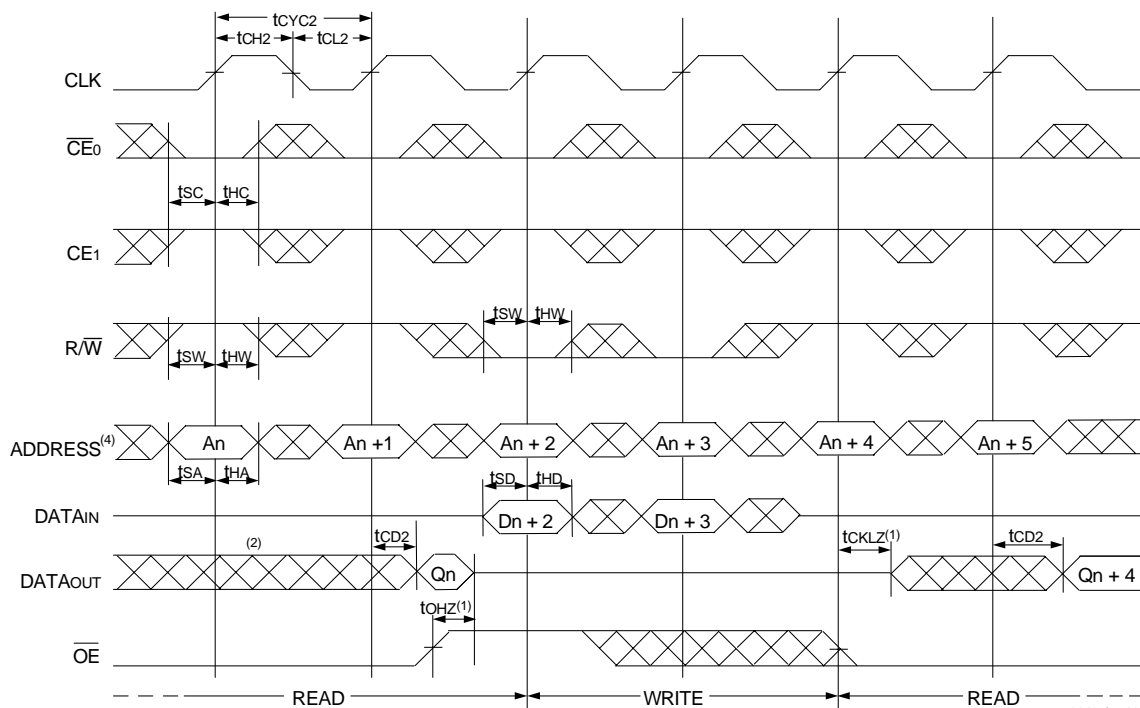
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. \overline{CE}_0 and $\overline{ADS} = V_{IL}$; CE_1 and $\overline{CNTRST} = V_{IH}$.
3. $\overline{OE} = V_{IL}$ for the Right Port, which is being read from. $\overline{OE} = V_{IH}$ for the Left Port, which is being written to.
4. If $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWD} .
If $t_{CCS} >$ maximum specified, then data from right port READ is not valid until $t_{CCS} + t_{CD1}$. t_{CWD} does not apply in this case.
5. All timing is the same for both Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite of Port "A".

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽³⁾



3242 drw 11

Timing Waveform of Pipelined Read-to-Write-to-Read (\overline{OE} Controlled)⁽³⁾

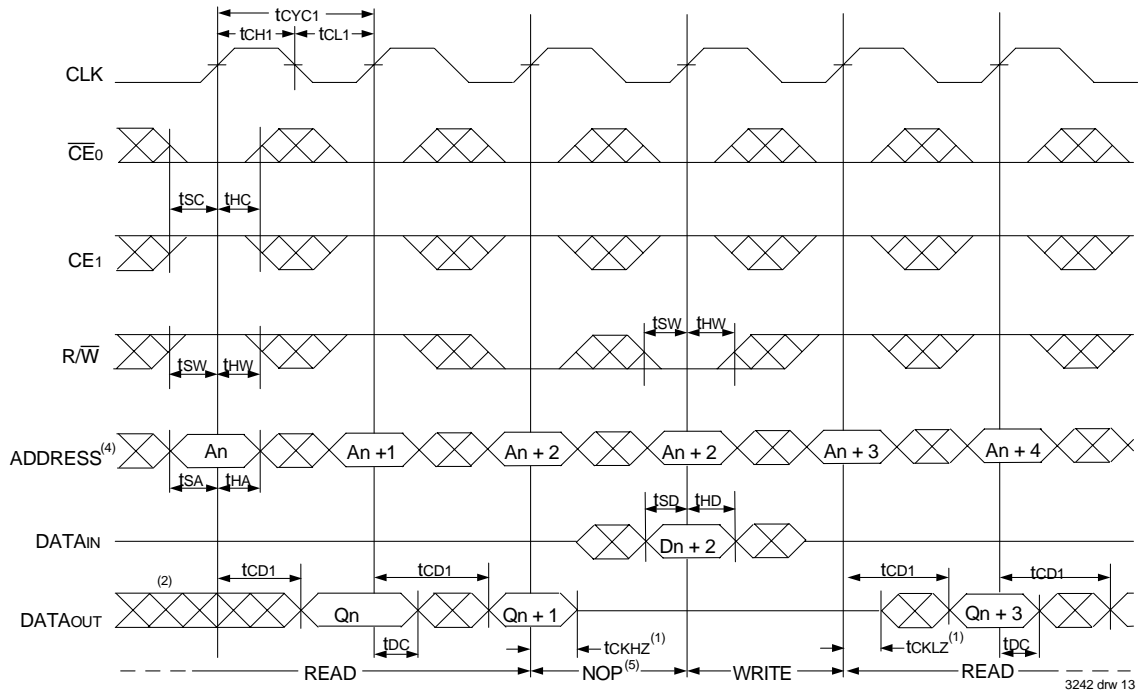


3242 drw 12

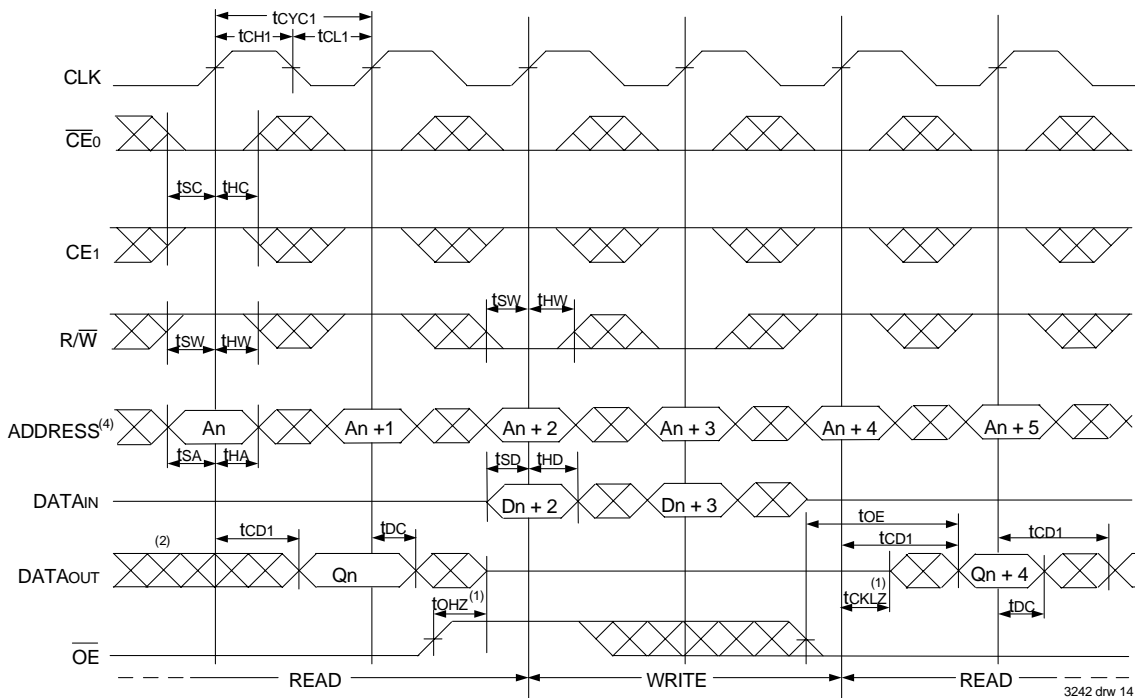
NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. \overline{CE}_0 and $\overline{ADS} = V_{IL}$; CE_1 and $\overline{CNTRST} = V_{IH}$.
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform Flow-Through Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽³⁾



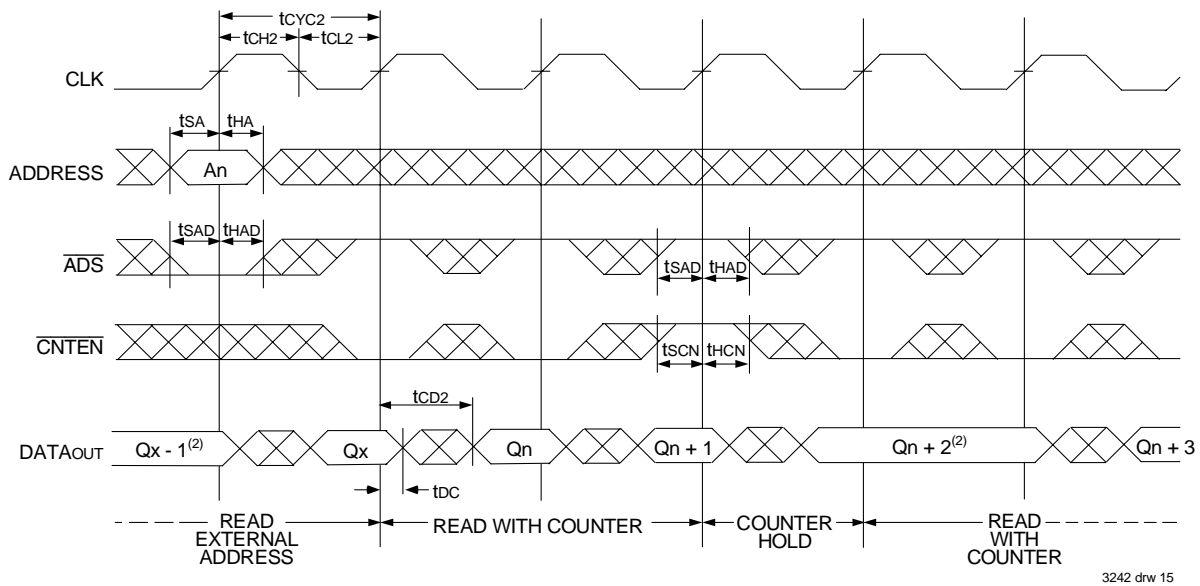
Timing Waveform of Flow-Through Read-to-Write-to-Read (\overline{OE} Controlled)⁽³⁾



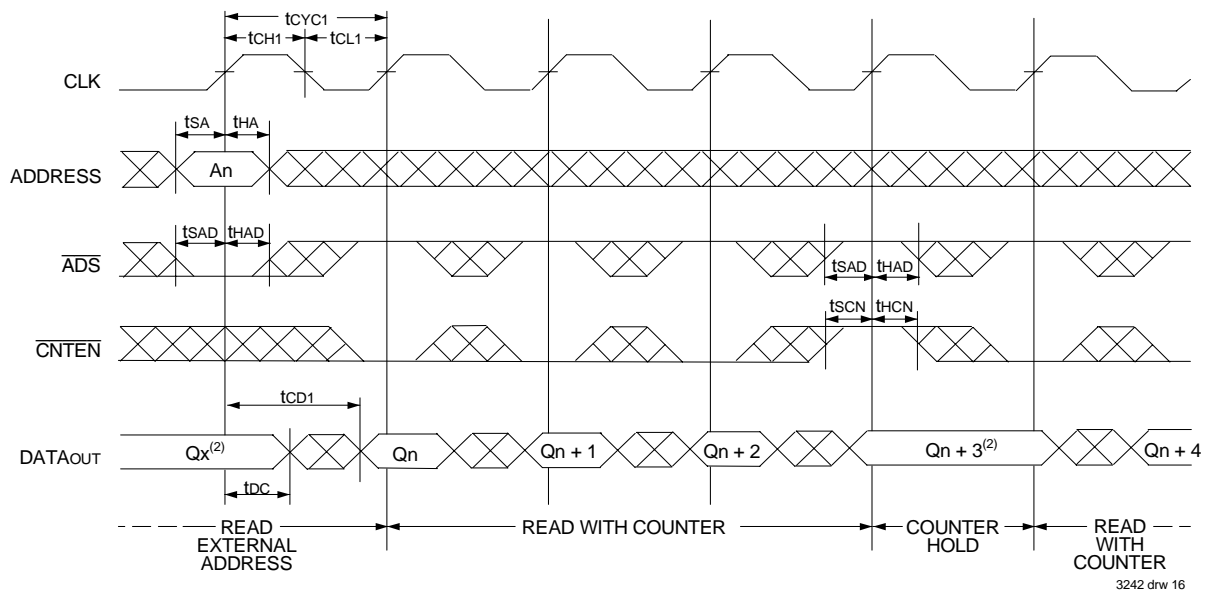
NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. $\overline{CE0}$ and $\overline{ADS} = V_{IL}$; $CE1$ and $\overline{CNTRST} = V_{IH}$.
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Pipelined Read with Address Counter Advance⁽¹⁾



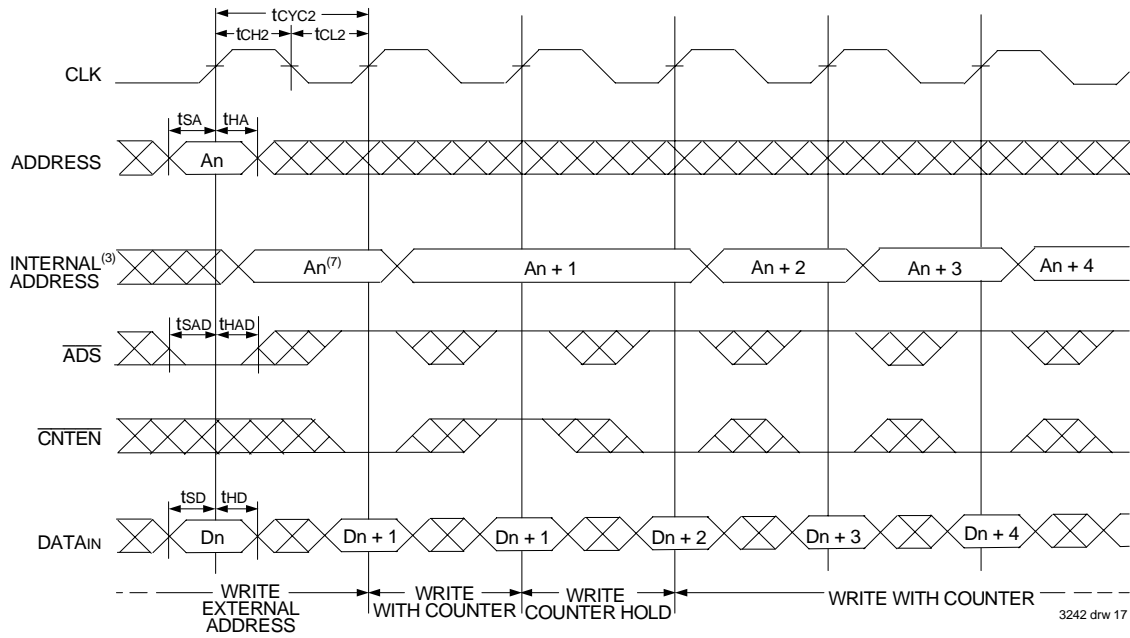
Timing Waveform of Flow-Through Read with Address Counter Advance⁽¹⁾



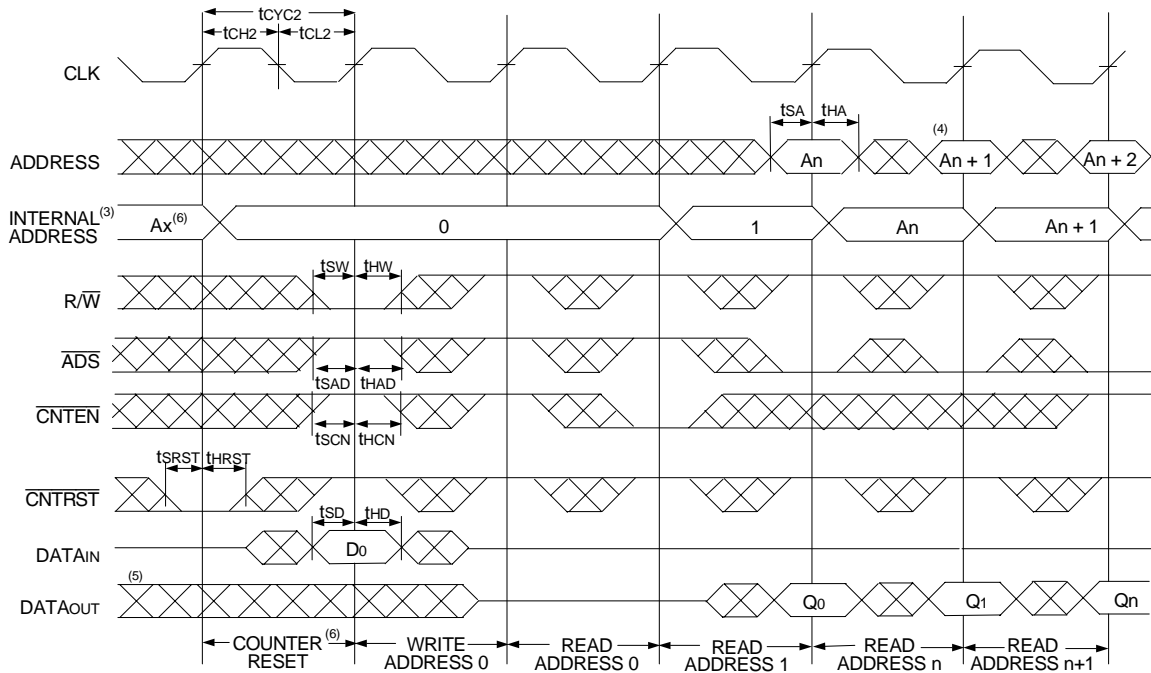
NOTES:

1. $\overline{CE0}$ and $\overline{OE} = V_{IL}$; $CE1$, R/\overline{W} , and $\overline{CNTRST} = V_{IH}$.
2. If there is no address change via $\overline{ADS} = V_{IL}$ (loading a new address) or $\overline{CNTEN} = V_{IL}$ (advancing the address), i.e. $\overline{ADS} = V_{IH}$ and $\overline{CNTEN} = V_{IH}$, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance (Flow-Through or Pipelined Outputs)⁽¹⁾



Timing Waveform of Counter Reset (Pipelined Outputs)⁽²⁾



NOTES:

1. \overline{CE}_0 and $\overline{R\overline{W}} = V_{IL}$; CE_1 and $\overline{CNTRST} = V_{IH}$.
2. $\overline{CE}_0 = V_{IL}$; $CE_1 = V_{IH}$.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS} = V_{IL}$ and equals the counter output when $\overline{ADS} = V_{IH}$.
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset. ADDR₀ will be accessed. Extra cycles are shown here simply for clarification.
7. $\overline{CNTEN} = V_{IL}$ advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1' Address is written to during this cycle.

Functional Description

The IDT709089/79 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE_0}$ or a LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT709089/79's for depth expansion configurations. When the Pipelined output mode is enabled, two cycles are required with $\overline{CE_0}$ LOW and CE_1 HIGH to reactivate the outputs.

Depth and Width Expansion

The IDT709089/79 features dual chip enables (refer to Truth Table 1) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT709089/79 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 16-bit or wider applications.

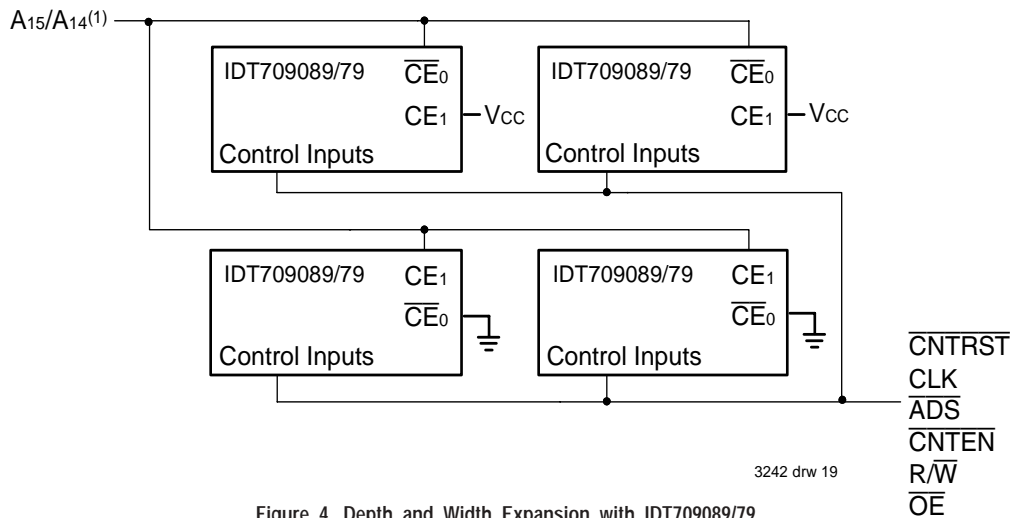
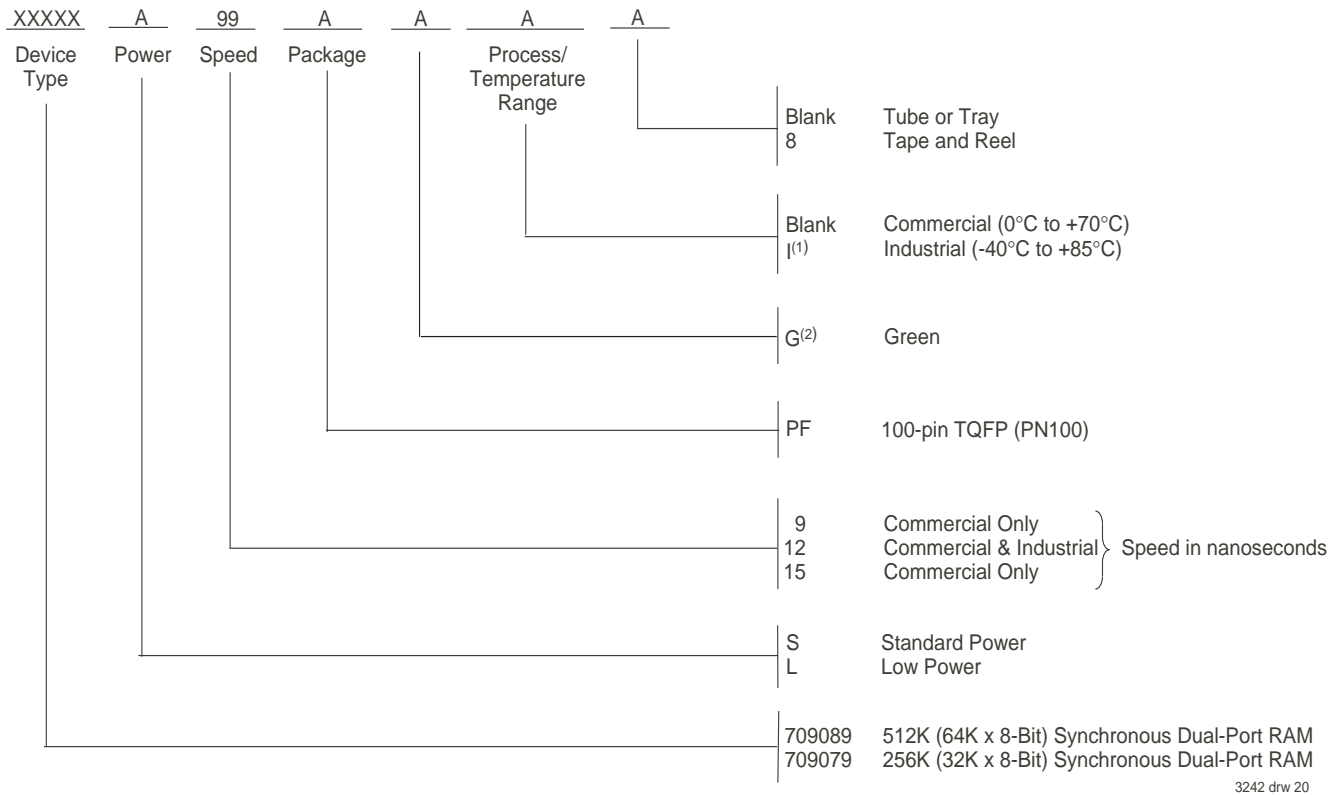


Figure 4. Depth and Width Expansion with IDT709089/79

NOTE:

1. A15 is for IDT709089, A14 is for IDT709079.

Ordering Information



NOTE:

- Contact your local sales office for industrial temp range for other speeds, packages and powers.
 - Green parts available. For specific speeds, packages and powers contact your sales office.
- LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

Ordering Information for Flow-through Devices

Old Flow-through Part	New Combined Part
70908S/L20	709089S/L9
70908S/L25	709089S/L12
70908S/L30	709089S/L15

3242 tbl 12

Datasheet Document History

- 1/12/99: Initiated datasheet document history
Converted to new format
Cosmetic and typographical corrections
Added additional notes to pin configurations
- 6/7/99: Page 15 Added Depth and Width Expansion note
Page 4 Changed drawing format
- 11/10/99: Deleted note 6 for Table II
Replaced IDT logo

Datasheet Document History (con't)

12/22/99:	Page 1	Removed "Separate upper-byte..." line
1/12/00:		Combined Pipelined 709089 family and Flow-through 70908 family offerings into one data sheet Changed $\pm 200\text{mV}$ in waveform notes to 0mV Added corresponding part chart with ordering information
2/18/00:	Pages 8 & 9 Page 9	Changed $\pm 220\text{mV}$ waveform notes to 0mV Changed "Operation" in heading to "Pipelined Output", fixed drawing 08 Removed PGA package
5/24/00:	Page 3 Page 4	Changed information in Truth Table II Increased storage temperature parameters Clarified TA parameter
	Page 5	DC Electrical parameters—changed wording from "open" to "disabled" Added Industrial Temperature Ranges and removed related notes
01/10/02:	Page 2 Page 5 & 7 Page 16 Page 1 & 17	Added date revision for pin configuration Removed industrial temp from column headings and values for 15ns from AC & DC Electrical Characteristics Removed industrial offering from 15ns ordering info and added industrial temp footnote Replaced IDT TM logo with [®] logo
06/21/04:		Consolidated multiple devices into one datasheet Removed Preliminary status from datasheet
	Page 4	Added Junction Temperature to Absolute Maximum Ratings Table Added Ambient Temperature footnote
	Page 5	Added 6ns & 7ns speed DC timing numbers to the DC Electrical Characteristics Table
	Page 8	Added 6ns & 7ns speed AC timing numbers to the AC Electrical Characteristics Table
	Page 17	Added 6ns & 7ns speed grades to ordering information Added IDT Clock Solution Table
01/29/09:	Page 1 & 18 Page 17	Replaced old [®] logo with new TM logo Removed "IDT" from orderable part number
07/26/10:	Page 1 Page 17 Page 8	Added green parts availability to features Added green indicator to ordering information In order to correct the header notes of the AC Elect Chars Table and align them with the Industrial temp range values located in the table, the commercial TA header note has been removed
	Pages 9-13	In order to correct the footnotes of timing diagrams, $\overline{\text{CNTEN}}$ has been removed to reconcile the footnotes with the $\overline{\text{CNTEN}}$ logic definition found in Truth Table II - Address Counter Control
05/28/15:	Page 1 Page 2 Page 2 Page 2 & 16 Page 5	Updated speed offerings and cycle time in Features Removed IDT in reference to fabrication Removed date for the 100-PIN TQFP configuration The package code PN100-1 changed to PN100 to match standard package codes Removed X6 and X7 speed grades from the DC Elec Chars table and combined X9, X12 & X15 speed grades into one DC Elec Chars table
	Page 6	Corrected typo in the Typical Output Derating drawing
	Page 7	Removed X6 and X7 speed grades from the AC Elec Chars table
	Page 16	Added Tape and Reel indicator to, removed X6 & X7 speed grades and updated the commercial and industrial offerings in Ordering Information
	Page 16	Removed the IDT Clock Solution table
02/22/16:	Page 2	Changed diagram for the PN100 pin configuration by rotating the pin1 orientation counter clockwise by 90 degrees for accurate representation of the part and added the black dot as the pin 1 indicator Added the IDT logo to the pin configuration and changed the text to be in alignment with new diagram marking specs and rotated the pin names on the vertical sides to an upright position Updated footnote references for the PN100 pin configuration
01/26/18:		Product Discontinuation Notice - PDN# SP-17-02 Last time buy expires June 15, 2018
04/22/19:		Datasheet changed to Obsolete Status

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.