

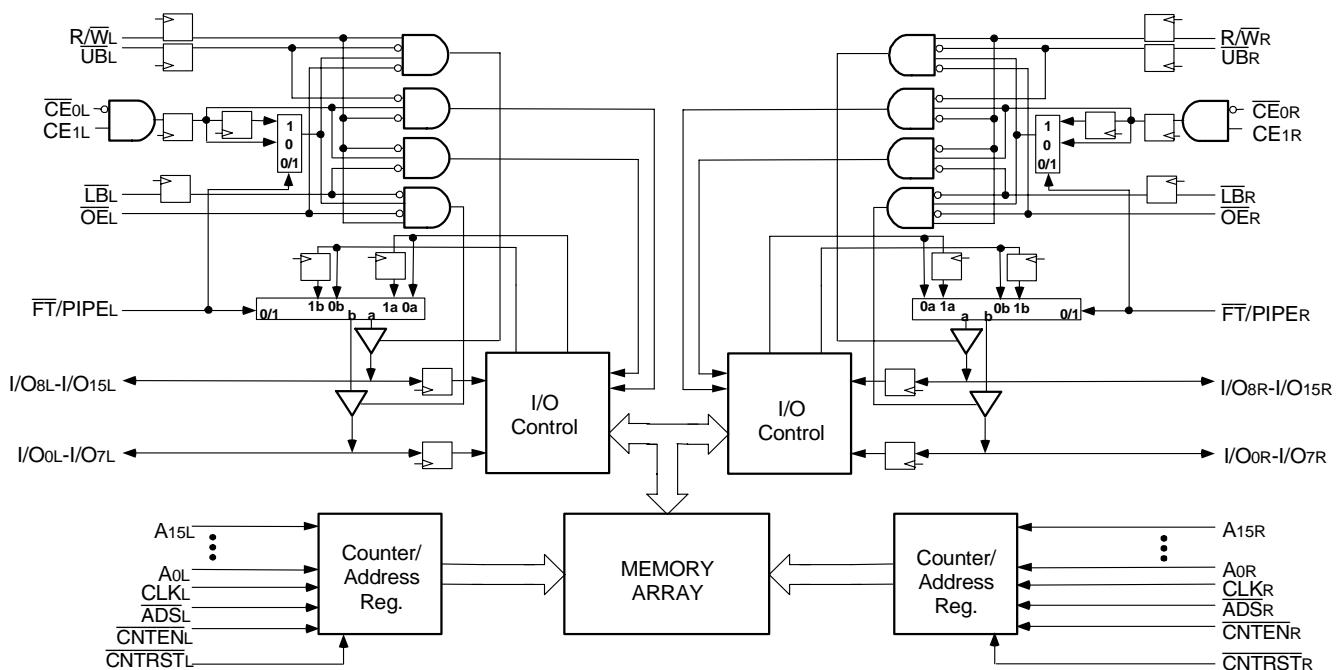
LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

Features

- True Dual-Ported memory cells which allow simultaneous access of the same memory location
- High-speed clock to data access
 - Commercial: 7.5/9/12ns (max.)
 - Industrial: 9ns (max.)
- Low-power operation
 - IDT709289L
 - Active: 1.2W (typ.)
 - Standby: 2.5mW (typ.)
- Flow-Through or Pipelined output mode on either Port via the $\overline{FT}/PIPE$ pins
- Counter enable and reset features
- Dual chip enables allow for depth expansion without additional logic

- Full synchronous operation on both ports
 - 4ns setup to clock and 0ns hold on all control, data, and address inputs
 - Data input, address, and control registers
 - Fast 7.5ns clock to data out in the Pipelined output mode
 - Self-timed write allows fast cycle time
 - 12ns cycle time, 83MHz operation in Pipelined output mode
- Separate upper-byte and lower-byte controls for multiplexed bus and bus matching compatibility
- TTL- compatible, single 5V ($\pm 10\%$) power supply
- Industrial temperature range (-40°C to $+85^{\circ}\text{C}$) is available for selected speeds
- Available in a 100-pin Thin Quad Flatpack (TQFP) package
- Green parts available, see ordering information

Functional Block Diagram



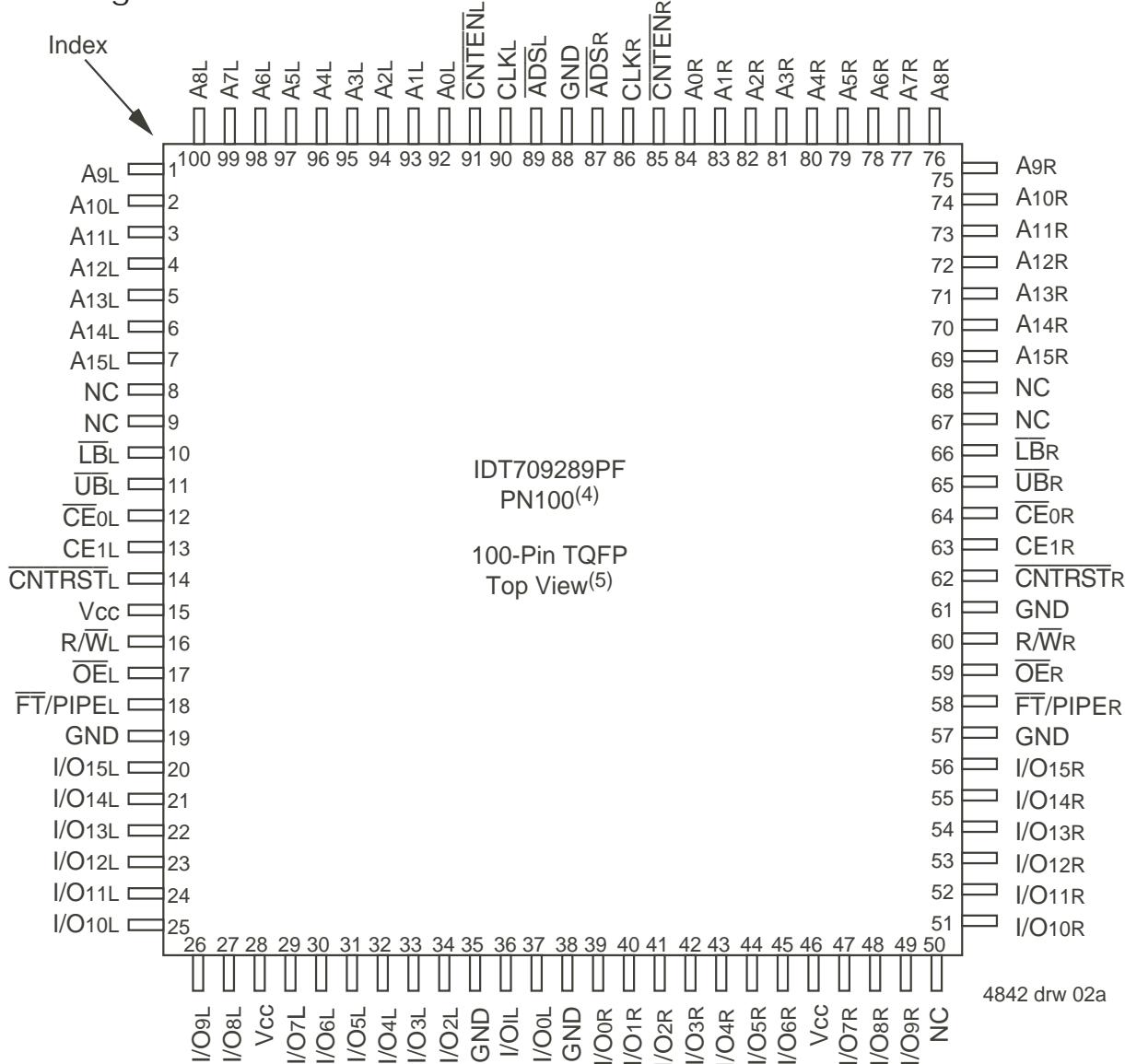
4842 drw 01

Description

The IDT709289 is a high-speed 64K x 16 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times.

With an input data register, the IDT709289 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by \overline{CE}_0 and CE_1 , permits the on-chip circuitry of each port to enter a very low standby power mode. Fabricated using CMOS high-performance technology, these devices typically operate on only 1.2W of power.

Pin Configurations^(1,2,3)



NOTES:

1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground.
3. Package body is approximately 14mm x 14mm x 1.4mm
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Names

| Left Port | Right Port | Names |
|--------------------------------|--------------------------------|-----------------------|
| \overline{CE}_0L , CE_{1L} | \overline{CE}_0R , CE_{1R} | Chip Enables |
| R/\overline{W}_L | R/\overline{W}_R | Read/Write Enable |
| \overline{OE}_L | \overline{OE}_R | Output Enable |
| A_{0L} - A_{15L} | A_{0R} - A_{15R} | Address |
| I/O_{0L} - I/O_{15L} | I/O_{0R} - I/O_{15R} | Data Input/Output |
| CLK_L | CLK_R | Clock |
| \overline{UB}_L | \overline{UB}_R | Upper Byte Select |
| \overline{LB}_L | \overline{LB}_R | Lower Byte Select |
| \overline{ADS}_L | \overline{ADS}_R | Address Strobe |
| $CNTEN_L$ | $CNTEN_R$ | Counter Enable |
| $CNTRST_L$ | $CNTRST_R$ | Counter Reset |
| $\overline{FT}/PIPE_L$ | $\overline{FT}/PIPE_R$ | Flow-Through/Pipeline |
| VCC | | Power |
| GND | | Ground |

4842tbl 01

Truth Table I—Read/Write and Enable Control^(1,2,3)

| \overline{OE} | CLK | \overline{CE}_0 | CE_1 | \overline{UB} | \overline{LB} | R/\overline{W} | Upper Byte I/O_{8-15} | Lower Byte I/O_{0-7} | Mode |
|-----------------|-----|-------------------|--------|-----------------|-----------------|------------------|----------------------------|---------------------------|--------------------------|
| X | ↑ | H | X | X | X | X | High-Z | High-Z | Deselected—Power Down |
| X | ↑ | X | L | X | X | X | High-Z | High-Z | Deselected—Power Down |
| X | ↑ | L | H | H | H | X | High-Z | High-Z | Both Bytes Deselected |
| X | ↑ | L | H | L | H | L | DATA _{IN} | High-Z | Write to Upper Byte Only |
| X | ↑ | L | H | H | L | L | High-Z | DATA _{IN} | Write to Lower Byte Only |
| X | ↑ | L | H | L | L | L | DATA _{IN} | DATA _{IN} | Write to Both Bytes |
| L | ↑ | L | H | L | H | H | DATA _{OUT} | High-Z | Read Upper Byte Only |
| L | ↑ | L | H | H | L | H | High-Z | DATA _{OUT} | Read Lower Byte Only |
| L | ↑ | L | H | L | L | H | DATA _{OUT} | DATA _{OUT} | Read Both Bytes |
| H | X | L | H | L | L | X | High-Z | High-Z | Outputs Disabled |

4842tbl 02

NOTES:

1. "H" = V_{IH} , "L" = V_{IL} , "X" = Don't Care.
2. \overline{ADS} , $CNTEN$, $CNTRST$ = X.
3. \overline{OE} is an asynchronous input signal.

Truth Table II—Address Counter Control^(1,2,6)

| Address | Previous Address | Addr Used | CLK | <u>ADS</u> | <u>CNTEN</u> | <u>CNTRST</u> | I/O ⁽³⁾ | Mode |
|---------|------------------|-----------|-----|------------------|------------------|---------------|---------------------|---|
| X | X | 0 | ↑ | X | X | L | D ₀₍₀₎ | Counter Reset to Address 0 |
| An | X | An | ↑ | L ⁽⁴⁾ | X | H | D _{0(n)} | External Address Loaded into Counter |
| An | Ap | Ap | ↑ | H | H | H | D _{0(p)} | External Address Blocked—Counter Disabled (Ap reused) |
| X | Ap | Ap + 1 | ↑ | H | L ⁽⁵⁾ | H | D _{0(p+1)} | Counter Enable—Internal Address Generation |

4842tbl 03

NOTES:

- "H" = V_{IH} , "L" = V_{IL} , "X" = Don't Care.
- \overline{CE}_0 , \overline{LB} , \overline{UB} , and \overline{OE} = V_{IL} ; CE_1 and $R/W = V_{IH}$.
- Outputs configured in Flow-Through Output mode: if outputs are in Pipelined mode the data out will be delayed by one cycle.
- ADS is independent of all other signals including \overline{CE}_0 , CE_1 , \overline{UB} and \overline{LB} .
- The address counter advances if $CNTEN = V_{IL}$ on the rising edge of CLK, regardless of all other signals including \overline{CE}_0 , CE_1 , \overline{UB} and \overline{LB} .
- While an external address is being loaded ($\overline{ADS} = V_{IL}$), $R/W = V_{IH}$ is recommended to ensure data is not written arbitrarily.

Recommended Operating Temperature and Supply Voltage

| Grade | Ambient Temperature ⁽²⁾ | GND | V _{cc} |
|------------|------------------------------------|-----|-----------------|
| Commercial | 0°C to +70°C | 0V | 5.0V \pm 10% |
| Industrial | -40°C to +85°C | 0V | 5.0V \pm 10% |

4842tbl 04

NOTES:

- This is the parameter T_A . This is the "instant on" case temperature.

Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------------|--------------------|---------------------|------|--------------------|------|
| V _{cc} | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Ground | 0 | 0 | 0 | V |
| V _{IH} | Input High Voltage | 2.2 | — | 6.0 ⁽¹⁾ | V |
| V _{IL} | Input Low Voltage | -0.5 ⁽²⁾ | — | 0.8 | V |

4842tbl 05

NOTES:

- V_{TERM} must not exceed $V_{cc} + 10\%$.
- $V_{IL} \geq -1.5V$ for pulse width less than 10ns.

Absolute Maximum Ratings⁽¹⁾

| Symbol | Rating | Commercial & Industrial | Unit |
|----------------------------------|--------------------------------------|-------------------------|------|
| V _{TERM} ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +7.0 | V |
| T _{BIAS} | Temperature Under Bias | -55 to +125 | °C |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| I _{OUT} | DC Output Current | 50 | mA |

4842tbl 06

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed $V_{cc} + 10\%$ for more than 25% of the cycle time or 10ns maximum, and is limited to $\leq 20mA$ for the period of $V_{TERM} \geq V_{cc} + 10\%$.

Capacitance⁽¹⁾

($T_A = +25^\circ C$, $f = 1.0MHz$)

| Symbol | Parameter | Conditions ⁽²⁾ | Max. | Unit |
|---------------------------------|--------------------|---------------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 3dV | 9 | pF |
| C _{OUT} ⁽³⁾ | Output Capacitance | V _{OUT} = 3dV | 10 | pF |

4842tbl 07

NOTES:

- These parameters are determined by device characterization, but are not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
- C_{OUT} also references C_{IO}.

DC Electrical Characteristics Over the Operating Temperature Supply Voltage Range ($V_{CC} = 5.0V \pm 10\%$)

| Symbol | Parameter | Test Conditions | 709289L | | Unit |
|----------|--------------------------------------|---|---------|------|---------|
| | | | Min. | Max. | |
| $ I_L $ | Input Leakage Current ⁽¹⁾ | $V_{CC} = 5.5V, V_{IN} = 0V$ to V_{CC} | — | 5 | μA |
| $ I_O $ | Output Leakage Current | $\bar{CE}_0 = V_{IH}$ or $CE_1 = V_{IL}$, $V_{OUT} = 0V$ to V_{CC} | — | 5 | μA |
| V_{OL} | Output Low Voltage | $I_{OL} = +4mA$ | — | 0.4 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -4mA$ | 2.4 | — | V |

4842 tbl 08

NOTE:

1. At $V_{CC} \leq 2.0V$ input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽³⁾ ($V_{CC} = 5V \pm 10\%$)

| Symbol | Parameter | Test Condition | Version | 709289L7 Com'l Only | | 709289L9 Com'l & Ind | | 709289L12 Com'l Only | | Unit |
|------------------|---|---|---------|------------------------|------|-------------------------|------|-------------------------|------|------|
| | | | | Typ. ⁽⁴⁾ | Max. | Typ. ⁽⁴⁾ | Max. | Typ. ⁽⁴⁾ | Max. | |
| I _{CC} | Dynamic Operating Current (Both Ports Active) | \bar{CE}_L and $\bar{CE}_R = V_{IL}$ Outputs Disabled $f = f_{MAX}^{(1)}$ | COM'L L | 275 | 465 | 250 | 400 | 230 | 355 | mA |
| | | | IND L | — | — | 300 | 430 | — | — | |
| I _{S81} | Standby Current (Both Ports - TTL Level Inputs) | $\bar{CE}_L = \bar{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$ | COM'L L | 95 | 150 | 80 | 135 | 70 | 110 | mA |
| | | | IND L | — | — | 95 | 160 | — | — | |
| I _{S82} | Standby Current (One Port - TTL Level Inputs) | $\bar{CE}^{(A)} = V_{IL}$ and $\bar{CE}^{(B)} = V_{IH}^{(3)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$ | COM'L L | 200 | 295 | 175 | 275 | 150 | 240 | mA |
| | | | IND L | — | — | 195 | 295 | — | — | |
| I _{S83} | Full Standby Current (Both Ports - CMOS Level Inputs) | Both Ports CER and $\bar{CE}_L \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V, f = 0^{(2)}$ | COM'L L | 0.5 | 3.0 | 0.5 | 3.0 | 0.5 | 3.0 | mA |
| | | | IND L | — | — | 0.5 | 6.0 | — | — | |
| I _{S84} | Full Standby Current (One Port - CMOS Level Inputs) | $\bar{CE}^{(A)} \leq 0.2V$ and $\bar{CE}^{(B)} \geq V_{CC} - 0.2V^{(5)}$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$ | COM'L L | 190 | 290 | 170 | 270 | 140 | 225 | mA |
| | | | IND L | — | — | 190 | 290 | — | — | |

4842 tbl 09

NOTES:

- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of $1/t_{cyc}$, using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$ means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{CC} = 5V, TA = 25^\circ C$ for Typ, and are not production tested. $I_{CC}(f=0) = 150mA$ (Typ).
- $\bar{CE}_X = V_L$ means $\bar{CE}_{0X} = V_{IL}$ and $CE_{1X} = V_{IH}$
 $\bar{CE}_X = V_{IH}$ means $\bar{CE}_{0X} = V_{IH}$ or $CE_{1X} = V_{IL}$
 $\bar{CE}_X \leq 0.2V$ means $\bar{CE}_{0X} \leq 0.2V$ and $CE_{1X} \geq V_{CC} - 0.2V$
 $\bar{CE}_X \geq V_{CC} - 0.2V$ means $\bar{CE}_{0X} \geq V_{CC} - 0.2V$ or $CE_{1X} \leq 0.2V$
"X" represents "L" for left port or "R" for right port.

AC Test Conditions

| | |
|-------------------------------|-------------------|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 3ns Max. |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| Output Load | Figures 1,2 and 3 |

4842 tbl 10

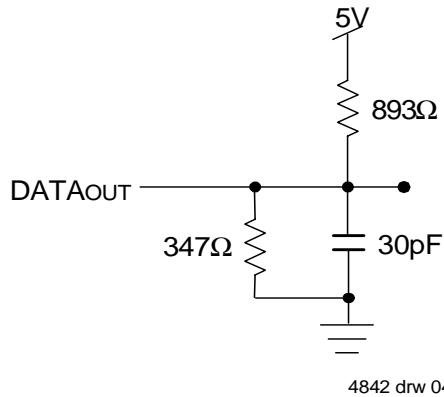


Figure 1. AC Output Test load.

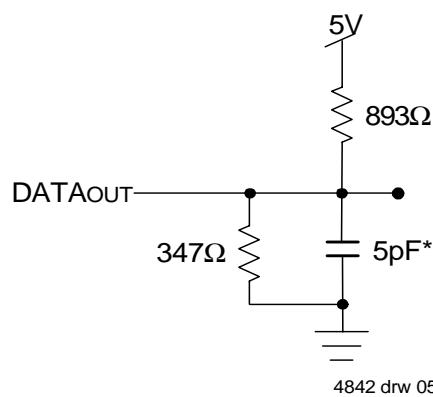


Figure 2. Output Test Load
(For tcklz, tckhz, tolz, and tohz).

*Including scope and jig.

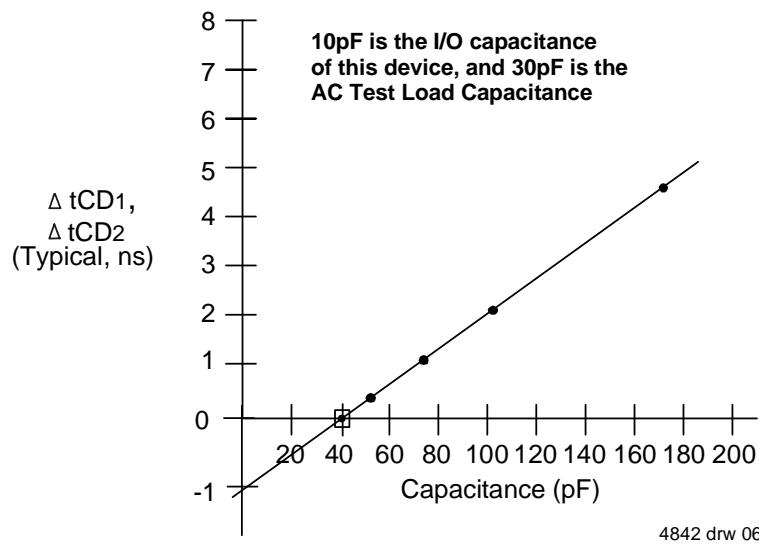


Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range
(Read and Write Cycle Timing)⁽³⁾ (V_{CC} = 5V ± 10%, TA = 0°C to +70°C)

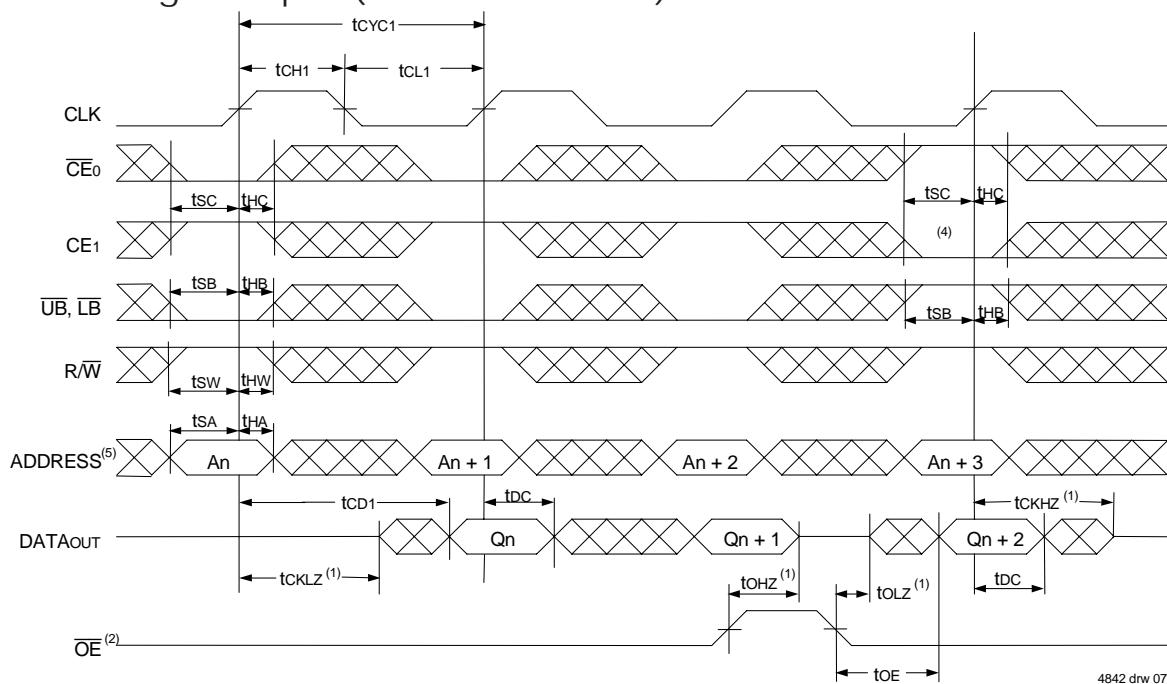
| Symbol | Parameter | 709289L7 Com'l Only | | 709289L9 Com'l & Ind | | 709289L12 Com'l Only | | Unit |
|---------------------------|---|------------------------|------|-------------------------|------|-------------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{CYC1} | Clock Cycle Time (Flow-Through) ⁽²⁾ | 22 | — | 25 | — | 30 | — | ns |
| t _{CYC2} | Clock Cycle Time (Pipelined) ⁽²⁾ | 12 | — | 15 | — | 20 | — | ns |
| t _{CH1} | Clock High Time (Flow-Through) ⁽²⁾ | 7.5 | — | 12 | — | 12 | — | ns |
| t _{CL1} | Clock Low Time (Flow-Through) ⁽²⁾ | 7.5 | — | 12 | — | 12 | — | ns |
| t _{CH2} | Clock High Time (Pipelined) ⁽²⁾ | 5 | — | 6 | — | 8 | — | ns |
| t _{CL2} | Clock Low Time (Pipelined) ⁽²⁾ | 5 | — | 6 | — | 8 | — | ns |
| t _R | Clock Rise Time | — | 3 | — | 3 | — | 3 | ns |
| t _F | Clock Fall Time | — | 3 | — | 3 | — | 3 | ns |
| t _{SA} | Address Setup Time | 4 | — | 4 | — | 4 | — | ns |
| t _{HA} | Address Hold Time | 0 | — | 1 | — | 1 | — | ns |
| t _{SC} | Chip Enable Setup Time | 4 | — | 4 | — | 4 | — | ns |
| t _{HC} | Chip Enable Hold Time | 0 | — | 1 | — | 1 | — | ns |
| t _{SB} | Byte Enable Setup Time | 4 | — | 4 | — | 4 | — | ns |
| t _{HB} | Byte Enable Hold Time | 0 | — | 1 | — | 1 | — | ns |
| t _{SW} | R/W Setup Time | 4 | — | 4 | — | 4 | — | ns |
| t _{HW} | R/W Hold Time | 0 | — | 1 | — | 1 | — | ns |
| t _{SD} | Input Data Setup Time | 4 | — | 4 | — | 4 | — | ns |
| t _{HD} | Input Data Hold Time | 0 | — | 1 | — | 1 | — | ns |
| t _{SAD} | ADS Setup Time | 4 | — | 4 | — | 4 | — | ns |
| t _{HAD} | ADS Hold Time | 0 | — | 1 | — | 1 | — | ns |
| t _{SCN} | CNTEN Setup Time | 4 | — | 4 | — | 4 | — | ns |
| t _{HCN} | CNTEN Hold Time | 0 | — | 1 | — | 1 | — | ns |
| t _{SRST} | CNTRST Setup Time | 4 | — | 4 | — | 4 | — | ns |
| t _{HRST} | CNTRST Hold Time | 0 | — | 1 | — | 1 | — | ns |
| t _{OE} | Output Enable to Data Valid | — | 9 | — | 12 | — | 12 | ns |
| t _{OLZ} | Output Enable to Output Low-Z ⁽¹⁾ | 2 | — | 2 | — | 2 | — | ns |
| t _{OHZ} | Output Enable to Output High-Z ⁽¹⁾ | 1 | 7 | 1 | 7 | 1 | 7 | ns |
| t _{CD1} | Clock to Data Valid (Flow-Through) ⁽²⁾ | — | 18 | — | 20 | — | 25 | ns |
| t _{CD2} | Clock to Data Valid (Pipelined) ⁽²⁾ | — | 7.5 | — | 9 | — | 12 | ns |
| t _{DC} | Data Output Hold After Clock High | 2 | — | 2 | — | 2 | — | ns |
| t _{CkHz} | Clock High to Output High-Z ⁽¹⁾ | 2 | 9 | 2 | 9 | 2 | 9 | ns |
| t _{CKLZ} | Clock High to Output Low-Z ⁽¹⁾ | 2 | — | 2 | — | 2 | — | ns |
| Port-to-Port Delay | | | | | | | | |
| t _{CWDD} | Write Port Clock High to Read Data Delay | — | 28 | — | 35 | — | 40 | ns |
| t _{CCS} | Clock-to-Clock Setup Time | — | 10 | — | 15 | — | 15 | ns |

NOTES:

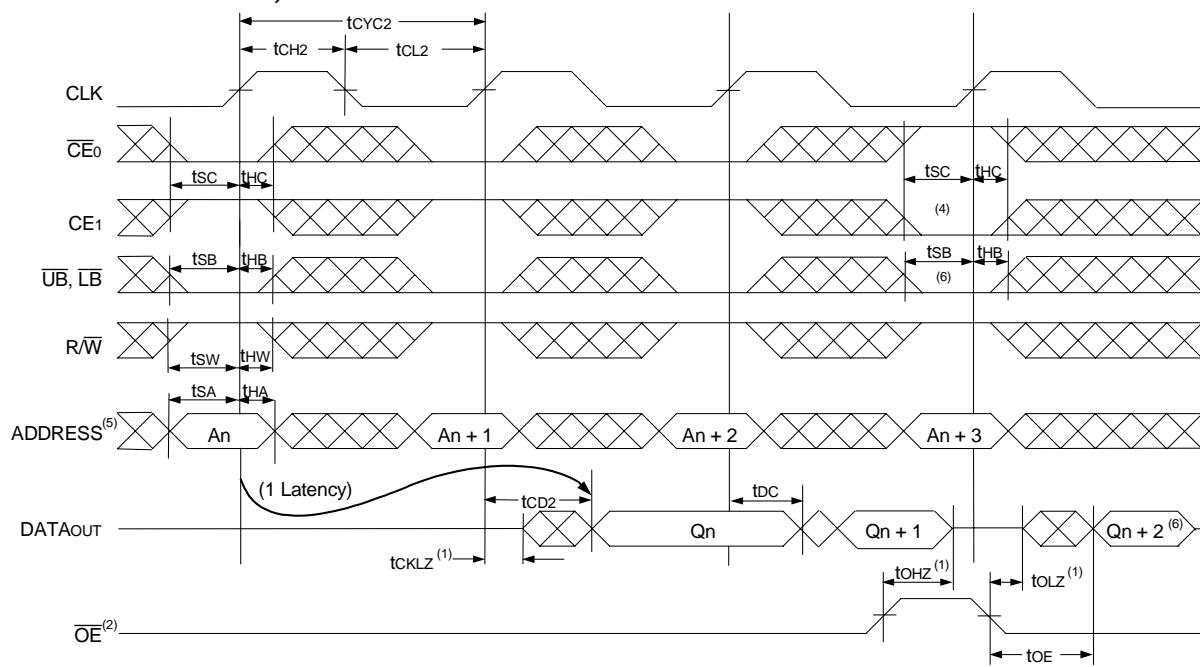
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
2. The Pipelined output parameters (t_{CYC2}, t_{CD2}) to either the Left or Right ports when $\overline{FT}/PIPE = V_{IH}$. Flow-Through parameters (t_{CYC1}, t_{CD1}) apply when $\overline{FT}/PIPE = V_{IL}$ for that port.
3. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable (\overline{OE}), $\overline{FT}/PIPE_R$ and $\overline{FT}/PIPE_L$.

4842tbl11

Timing Waveform of Read Cycle for
Flow-Through Output ($\overline{FT}/PIPE^X = V_{IL}$)^(3,7)



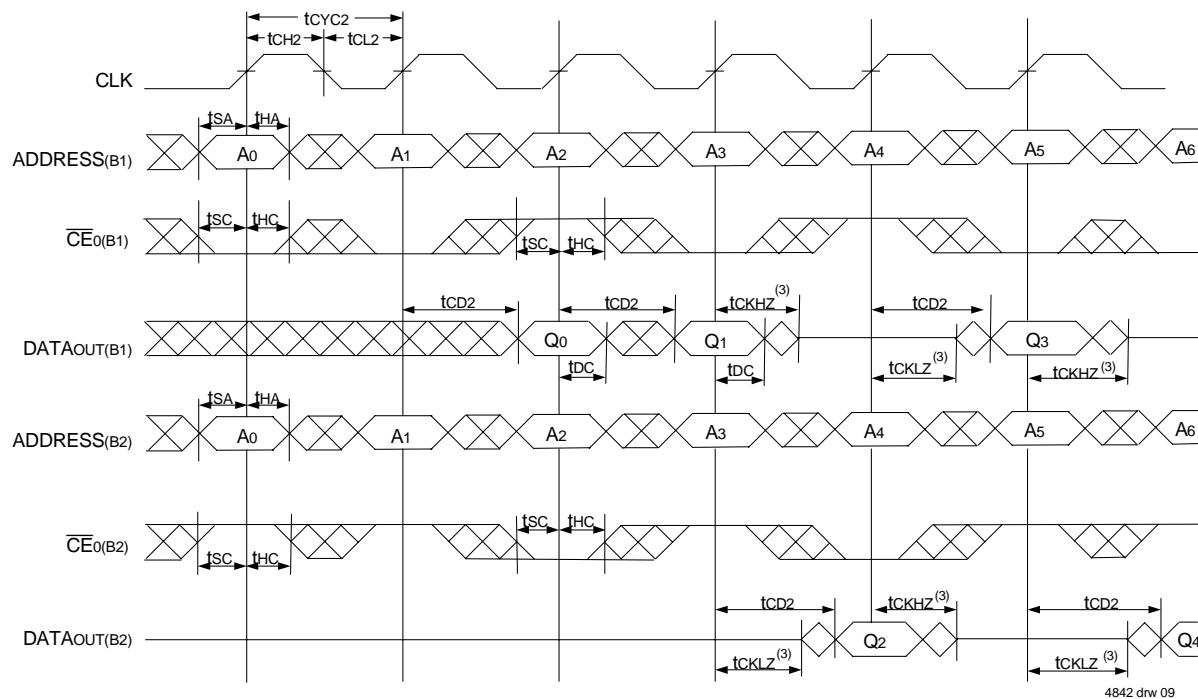
Timing Waveform of Read Cycle for Pipelined Operation
($\overline{FT}/PIPE^X = V_{IH}$)^(3,7)



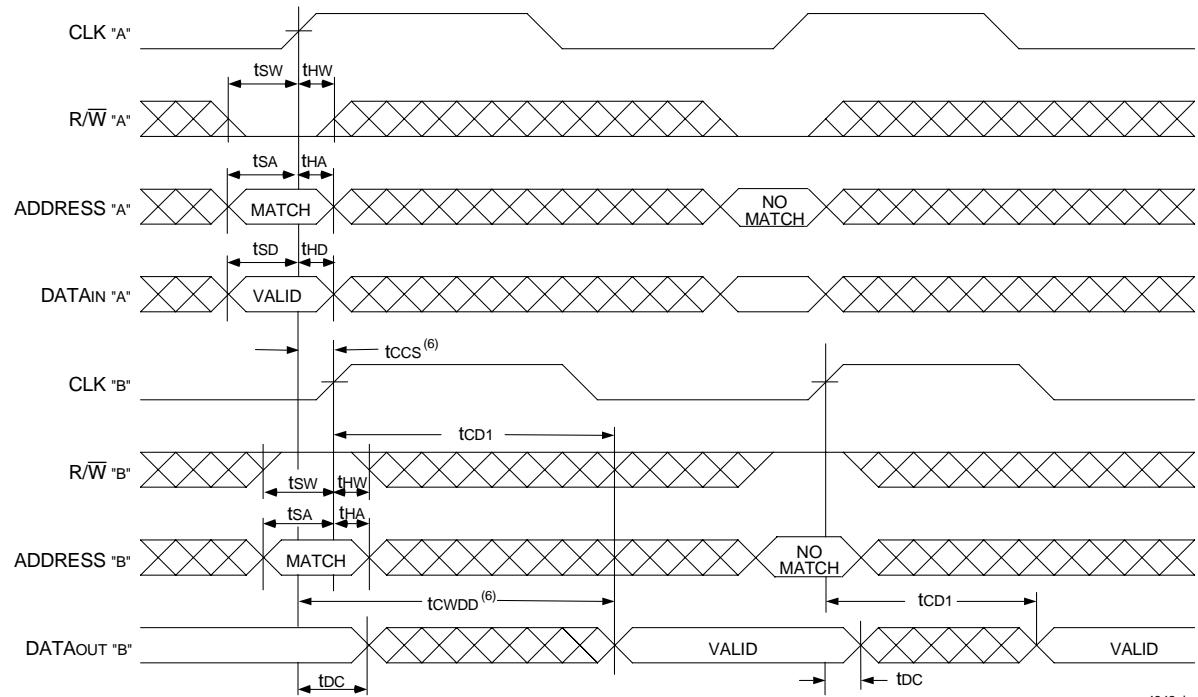
NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. \overline{OE} is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
3. $\overline{ADS} = V_{IL}$, \overline{CNTEN} and $\overline{CNTRST} = V_{IH}$.
4. The output is disabled (High-Impedance state) by $\overline{CE}_0 = V_{IH}$, $CE_1 = V_{IL}$, $\overline{UB} = V_{IH}$, or $\overline{LB} = V_{IH}$ following the next rising edge of the clock. Refer to Truth Table 1.
5. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
6. If \overline{UB} or \overline{LB} was HIGH, then the Upper Byte and/or Lower Byte of DATAout for Q_{n+2} would be disabled (High-Impedance state).
7. "X" here denotes Left or Right port. The diagram is with respect to that port.

Timing Waveform of a Bank Select Pipelined Read^(1,2)



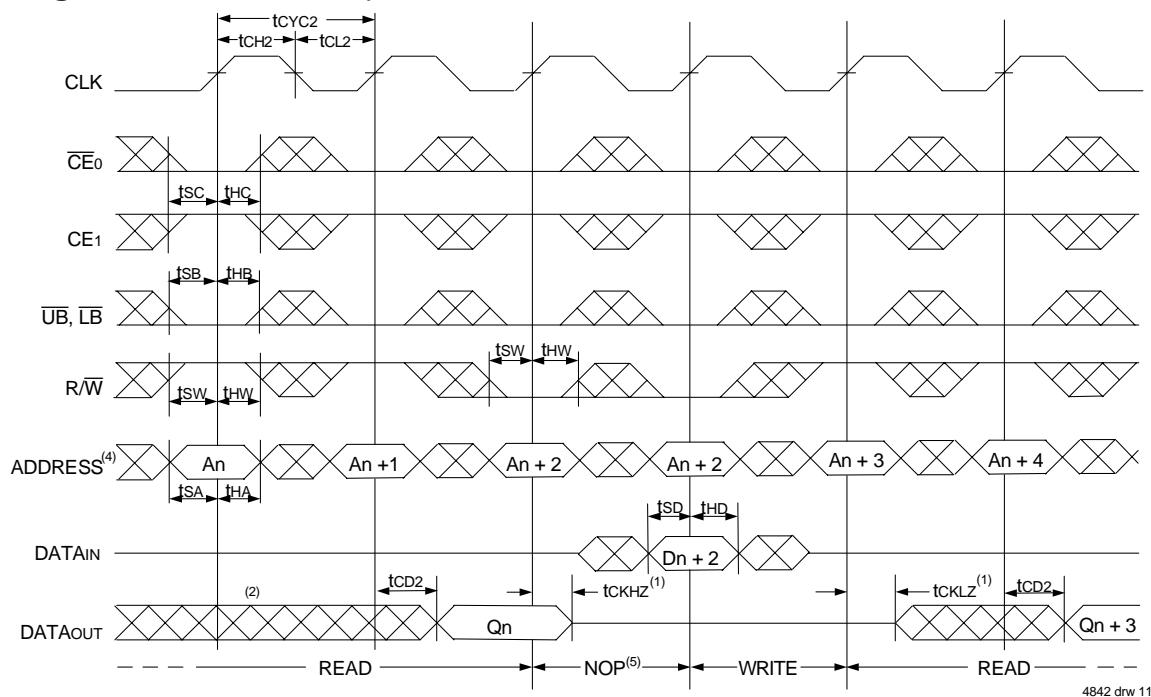
Timing Waveform of Write with Port-to-Port Flow-Through Read^(4,5,7)



NOTES:

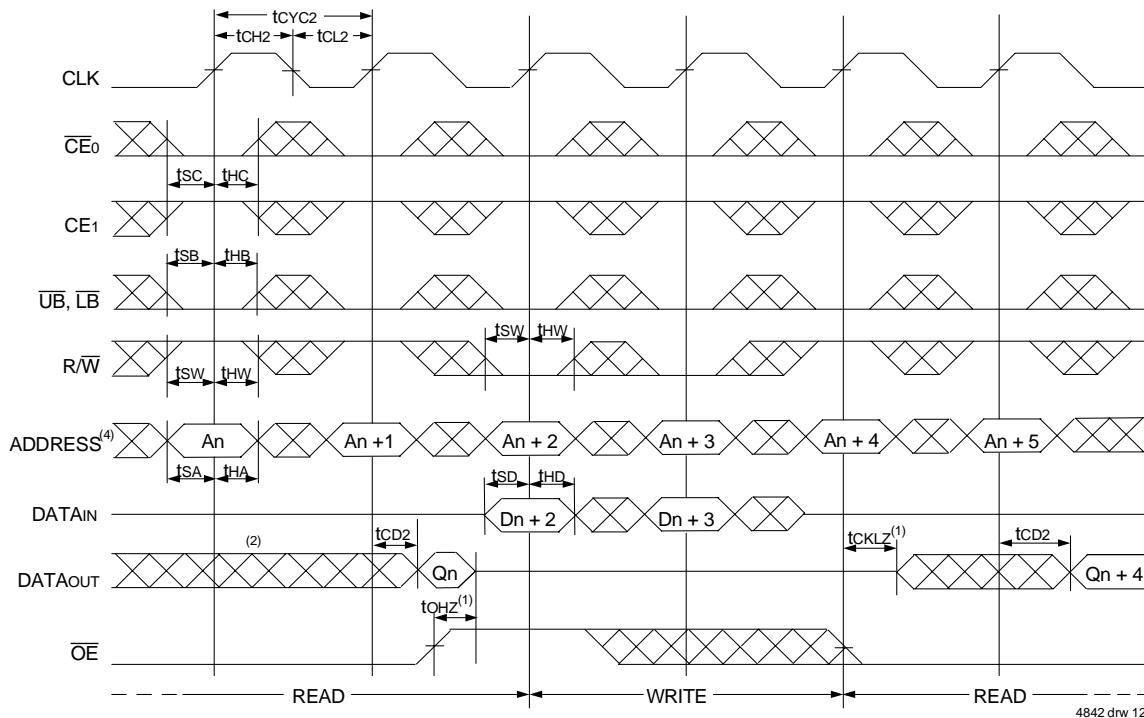
1. B1 Represents Bank #1; B2 Represents Bank #2. Each Bank consists of one IDT709289 for this waveform, and are setup for depth expansion in this example. ADDRESS_(B1) = ADDRESS_(B2) in this situation.
2. \overline{UB} , \overline{LB} , \overline{OE} , and \overline{ADS} = V_{IL} ; $CE1(B1)$, $CE1(B2)$, \overline{RW} , \overline{CNTEN} , and \overline{CNTRST} = V_{IH} .
3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4. $\overline{CE0}$, \overline{UB} , \overline{LB} , and \overline{ADS} = V_{IL} ; $CE1$, \overline{CNTEN} , and \overline{CNTRST} = V_{IH} .
5. OE = V_{IL} for the Right Port, which is being read from. OE = V_{IH} for the Left Port, which is being written to.
6. If $tccs \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for $tCWDD$. If $tccs >$ maximum specified, then data from right port READ is not valid until $tccs + tCD1$. $tCWDD$ does not apply in this case.
7. All timing is the same for both Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite from Port "A".

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽³⁾



4842 drw 11

Timing Waveform of Pipelined Read-to-Write-to-Read (\overline{OE} Controlled)⁽³⁾

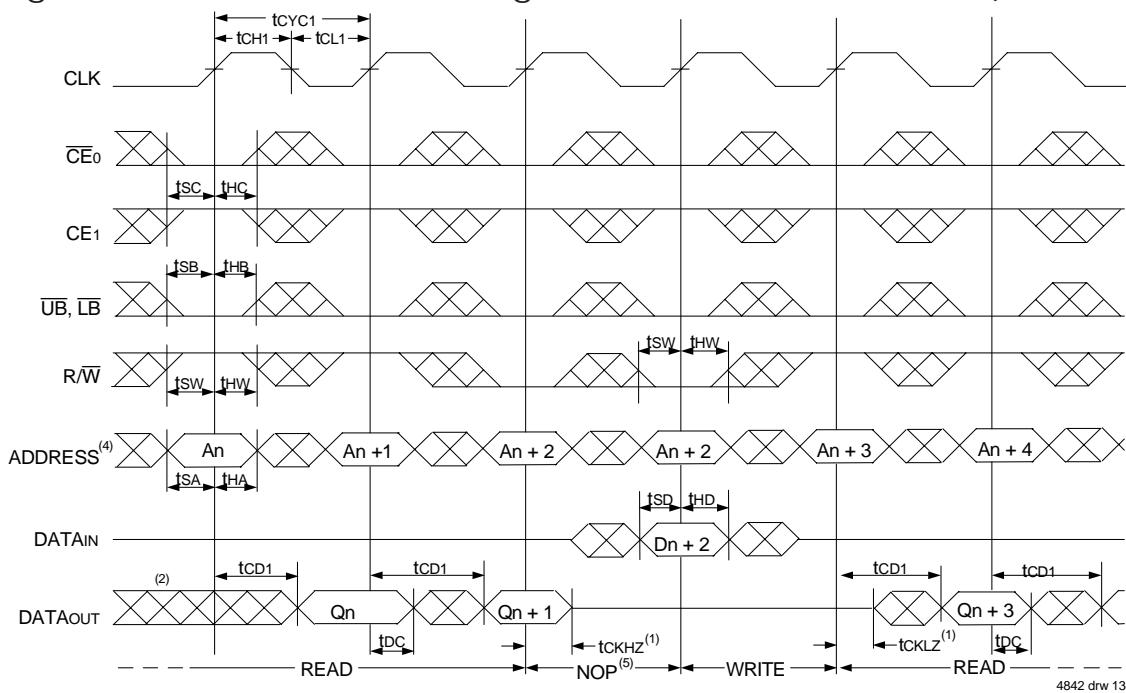


4842 drw 12

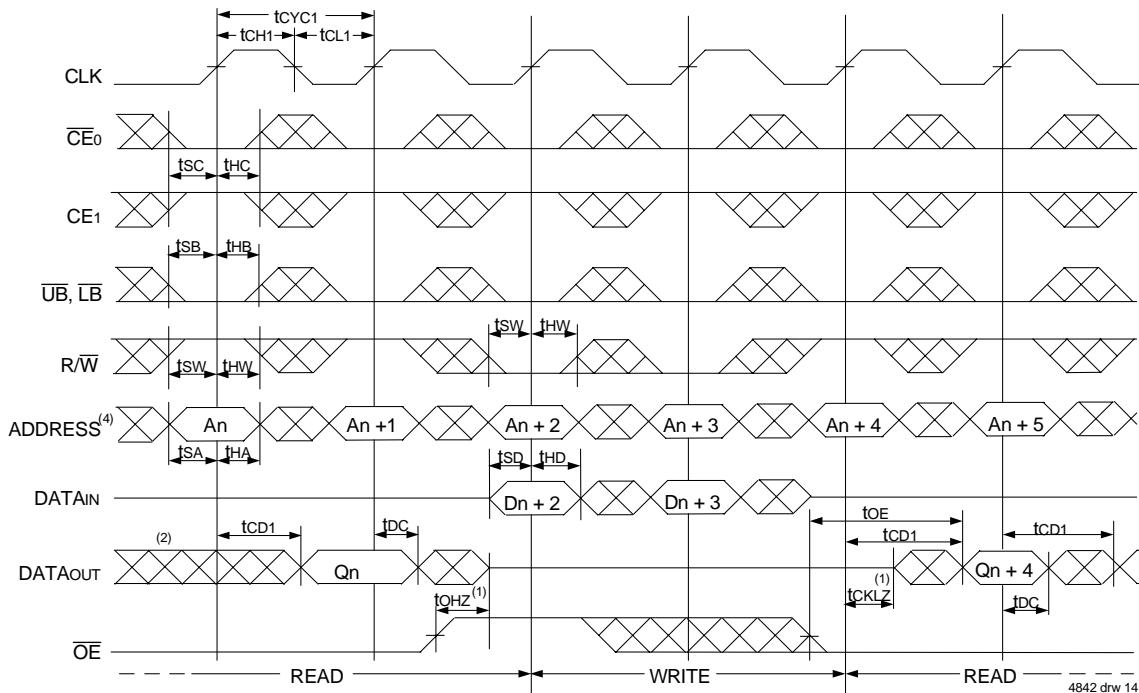
NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. \overline{CE}_0 , \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; CE_1 , $CNTEN$, and $\overline{CNTRST} = V_{IH}$. "NOP" is "No Operation".
4. Addresses do not have to be accessed sequentially since $ADS = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽³⁾



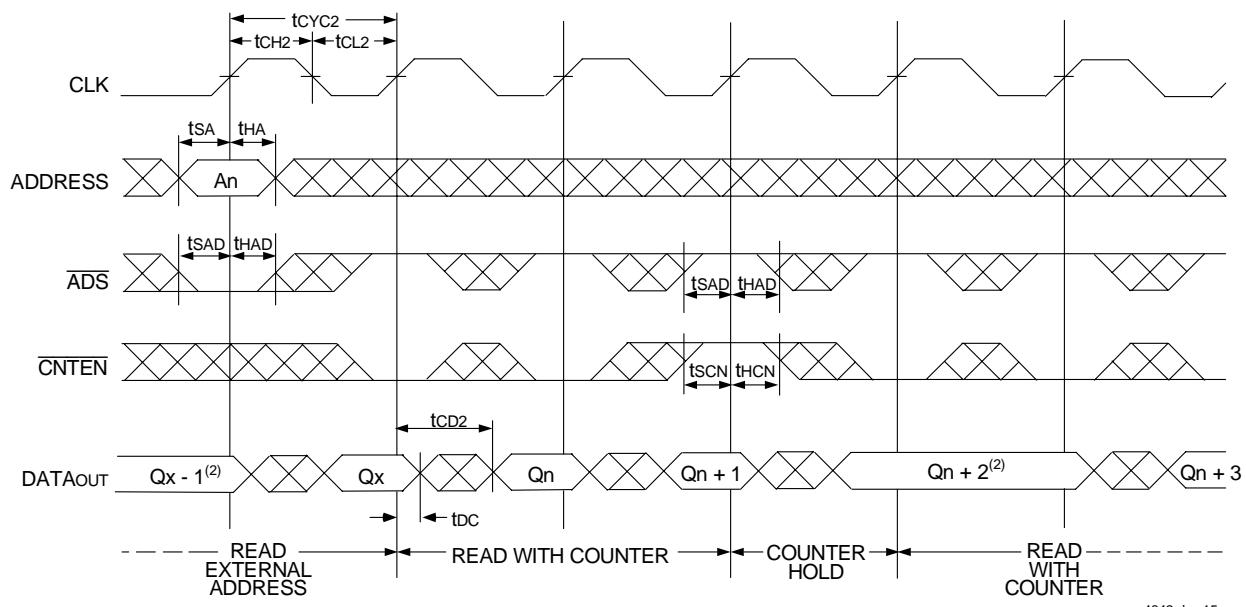
Timing Waveform of Flow-Through Read-to-Write-to-Read (\overline{OE} Controlled)⁽³⁾



NOTES:

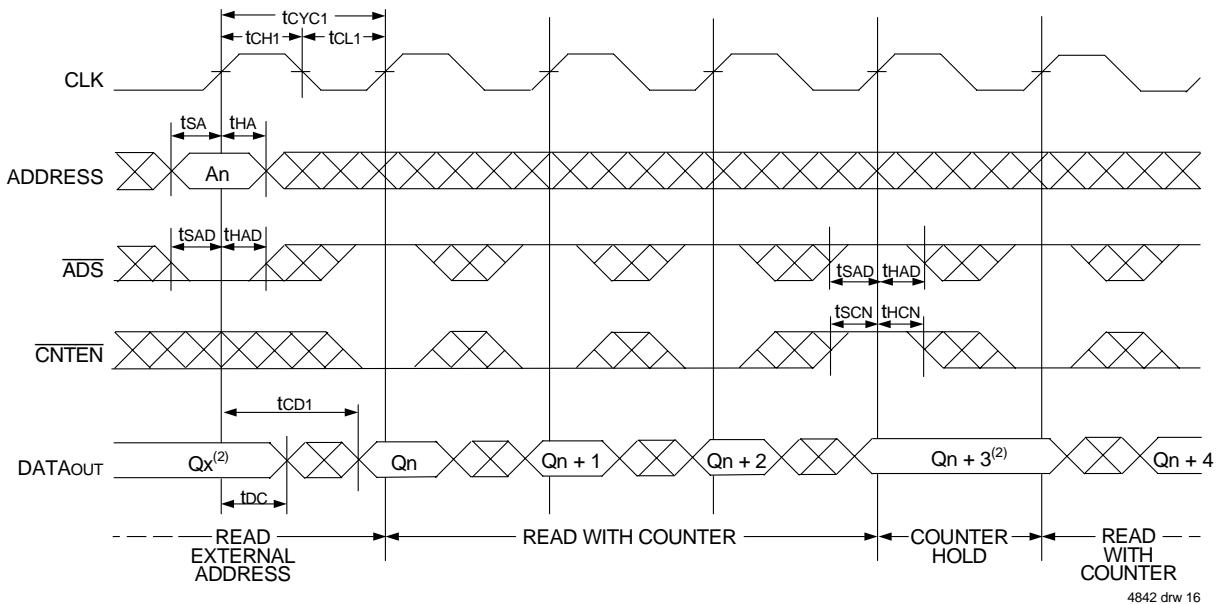
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. \overline{CE}_0 , \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; \overline{CE}_1 , \overline{CNTEN} , and $\overline{CNTRST} = V_{IH}$. "NOP" is "No Operation".
4. Addresses do not have to be accessed sequentially since $ADS = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Pipelined Read with Address Counter Advance⁽¹⁾



4842 drw 15

Timing Waveform of Flow-Through Read with Address Counter Advance⁽¹⁾

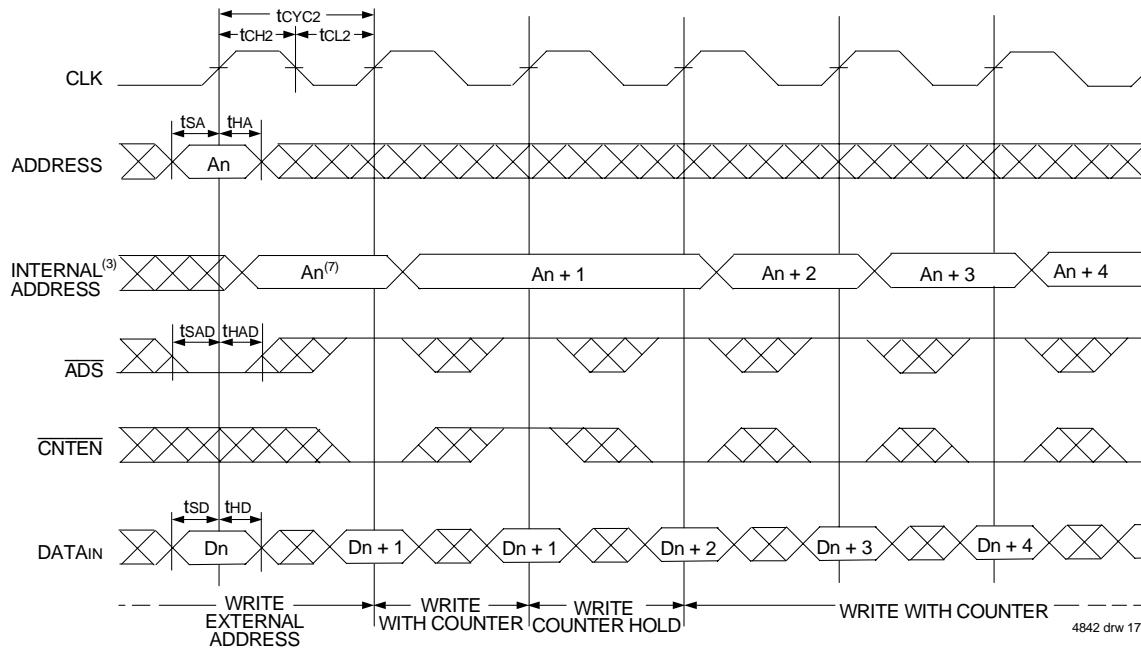


4842 drw 16

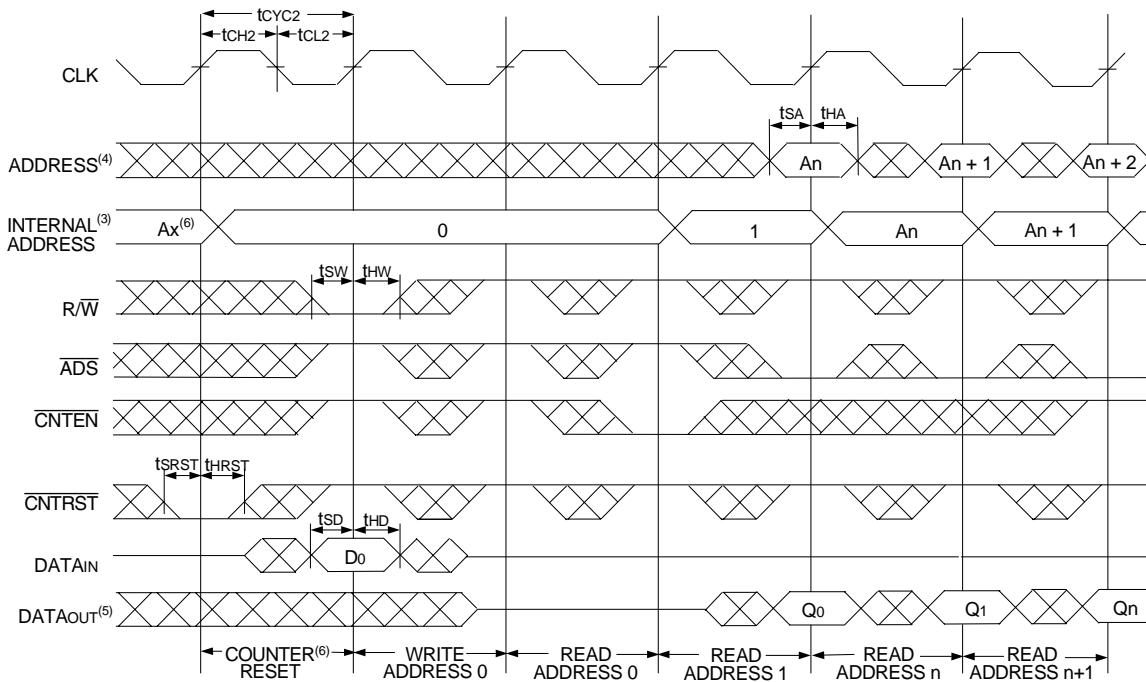
NOTES:

1. \overline{CE}_0 , \overline{OE} , \overline{UB} , and $\overline{LB} = V_{IL}$; CE_1 , R/W , and $\overline{CNTRST} = V_{IH}$.
2. If there is no address change via $\overline{ADS} = V_{IL}$ (loading a new address) or $\overline{CNTEN} = V_{IL}$ (advancing the address), i.e. $\overline{ADS} = V_{IH}$ and $\overline{CNTEN} = V_{IH}$, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance (Flow-Through or Pipelined Outputs)⁽¹⁾



Timing Waveform of Counter Reset (Pipelined Outputs)⁽²⁾



NOTES:

1. $\overline{CE}_0, \overline{UB}, \overline{LB}$, and $\overline{R/W} = V_{IL}$; CE_1 and $\overline{CNTRST} = V_{IH}$.
2. $\overline{CE}_0, \overline{UB}, \overline{LB} = V_{IL}$; $CE_1 = V_{IH}$.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS} = V_{IL}$ and equals the counter output when $\overline{ADS} = V_{IH}$.
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle.
7. $CNTEN = V_{IL}$ advances Internal Address from 'An' to 'An + 1'. The transition shown indicates the time required for the counter to advance. The 'An + 1' Address is written to during this cycle.

A Functional Description

The IDT709289 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

$\overline{CE}_0 = V_{IH}$ or $CE1 = V_{IL}$ for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT709289's for depth expansion configurations. When the Pipelined output mode is enabled, two cycles are required with $\overline{CE}_0 = V_{IL}$ and $CE1 = V_{IH}$ to reactivate the outputs.

Depth and Width Expansion

The IDT709289 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The 709289 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 32-bit or wider applications.

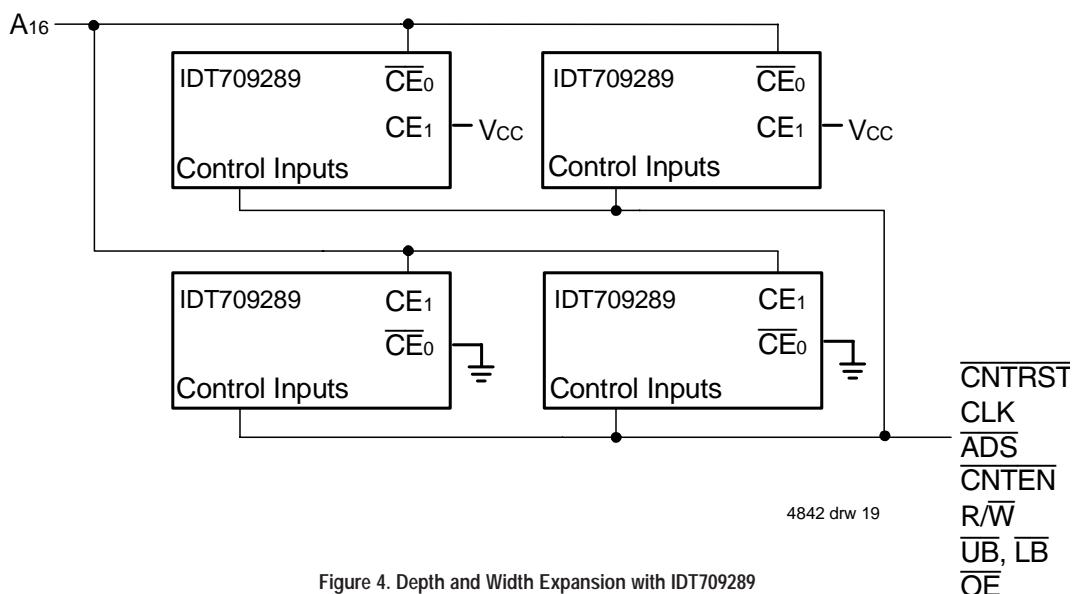
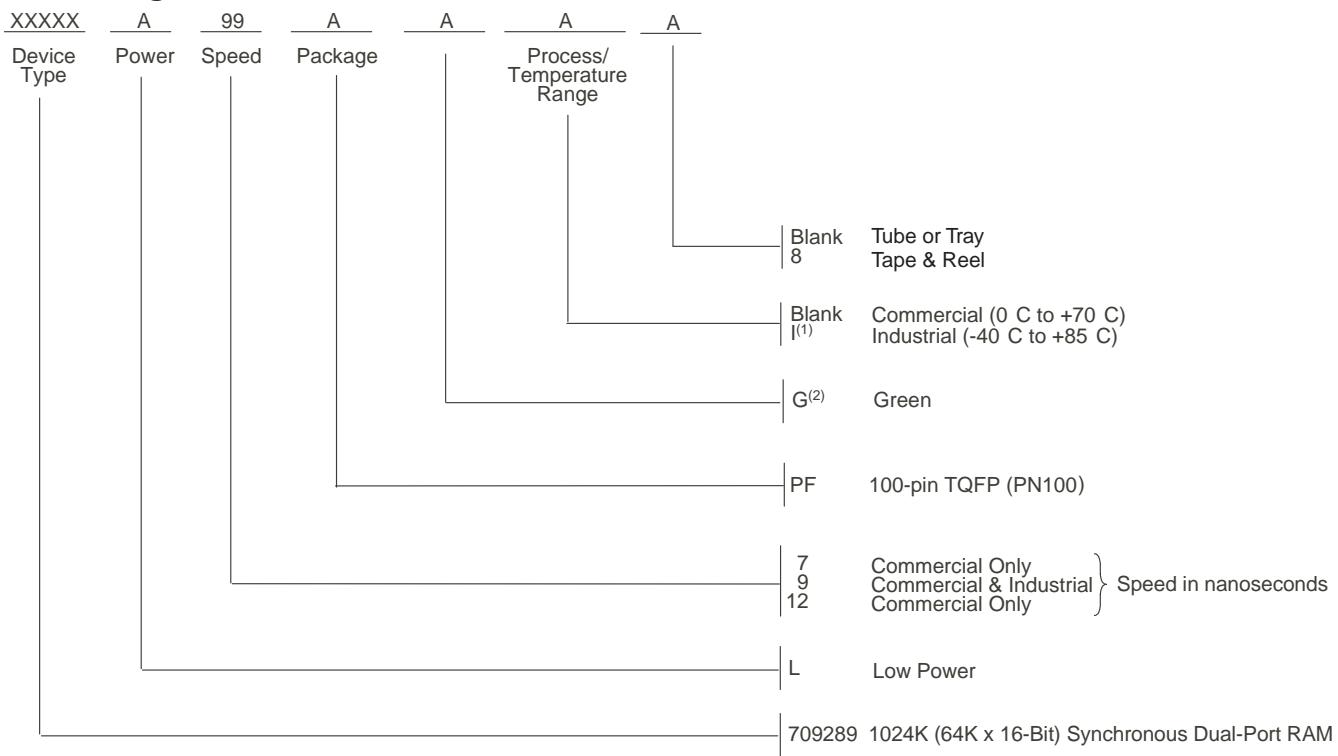


Figure 4. Depth and Width Expansion with IDT709289

Ordering Information



4842 drw 20

NOTES:

1. Industrial temperature range is available. For specific speeds, packages and powers contact your sales office.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.

LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

Datasheet Document History

| | |
|-----------|---|
| 9/30/99: | Initial Public Release |
| 11/10/99: | Replaced IDT logo |
| 12/22/99: | Page 1 Added missing diamond |
| 1/5/01: | Page 4 Changed information in Truth Table II Increased storage temperature parameter Clarified TA parameter Page 5 DC Electrical parameters—changed wording from "open" to "disabled" Changed ±200mV to 0mV in notes Removed Preliminary specification |
| 10/18/01: | Page 2 Added date revision for pin configuration Page 5 & 7 Added Industrial temp to column heading and values for 9ns speed to DC & AC Electrical Characteristics Page 15 Added Industrial temp offering to 9ns ordering information Page 4, 5 & 7 Removed Industrial temp footnote from all tables Page 1 & 15 Replace ™ logo with ® logo |

Datasheet Document History (con't on next page)

Datasheet Document History

05/05/06: Page 1 Added green availability to features
 Page 15 Added green indicator to ordering information

01/19/09: Page 15 Removed "IDT" from orderable part number

02/27/15: Page 2 Removed IDT in reference to fabrication
 Page 2 Removed date from PN100 pin configuration
 Page 2&15 The package code PN100-1 changed to PN100 to match standard package codes,
 Page 6 Removed typo from typical output derating drawing
 Page 15 Added Tape & Reel to the Ordering Information

02/26/18: Product Discontinuation Notice - PDN# SP-17-02
 Last time buy expires June 15, 2018

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.