



HIGH-SPEED 3.3V 8/4K x 18 SYNCHRONOUS PIPELINED DUAL-PORT STATIC RAM

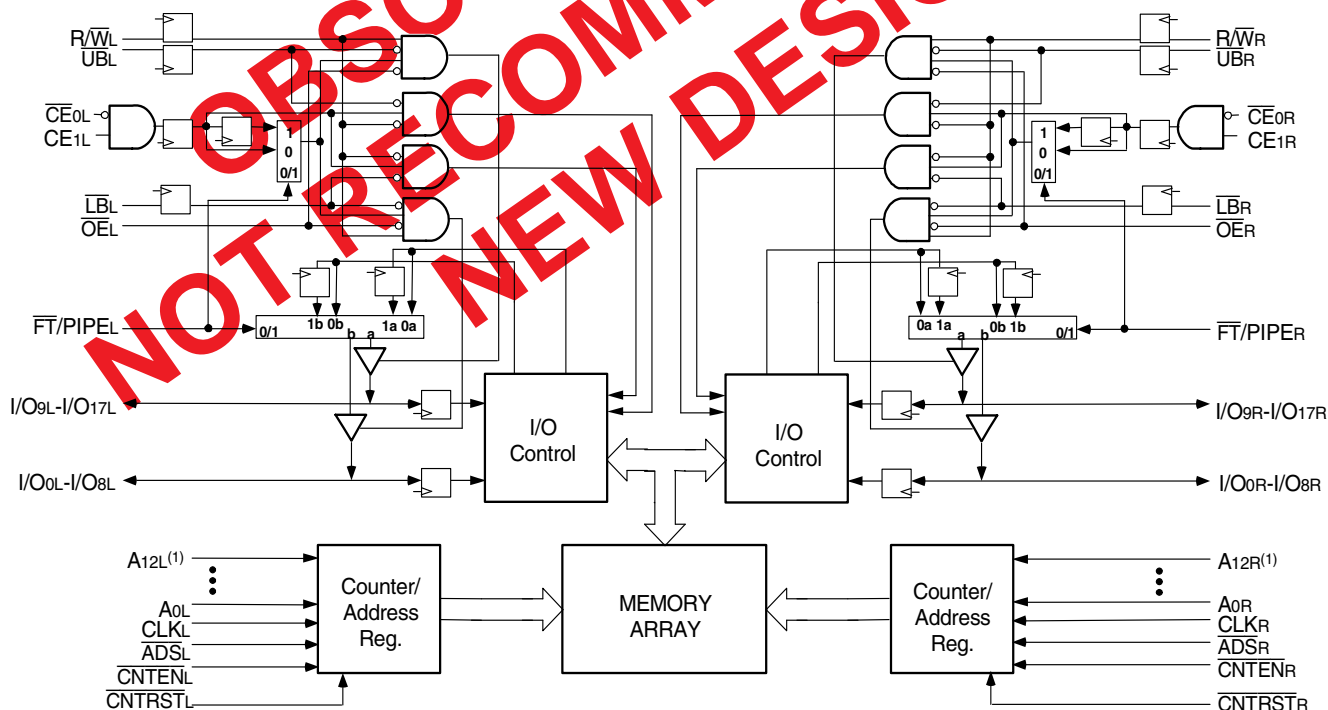
IDT70V9359/49L
OBSOLETE PARTS

LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

Features:

- ♦ True Dual-Ported memory cells which allow simultaneous access of the same memory location
- ♦ High-speed clock to data access
 - Commercial: 6.5/7.5/9ns (max.)
 - Industrial: 7.5ns (max.)
- ♦ Low-power operation
 - IDT70V9359/49L
 - Active: 450mW (typ.)
 - Standby: 1.5mW (typ.)
- ♦ Flow-Through or Pipelined output mode on either port via the $\overline{\text{FT}}/\text{PIPE}$ pins
- ♦ Counter enable and reset features
- ♦ Dual chip enables allow for depth expansion without additional logic
- ♦ Full synchronous operation on both ports
 - 3.5ns setup to clock and 0ns hold on all control, data, and address inputs
 - Data input, address, and control registers
 - Fast 6.5ns clock to data out in the Pipelined output mode
 - Self-timed write allows fast cycle time
 - 10ns cycle time, 100MHz operation in Pipelined output mode
- ♦ Separate upper byte and lower-byte controls for multiplexed bus and bus matching compatibility
- ♦ LVTTTL-compatible, single 3.3V ($\pm 0.3\text{V}$) power supply
- ♦ Industrial temperature range (-40°C to $+85^\circ\text{C}$) is available for 83 MHz
- ♦ Available in a 100-pin Thin Quad Flatpack (TQFP) and 100-pin Fine Pitch Ball Grid Array (FPBGA) packages
- ♦ Green parts available, see ordering information

Functional Block Diagram



NOTE:

1. A12 is a NC for IDT70V9349.

5638 drw 01

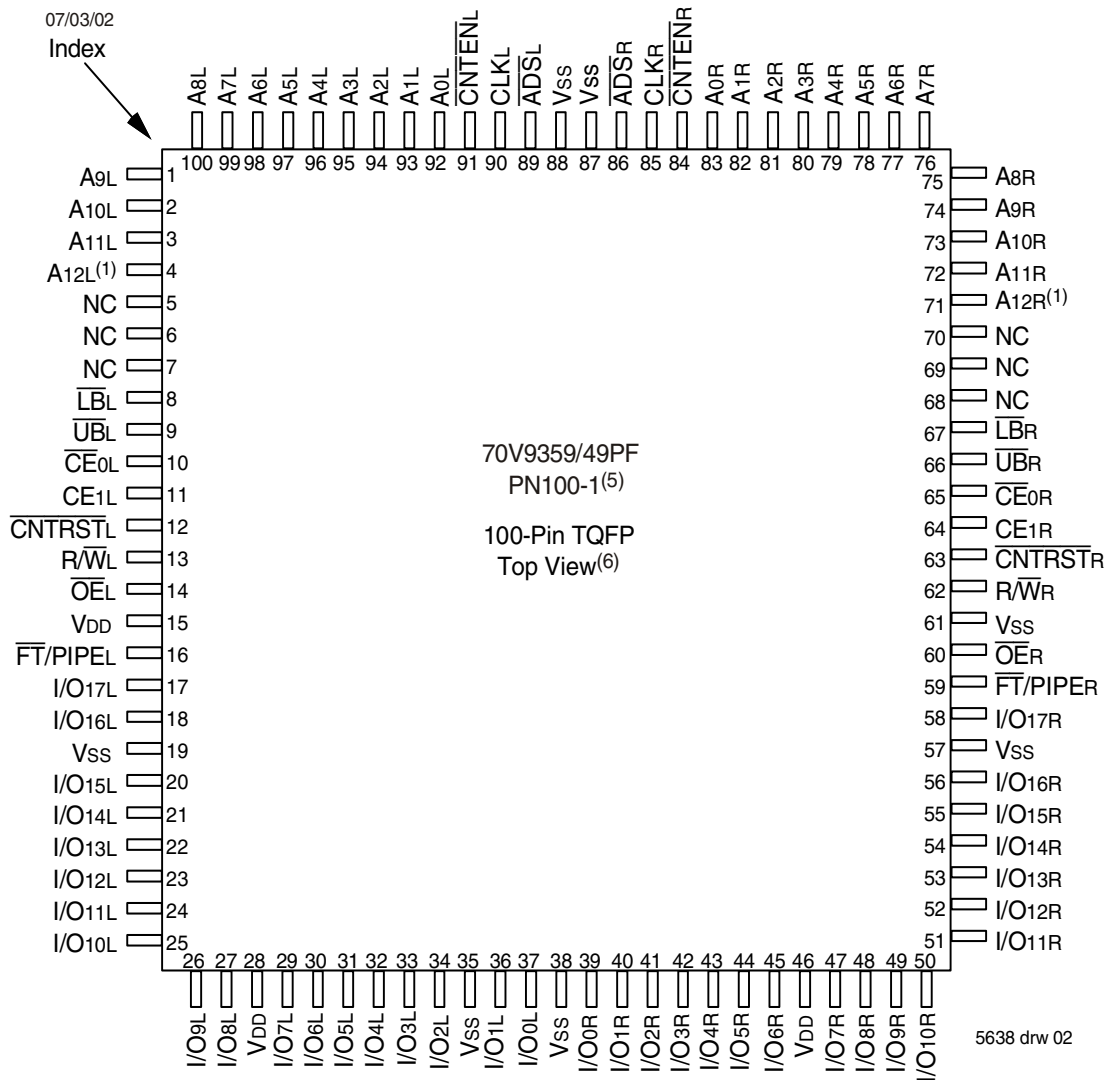
MARCH 2018

Description:

The IDT70V9359/49 is a high-speed 8/4K x 18 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times.

With an input data register, the IDT70V9359/49 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{CE_0}$ and CE_1 , permits the on-chip circuitry of each port to enter a very low standby power mode. Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 450mW of power.

Pin Configurations^(1,2,3,4)



NOTES:

1. A12 is a NC for IDT70V9349.
2. All V_{DD} pins must be connected to power supply.
3. All V_{SS} pins must be connected to ground supply.
4. Package body is approximately 14mm x 14mm x 1.4mm.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configurations(cont'd)^(1,2,3,4)

70V9359/49BF

BF100⁽⁵⁾

100-Pin fpBGA

Top View⁽⁶⁾

07/03/02

| | | | | | | | | | |
|--|--|--|--|---|---|---|--------------|--------------|---------------|
| A1 A8R | A2 A11R | A3 $\overline{\text{UBR}}$ | A4 $\overline{\text{CNTRST}}_{\text{TR}}$ | A5 Vss | A6 Vss | A7 Vss | A8 I/O13R | A9 I/O10R | A10 I/O17R |
| B1 A6R | B2 A7R | B3 A10R | B4 A12R ⁽¹⁾ | B5 $\text{R}/\overline{\text{WL}}$ | B6 $\overline{\text{OER}}$ | B7 $\text{PL}/\overline{\text{FT}}_{\text{R}}$ | B8 I/O12R | B9 I/O9R | B10 I/O6R |
| C1 A3R | C2 A4R | C3 A5R | C4 A9R | C5 CE1R | C6 I/O16R | C7 I/O15R | C8 I/O11R | C9 I/O7R | C10 I/O3R |
| D1 A0R | D2 CLKR | D3 A1R | D4 A2R | D5 $\overline{\text{LBR}}$ | D6 $\overline{\text{CE}}_{\text{OR}}$ | D7 I/O14R | D8 I/O8R | D9 I/O5R | D10 I/O1R |
| E1 Vss | E2 $\overline{\text{ADS}}_{\text{R}}$ | E3 $\overline{\text{CNTEN}}_{\text{R}}$ | E4 A1L | E5 $\overline{\text{ADSL}}$ | E6 Vss | E7 I/O4R | E8 I/O2R | E9 I/O0R | E10 VDD |
| F1 Vss | F2 CLKL | F3 A0L | F4 A3L | F5 VDD | F6 Vss | F7 VDD | F8 I/O2L | F9 I/O1L | F10 I/O0L |
| G1 $\overline{\text{CNTEN}}_{\text{L}}$ | G2 A4L | G3 A7L | G4 $\overline{\text{UBL}}$ | G5 Vss | G6 I/O13L | G7 NC | G8 I/O4L | G9 Vss | G10 I/O3L |
| H1 A2L | H2 A6L | H3 A11L | H4 $\overline{\text{CE}}_{\text{OL}}$ | H5 $\overline{\text{CNTRST}}_{\text{L}}$ | H6 I/O15L | H7 I/O9L | H8 I/O7L | H9 I/O6L | H10 I/O5L |
| J1 A5L | J2 A9L | J3 A12L ⁽¹⁾ | J4 $\text{R}/\overline{\text{WL}}$ | J5 $\overline{\text{OEL}}$ | J6 $\text{PL}/\overline{\text{FT}}_{\text{L}}$ | J7 I/O12L | J8 I/O10L | J9 Vss | J10 I/O8L |
| K1 A8L | K2 A10L | K3 $\overline{\text{LBL}}$ | K4 CE1L | K5 VDD | K6 VDD | K7 I/O16L | K8 I/O14L | K9 I/O11L | K10 I/O17L |

5638 drw 03

NOTES:

1. A12 is a NC for IDT70V9349.
2. All VDD pins must be connected to power supply.
3. All Vss pins must be connected to ground supply.
4. Package body is approximately 10mm x 10mm x 1.4mm with 0.8mm ball pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Names

| Left Port | Right Port | Names |
|----------------------------------|----------------------------------|----------------------------------|
| \overline{CE}_{0L} , CE_{1L} | \overline{CE}_{0R} , CE_{1R} | Chip Enables ⁽³⁾ |
| R/\overline{WL} | R/\overline{WR} | Read/Write Enable |
| \overline{OE}_L | \overline{OE}_R | Output Enable |
| $A_{0L} - A_{12L}^{(1)}$ | $A_{0R} - A_{12R}^{(1)}$ | Address |
| $I/O_{0L} - I/O_{17L}$ | $I/O_{0R} - I/O_{17R}$ | Data Input/Output |
| CLK_L | CLK_R | Clock |
| \overline{UB}_L | \overline{UB}_R | Upper Byte Select ⁽²⁾ |
| \overline{LB}_L | \overline{LB}_R | Lower Byte Select ⁽²⁾ |
| \overline{ADS}_L | \overline{ADS}_R | Address Strobe Enable |
| \overline{CNTEN}_L | \overline{CNTEN}_R | Counter Enable |
| \overline{CNTRST}_L | \overline{CNTRST}_R | Counter Reset |
| $\overline{FT}/PIPE_L$ | $\overline{FT}/PIPE_R$ | Flow-Through / Pipeline |
| V_{DD} | | Power (3.3V) |
| V_{SS} | | Ground (0V) |

5638 tbl 01

NOTE:

1. A_{12} is a NC for IDT70V9349.
2. \overline{LB} and \overline{UB} are single buffered regardless of state of $\overline{FT}/PIPE$.
3. \overline{CE}_0 and CE_1 are single buffered when $\overline{FT}/PIPE = V_{IL}$,
 \overline{CE}_0 and CE_1 are double buffered when $\overline{FT}/PIPE = V_{IH}$,
i.e. the signals take two cycles to deselect.

Truth Table I—Read/Write and Enable Control^(1,2,3)

| \overline{OE} | CLK | $\overline{CE}_0^{(5)}$ | $CE_1^{(5)}$ | $\overline{UB}^{(4)}$ | $\overline{LB}^{(4)}$ | R/\overline{W} | Upper Byte I/O_{9-17} | Lower Byte I/O_{0-8} | MODE |
|-----------------|-----|-------------------------|--------------|-----------------------|-----------------------|------------------|----------------------------|---------------------------|--------------------------|
| X | ↑ | H | X | X | X | X | High-Z | High-Z | Deselected—Power Down |
| X | ↑ | X | L | X | X | X | High-Z | High-Z | Deselected—Power Down |
| X | ↑ | L | H | H | H | X | High-Z | High-Z | Both Bytes Deselected |
| X | ↑ | L | H | L | H | L | DATA _{IN} | High-Z | Write to Upper Byte Only |
| X | ↑ | L | H | H | L | L | High-Z | DATA _{IN} | Write to Lower Byte Only |
| X | ↑ | L | H | L | L | L | DATA _{IN} | DATA _{IN} | Write to Both Bytes |
| L | ↑ | L | H | L | H | H | DATA _{OUT} | High-Z | Read Upper Byte Only |
| L | ↑ | L | H | H | L | H | High-Z | DATA _{OUT} | Read Lower Byte Only |
| L | ↑ | L | H | L | L | H | DATA _{OUT} | DATA _{OUT} | Read Both Bytes |
| H | X | L | H | X | X | X | High-Z | High-Z | Outputs Disabled |

5638 tbl 02

NOTES:

1. "H" = V_{IH} , "L" = V_{IL} , "X" = Don't Care.
2. \overline{ADS} , \overline{CNTEN} , \overline{CNTRST} = X.
3. \overline{OE} is an asynchronous input signal.
4. \overline{LB} and \overline{UB} are single buffered regardless of state of $\overline{FT}/PIPE$.
5. \overline{CE}_0 and CE_1 are single buffered when $\overline{FT}/PIPE = V_{IL}$. \overline{CE}_0 and CE_1 are double buffered when $\overline{FT}/PIPE = V_{IH}$, i.e. the signals take two cycles to deselect.

Truth Table II—Address Counter Control^(1,2)

| External Address | Previous Internal Address | Internal Address Used | CLK | \overline{ADS} | \overline{CNTEN} | \overline{CNRST} | I/O ⁽³⁾ | MODE |
|------------------|---------------------------|-----------------------|-----|------------------|--------------------|--------------------|-----------------------|---|
| An | X | An | ↑ | L ⁽⁴⁾ | X | H | D _{IO} (n) | External Address Used |
| X | An | An + 1 | ↑ | H | L ⁽⁵⁾ | H | D _{IO} (n+1) | Counter Enabled—Internal Address generation |
| X | An + 1 | An + 1 | ↑ | H | H | H | D _{IO} (n+1) | External Address Blocked—Counter disabled (An + 1 reused) |
| X | X | A0 | ↑ | X | X | L ⁽⁴⁾ | D _{IO} (0) | Counter Reset to Address 0 |

NOTES:

5638 tbl 03

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- $\overline{CE_0}$, \overline{LB} , \overline{UB} , and \overline{OE} = V_{IL}; CE₁ and R/W = V_{IH}.
- Outputs configured in Flow-Through Output mode: if outputs are in Pipelined mode the data out will be delayed by one cycle.
- \overline{ADS} and \overline{CNRST} are independent of all other signals including $\overline{CE_0}$, CE₁, \overline{UB} and \overline{LB} .
- The address counter advances if \overline{CNTEN} = V_{IL} on the rising edge of CLK, regardless of all other signals including $\overline{CE_0}$, CE₁, \overline{UB} and \overline{LB} .

Recommended Operating Temperature and Supply Voltage

| Grade | Ambient Temperature ⁽¹⁾ | GND | V _{DD} |
|------------|------------------------------------|-----|-----------------|
| Commercial | 0°C to +70°C | 0V | 3.3V ± 0.3V |
| Industrial | -40°C to +85°C | 0V | 3.3V ± 0.3V |

5638 tbl 04

NOTES:

- This is the parameter T_A. This is the "instant on" case temperature.

Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------------|--------------------|---------------------|------|--------------------------------------|------|
| V _{DD} | Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| V _{SS} | Ground | 0 | 0 | 0 | V |
| V _{IH} | Input High Voltage | 2.0 | — | V _{DD} +0.3V ⁽²⁾ | V |
| V _{IL} | Input Low Voltage | -0.3 ⁽¹⁾ | — | 0.8 | V |

5638 tbl 05

NOTES:

- V_{IL} ≥ -1.5V for pulse width less than 10 ns.
- V_{TERM} must not exceed V_{DD}+0.3V.

Absolute Maximum Ratings⁽¹⁾

| Symbol | Rating | Commercial & Industrial | Unit |
|----------------------------------|--------------------------------------|-------------------------|------|
| V _{TERM} ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +4.6 | V |
| T _{BIAS} | Temperature Under Bias | -55 to +125 | °C |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| I _{OUT} | DC Output Current | 50 | mA |

5638 tbl 06

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed V_{DD} + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ V_{DD} + 0.3V.

Capacitance⁽¹⁾(T_A = +25°C, f = 1.0MHz)

| Symbol | Parameter | Conditions ⁽²⁾ | Max. | Unit |
|---------------------------------|--------------------|---------------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 3dV | 9 | pF |
| C _{OUT} ⁽³⁾ | Output Capacitance | V _{OUT} = 3dV | 10 | pF |

5638 tbl 07

NOTES:

- These parameters are determined by device characterization, but are not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
- C_{OUT} also references C_{I/O}.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{DD} = 3.3V \pm 0.3V$)

| Symbol | Parameter | Test Conditions | 70V9359/49L | | Unit |
|------------|--------------------------------------|---|-------------|------|---------|
| | | | Min. | Max. | |
| $ I_{LI} $ | Input Leakage Current ⁽¹⁾ | $V_{DD} = 3.6V, V_{IN} = 0V$ to V_{DD} | — | 5 | μA |
| $ I_{LO} $ | Output Leakage Current | $\overline{CE} = V_{IH}$ or $CE_1 = V_{IL}, V_{OUT} = 0V$ to V_{DD} | — | 5 | μA |
| V_{OL} | Output Low Voltage | $I_{OL} = +4mA$ | — | 0.4 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -4mA$ | 2.4 | — | V |

NOTE:

5638 tbl 08

1. At $V_{DD} \leq 2.0V$ input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature Supply Voltage Range⁽³⁾ ($V_{DD} = 3.3V \pm 0.3V$)

| Symbol | Parameter | Test Condition | Version | 70V9359/49L6 Com'l Only | | 70V9359/49L7 Com'l & Ind | | 70V9359/49L9 Com'l Only | | Unit |
|----------|---|--|---------|----------------------------|------|-----------------------------|------|----------------------------|------|------|
| | | | | Typ. ⁽⁴⁾ | Max. | Typ. ⁽⁴⁾ | Max. | Typ. ⁽⁴⁾ | Max. | |
| I_{DD} | Dynamic Operating Current (Both Ports Active) | \overline{CE}_L and $\overline{CE}_R = V_{IL}$, Outputs Disabled, $f = f_{MAX}$ ⁽¹⁾ | COM'L L | 175 | 330 | 155 | 280 | 135 | 230 | mA |
| | | | IND L | — | — | 155 | 330 | — | — | |
| ISB1 | Standby Current (Both Ports - TTL Level Inputs) | $\overline{CE}_L = \overline{CE}_R = V_{IH}$ $f = f_{MAX}$ ⁽¹⁾ | COM'L L | 50 | 80 | 40 | 70 | 30 | 60 | mA |
| | | | IND L | — | — | 40 | 80 | — | — | |
| ISB2 | Standby Current (One Port - TTL Level Inputs) | $\overline{CE}^*A = V_{IL}$ and $\overline{CE}^*B = V_{IH}$ ⁽⁶⁾ Active Port Outputs Disabled, $f = f_{MAX}$ ⁽¹⁾ | COM'L L | 115 | 185 | 105 | 170 | 95 | 155 | mA |
| | | | IND L | — | — | 105 | 180 | — | — | |
| ISB3 | Full Standby Current (Both Ports - CMOS Level Inputs) | Both Ports \overline{CE}_L and $\overline{CE}_R \geq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V, f = 0$ ⁽²⁾ | COM'L L | 0.5 | 3.0 | 0.5 | 3.0 | 0.5 | 3.0 | mA |
| | | | IND L | — | — | 0.5 | 3.0 | — | — | |
| ISB4 | Full Standby Current (One Port - CMOS Level Inputs) | $\overline{CE}^*A \leq 0.2V$ and $\overline{CE}^*B \geq V_{DD} - 0.2V$ ⁽⁶⁾ $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$, Active Port, Outputs Disabled, $f = f_{MAX}$ ⁽¹⁾ | COM'L L | 105 | 175 | 95 | 160 | 85 | 145 | mA |
| | | | IND L | — | — | 95 | 175 | — | — | |

5638 tbl 09

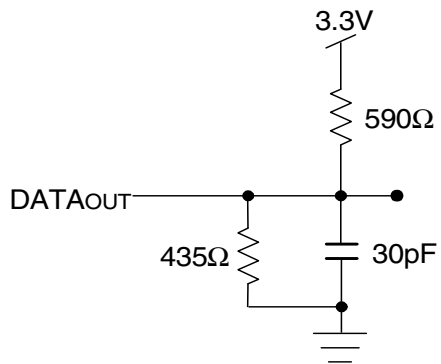
NOTES:

- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of $1/t_{cyc}$, using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$ means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 3.3V, T_A = 25^\circ C$ for Typ, and are not production tested. $I_{CC DC}(f=0) = 90mA$ (Typ).
- $\overline{CE}_X = V_{IL}$ means $\overline{CE}_{0X} = V_{IL}$ and $CE_{1X} = V_{IH}$
 $\overline{CE}_X = V_{IH}$ means $\overline{CE}_{0X} = V_{IH}$ or $CE_{1X} = V_{IL}$
 $\overline{CE}_X \leq 0.2V$ means $\overline{CE}_{0X} \leq 0.2V$ and $CE_{1X} \geq V_{DD} - 0.2V$
 $\overline{CE}_X \geq V_{DD} - 0.2V$ means $\overline{CE}_{0X} \geq V_{DD} - 0.2V$ or $CE_{1X} \leq 0.2V$
 "X" represents "L" for left port or "R" for right port.

AC Test Conditions

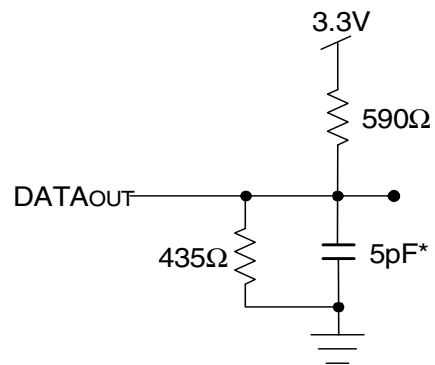
| | |
|-------------------------------|---------------------|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 2ns Max. |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| Output Load | Figures 1, 2, and 3 |

5638 tbl 10



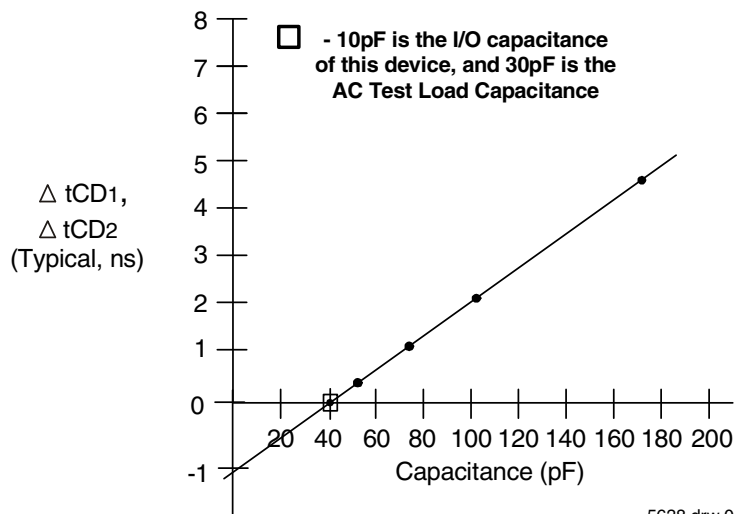
5638 drw 04

Figure 1. AC Output Test load.



5638 drw 05

Figure 2. Output Test Load
(For t_{CKLZ} , t_{CKHZ} , t_{OLZ} , and t_{OHZ}).
*Including scope and jig.



5638 drw 06

Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)⁽³⁾ ($V_{DD} = 3.3V \pm 0.3V$)

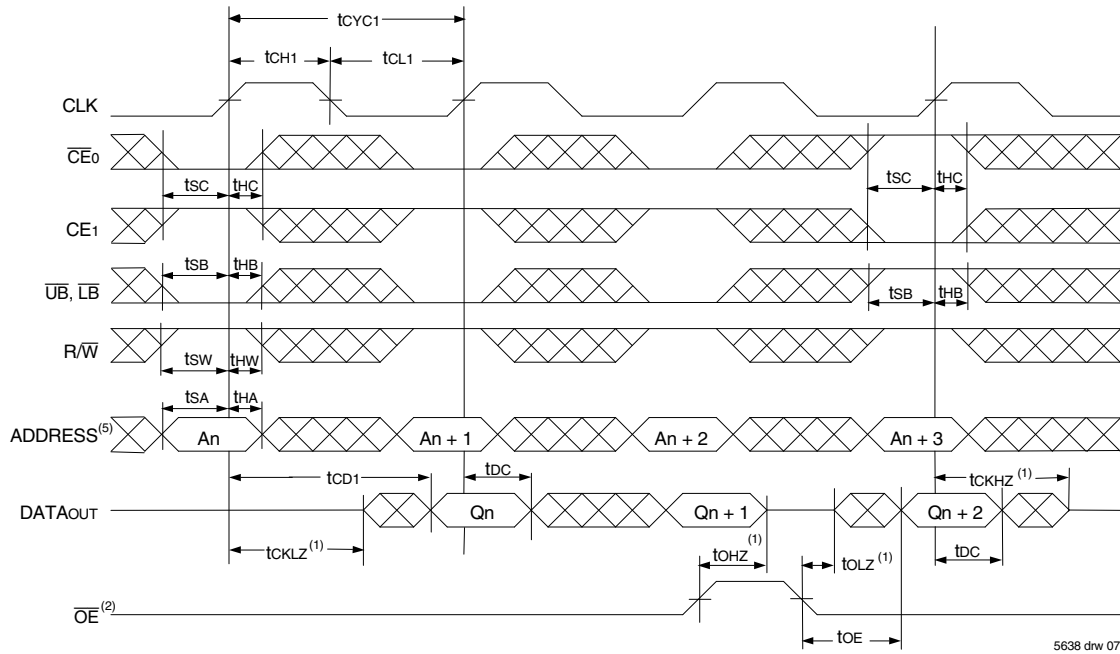
| Symbol | Parameter | 70V9359/49L6 Com'l Only | | 70V9359/49L7 Com'l & Ind | | 70V9359/49L9 Com'l Only | | Unit |
|---------------------------|---|----------------------------|------|-----------------------------|------|----------------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{CYC1} | Clock Cycle Time (Flow-Through) ⁽²⁾ | 19 | — | 22 | — | 25 | — | ns |
| t _{CYC2} | Clock Cycle Time (Pipelined) ⁽²⁾ | 10 | — | 12 | — | 15 | — | ns |
| t _{CH1} | Clock High Time (Flow-Through) ⁽²⁾ | 6.5 | — | 7.5 | — | 12 | — | ns |
| t _{CL1} | Clock Low Time (Flow-Through) ⁽²⁾ | 6.5 | — | 7.5 | — | 12 | — | ns |
| t _{CH2} | Clock High Time (Pipelined) ⁽²⁾ | 4 | — | 5 | — | 6 | — | ns |
| t _{CL2} | Clock Low Time (Pipelined) ⁽²⁾ | 4 | — | 5 | — | 6 | — | ns |
| t _r | Clock Rise Time | — | 3 | — | 3 | — | 3 | ns |
| t _f | Clock Fall Time | — | 3 | — | 3 | — | 3 | ns |
| t _{SA} | Address Setup Time | 3.5 | — | 4 | — | 4 | — | ns |
| t _{HA} | Address Hold Time | 0 | — | 0 | — | 1 | — | ns |
| t _{SC} | Chip Enable Setup Time | 3.5 | — | 4 | — | 4 | — | ns |
| t _{HC} | Chip Enable Hold Time | 0 | — | 0 | — | 1 | — | ns |
| t _{SB} | Byte Enable Setup Time | 3.5 | — | 4 | — | 4 | — | ns |
| t _{HB} | Byte Enable Hold Time | 0 | — | 0 | — | 1 | — | ns |
| t _{SW} | R/W Setup Time | 3.5 | — | 4 | — | 4 | — | ns |
| t _{HW} | R/W Hold Time | 0 | — | 0 | — | 1 | — | ns |
| t _{SD} | Input Data Setup Time | 3.5 | — | 4 | — | 4 | — | ns |
| t _{HD} | Input Data Hold Time | 0 | — | 0 | — | 1 | — | ns |
| t _{SAD} | \overline{ADS} Setup Time | 3.5 | — | 4 | — | 4 | — | ns |
| t _{HAD} | \overline{ADS} Hold Time | 0 | — | 0 | — | 1 | — | ns |
| t _{SCN} | \overline{CNTEN} Setup Time | 3.5 | — | 4 | — | 4 | — | ns |
| t _{HCN} | \overline{CNTEN} Hold Time | 0 | — | 0 | — | 1 | — | ns |
| t _{SRST} | \overline{CNTRST} Setup Time | 3.5 | — | 4 | — | 4 | — | ns |
| t _{HRST} | \overline{CNTRST} Hold Time | 0 | — | 0 | — | 1 | — | ns |
| t _{OE} | Output Enable to Data Valid | — | 6.5 | — | 7.5 | — | 9 | ns |
| t _{OLZ} | Output Enable to Output Low-Z ⁽¹⁾ | 2 | — | 2 | — | 2 | — | ns |
| t _{OHZ} | Output Enable to Output High-Z ⁽¹⁾ | 1 | 7 | 1 | 7 | 1 | 7 | ns |
| t _{CD1} | Clock to Data Valid (Flow-Through) ⁽²⁾ | — | 15 | — | 18 | — | 20 | ns |
| t _{CD2} | Clock to Data Valid (Pipelined) ⁽²⁾ | — | 6.5 | — | 7.5 | — | 9 | ns |
| t _{DC} | Data Output Hold After Clock High | 2 | — | 2 | — | 2 | — | ns |
| t _{CKHZ} | Clock High to Output High-Z ⁽¹⁾ | 2 | 9 | 2 | 9 | 2 | 9 | ns |
| t _{CKLZ} | Clock High to Output Low-Z ⁽¹⁾ | 2 | — | 2 | — | 2 | — | ns |
| Port-to-Port Delay | | | | | | | | |
| t _{CWDD} | Write Port Clock High to Read Data Delay | — | 24 | — | 28 | — | 35 | ns |
| t _{CSS} | Clock-to-Clock Setup Time | — | 9 | — | 10 | — | 15 | ns |

NOTES:

5638 tbl 11

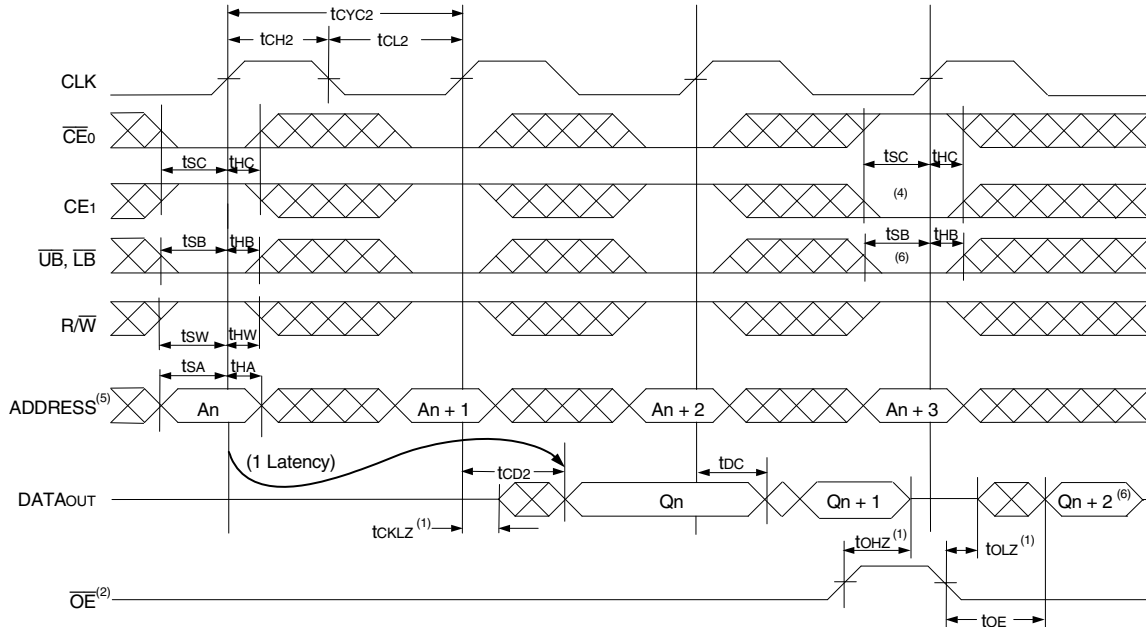
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
2. The Pipelined output parameters (t_{CYC2}, t_{CD2}) apply to either or both the Left and Right ports when $\overline{FT}/PIPE = V_{IH}$. Flow-through parameters (t_{CYC1}, t_{CD1}) apply when $\overline{FT}/PIPE = V_{IL}$ for that port.
3. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable (\overline{OE}), $\overline{FT}/PIPE_R$, and $\overline{FT}/PIPE_L$.

Timing Waveform of Read Cycle for Flow-Through Output

 $(\overline{\text{FT}}/\text{PIPE} "X" = V_{\text{IL}})^{(3,7)}$ 

5638 drw 07

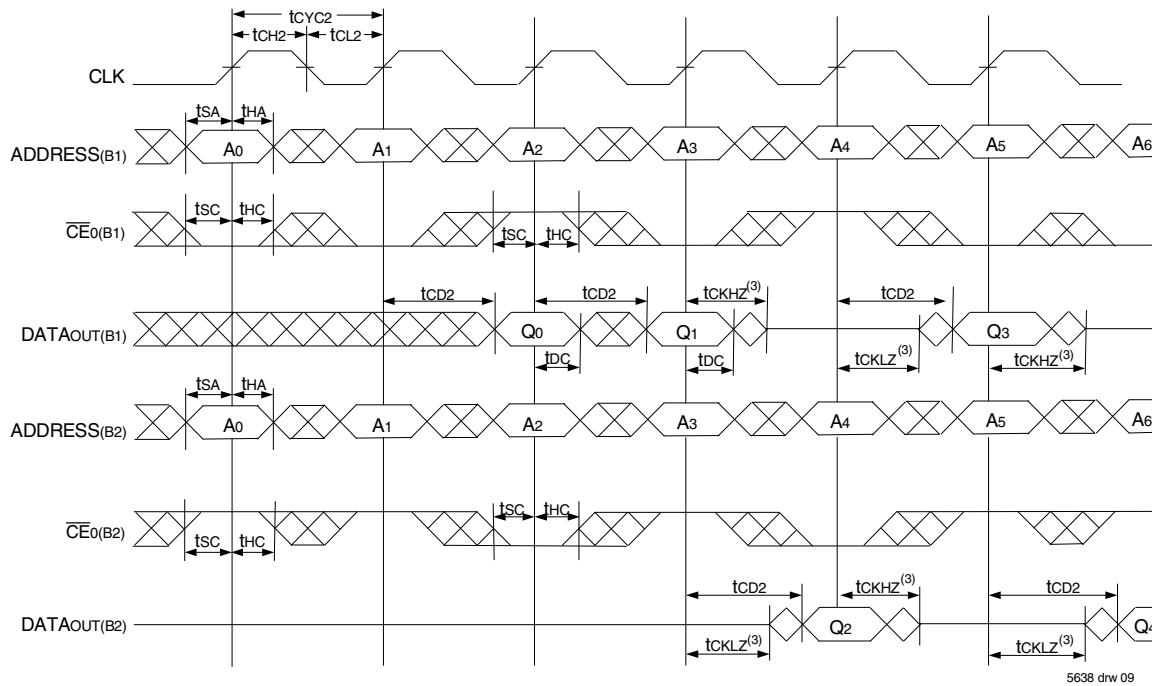
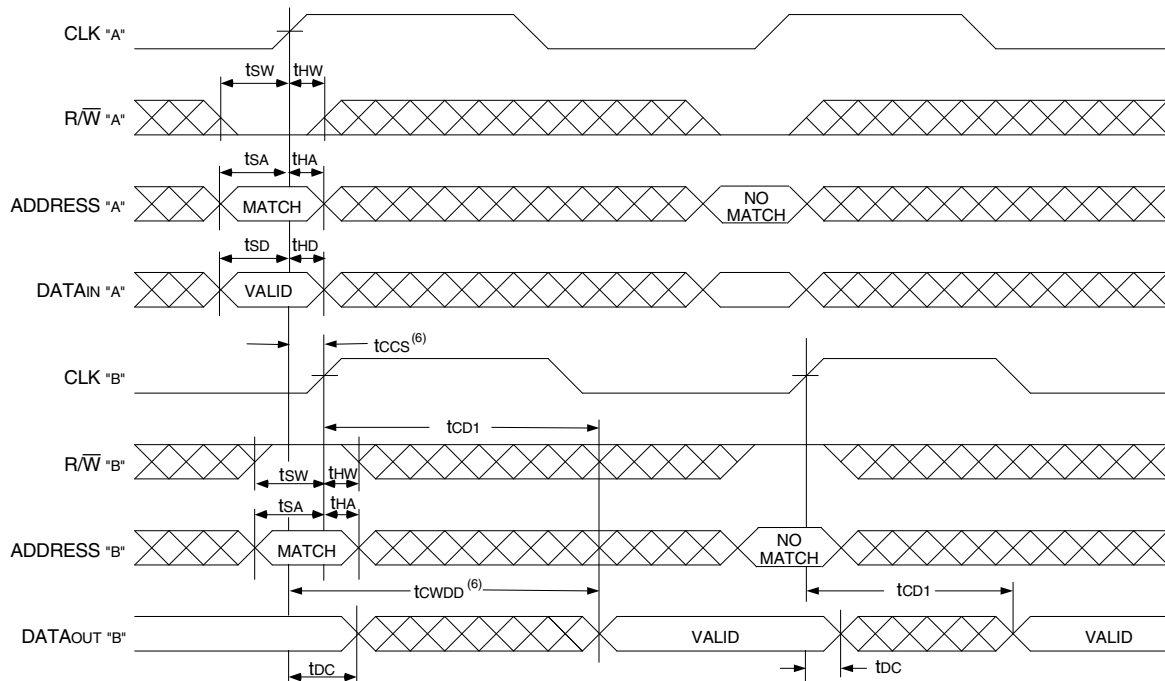
Timing Waveform of Read Cycle for Pipelined Operation

 $(\overline{\text{FT}}/\text{PIPE} "X" = V_{\text{IH}})^{(3,7)}$ 

5638 drw 08

NOTES:

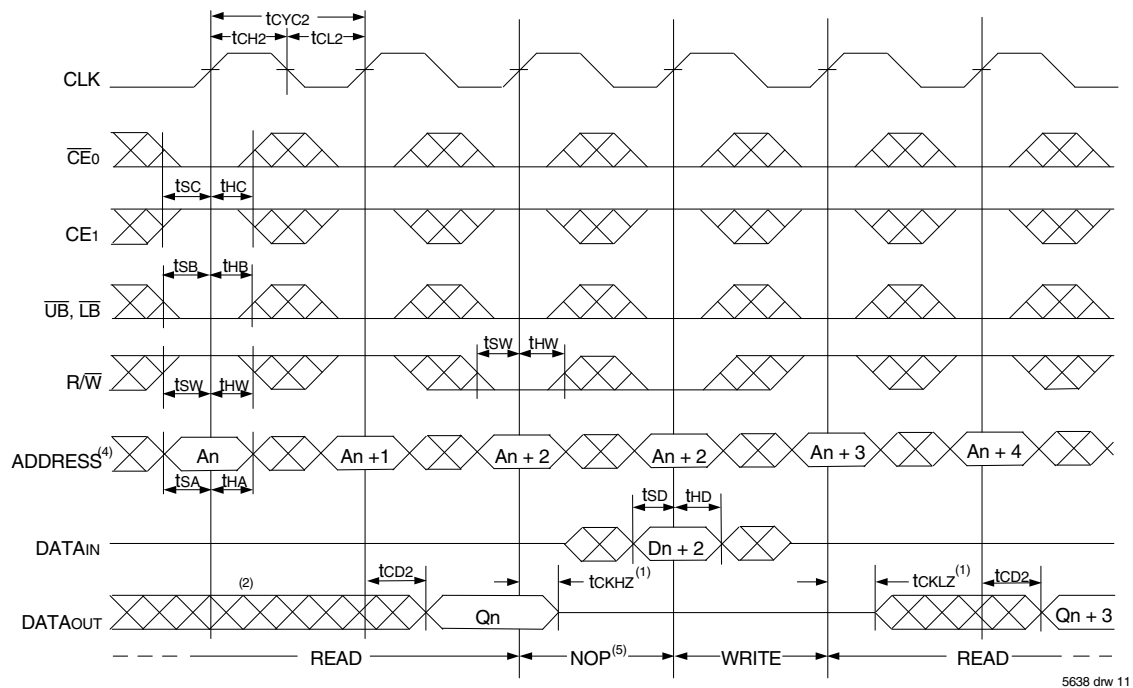
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $\overline{\text{OE}}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
3. $\overline{\text{ADS}} = V_{\text{IL}}$ and $\overline{\text{CNTRST}} = V_{\text{IH}}$.
4. The output is disabled (High-Impedance state) by $\overline{\text{CE}}_0 = V_{\text{IH}}$, $\text{CE}_1 = V_{\text{IL}}$ following the next rising edge of the clock. Refer to Truth Table 1.
5. Addresses do not have to be accessed sequentially since $\overline{\text{ADS}} = V_{\text{IL}}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
6. If $\overline{\text{UB}}$ or $\overline{\text{LB}}$ was HIGH, then the Upper Byte and/or Lower Byte of DATAOUT for Q_{n+2} would be disabled (High-Impedance state).
7. "X" here denotes Left or Right port. The diagram is with respect to that port.

Timing Waveform of a Bank Select Pipelined Read^(1,2)Timing Waveform with Port-to-Port Flow-Through Read^(4,5,7)

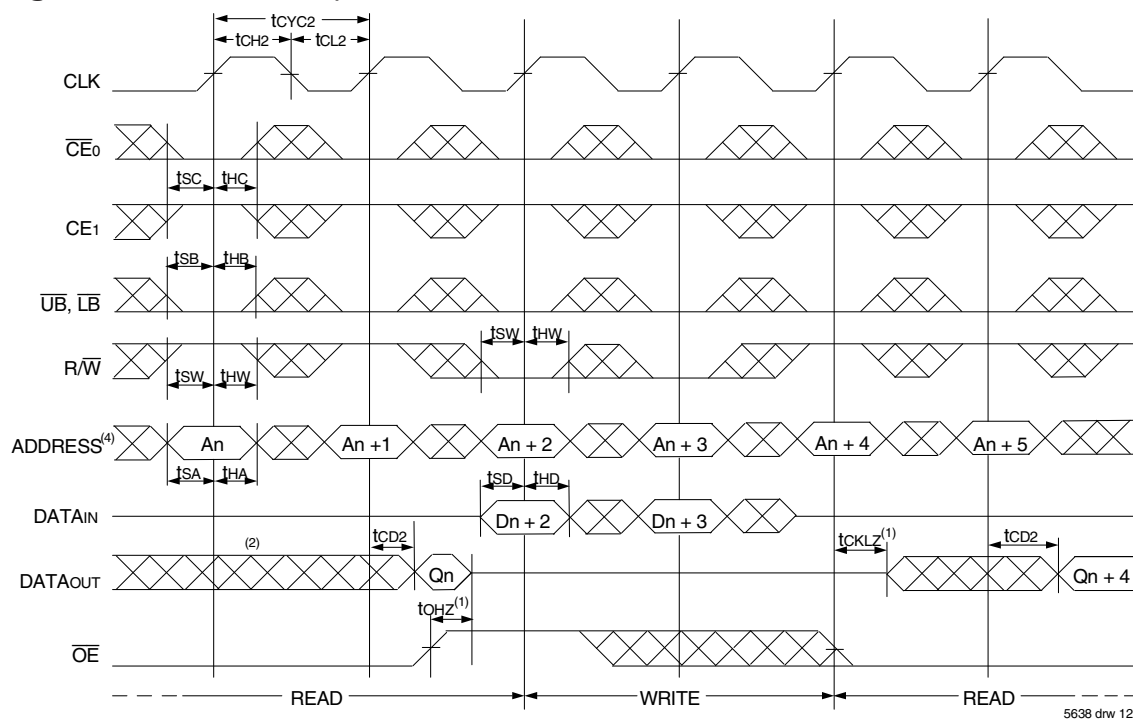
NOTES:

1. B1 Represents Bank #1; B2 Represents Bank #2. Each Bank consists of one IDT70V9359/49 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. \overline{UB} , \overline{LB} , \overline{OE} , and $\overline{ADS} = V_{IL}$; $CE_1(B1)$, $CE_1(B2)$, R/\overline{W} and $\overline{CNTRST} = V_{IH}$.
3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4. $\overline{CE_0}$, \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; CE_1 and $\overline{CNTRST} = V_{IH}$.
5. $\overline{OE} = V_{IL}$ for the Right Port, which is being read from. $\overline{OE} = V_{IH}$ for the Left Port, which is being written to.
6. If $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWD} . If $t_{CCS} >$ maximum specified, then data from right port READ is not valid until $t_{CCS} + t_{CD1}$. t_{CWD} does not apply in this case.
7. All timing is the same for both Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite from Port "A".

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{\text{OE}} = \text{VIL}$)⁽³⁾

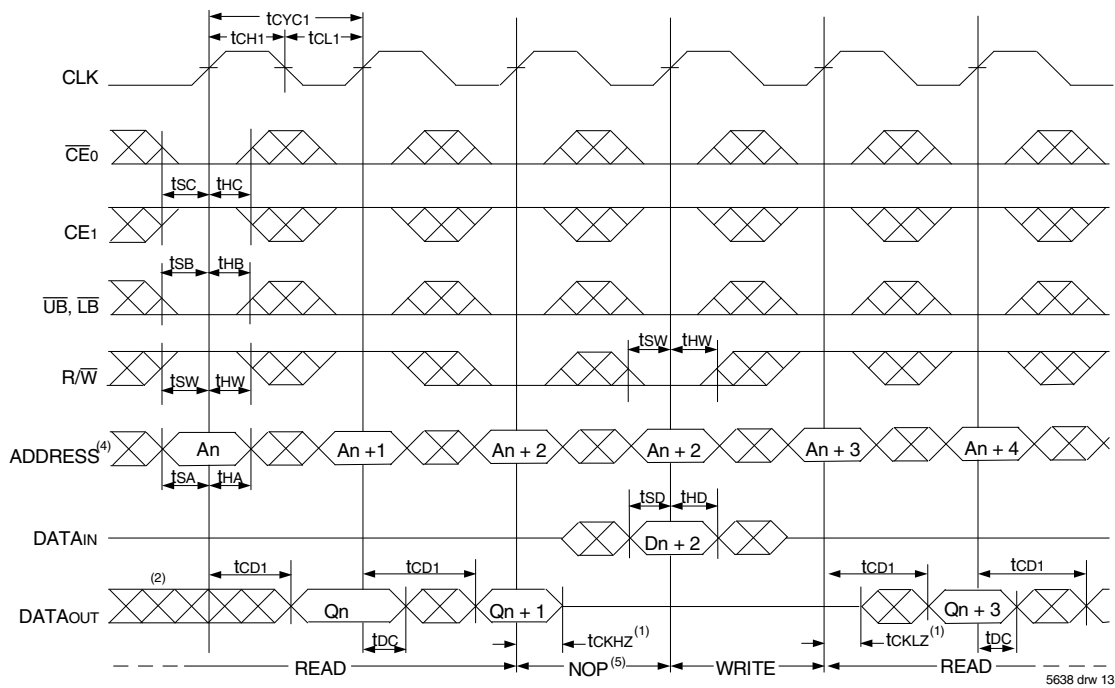
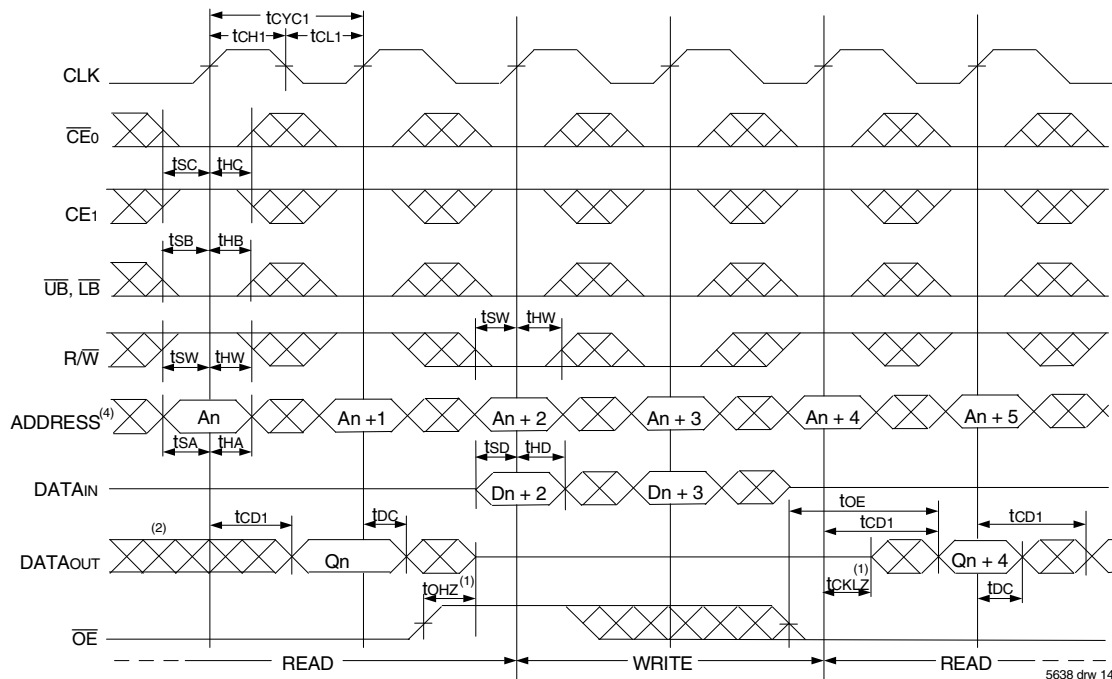


Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{\text{OE}}$ Controlled)⁽³⁾



NOTES:

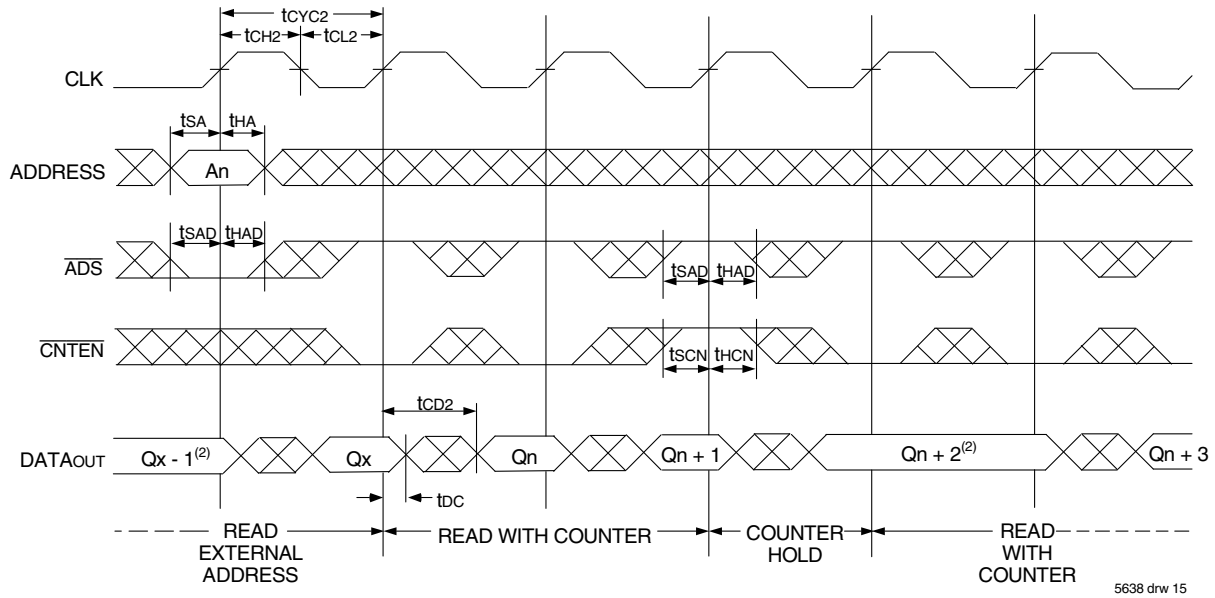
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. $\overline{CE0}$, \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; $\overline{CE1}$ and $\overline{CNRST} = V_{IH}$. "NOP" is "No Operation".
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽³⁾Timing Waveform of Flow-Through Read-to-Write-to-Read (\overline{OE} Controlled)⁽³⁾

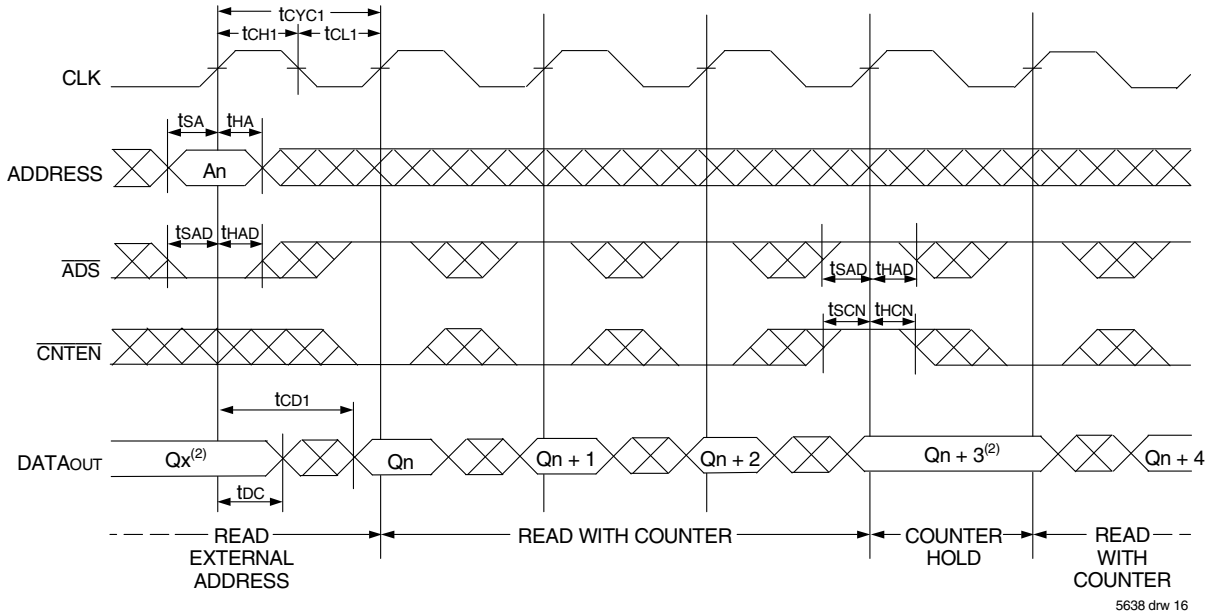
NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. $\overline{CE0}$, \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; $\overline{CE1}$ and $\overline{CNTRST} = V_{IH}$. "NOP" is "No Operation".
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Pipelined Read with Address Counter Advance⁽¹⁾



Timing Waveform of Flow-Through Read with Address Counter Advance⁽¹⁾

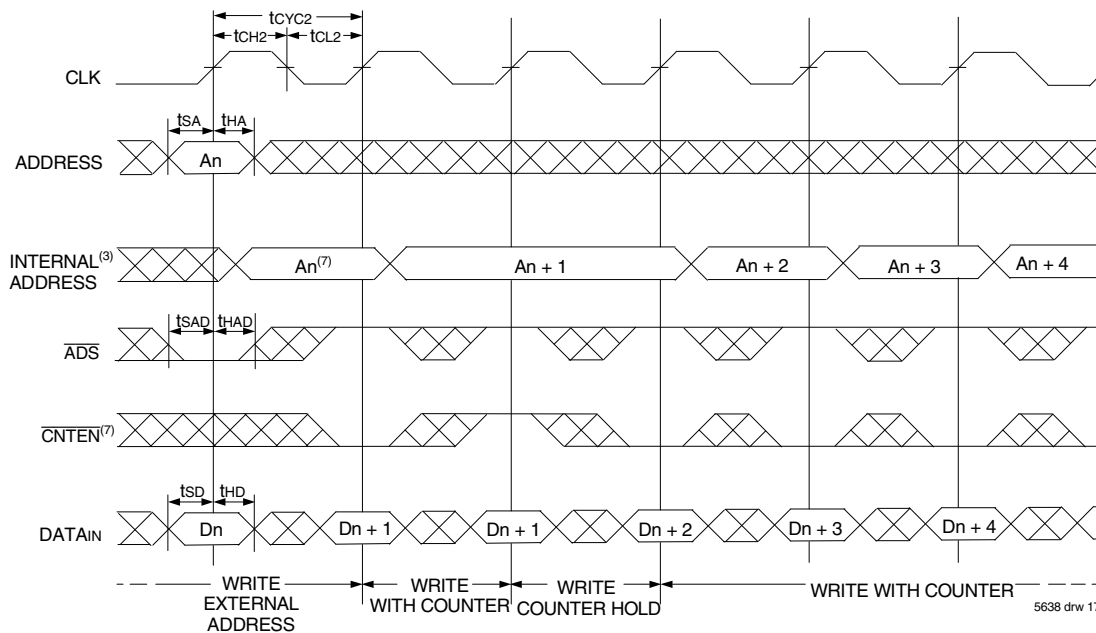


NOTES:

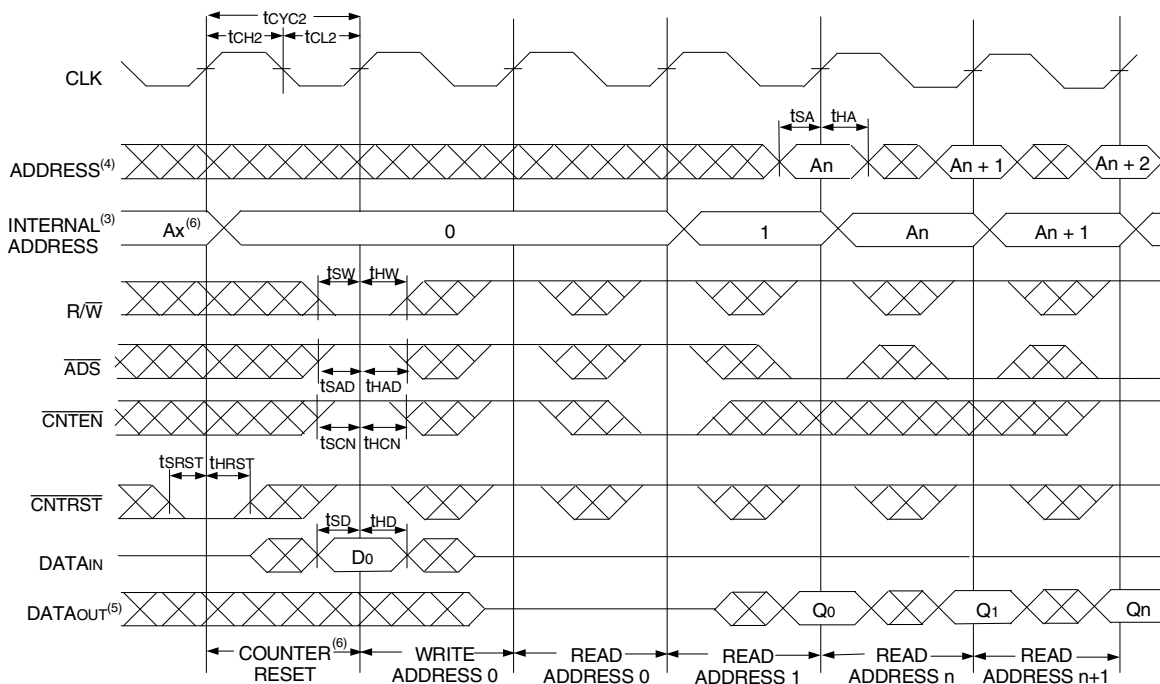
1. $\overline{CE_0}$, \overline{OE} , \overline{UB} , and $\overline{LB} = V_{IL}$; $\overline{CE_1}$, \overline{RW} , and $\overline{CNTRST} = V_{IH}$.

2. If there is no address change via $\overline{ADS} = V_{IL}$ (loading a new address) or $\overline{CNTEN} = V_{IL}$ (advancing the address), i.e. $\overline{ADS} = V_{IH}$ and $\overline{CNTEN} = V_{IH}$, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance (Flow-Through or Pipelined Outputs)⁽¹⁾



Timing Waveform of Counter Reset (Pipelined Outputs)⁽²⁾



NOTES:

1. \overline{CE}_0 , \overline{UB} , \overline{LB} , and R/\overline{W} = V_{IL} ; CE_1 and \overline{CNTRST} = V_{IH} .
2. \overline{CE}_0 , \overline{UB} , \overline{LB} = V_{IL} ; CE_1 = V_{IH} .
3. The "Internal Address" is equal to the "External Address" when \overline{ADS} = V_{IL} and equals the counter output when \overline{ADS} = V_{IH} .
4. Addresses do not have to be accessed sequentially since \overline{ADS} = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle. $ADDR_0$ will be accessed. Extra cycles are shown here simply for clarification.
7. \overline{CNTEN} = V_{IL} advances Internal Address from 'An' to 'An + 1'. The transition shown indicates the time required for the counter to advance. The 'An + 1' Address is written to during this cycle.

Functional Description

The IDT70V9359/49 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW-to-HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

$\overline{CE_0} = V_{IL}$ and $CE_1 = V_{IH}$ for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V9359/49's for depth expansion configurations. When the Pipelined output mode is enabled, two cycles are required with $\overline{CE_0} = V_{IL}$ and $CE_1 = V_{IH}$ to re-activate the outputs.

Depth and Width Expansion

The IDT70V9359/49 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V9359/49 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 36-bit or wider applications.

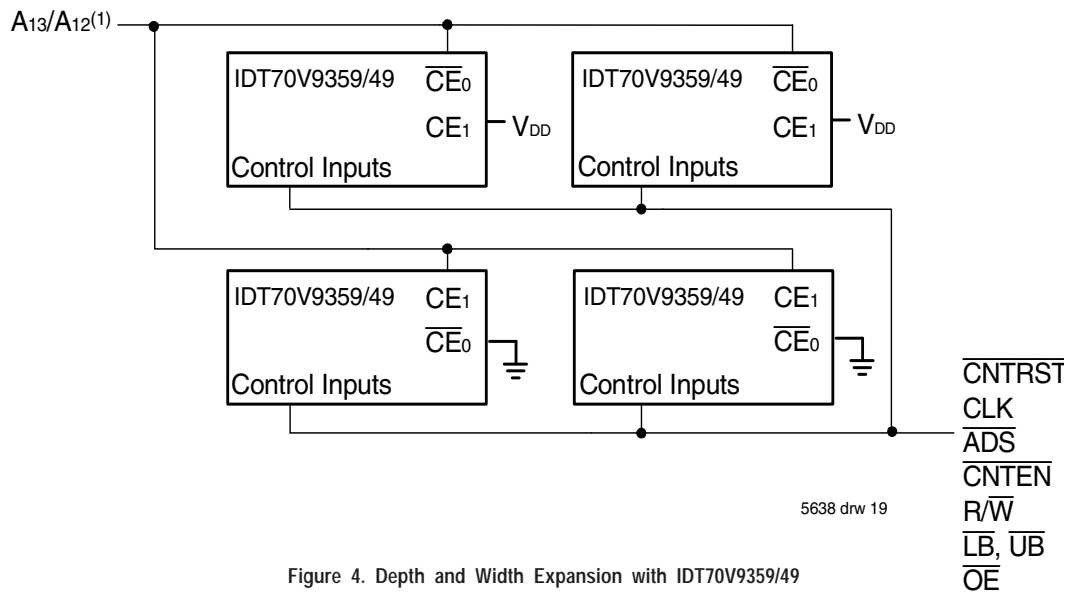


Figure 4. Depth and Width Expansion with IDT70V9359/49

NOTE:

1. A13 is for IDT70V9359, A12 is for IDT70V9349.

Ordering Information

| XXXXX | A | 99 | A | A | A | | |
|-------------|-------|-------|---------|---|-------------------------------|---------------------------|---|
| Device Type | Power | Speed | Package | | Process/ Temperature Range | | |
| | | | | | | Blank I ⁽¹⁾ | Commercial (0°C to +70°C) Industrial (-40°C to +85°C) |
| | | | | | | G ⁽²⁾ | Green |
| | | | | | | PF BF | 100-pin TQFP (PN100-1) 100-pin fpBGA (BF100) |
| | | | | | | 6 7 9 | Commercial Only Commercial & Industrial Commercial Only |
| | | | | | | L | Low Power |
| | | | | | | 70V9359 70V9349 | 144K (8K x 18-Bit) Synchronous Dual-Port RAM 72K (4K x 18-Bit) Synchronous Dual-Port RAM |

Speed in nanoseconds

5638 drw 20

NOTE:

1. Contact your local sales office for Industrial temp range for other speeds, packages and powers.
 2. Green parts available. For specific speeds, packages and powers contact your sales office.
- LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

IDT Clock Solution for IDT70V9359/49 Dual-Port

| IDT Dual-Port Part Number | Dual-Port I/O Specifications | | Clock Specifications | | | | IDT PLL Clock Device | IDT Non-PLL Clock Device |
|------------------------------|------------------------------|--------|----------------------|------------------------------------|----------------------|---------------------|-------------------------------|--|
| | Voltage | I/O | Input Capacitance | Input Duty Cycle Requirement | Maximum Frequency | Jitter Tolerance | | |
| 70V9359/49 | 3.3 | LVTTTL | 9pF | 40% | 100 | 150ps | IDT2305 IDT2308 IDT2309 | FCT3805 FCT3805D/E FCT3807 FCT3807D/E |

5638 tbl 12

Datasheet Document History

| | | |
|-----------|-------------|---|
| 10/01/01: | | Initial Public Release |
| 07/03/02: | Pages 2 & 3 | Added data revision for pin configurations Consolidated multiple devices into one datasheet |
| 08/15/03: | | Removed Preliminary status |
| | Page 16 | Added IDT Clock Solution Table |
| 01/29/09: | Page 16 | Removed "IDT" from orderable part number |
| 07/26/10: | Page 1 | Added green parts availability to features |
| | Page 16 | Added green indicator to ordering information |
| | Page 8 | In order to correct the header notes of the AC Elect Chars Table and align them with the Industrial temp range values located in the table, the commercial TA header note has been removed |
| | Pages 9-12 | In order to correct the footnotes of timing diagrams, $\overline{\text{CNTEN}}$ has been removed to reconcile the footnotes with the $\overline{\text{CNTEN}}$ logic definition found in Truth Table II - Address Counter Control |
| 03/02/18: | | Product Discontinuation Notice - PDN# SP-17-02 |
| | | Last time buy expires June 15, 2018 |
| 03/06/20: | | Datasheet changed to Obsolete Status |



CORPORATE HEADQUARTERS

6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:

800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:

408-284-2794
DualPortHelp@idt.com

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.