#### **Features**

- 64K x 16 advanced high-speed CMOS Static RAM
- Equal access and cycle times
  - Commercial: 12/15/20ns
  - Industrial: 15/20ns
- One Chip Select plus one Output Enable pin
- Bidirectional data inputs and outputs directly TTLcompatible
- Low power consumption via chip deselect
- Upper and Lower Byte Enable Pins
- Commercial and industrial product available in 44-pin Plastic SOJ package and 44-pin TSOP package

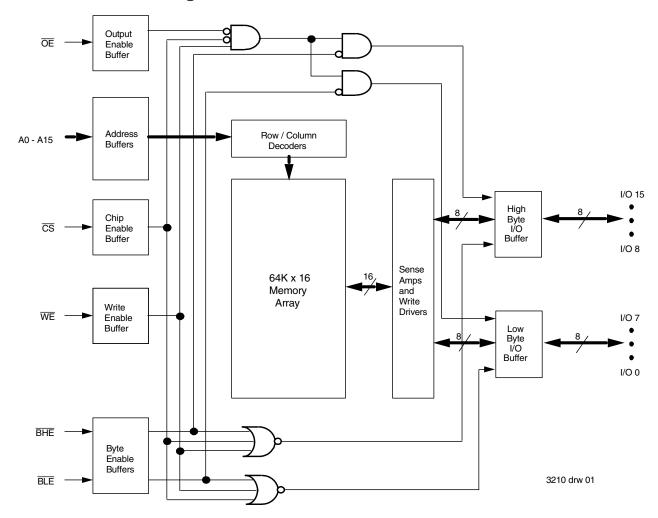
### Description

The IDT71016 is a 1,048,576-bit high-speed Static RAM organized as 64K x 16. It is fabricated using high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

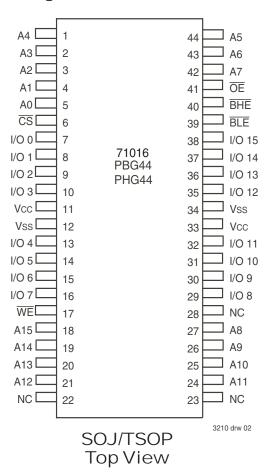
The IDT71016 has an output enable pin which operates as fast as 7ns, with address access times as fast as 12ns. All bidirectional inputs and outputs of the IDT71016 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71016 is packaged in a JEDEC standard 44-pin Plastic SOJ and 44-pin TSOP Type II.

### Functional Block Diagram



## Pin Configurations<sup>(1)</sup>



Pin Descriptions

A0 - A15	Address Inputs	Input
<u></u> <del>C</del> <del>S</del>	Chip Select	Input
WE	Write Enable	Input
ŌĒ	Output Enable	Input
BHE	High Byte Enable	Input
BLE	Low Byte Enable	Input
I/Oo - I/O15	Data Input/Output	I/O
Vcc	5.0V Power	Pwr
Vss	Ground	Gnd

3210 tbl 01

#### NOTE:

1. This text does not indicate orientation of actual part-marking.

### Truth Table (1)

<u></u> <del> </del>	ŌĒ	WE	BLE	BHE	I/O <sub>0</sub> - I/O <sub>7</sub>	I/O8 - I/O15	Function
Н	Х	Χ	Χ	Χ	High-Z	High-Z	Deselected - Standby
L	L	Н	L	Н	DATAOUT	High-Z	Low Byte Read
L	L	Н	Н	L	High-Z	DATAOUT	High Byte Read
L	L	Н	L	L	DATAOUT	DATAOUT	Word Read
L	Χ	Ш	L	L	DATAIN	DATAIN	Word Write
L	Х	L	L	Н	DATAIN	High-Z	Low Byte Write
L	Х	L	Н	L	High-Z	DATAIN	High Byte Write
L	Н	Н	Х	Χ	High-Z	High-Z	Outputs Disabled
L	Χ	Χ	Н	Н	High-Z	High-Z	Outputs Disabled

NOTE:

1.  $H = V_{IH}$ ,  $L = V_{IL}$ , X = Don't care.

3210 tbl 02

### Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Value	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TBIAS	Temperature Under Bias	-55 to +125	°C
Tstg	Storage Temperature	-55 to +125	°C
Рт	Power Dissipation	1.25	W
Іоит	DC Output Current	50	mA

#### NOTES:

 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. VTERM must not exceed Vcc + 0.5V.

# Recommended Operating Temperature and Supply Voltage

Grade	Temperature	GND	<b>V</b> cc	
Commercial	0°C to +70°C	0V	5.0V ± 10%	
Industrial	-40°C to +85°C	0V	5.0V ± 10%	

3210 tbl 04

# Recommended DC Operating Conditions

Symbol	Parameter	Min.	Тур.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
VIH	Input High Voltage	2.2		VDD +0.5	٧
VIL	Input Low Voltage	-0.5 <sup>(1)</sup>		0.8	V

NOTE:

3210 tbl 03a

3210 tbl 05

1. VIL (min.) = -1.5V for pulse width less than tRC/2, once per cycle.

### Capacitance

 $(TA = +25^{\circ} C, f = 1.0MHz, SOJ/TSOP Package)$ 

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
Cin	Input Capacitance	VIN = 3dV	6	pF
Cvo	I/O Capacitance	Vout = 3dV	7	pF

NOTE:

3210 tbl 06

 This parameter is guaranteed by device characterization, but not production tested.

#### DC Electrical Characteristics

(Vcc = 5.0V ± 10%, Commercial and Industrial Temperature Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
Iu	Input Leakage Current	Vcc = Max., Vin = GND to Vcc		5	μA
ILO	Output Leakage Current	Vcc = Max., $\overline{\text{CS}}$ = Vih, Vout = GND to Vcc		5	μΑ
Vol	Output Low Voltage	IOL = 8mA, Vcc = Min.		0.4	V
Vон	Output High Voltage	Iон = -4mA, Vcc = Min.	2.4		V

3210 tbl 07

### DC Electrical Characteristics(1)

 $(VCC = 5.0V \pm 10\%, VLC = 0.2V, VHC = VCC-0.2V)$ 

		71016S12	7101	6S15	7101	6S20	
Symbol	Parameter	Com'l.	Com'l.	Ind.	Com'l.	Ind.	Unit
Icc	Dynamic Operating Current $\overline{CS} \leq V_{IL}$ , Outputs Open, $V_{CC} = Max.$ , $f = f_{MAX}^{(2)}$	210	180	180	170	170	mA
ISB	Standby Power Supply Current (TTL Level) $\overline{\text{CS}} \geq \text{Vih}$ , Outputs Open, $\text{Vcc} = \text{Max.}$ , $F = \text{fmax}^{(2)}$	60	50	50	45	45	mA
ISB1	Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V$ Hc, Outputs Open, Vcc = Max., $f = 0^{(2)}$ $V$ IN $\le V$ LC or $V$ IN $\ge V$ HC	10	10	10	10	10	mA

All values are maximum guaranteed values.

2. fmax = 1/trc (all address inputs are cycling at fmax); f = 0 means no address input lines are changing.

3210 tbl 08

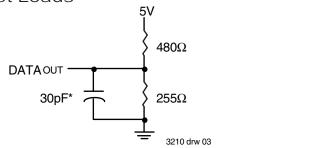


#### **AC Test Conditions**

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1.5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figure 1, 2 and 3

3210 tbl 09

### **AC Test Loads**



DATA OUT  $\begin{array}{c} \\ \\ \\ \\ \\ \\ \end{array}$ 

\*Including jig and scope capacitance.

Figure 1. AC Test Load

Figure 2. AC Test Load (for tclz, tolz, tchz, tohz, tow, and twhz)

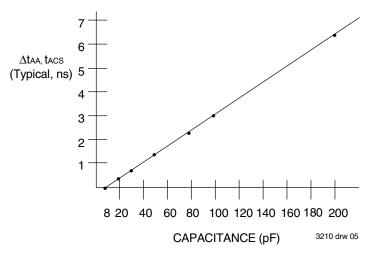


Figure 3. Output Capacitive Derating

### AC Electrical Characteristics (VCC = 5.0V ± 10%, Commercial and Industrial Range)

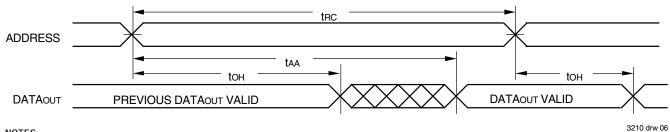
		71016S12 <sup>(2)</sup>		71016S15		71016S20		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYCLE								
trc	Read Cycle Time	12		15		20		ns
taa	Address Access Time		12		15		20	ns
tacs	Chip Select Access Time		12		15		20	ns
tcLz <sup>(1)</sup>	Chip Select Low to Output in Low-Z	4		5		5		ns
tchz <sup>(1)</sup>	Chip Select High to Output in High-Z	_	6		6	_	8	ns
toe	Output Enable Low to Output Valid		7		8		10	ns
tolz <sup>(1)</sup>	Output Enable Low to Output in Low-Z	0		0		0		ns
tonz <sup>(1)</sup>	Output Enable High to Output in High-Z	_	6		6		8	ns
tон	Output Hold from Address Change	4	_	4		5	_	ns
tBE	Byte Enable Low to Output Valid		7		8		10	ns
tBLZ <sup>(1)</sup>	Byte Enable Low to Output in Low-Z	0	_	0	_	0		ns
t <sub>B</sub> Hz <sup>(1)</sup>	Byte Enable High to Output in High-Z		6		6		8	ns
WRITE CYCL	E	•	•	•	•		•	
twc	Write Cycle Time	12	_	15		20		ns
taw	Address Valid to End of Write	9	_	10	_	12		ns
tcw	Chip Select Low to End of Write	9	_	10	_	12	_	ns
tBW	Byte Enable Low to End of Write	9	_	10		12		ns
tas	Address Set-up Time	0		0		0		ns
twr	Address Hold from End of Write	0		0		0		ns
twp	Write Pulse Width	9		10		12		ns
tow	Data Valid to End of Write	7		8		10		ns
tDH	Data Hold Time	0		0		0		ns
tow <sup>(1)</sup>	Write Enable High to Output in Low-Z	1		1		1		ns
twhz <sup>(1)</sup>	Write Enable Low to Output in High-Z	_	6		6		8	ns

#### NOTE:

3210 tbl 10

- 1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.
- 2. 12ns commercial only.

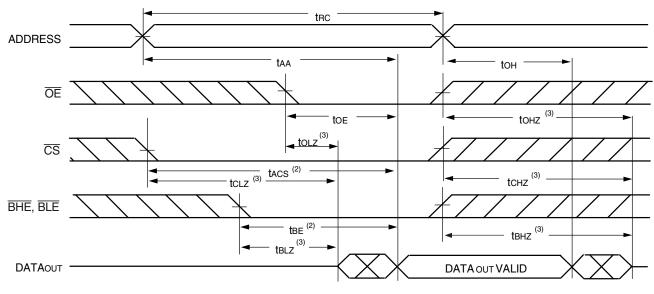
### Timing Waveform of Read Cycle No. 1<sup>(1,2,3)</sup>



#### NOTES:

- 1.  $\overline{\text{WE}}$  is HIGH for Read Cycle.
- 2. Device is continuously selected,  $\overline{\text{CS}}$  is LOW.
- 3.  $\overline{OE}$ ,  $\overline{BHE}$ , and  $\overline{BLE}$  are LOW.

### Timing Waveform of Read Cycle No. 2<sup>(1)</sup>

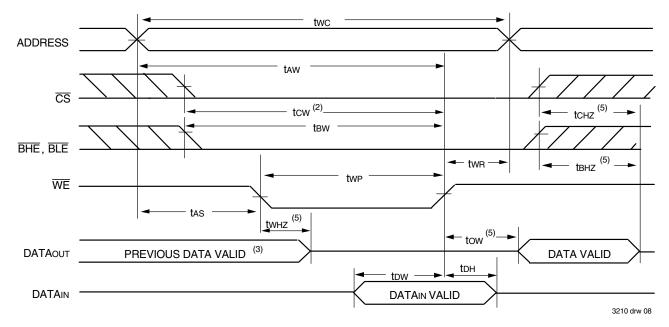


#### NOTES:

3210 drw 07

- 1. WE is HIGH for Read Cycle.
- 2. Address must be valid prior to or coincident with the later of  $\overline{\text{CS}}$ ,  $\overline{\text{BHE}}$ , or  $\overline{\text{BLE}}$  transition LOW; otherwise tax is the limiting parameter.
- 3. Transition is measured ±200mV from steady state.

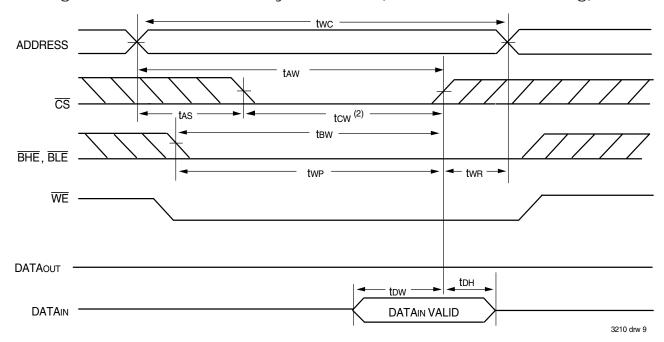
# Timing Waveform of Write Cycle No. 1 (WE Controlled Timing)(1,2,4)



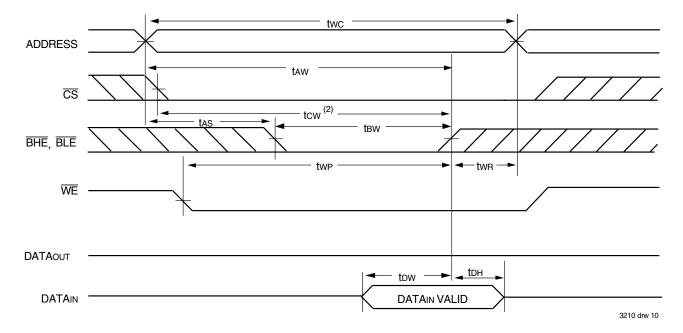
#### NOTES:

- 1. A write occurs during the overlap of a LOW  $\overline{\text{CS}}$ , LOW  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}}$ , and a LOW  $\overline{\text{WE}}$ .
- 2.  $\overline{\text{OE}}$  is continuously HIGH. If during a  $\overline{\text{WE}}$  controlled write cycle  $\overline{\text{OE}}$  is LOW, twp must be greater than or equal to twHz + tow to allow the I/O drivers to turn off and data to be placed on the bus for the required tow. If  $\overline{\text{OE}}$  is HIGH during a  $\overline{\text{WE}}$  controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified twp.
- 3. During this period, I/O pins are in the output state, and input signals must not be applied.
- 4. If the CS LOW or BHE and BLE LOW transition occurs simultaneously with or after the WE LOW transition, the outputs remain in a high-impedance state.
- 5. Transition is measured ±200mV from steady state.

## Timing Waveform of Write Cycle No. 2 (CS Controlled Timing)(1,4)



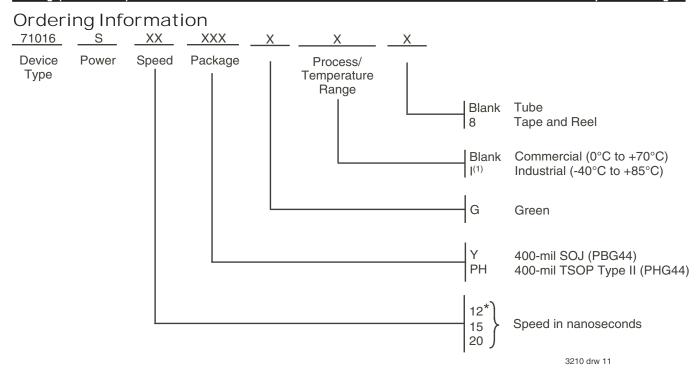
# Timing Waveform of Write Cycle No. 3 (BHE, BLE Controlled Timing)(1,4)



#### NOTES:

- 1. A write occurs during the overlap of a LOW  $\overline{CS}$ , LOW  $\overline{BHE}$  or  $\overline{BLE}$ , and a LOW  $\overline{WE}$ .

  2.  $\overline{OE}$  is continuously HIGH. If during a  $\overline{WE}$  controlled write cycle  $\overline{OE}$  is LOW, two must be greater than or equal to twhz + tow to allow the I/O drivers to turn off and data to be placed on the bus for the required tow. If  $\overline{\text{OE}}$  is HIGH during a  $\overline{\text{WE}}$  controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified twp.
- 3. During this period, I/O pins are in the output state, and input signals must not be applied.
- 4. If the CS LOW or BHE and BLE LOW transition occurs simultaneously with or after the WE LOW transition, the outputs remain in a high-impedance state.
- Transition is measured ±200mV from steady state.



\*Commercial temperature range only

#### NOTE:

1. Contact your local sales office for industrial temp range for other speeds, packages and powers.

### Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
12	71016S12PHG	PHG44	TSOP	С
	71016S12PHG8	PHG44	TSOP	С
	71016S12YG	PBG44	SOJ	С
	71016S12YG8	PBG44	SOJ	С
15	71016S15PHG	PHG44	TSOP	С
	71016S15PHG8	PHG44	TSOP	С
	71016S15PHGI	PHG44	TSOP	I
	71016S15PHGI8	PHG44	TSOP	I
	71016S15YG	PBG44	SOJ	С
	71016S15YG8	PBG44	SOJ	С
	71016S15YGI	PBG44	SOJ	I
	71016S15YGl8	PBG44	SOJ	I
20	71016S20PHG	PHG44	TSOP	С
	71016S20PHG8	PHG44	TSOP	С
	71016S20PHGI	PHG44	TSOP	I
	71016S20PHGI8	PHG44	TSOP	-
	71016S20YG	PBG44	SOJ	С
	71016S20YG8	PBG44	SOJ	С
	71016S20YGI	PBG44	SOJ	I
	71016S20YGI8	PBG44	SOJ	I

# Datasheet Document History

07/30/99:		Updated to new format
080/5/99:	Pg. 3	Expressed commercial and industrial ranges on DC Electrical table
	Ü	Removed Icc, IsB, and IsB1 values for S12 industrial speed
	Pg. 5	Expressed commercial and industrial ranges on AC Electrical table
	Ü	Changed footnote #2 to commercial temperature only
	Pg. 6	Revised footnotes on Write Cycle No.1 diagram
	Pg. 7	Revised footnotes on Write Cycle No.2 and No.3 diagrams
	Pg. 8	Removed SCD 2752 footnote
		Added commercial only for 12ns speed
08/13/99:	Pg. 9	Added Datasheet Document History
09/30/99:	Pg. 3, 5, 8	Added 12ns industrial temperature speed grade offering
08/09/00:		Not recommended for new designs
02/01/01:		Removed "Not recommended for new designs"
01/30/04:	Pg. 8	Added "Restricted hazardous substance device" to order information
01/30/06:	Pg. 3	Updated Capacitance table to include TSOP
02/13/07:	Pg. 8	Added N generation die step to data sheet ordering information
10/13/08:	Pg. 8	Removed "IDT" from orderable part number
09/25/13:	Pg. 1	Updated Commercial and Industrial speed grade offerings
		Removed IDT reference to fabrication
	Pg. 3	$RemovedCommercialT_AinformationfromtheAbsoluteMaximumRatingstable$
		Removed Ind. temp values for the 12ns speed grade from the DC Elec Chars table
	Pg. 5	Added the footnote annotation to the AC Elec Chars table and the footnote for 12ns commercial only
	Pg. 8	Added T & R to, updated Restricted Hazardous Substance Device wording to "Green", added
		annotation indicating "Commercial temperature range only" and removed Die Stepping indicator from
		the ordering information
06/02/20:	Pg. 1 - 10	Rebranded as Renesas datasheet
	Pg. 2 & 8	Updated package codes
	Pg. 8	Added Industrial temp footnote to Ordering Information
	Pg. 8	Added Orderable Part Information table

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