![RENESAS]

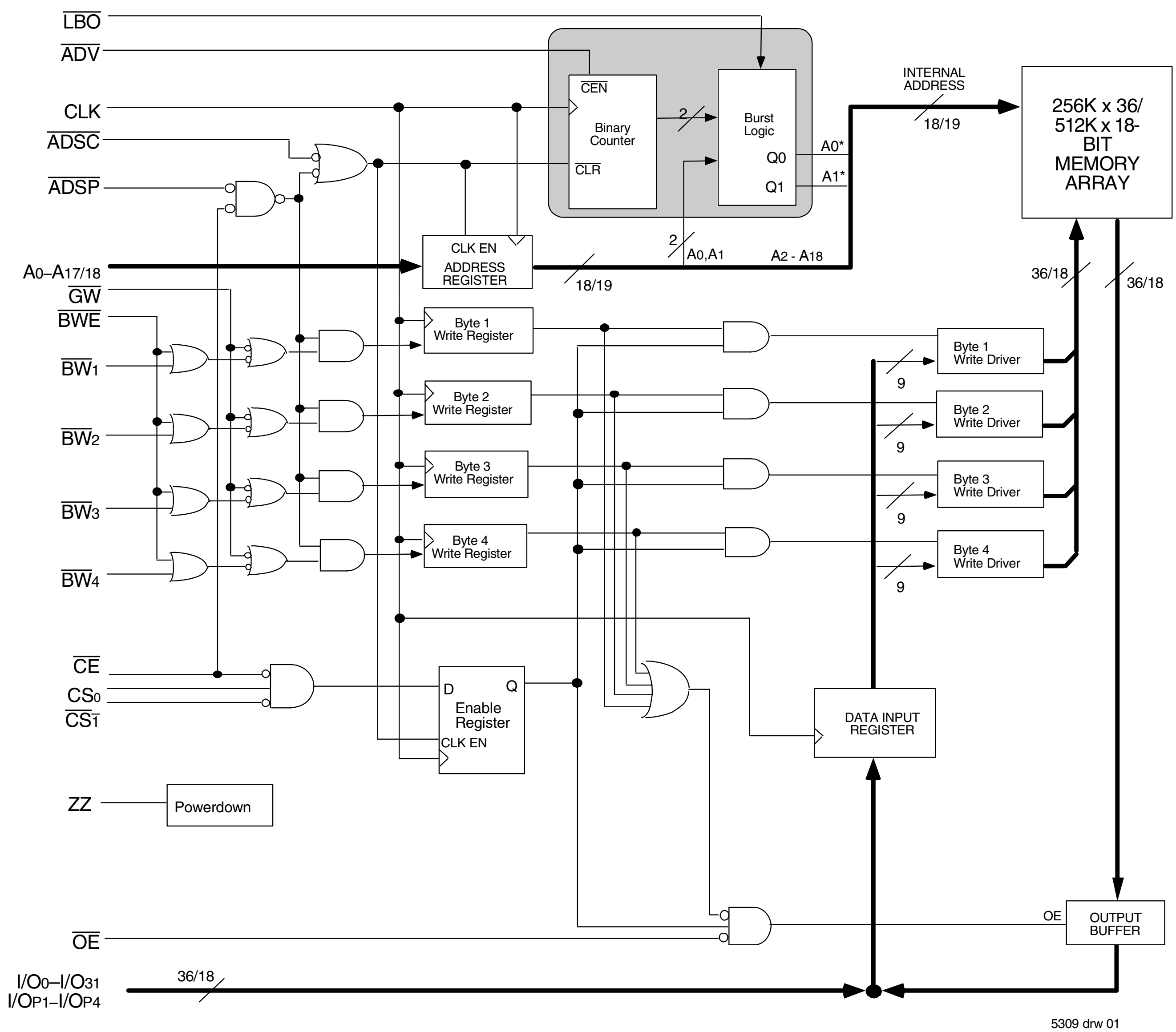
256K X 36, 512K X 18 3.3V Synchronous SRAMs 3.3V I/O, Burst Counter Flow-Through Outputs, Single Cycle Deselect

71V67703
71V67903

Features

- 256K x 36, 512K x 18 memory configurations
- Supports fast access times:
  - *7.5ns up to 117MHz clock frequency*
  - *8.0ns up to 100MHz clock frequency*
  - *8.5ns up to 87MHz clock frequency*
- LBO input selects interleaved or linear burst mode
- Self-timed write cycle with global write control (GW), byte write enable (BWE), and byte writes (BWx)
- 3.3V core power supply
- Power down controlled by ZZ input
- 3.3V I/O supply (VDDQ)
- Packaged in a JEDEC Standard 100-pin thin plastic quad flatpack (TQFP), 119 ball grid array (BGA) and 165 fine pitch ball grid array (fBGA)
- Industrial temperature range (–40°C to +85°C) is available for selected speeds
- Green parts available, see ordering information

Functional Block Diagram



Description

The IDT71V67703/7903 are high-speed SRAMs organized as 256K x 36/512K x 18. The IDT71V67703/7903 SRAMs contain write, data, address and control registers. There are no registers in the data output path (flow-through architecture). Internal logic allows the SRAM to generate a self-timed write based upon a decision which can be left until the end of the write cycle.

The burst mode feature offers the highest level of performance to the system designer, as the IDT71V67703/7903 can provide four cycles of data for a single address presented to the SRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will flow-through from the array after a clock-to-data access time delay from the rising clock edge of the same cycle. If burst mode operation is selected ($\overline{ADV}$=LOW), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The order of these three addresses are defined by the internal burst counter and the $\overline{LBO}$ input pin.

The IDT71V67703/7903 SRAMs utilize a high-performance CMOS process and are packaged in a JEDEC standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) as well as a 119 ball grid array (BGA) and a 165 fine pitch ball grid array (fBGA).

Pin Description Summary

A_0-A_{18}	Address Inputs	Input	Synchronous
$\overline{CE}$	Chip Enable	Input	Synchronous
CS_0, $\overline{CS}_1$	Chip Selects	Input	Synchronous
$\overline{OE}$	Output Enable	Input	Asynchronous
$\overline{GW}$	Global Write Enable	Input	Synchronous
$\overline{BWE}$	Byte Write Enable	Input	Synchronous
$\overline{BW}_1$, $\overline{BW}_2$, $\overline{BW}_3$, $\overline{BW}_4$(1)	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
$\overline{ADV}$	Burst Address Advance	Input	Synchronous
$\overline{ADSC}$	Address Status (Cache Controller)	Input	Synchronous
$\overline{ADSP}$	Address Status (Processor)	Input	Synchronous
$\overline{LBO}$	Linear / Interleaved Burst Order	Input	DC
ZZ	Sleep Mode	Input	Asynchronous
I/O_0-I/O_{31}, I/O_{P1}-I/O_{P4}	Data Input / Output	I/O	Synchronous
V_{DD}, V_{DDQ}	Core Power, I/O Power	Supply	N/A
V_{SS}	Ground	Supply	N/A

5309 tbl 01

NOTE:
1. $\overline{BW}_3$ and $\overline{BW}_4$ are not applicable for the IDT71V67903.

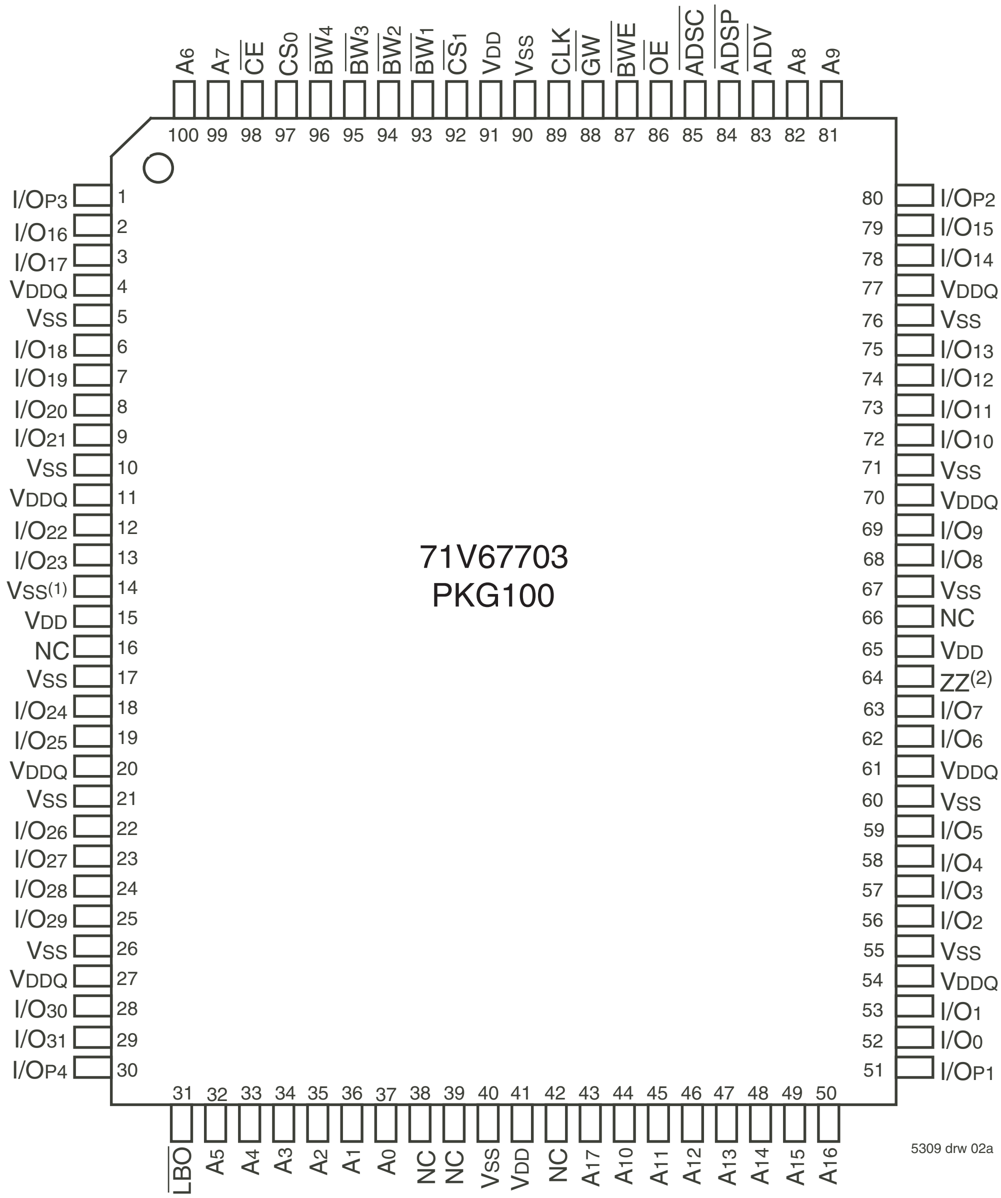
Pin Definitions[1]

Symbol	Pin Function	I/O	Active	Description
A_0-A_{18}	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combi-nation of the rising edge of CLK and $\overline{ADSC}$ Low or $\overline{ADSP}$ Low and $\overline{CE}$ Low.
$\overline{ADSC}$	Address Status (Cache Controller)	I	LOW	Synchronous Address Status from Cache Controller. $\overline{ADSC}$ is an active LOW input that is used to load the address registers with new addresses.
$\overline{ADSP}$	Address Status (Processor)	I	LOW	Synchronous Address Status from Processor. $\overline{ADSP}$ is an active LOW input that is used to load the address registers with new addresses. $\overline{ADSP}$ is gated by $\overline{CE}$.
$\overline{ADV}$	Burst Address Advance	I	LOW	Synchronous Address Advance. $\overline{ADV}$ is an active LOW input that is used to advance the internal burst counter, controlling burst access after the initial address is loaded. When the input is HIGH the burst counter is not incremented; that is, there is no address advance.
$\overline{BWE}$	Byte Write Enable	I	LOW	Synchronous byte write enable gates the byte write inputs $\overline{BW_1}$-$\overline{BW_4}$. If $\overline{BWE}$ is LOW at the rising edge of CLK then $\overline{BW}$x inputs are passed to the next stage in the circuit. If $\overline{BWE}$ is HIGH then the byte write inputs are blocked and only $\overline{GW}$ can initiate a write cycle.
$\overline{BW_1}$-$\overline{BW_4}$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. $\overline{BW_1}$ controls I/O_{0-7}, I/O_{P1}, $\overline{BW_2}$ controls I/O_{8-15}, I/O_{P2}, etc. Any active byte write causes all outputs to be disabled.
$\overline{CE}$	Chip Enable	I	LOW	Synchronous chip enable. $\overline{CE}$ is used with CS_0 and $\overline{CS_1}$ to enable the IDT71V67703/7903. $\overline{CE}$ also gates $\overline{ADSP}$.
CLK	Clock	I	N/A	This is the clock input. All timing references for the device are made with respect to this input.
CS_0	Chip Select 0	I	HIGH	Synchronous active HIGH chip select. CS_0 is used with $\overline{CE}$ and $\overline{CS_1}$ to enable the chip.
$\overline{CS_1}$	Chip Select 1	I	LOW	Synchronous active LOW chip select. $\overline{CS_1}$ is used with $\overline{CE}$ and CS_0 to enable the chip.
$\overline{GW}$	Global Write Enable	I	LOW	Synchronous global write enable. This input will write all four 9-bit data bytes when LOW on the rising edge of CLK. $\overline{GW}$ supersedes individual byte write enables.
I/O_0-I/O_{31} I/O_{P1}-I/O_{P4}	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. The data input path is registered, triggered by the rising edge of CLK. The data output path is flow-through (no output register).
$\overline{LBO}$	Linear Burst Order	I	LOW	Asynchronous burst order selection input. When $\overline{LBO}$ is HIGH, the inter-leaved burst sequence is selected. When $\overline{LBO}$ is LOW the Linear burst sequence is selected. $\overline{LBO}$ is a static input and must not change state while the device is operating.
$\overline{OE}$	Output Enable	I	LOW	Asynchronous output enable. When $\overline{OE}$ is LOW the data output drivers are enabled on the I/O pins if the chip is also selected. When $\overline{OE}$ is HIGH the I/O pins are in a high-impedance state.
V_{DD}	Power Supply	N/A	N/A	3.3V core power supply.
V_{DDQ}	Power Supply	N/A	N/A	3.3V I/O Supply.
V_{SS}	Ground	N/A	N/A	Ground.
NC	No Connect	N/A	N/A	NC pins are not electrically connected to the device.
ZZ	Sleep Mode	1	HIGH	Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V67703/7903 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode.

5309 tbl 02

NOTE:
1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

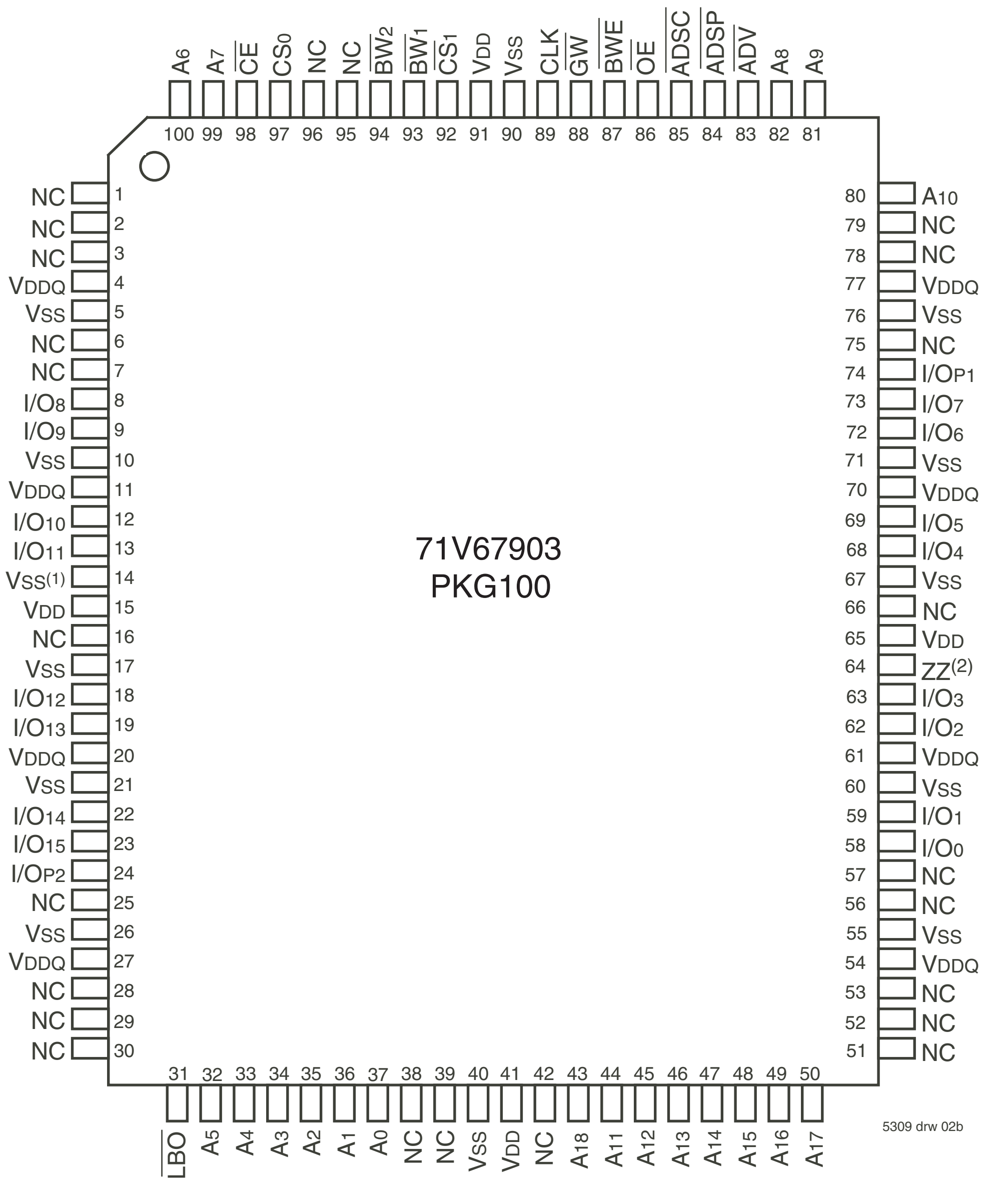
Pin Configuration – 256K x 36, PKG100(3)



Top View

NOTES:
1. Pin 14 does not have to be directly connected to VSS as long as the input voltage is ≤ VIL.
2. Pin 64 can be left unconnected and the device will always remain in active mode.
3. This text does not indicate orientation of actual part-marking.

Pin Configuration – 512K x 18, PKG100(3)



Top View

NOTES:
1. Pin 14 does not have to be directly connected to VSS as long as the input voltage is ≤ VIL.
2. Pin 64 can be left unconnected and the device will always remain in active mode.
3. This text does not indicate orientation of actual part-marking,

Pin Configuration – 256K x 36, BG119, BGG119(4)

	1	2	3	4	5	6	7
A	VDDQ	A6	A4	ADSP	A8	A16	VDDQ
B	NC	CS0	A3	ADSC	A9	A17	NC
C	NC	A7	A2	VDD	A12	A15	NC
D	I/O16	I/OP3	VSS	NC	VSS	I/OP2	I/O15
E	I/O17	I/O18	VSS	CE	VSS	I/O13	I/O14
F	VDDQ	I/O19	VSS	OE	VSS	I/O12	VDDQ
G	I/O20	I/O21	BW3	ADV	BW2	I/O11	I/O10
H	I/O22	I/O23	VSS	GW	VSS	I/O9	I/O8
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	I/O24	I/O26	VSS	CLK	VSS	I/O6	I/O7
L	I/O25	I/O27	BW4	NC	BW1	I/O4	I/O5
M	VDDQ	I/O28	VSS	BWE	VSS	I/O3	VDDQ
N	I/O29	I/O30	VSS	A1	VSS	I/O2	I/O1
P	I/O31	I/OP4	VSS	A0	VSS	I/OP1	I/O0
R	NC	A5	LBO	VDD	VSS(1)	A13	NC
T	NC	NC	A10	A11	A14	NC	ZZ(2)
U	VDDQ	DNU(3)	DNU(3)	DNU(3)	DNU(3)	DNU(3)	VDDQ

5309 drw 02c

Top View

Pin Configuration – 512K x 18, BG119, BGG119(4)

	1	2	3	4	5	6	7
A	VDDQ	A6	A4	ADSP	A8	A16	VDDQ
B	NC	CS0	A3	ADSC	A9	A18	NC
C	NC	A7	A2	VDD	A13	A17	NC
D	I/O8	NC	VSS	NC	VSS	I/OP1	NC
E	NC	I/O9	VSS	CE	VSS	NC	I/O7
F	VDDQ	NC	VSS	OE	VSS	I/O6	VDDQ
G	NC	I/O10	BW2	ADV	VSS	NC	I/O5
H	I/O11	NC	VSS	GW	VSS	I/O4	NC
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	NC	I/O12	VSS	CLK	VSS	NC	I/O3
L	I/O13	NC	VSS	NC	BW1	I/O2	NC
M	VDDQ	I/O14	VSS	BWE	VSS	NC	VDDQ
N	I/O15	NC	VSS	A1	VSS	I/O1	NC
P	NC	I/OP2	VSS	A0	VSS	NC	I/O0
R	NC	A5	LBO	VDD	VSS(1)	A12	NC
T	NC	A10	A15	NC	A14	A11	ZZ(2)
U	VDDQ	DNU(3)	DNU(3)	DNU(3)	DNU(3)	DNU(3)	VDDQ

5309 drw 02d

Top View

NOTES:
1. R5 does not have to be directly connected to VSS as long as the input voltage is ≤ VIL.
2. T7 can be left unconnected and the device will always remain in active mode.
3. DNU= Do not use; these signals can either be left unconnected or tied to Vss.
4. This text does not indicate orientation of part-marking.

Pin Configuration – 256K x 36, BQ165, BQG165(4)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A7	$\overline{CE}$	$\overline{BW3}$	$\overline{BW2}$	$\overline{CS1}$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A8	NC
B	NC	A6	CS0	$\overline{BW4}$	$\overline{BW1}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A9	NC
C	I/OP3	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	I/OP2
D	I/O17	I/O16	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O15	I/O14
E	I/O19	I/O18	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O13	I/O12
F	I/O21	I/O20	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O11	I/O10
G	I/O23	I/O22	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O9	I/O8
H	VSS(1)	NC	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ(2)
J	I/O25	I/O24	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O7	I/O6
K	I/O27	I/O26	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O5	I/O4
L	I/O29	I/O28	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O3	I/O2
M	I/O31	I/O30	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O1	I/O0
N	I/OP4	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	I/OP1
P	NC	NC	A5	A2	DNU(3)	A1	DNU(3)	A10	A13	A14	A17
R	$\overline{LBO}$	NC	A4	A3	DNU(3)	A0	DNU(3)	A11	A12	A15	A16

5309tbl 17a

Pin Configuration – 512K x 18, BQ165, BQG165(4)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A7	$\overline{CE}$	$\overline{BW2}$	NC	$\overline{CS1}$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A8	A10
B	NC	A6	CS0	NC	$\overline{BW1}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A9	NC
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	I/OP1
D	NC	I/O8	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O7
E	NC	I/O9	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O6
F	NC	I/O10	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O5
G	NC	I/O11	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O4
H	VSS(1)	NC	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ(2)
J	I/O12	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O3	NC
K	I/O13	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O2	NC
L	I/O14	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O1	NC
M	I/O15	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O0	NC
N	I/OP2	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	NC
P	NC	NC	A5	A2	DNU(3)	A1	DNU(3)	A11	A14	A15	A18
R	$\overline{LBO}$	NC	A4	A3	DNU(3)	A0	DNU(3)	A12	A13	A16	A17

5309 tbl 17b

NOTES:
1. H1 does not have to be directly connected to VSS, as long as the input voltage is $\leq$ VIL.
2. H11 can be left unconnected and the device will always remain in active mode.
3. DNU= Do not use; these signals can either be left unconnected or tied to Vss.
4. This text does not indicate orientation of actual part-marking.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V_{TERM}(3,6)	Terminal Voltage with Respect to GND	-0.5 to V_{DD}	V
V_{TERM}(4,6)	Terminal Voltage with Respect to GND	-0.5 to V_{DD} +0.5	V
V_{TERM}(5,6)	Terminal Voltage with Respect to GND	-0.5 to V_{DDQ} +0.5	V
T_A(7)	Operating Temperature	-0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	2.0	W
I_{OUT}	DC Output Current	50	mA

5309 tbl 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} terminals only.
3. V_{DDQ} terminals only.
4. Input terminals only.
5. I/O terminals only.
6. This is a steady-state DC parameter that applies after the power supplies have ramped up. Power supply sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
7. T_A is the "instant on" case temperature.

Recommended Operating Temperature Supply Voltage

Grade	Temperature(1)	Vss	VDD	VDDQ
Commercial	0°C to +70°C	0V	3.3V±5%	3.3V±5%
Industrial	-40°C to +85°C	0V	3.3V±5%	3.3V±5%

5309 tbl 04

NOTE:
1. T_A is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.135	3.3	3.465	V
V_{DDQ}	I/O Supply Voltage	3.135	3.3	3.465	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage - Inputs	2.0	—	V_{DD} +0.3	V
V_{IH}	Input High Voltage - I/O	2.0	—	V_{DDQ} +0.3	V
V_{IL}	Input Low Voltage	-0.3(1)	—	0.8	V

5309 tbl 05

NOTE:
1. V_{IL} (min) = -1.0V for pulse width less than $t_{CYC/2}$, once per cycle.

100-Pin TQFP Capacitance
(T_A = +25° C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	5	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5309 tbl 07

165 fBGA Capacitance
(T_A = +25° C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5309 tbl 07b

119 BGA Capacitance
(T_A = +25° C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5309 tbl 07a

NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 5%)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	5	µA
$\lvert I_{LI} \rvert$	$\overline{\text{LBO}}$ Input Leakage Current(1)	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	30	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{OUT} = 0V to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +8mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -8mA, V_{DD} = Min.	2.4	—	V

5309 tbl 08

NOTE:
1. The $\overline{\text{LBO}}$ pin will be internally pulled to V_{DD} if it is not actively driven in the application and the ZZ in will be internally pulled to V_{SS} if not actively driven.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (1)

Symbol	Parameter	Test Conditions	7.5ns		8ns		8.5ns		Unit
			Com'l	Ind	Com'l	Ind	Com'l	Ind	
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}(2)	265	285	210	230	190	210	mA
I_{SB1}	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0(2,3)	50	70	50	70	50	70	mA
I_{SB2}	Clock Running Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = f_{MAX} (2,,3)	145	165	140	160	135	155	mA
I_{ZZ}	Full Sleep Mode Supply Current	ZZ $\geq V_{HD}$, V_{DD} = Max.	50	70	50	70	50	70	mA

5309 tbl 09

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of $1/t_{CYC}$ while $\overline{\text{ADSC}}$ = LOW; f=0 means no input lines are changing.
3. For I/Os V_{HD} = V_{DDQ} - 0.2V, V_{LD} = 0.2V. For other inputs V_{HD} = V_{DD} - 0.2V, V_{LD} = 0.2V.

AC Test Conditions (V_{DDQ} = 3.3V/2.5V)

Input Pulse Levels	0 to 3V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figure 1

5309 tbl 10

AC Test Load

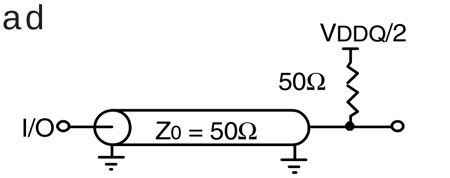
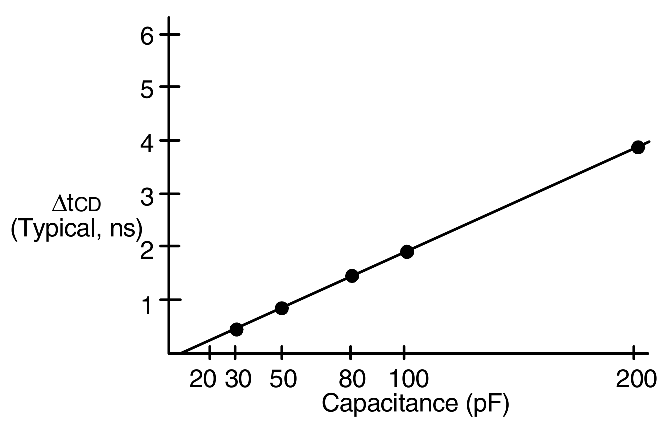


Figure 1. AC Test Load 5309 drw 03



5309 drw 05

Figure 2. Lumped Capacitive Load, Typical Derating

Synchronous Truth Table (1,3)

Operation	Address Used	$\overline{CE}$	CS_0	$\overline{CS_1}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_x}$	$\overline{OE}$(2)	CLK	I/O
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	X	H	L	X	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	L	X	L	X	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	X	H	X	L	X	X	X	X	X	↑	HI-Z
Deselected Cycle, Power Down	None	L	L	X	X	L	X	X	X	X	X	↑	HI-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	L	↑	D_{OUT}
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	H	↑	HI-Z
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	H	X	L	↑	D_{OUT}
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	L	↑	D_{OUT}
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	H	↑	HI-Z
Write Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	L	X	↑	D_{IN}
Write Cycle, Begin Burst	External	L	H	L	H	L	X	L	X	X	X	↑	D_{IN}
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	L	↑	D_{OUT}
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	H	↑	HI-Z
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	L	↑	D_{OUT}
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	H	↑	HI-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	L	↑	D_{OUT}
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	H	↑	HI-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	L	↑	D_{OUT}
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	H	↑	HI-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L	X	↑	D_{IN}
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	X	X	↑	D_{IN}
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L	X	↑	D_{IN}
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	X	X	↑	D_{IN}
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	L	↑	D_{OUT}
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	H	↑	HI-Z
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	L	↑	D_{OUT}
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	H	↑	HI-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	L	↑	D_{OUT}
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	H	↑	HI-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	L	↑	D_{OUT}
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	H	↑	HI-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L	X	↑	D_{IN}
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	X	X	↑	D_{IN}
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L	X	↑	D_{IN}
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	X	X	↑	D_{IN}

5309 tbl 11

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. $\overline{OE}$ is an asynchronous input.
3. ZZ - low for the table.

Synchronous Write Function Truth Table (1, 2)

Operation	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_1}$	$\overline{BW_2}$	$\overline{BW_3}$	$\overline{BW_4}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write all Bytes	L	X	X	X	X	X
Write all Bytes	H	L	L	L	L	L
Write Byte 1(3)	H	L	L	H	H	H
Write Byte 2(3)	H	L	H	L	H	H
Write Byte 3(3)	H	L	H	H	L	H
Write Byte 4(3)	H	L	H	H	H	L

5309 tbl 12

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. $\overline{BW_3}$ and $\overline{BW_4}$ are not applicable for the IDT71V67903.
3. Multiple bytes may be selected during the same cycle.

Asynchronous Truth Table (1)

Operation(2)	$\overline{OE}$	ZZ	I/O Status	Power
Read	L	L	Data Out	Active
Read	H	L	High-Z	Active
Write	X	L	High-Z – Data In	Active
Deselected	X	L	High-Z	Standby
Sleep Mode	X	H	High-Z	Sleep

5309 tbl 13

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. Synchronous function pins must be biased appropriately to satisfy operation requirements.

Interleaved Burst Sequence Table ($\overline{LBO}$=V_{DD})

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	1	0	0	1	0	0

5309 tbl 14

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state.

Linear Burst Sequence Table ($\overline{LBO}$=V_{SS})

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	0	0	0	1	1	0

5309 tbl 15

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state.

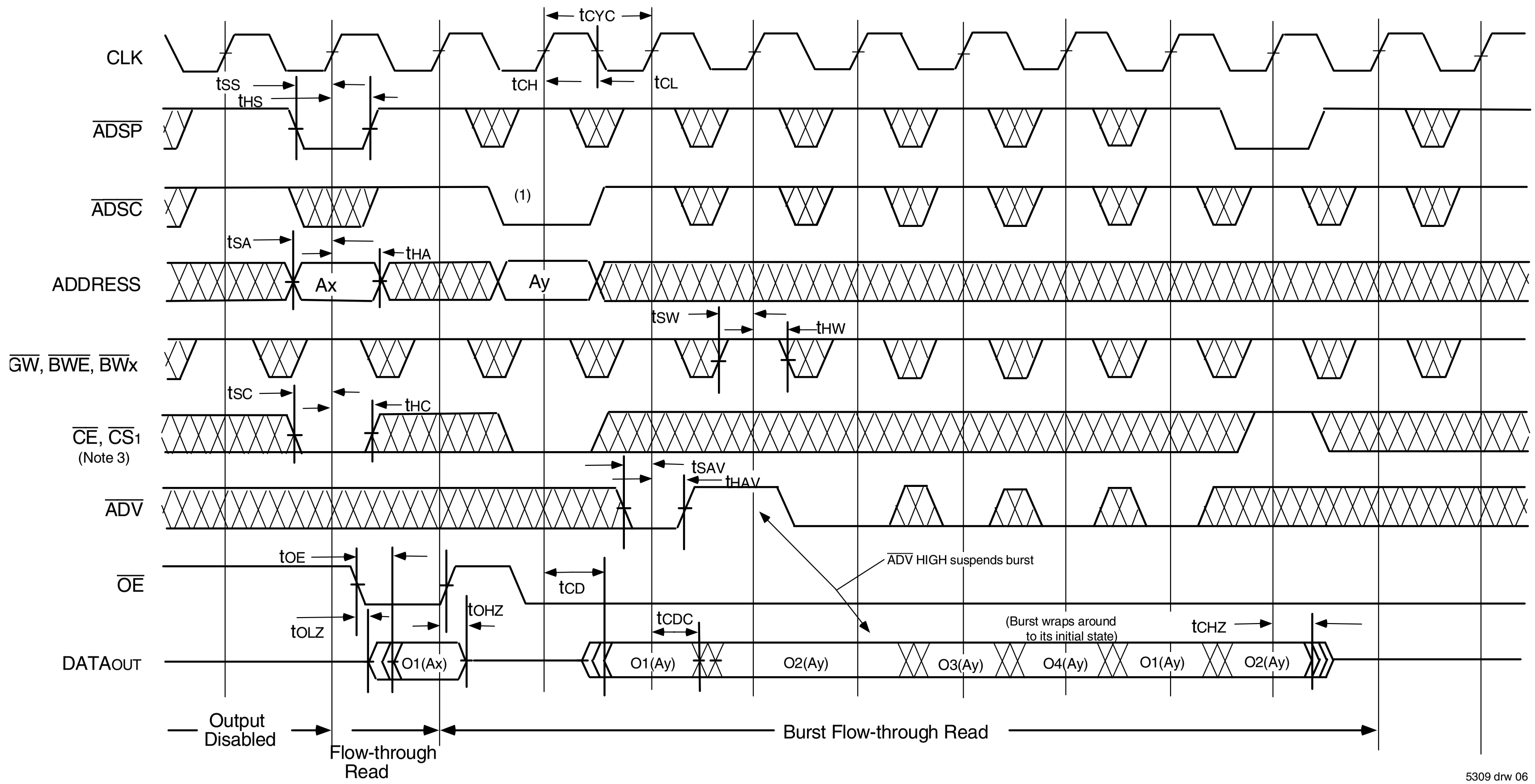
AC Electrical Characteristics
(VDD = 3.3V ±5%, Commercial and Industrial Temperature Ranges)

Symbol	Parameter	7.5ns		8ns		8.5ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Clock Parameter								
t_{CYC}	Clock Cycle Time	8.5	—	10	—	11.5	—	ns
t_{CH}(1)	Clock High Pulse Width	3	—	4	—	4.5	—	ns
t_{CL}(1)	Clock Low Pulse Width	3	—	4	—	4.5	—	ns
Output Parameters								
t_{CD}	Clock High to Valid Data	—	7.5	—	8	—	8.5	ns
t_{CDC}	Clock High to Data Change	2	—	2	—	2	—	ns
t_{CLZ}(2)	Clock High to Output Active	0	—	0	—	0	—	ns
t_{CHZ}(2)	Clock High to Data High-Z	2	3.5	2	3.5	2	3.5	ns
t_{OE}	Output Enable Access Time	—	3.5	—	3.5	—	3.5	ns
t_{OLZ}(2)	Output Enable Low to Output Active	0	—	0	—	0	—	ns
t_{OHZ}(2)	Output Enable High to Output High-Z	—	3.5	—	3.5	—	3.5	ns
Set Up Times								
t_{SA}	Address Setup Time	1.5	—	2	—	2	—	ns
t_{SS}	Address Status Setup Time	1.5	—	2	—	2	—	ns
t_{SD}	Data In Setup Time	1.5	—	2	—	2	—	ns
t_{SW}	Write Setup Time	1.5	—	2	—	2	—	ns
t_{SAV}	Address Advance Setup Time	1.5	—	2	—	2	—	ns
t_{SC}	Chip Enable/Select Setup Time	1.5	—	2	—	2	—	ns
Hold Times								
t_{HA}	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HS}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HD}	Data In Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HW}	Write Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HAV}	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HC}	Chip Enable/Select Hold Time	0.5	—	0.5	—	0.5	—	ns
Sleep Mode and Configuration Parameters								
t_{ZZPW}	ZZ Pulse Width	100	—	100	—	100	—	ns
t_{ZZR}(3)	ZZ Recovery Time	100	—	100	—	100	—	ns
t_{CFG}(4)	Configuration Set-up Time	34	—	40	—	50	—	ns

5309 tbl 16

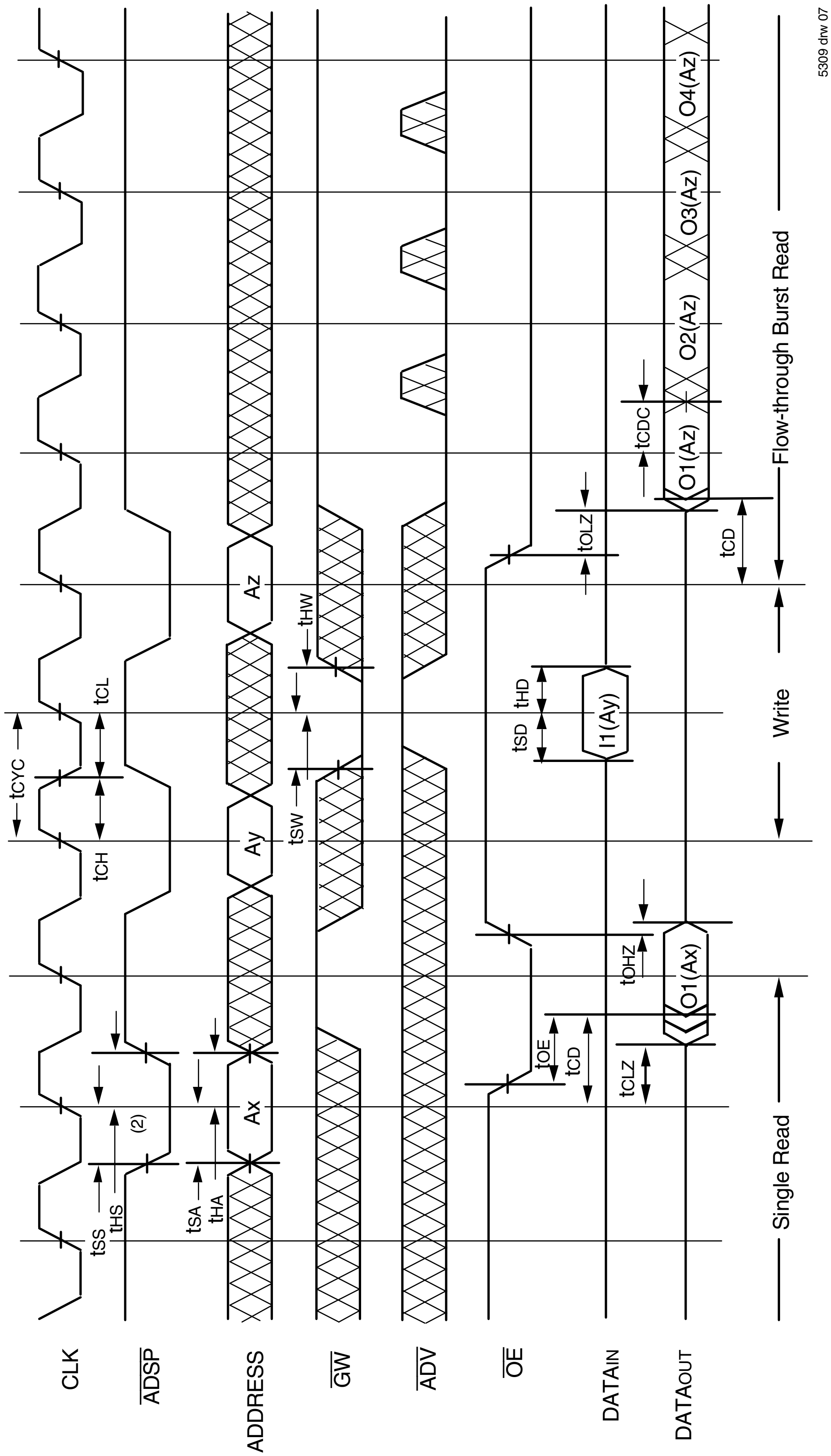
NOTES:
1. Measured as HIGH above V_{IH} and LOW below V_{IL}.
2. Transition is measured ±200mV from steady-state.
3. Device must be deselected when powered-up from sleep mode.
4. t_{CFG} is the minimum time required to configure the device based on the $\overline{LBO}$ input. $\overline{LBO}$ is a static input and must not change during normal operation.

Timing Waveform of Flow-Through Read Cycle (1,2)



NOTES:
1. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
2. ZZ input is LOW and $\overline{LBO}$ is Don't Care for this cycle.
3. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS}$1 signals. For example, when $\overline{CE}$ and $\overline{CS}$1 are LOW on this waveform, CS0 is HIGH.

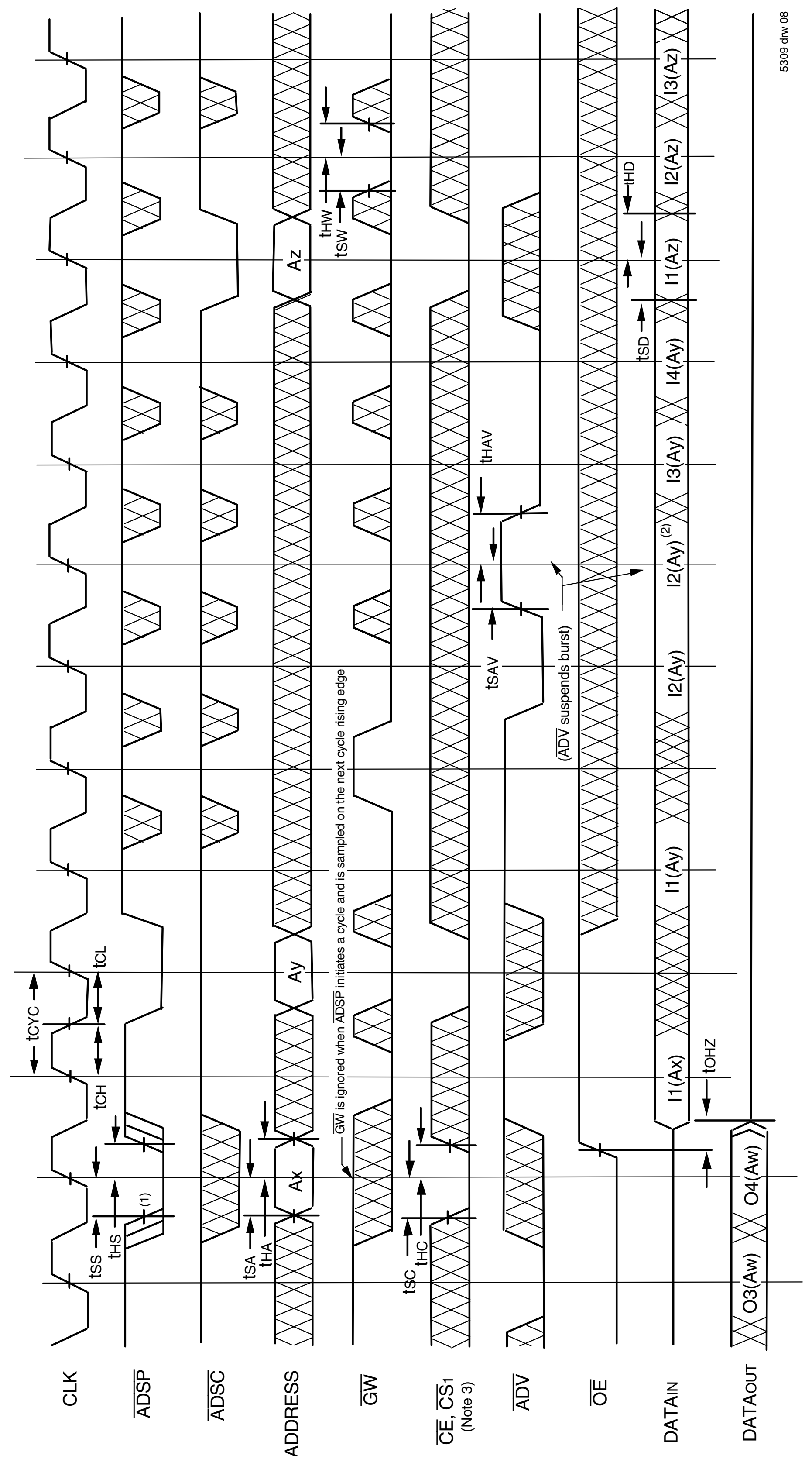
Timing Waveform of Combined Flow-Through Read and Write Cycles (1,2,3)



NOTES:

1. Device is selected through entire cycle; $\overline{CE}$ and $\overline{CS1}$ are LOW, CS0 is HIGH.
2. ZZ input is LOW and $\overline{LBO}$ is Don't Care for this cycle.
3. O1 (Ax) represents the first output from the external address Ax. I1 (Ay) represents the first input from the external address Ay; O1 (Az) represents the first output from the external address Az; O2 (Az) represents the next output data in the burst sequence of the base address Az, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.

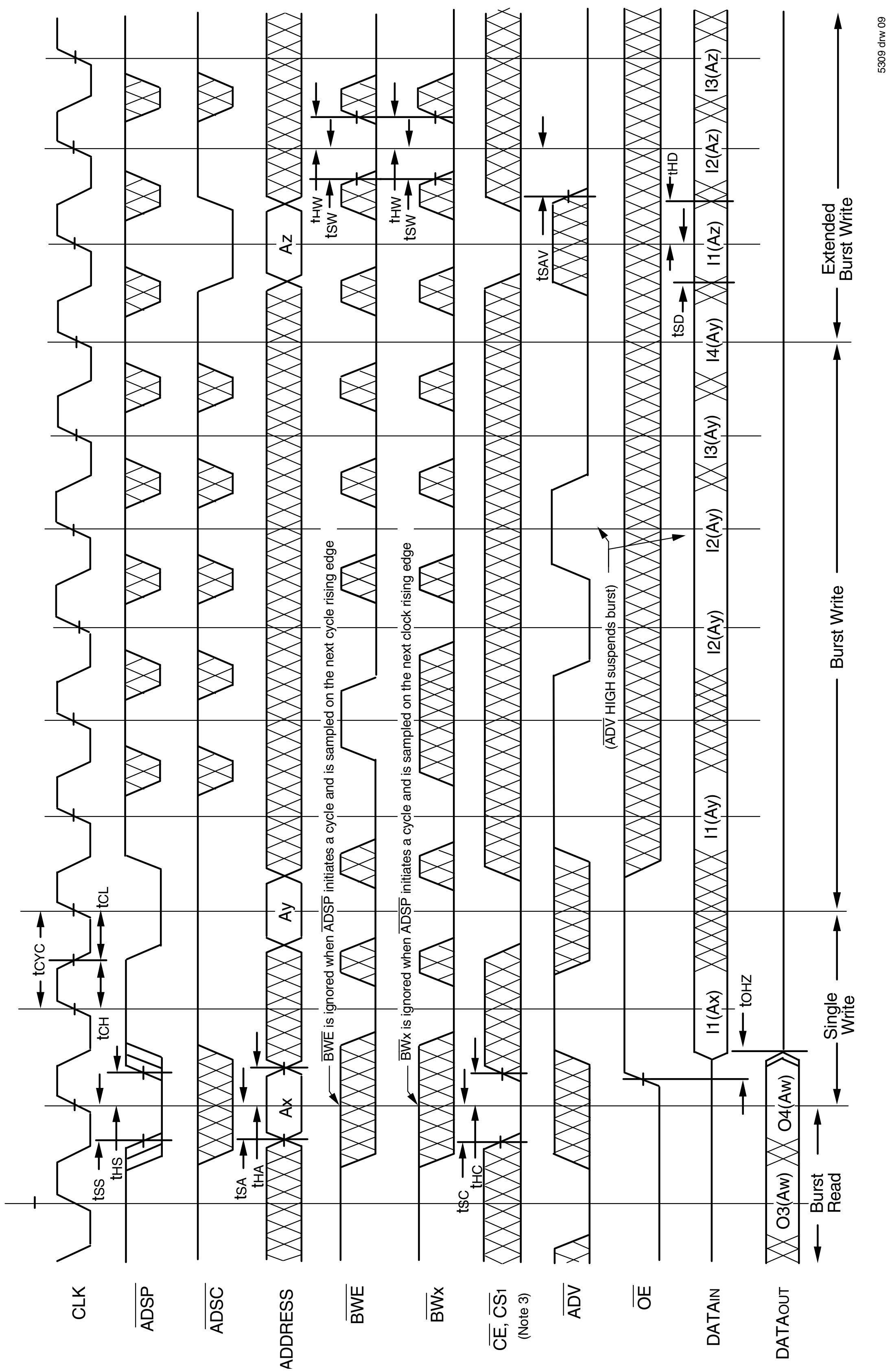
Timing Waveform of Write Cycle No. 1 - $\overline{GW}$ Controlled (1,2,3)



NOTES:

1. ZZ input is LOW, $\overline{BWE}$ is HIGH and $\overline{LBO}$ is Don't Care for this cycle.
2. O4 (Aw) represents the final output data in the burst sequence of the base address Aw. I1 (Ax) represents the first input from the external address Ax. I1 (Ay) represents the first input from the external address Ay; I2 (Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input. In the case of input I2 (Ay) this data is valid for two cycles because $\overline{ADV}$ is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS1}$ signals. For example, when $\overline{CE}$ and $\overline{CS1}$ are LOW on this waveform, CS0 is HIGH.

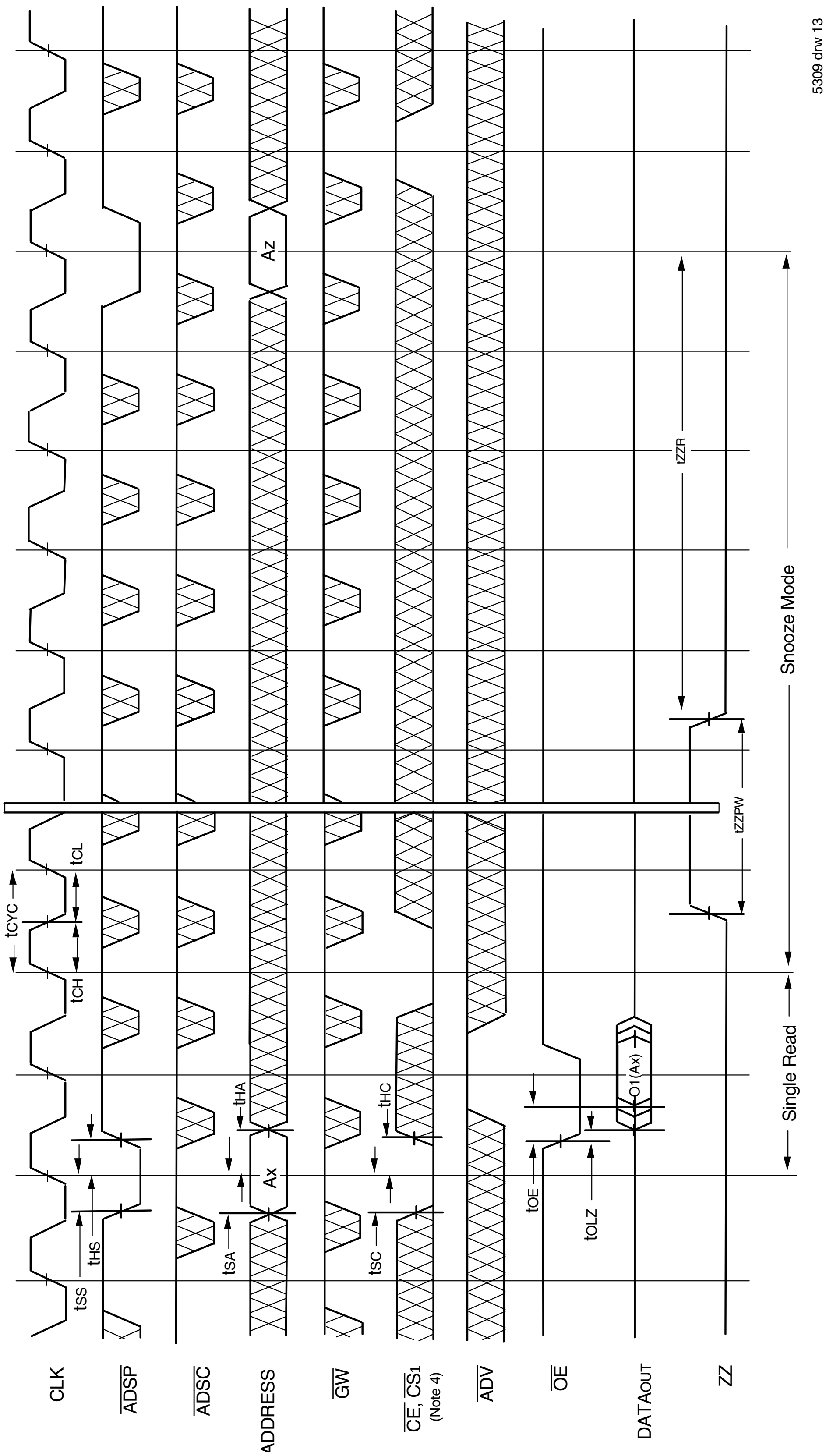
Timing Waveform of Write Cycle No. 2 - Byte Controlled (1,2,3)



NOTES:

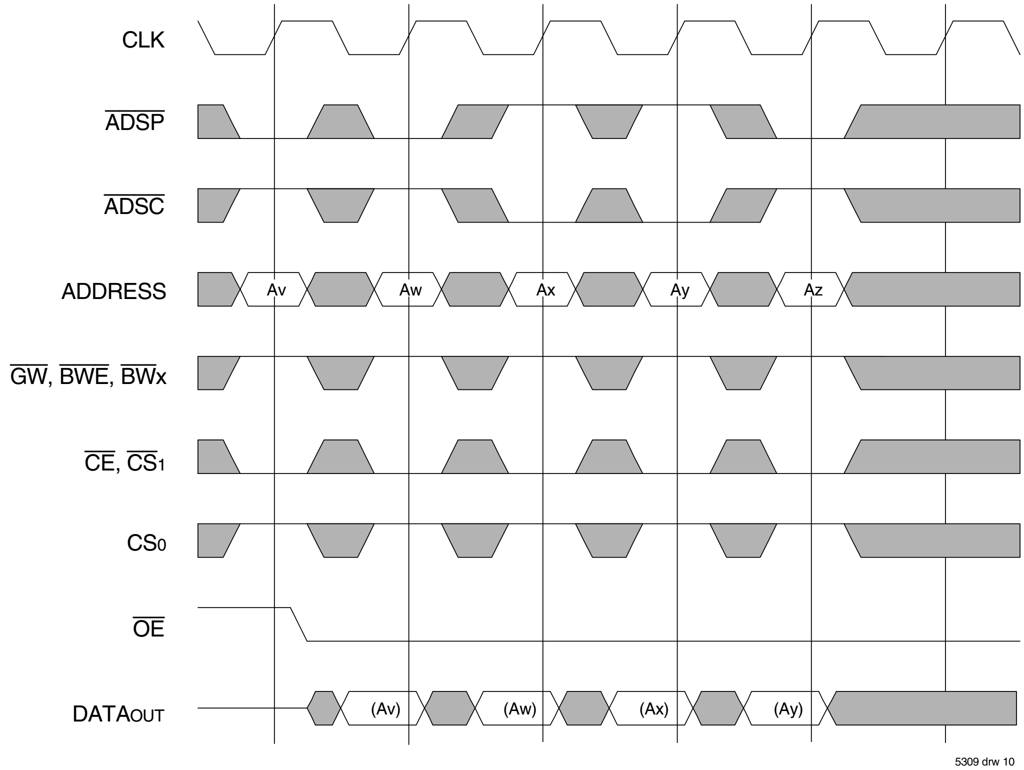
1. ZZ input is LOW, $\overline{GW}$ is HIGH and $\overline{LBO}$ is Don't Care for this cycle.
2. O4 (Aw) represents the final output data in the burst sequence of the base address Aw. I1 (Ax) represents the first input from the external address Ax. I1 (Ay) represents the first input from the external address Ay; I2 (Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input. In the case of input I2 (Ay) this data is valid for two cycles because $\overline{ADV}$ is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS1}$ signals. For example, when $\overline{CE}$ and $\overline{CS1}$ are LOW on this waveform, CS0 is HIGH.

Timing Waveform of Sleep (ZZ) and Power-Down Modes (1,2,3)



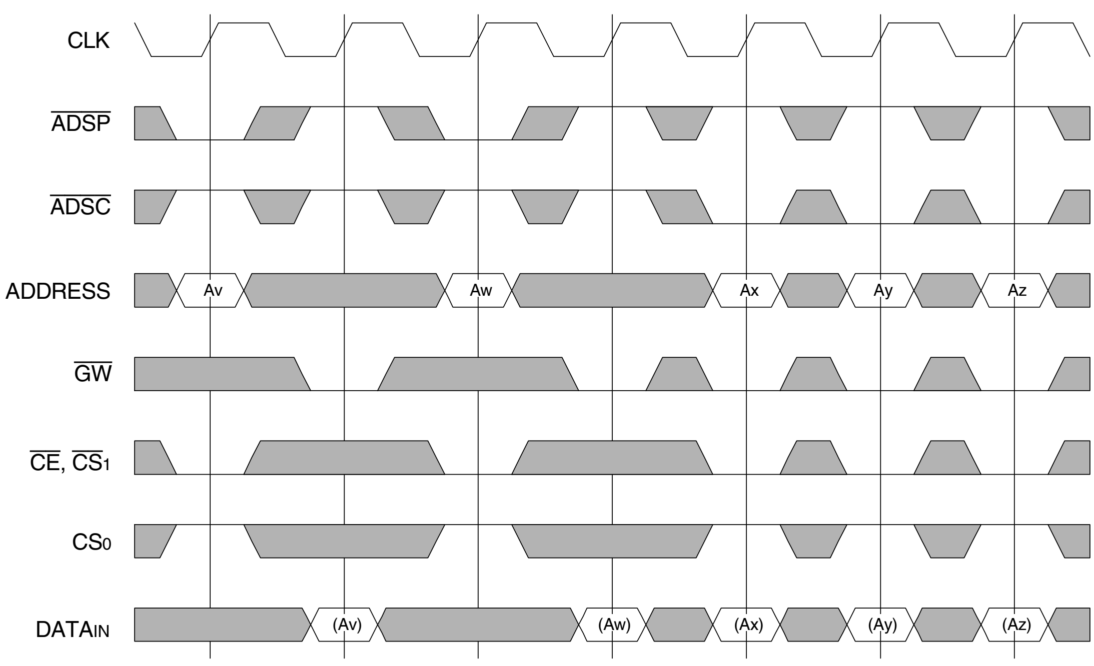
NOTES:
1. Device must power up in deselected Mode.
2. LBO is Don't Care for this cycle.
3. It is not necessary to retain the state of the input registers throughout the Power-down cycle.
4. CS0 timing transitions are identical but inverted to the CE and CS1 signals. For example, when CE and CS1 are LOW on this waveform, CS0 is HIGH.

Non-Burst Read Cycle Timing Waveform



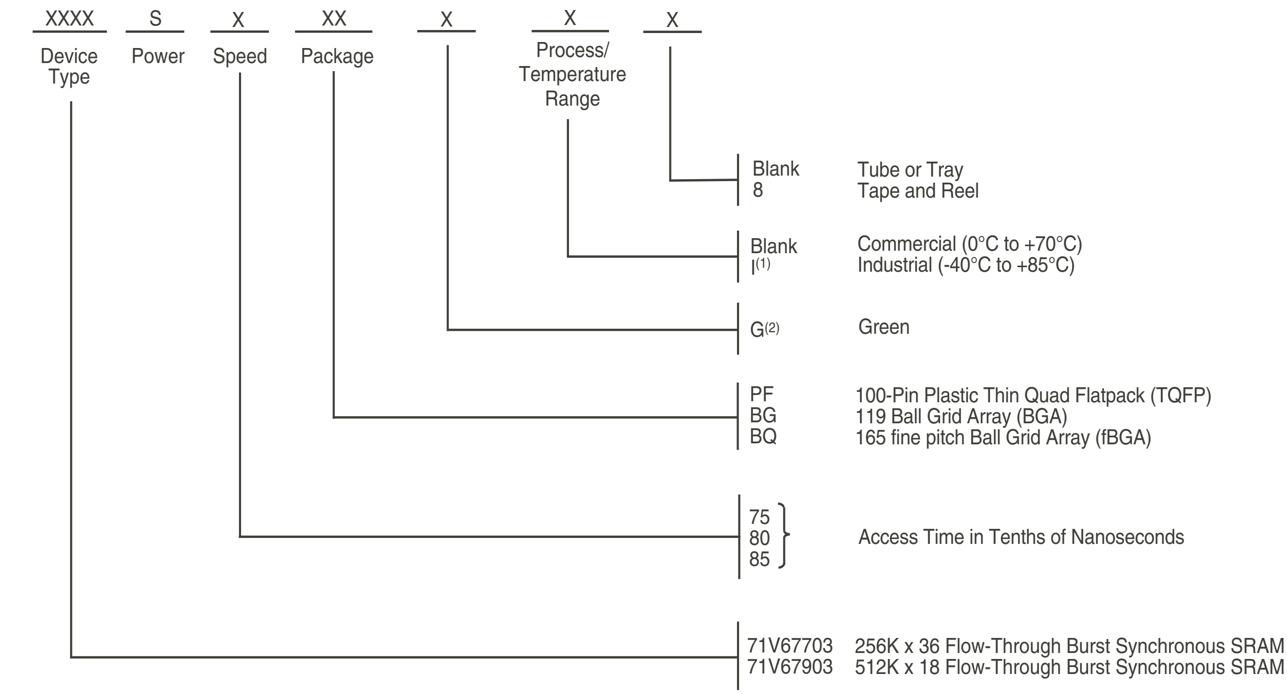
NOTES:
1. ZZ input is LOW, $\overline{ADV}$ is HIGH and $\overline{LBO}$ is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. For read cycles, $\overline{ADSP}$ and $\overline{ADSC}$ function identically and are therefore interchangeable.

Non-Burst Write Cycle Timing Waveform



NOTES:
1. ZZ input is LOW, $\overline{ADV}$ and $\overline{OE}$ are HIGH, and $\overline{LBO}$ is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. Although only $\overline{GW}$ writes are shown, the functionality of $\overline{BWE}$ and $\overline{BWx}$ together is the same as $\overline{GW}$.
4. For write cycles, $\overline{ADSP}$ and $\overline{ADSC}$ have different limitations.

Ordering Information



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NOTES:
1. Contact your local sales office for Industrial temp range for other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
7.5	71V67703S75BG	BG119	PBGA	C
	71V67703S75BG8	BG119	PBGA	C
	71V67703S75BGG	BGG119	PBGA	C
	71V67703S75BGG8	BGG119	PBGA	C
	71V67703S75BGGI	BGG119	PBGA	I
	71V67703S75BGGI8	BGG119	PBGA	I
	71V67703S75BQ	BQ165	CABGA	C
	71V67703S75BQ8	BQ165	CABGA	C
	71V67703S75BQG	BQG165	CABGA	C
	71V67703S75BQG8	BQG165	CABGA	C
	71V67703S75BQGI	BQG165	CABGA	I
	71V67703S75BQGI8	BQG165	CABGA	I
	71V67703S75PFG	PKG100	TQFP	C
	71V67703S75PFG8	PKG100	TQFP	C
	71V67703S75PFGI	PKG100	TQFP	I
	71V67703S75PFGI8	PKG100	TQFP	I
8.0	71V67703S80BG	BG119	PBGA	C
	71V67703S80BG8	BG119	PBGA	C
	71V67703S80BGG	BGG119	PBGA	C
	71V67703S80BGG8	BGG119	PBGA	C
	71V67703S80BGGI	BGG119	PBGA	I
	71V67703S80BGGI8	BGG119	PBGA	I
	71V67703S80BQ	BQ165	CABGA	C
	71V67703S80BQ8	BQ165	CABGA	C
	71V67703S80BQG	BQG165	CABGA	C
	71V67703S80BQG8	BQG165	CABGA	C
	71V67703S80BQGI	BQG165	CABGA	I
	71V67703S80BQGI8	BQG165	CABGA	I
	71V67703S80BQI	BQ165	CABGA	I
	71V67703S80BQI8	BQ165	CABGA	I
	71V67703S80PFG	PKG100	TQFP	C
	71V67703S80PFG8	PKG100	TQFP	C
	71V67703S80PFGI	PKG100	TQFP	I
	71V67703S80PFGI8	PKG100	TQFP	I

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
8.5	71V67703S85BG	BG119	PBGA	C
	71V67703S85BG8	BG119	PBGA	C
	71V67703S85BGG	BGG119	PBGA	C
	71V67703S85BGG8	BGG119	PBGA	C
	71V67703S85BGGI	BGG119	PBGA	I
	71V67703S85BGGI8	BGG119	PBGA	I
	71V67703S85BQ	BQ165	CABGA	C
	71V67703S85BQ8	BQ165	CABGA	C
	71V67703S85BQG	BQG165	CABGA	C
	71V67703S85BQG8	BQG165	CABGA	C
	71V67703S85BQGI	BQG165	CABGA	I
	71V67703S85BQGI8	BQG165	CABGA	I
	71V67703S85BQI	BQ165	CABGA	I
	71V67703S85BQI8	BQ165	CABGA	I
	71V67703S85PFG	PKG100	TQFP	C
	71V67703S85PFG8	PKG100	TQFP	C
	71V67703S85PFGI	PKG100	TQFP	I
	71V67703S85PFGI8	PKG100	TQFP	I

Orderable Part Information (con't)

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
7.5	71V67903S75BG	BG119	PBGA	C
	71V67903S75BG8	BG119	PBGA	C
	71V67903S75BQ	BQ165	CABGA	C
	71V67903S75BQ8	BQ165	CABGA	C
	71V67903S75BQI	BQ165	CABGA	I
	71V67903S75BQI8	BQ165	CABGA	I
	71V67903S75PFG	PKG100	TQFP	C
	71V67903S75PFG8	PKG100	TQFP	C
	71V67903S75PFGI	PKG100	TQFP	I
	71V67903S75PFGI8	PKG100	TQFP	I
8.0	71V67903S80BG	BG119	PBGA	C
	71V67903S80BG8	BG119	PBGA	C
	71V67903S80BQ	BQ165	CABGA	C
	71V67903S80BQ8	BQ165	CABGA	C
	71V67903S80BQI	BQ165	CABGA	I
	71V67903S80BQI8	BQ165	CABGA	I
	71V67903S80PFG	PKG100	TQFP	C
	71V67903S80PFG8	PKG100	TQFP	C
	71V67903S80PFGI	PKG100	TQFP	I
	71V67903S80PFGI8	PKG100	TQFP	I
8.5	71V67903S85BG	BG119	PBGA	C
	71V67903S85BG8	BG119	PBGA	C
	71V67903S85BQ	BQ165	CABGA	C
	71V67903S85BQ8	BQ165	CABGA	C
	71V67903S85BQI	BQ165	CABGA	I
	71V67903S85BQI8	BQ165	CABGA	I
	71V67903S85PFG	PKG100	TQFP	C
	71V67903S85PFG8	PKG100	TQFP	C
	71V67903S85PFGI	PKG100	TQFP	I
	71V67903S85PFGI8	PKG100	TQFP	I

Datasheet Document History

12/31/99		Created Datasheet from 71V677 and 71V679 Datasheets For 2.5V I/O offering, see 71V67702 AND 71V67902 Datasheets.
04/26/00	Pg. 4	Add capacitance for BGA package; Insert clarification note to Absolute Max Ratings and Recommended Operating Temperature tables.
	Pg. 7	Replace Pin U6 with $\overline{\text{TRST}}$ pin in BGA pin configuration; Add pin description note in pinout
	Pg. 18	Inserted 100 pin TQFP Package Diagram Outline
05/24/00	Pg. 1,4,8,21 22	Add new package offering, 13 x 15 fBGA
	Pg. 5,6,7,8	Correct note 2 on BGA and TQFP pin configuration
	Pg. 20	Correction in the 119 BGA Package Diagram Outline
07/12/00	Pg. 5,6,8	Remove note from TQFP and BQ165 pinouts
	Pg. 7	Add/Remove note from BG119 pinout
	Pg. 20	Update BG 119 pinout
12/18/00	Pg. 9	Updated ISB2 levels for 7.5-8.5ns.
10/29/01	Pg. 1,2	Remove JTAG pins
	Pg. 7	Changed U2-U6 pins to DNU.
	Pg. 8	Changed P5,P7,R5 & R7 to DNU pins.
	Pg. 9	Raised specs by 10mA on 7.5ns, 8ns and 8.5ns.
10/22/02	Pg. 1-23	Changed datasheet from Advanced to Final Release.
	Pg. 4,9,12, 22	Added I temp to datasheet.
04/15/03	Pg. 4	Updated 165 fBGA table from TBD to 7.
12/20/03	Pg. 7	Updated 119BGS pin configurations- reordered I/O signals on P6, P7 (128K x 36) and P7, N6, L6, K7, H6, G7, F6, E7, D6 (256K x 18).
02/20/09	Pg.22	Removed "IDT" from the orderable part number
11/19/14	Pg.1 & 20	Added green parts available note to Features & to Ordering Information
	Pg. 1-3	Moved the FBD, the pin description and pin definition tables to pages 1 - 3 respectively to align the datasheet reading flow to that of our other established datasheets
	Pg. 20	Added tape & reel to ordering information
	Pg. 19-21	Removed three Package Diagram Outlines. from this datasheet. Please see idt.com for Package Diagram Outlines specific to these devices.
08/11/21	Pg. 1-23	Rebranded as Renesas datasheet
	Pg. 1 & 19	Updated Industrial temp range and green availability
	Pg. 4-7	Updated package codes
	Pg. 20 & 21	Added Orderable Part Information tables

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For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.