16 x 16 PARALLEL CMOS MULTIPLIER-ACCUMULATOR

IDT7210L

FEATURES:

- 16 x 16 parallel multiplier-accumulator with selectable accumulation and subtraction
- High-speed: 20ns multiply-accumulate time
- IDT7210 features selectable accumulation, subtraction, rounding and preloading with 35-bit result
- IDT7210 is pin and function compatible with the TRW TDC1010J, TMC2210, Cypress CY7C510, and AMD AM29510
- Performs subtraction and double precision addition and multiplication
- Produced using advanced CMOS high-performance technology
- TTL-compatible
- Available in topbraze DIP, PLCC, Flatpack and Pin Grid Array
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-88733 is listed on this function
- Speeds available:
  Commercial: L20/25/35/45/55/65
  Military: L25/30/40/55/65/75

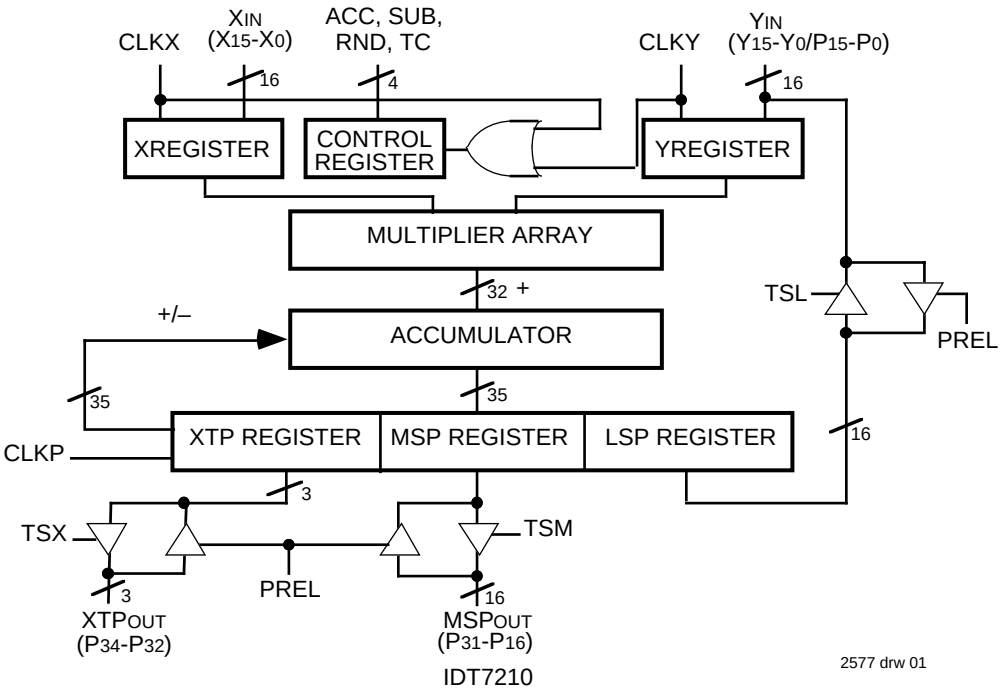
DESCRIPTION:

The IDT7210 is a high-speed, low-power 16 x 16-bit parallel multiplier-accumulator that is ideally suited for real-time digital signal processing applications. Fabricated using CMOS silicon gate technology, this device offers a very low-power alternative to existing bipolar and NMOS counterparts, with only 1/7 to 1/10 the power dissipation and exceptional speed (25ns maximum) performance.

A pin and functional replacement for TRW's TDC1010J the IDT7210 operates from a single 5 volt supply and is compatible with standard TTL logic levels. The architecture of the IDT7210 is fairly straightforward, featuring individual input and output registers with clocked D-type flip-flop, a preload capability which enables input data to be preloaded into the output registers, individual three-state output ports for the Extended Product (XTP) and Most Significant Product (MSP) and a Least Significant Product output (LSP) which is multiplexed with the Y input.

The X_{IN} and Y_{IN} data input registers may be specified through the use of the Two's Complement input (TC) as either a two's complement or an unsigned magnitude, yielding a full-precision 32-bit result that may be accumulated to a full 35-bit result. The three output registers – Extended Product (XTP), Most Most Significant Product (MSP) and Least Significant Product (LSP) – are controlled by the respective TSX, TSM and TSL input lines. The LSP output can be routed through Y_{IN} ports.

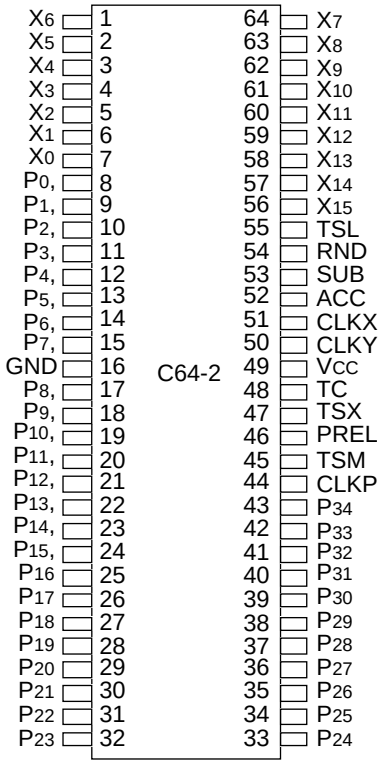
FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION (Continued)

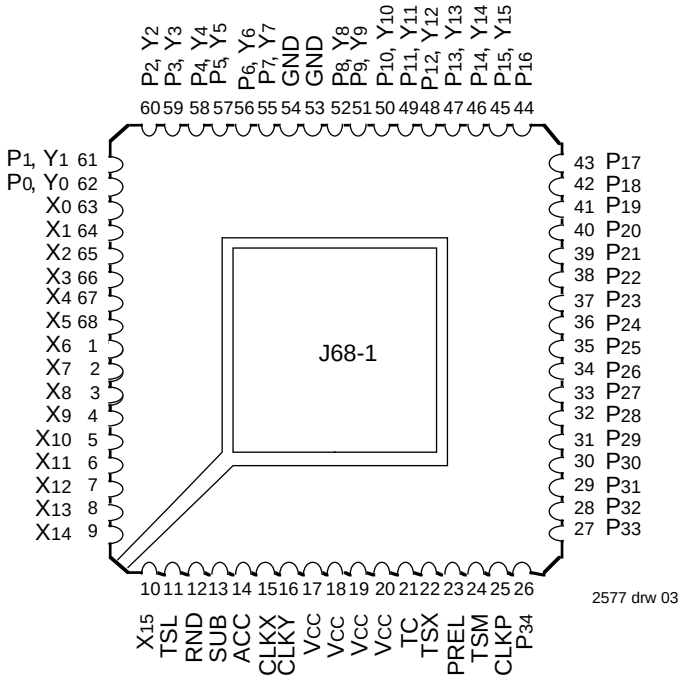
The Accumulate input (ACC) enables the device to perform either a multiply or a multiply-accumulate function. In the multiply-accumulate mode, output data can be added to or subtracted from previous results. When the Subtraction (SUB) input is active simultaneously with an active ACC, a subtraction can be performed. The double precision accumulated result is rounded down to either a single precision or single precision plus 3-bit extended result. In the multiply mode, the Extended Product output (XTP) is sign extended in the two's complement mode or set to zero in the unsigned mode. The Round (RND) control rounds up the Most Significant Product (MSP) and the 3-bit Extended Product (XTP) outputs. When Preload input (PREL) is active, all the output buffers are forced into a high-impedance state (see Preload truth table) and external data can be loaded into the output register by using the TSX, TSL and TSM signals as input controls.

PIN CONFIGURATIONS



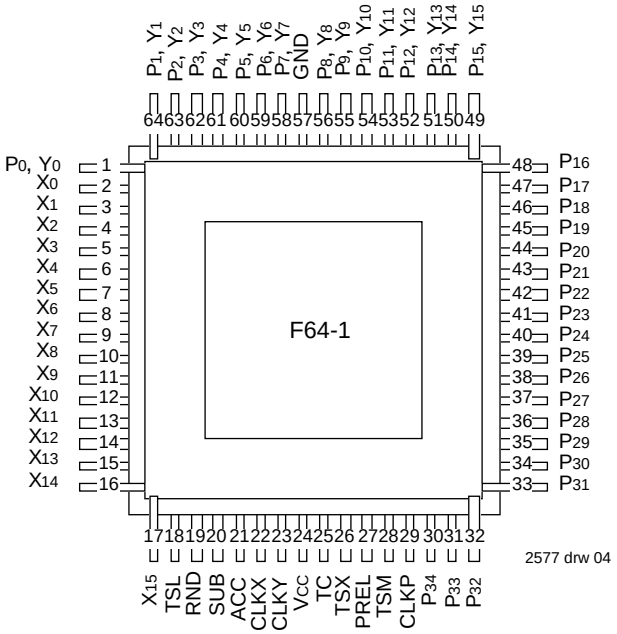
2577 drw 02

DIP
TOP VIEW



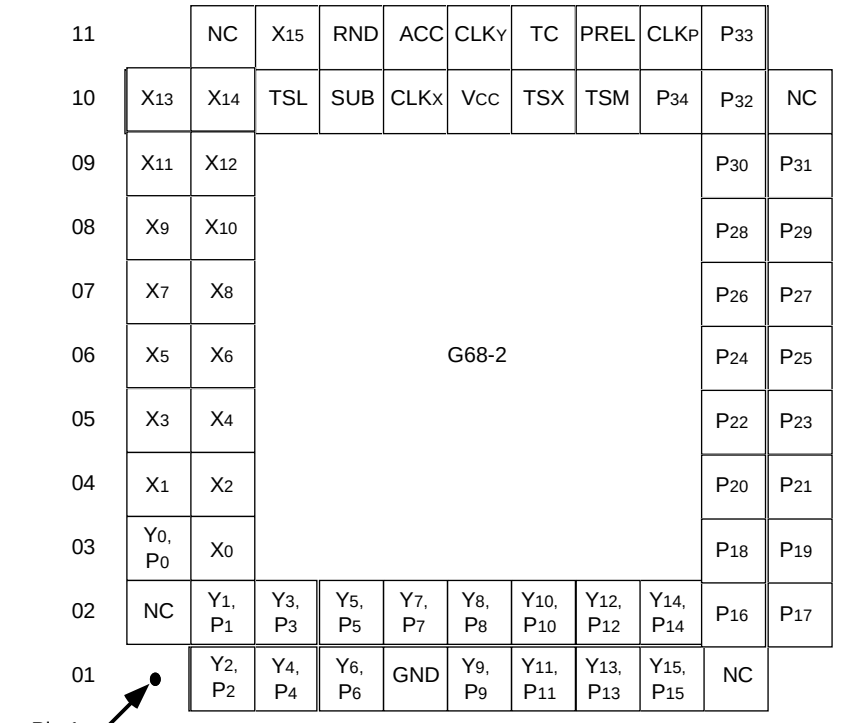
2577 drw 03

PLCC
TOP VIEW



2577 drw 04

FLATPACK
TOP VIEW



PGA
TOP VIEW

2577 drw 05

PIN DESCRIPTIONS

Pin Name	I/O	Description
$X_{0 - 15}$	I	Data Inputs
$Y_{0 - 15}$/ $P_{0 - 15}$	I/O	Multiplexed I/O port. $Y_{0 - 15}$ are data inputs and can be used to preload LSP register on PREL = 1. $P_{0 - 15}$ are LSP register outputs - enabled by TSL.
$P_{16 - 31}$	I/O	MSP register outputs - enabled by TSM. MSP register can be preloaded when PREL = 1.
$P_{32 - 34}$	I/O	XTP register outputs - enabled by TSX. XTP register can be preloaded through these inputs when PREL = 1.
CLKX	I	Input data $X_{0 - 15}$ loaded in X input register on CLKX rising edge.
CLKY	I	Input data $Y_{0 - 15}$ loaded in Y input register on CLKY rising edge.
CLKP	I	Output data loaded into output register on rising edge of CLKP.
TSX	I	TSX = 0 enables XTP outputs, TSX = 1 tristates $P_{32 - 34}$ lines.
TSM	I	TSM = 0 enables MSP outputs, TSM = 1 tristates $P_{16 - 31}$ lines.
TSL	I	TSL = 0 enables LSP outputs, TSL = 1 tristates $P_{0 - 15}$ lines.
PREL	I	When PREL= 1 data is input on $P_{0 - 15}$ lines. When PREL = 0, inputs on these lines are ignored.
ACC	I	This input is loaded into the control register on the rising edge of (CLKX + CLKY). When ACC = 1 and SUB = 0 an accumulate operation is performed. When ACC = 1 and SUB = 1, a subtract operation is performed. When ACC = 0, the SUB input is a don't care and the device acts as a simple multipler with no accumulation
SUB	I	This input is loaded into the control register on the rising edge of (CLKX + CLKY). This input is active only when ACC = 1. When SUB = 1 the contents of the output register are subtracted from the result and stored back in the output register. When SUB = 0 the contents of the output register are added to the result and stored back in the output register
TC	I	This input is loaded into the control register on the rising edge of (CLKX + CLKY). When TC = 1, the X and Y input are assumed to be in two's complement form. When TC = 0, X and Y inputs are assumed to be in unsigned magnitude form
RND	I	This input is loaded into the control register on the rising edge of (CLKX + CLKY). RND is inactive when low. RND = 1, adds a "1" to the most significant bit of the LSP, to round MSP and XTP data

2577 tbl 01

PRELOAD TRUTH TABLE

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Hi Z
0	0	1	0	Q	Hi Z	Q
0	0	1	1	Q	Hi Z	Hi Z
0	1	0	0	Hi Z	Q	Q
0	1	0	1	Hi Z	Q	Hi Z
0	1	1	0	Hi Z	Hi Z	Q
0	1	1	1	Hi Z	Hi Z	Hi Z
1	0	0	0	Hi Z	Hi Z	Hi Z
1	0	0	1	Hi Z	Hi Z	PL
1	0	1	0	Hi Z	PL	Hi Z
1	0	1	1	Hi Z	PL	PL
1	1	0	0	PL	Hi Z	Hi Z
1	1	0	1	PL	Hi Z	PL
1	1	1	0	PL	PL	Hi Z
1	1	1	1	PL	PL	PL

NOTES: 2577 tbl 02

Hi Z = Output buffers at high impedance (output disabled)
Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.
PL = Output buffers at high impedance or output disabled. Preload data supplied externally at output pins will be loaded into the output register at the rising edge of CLKP.

NOTES ON TWO'S COMPLEMENT FORMATS

1. In two's complement notation, the location of the binary point that signifies the separation of the fractional and integer fileds is just after the sign, between the sign bit (-2^0) and the next significant bit for the multiplier inputs. This same format is carried over to the output format, except that the extended significance of the integer filed is provided to extend the utility of the accumulator. In the case of the output rotation, the output binary point is located between the2^0 and 2^1 bit positions. The location of the binary point is arbitrary, as long as there is consistency with both the input and output formats. The number filed can be considered entirely integer with the binary point just to the right of the least significant bit for the input, product and the accumulated sum.
2. When in the non-accumulating mode, the first four bits (P_{34} to P_{31}) will all indicate the sign of the product. Additionally, the P_{30} term will also indicate the sign with one exception, when multiplying -1 x -1. With the additional bits that are available in this multiplier, the –1 x –1 is a valid operation that yields a +1 product.
3. In operations that require the accumulation of single products or sum of products, there is no change in format. To allow for a valid summation beyond that available for a single multiplication product, three additional significant bits (guard bits) are provided. This is the same as if the product was accumulated off-chip in a separate 35-bit wide adder. Taking the sign at the most significant bit position will guarantee that the largest number field will be used. When the accumulated sum only occupies the right hand portion of the accumulator, the sign will be extended into the lesser significant bit positions.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{CC}	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5V	–0.5 to V_{CC} +0.5V	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2577 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2577 tbl 04

1. This parameter is measured at characterization and not 100%tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

Symbol	Parameter	Test Conditions[5]	Commercial			Military			Unit
			Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max.	
V_{IH}	Input High Voltage	Guaranteed Logic HIGH Level	2.0	—	—	2.0	—	—	V
V_{IL}	Input Low Voltage	Guaranteed Logic LOW Level	—	—	0.8	—	—	0.8	V
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0V to V_{CC}	—	—	10	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., Outputs Disabled V_{OUT} = 0 to V_{CC}	—	—	10	—	—	10	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0mA	2.4	—	—	2.4	—	—	V
V_{OL}[4]	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	—	0.4	—	—	0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_0 GND	-20	—	-100	-20	—	-100	mA
I_{CC}[2]	Operating Power Supply Current	V_{CC} = Max., Outputs Enabled f= 10MHz[2] C_L = 50 pF	—	45	90	—	45	110	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	20	30	—	20	30	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ –0.2V, $V_{IN} \leq$ 0.2V	—	4	10	—	4	12	mA
I_{CC}/f[2,3]	Increase in Power Supply Current MHz	V_{CC} = Max., Outputs Disabled	—	—	6	—	—	8	mA/ MHz

NOTES:

2577 tbl 05

1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = 0 to 3V. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 90+ 6(f –10)mA, where f = operating frequency in MHz. For the military range, I_{CC} = 110 + 8(f –10). f = operating frequency in MHz, f = 1/t_{MA}.
3. For frequencies greater than 10MHz, guaranteed by design, not production tested.
4. I_{OL} = 4mA for t_{MA} > 55ns.
5. For conditions shown as Max. or Min., use appropriate value specified under electrical characteristics.

AC ELECTRICAL CHARACTERISTICS COMMERCIAL (V_{CC} = 5V ± 10%, T_A = 0° to +70°C)

Symbol	Parameter	7210L20		7210L25		7210L35		7210L45		7210L55		7210L65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{MA}	Multiply-Accumulate Time[2]	2.0	20	2.0	25	2.0	35	2.0	45	2.0	55	2.0	65	ns
t_D	Output Delay[2]	2.0	18	2.0	20	2.0	25	2.0	25	2.0	30	2.0	35	ns
t_{ENA}	3-State Enable Time	—	18	–	20	–	25	–	25	–	30	–	30	ns
t_{DIS}	3-State Disable Time[1]	—	18	–	20	–	25	–	25	–	30	–	30	ns
t_S	Input Register Set-up Time	10	—	12	–	12	–	15	–	20	–	25	–	ns
t_H	Input Register Hold Time	3	—	3	–	3	–	3	–	3	–	3	–	ns
t_{PW}	Clock Pulse Width	9	—	10	–	10	–	15	–	20	–	25	–	ns
t_{HCL}	Relative Hold Time	0	—	0	–	0	–	0	–	0	–	0	–	ns

NOTES:

2577 tbl 06

1. Transition is measured ±500mV from steady state voltage.
2. Minimum delays guaranteed but not tested

AC ELECTRICAL CHARACTERISTICS MILITARY (V_{CC} = 5V ± 10%, T_A = –55° to +125°C)

Symbol	Parameter	7210L25		7210L30		7210L40		7210L55		7210L65		7210L75		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{MA}	Multiply-Accumulate Time[2]	2.0	25	2.0	30	2.0	40	2.0	55	2.0	65	2.0	75	ns
t_D	Output Delay[2]	2.0	20	2.0	20	2.0	25	2.0	30	2.0	35	2.0	35	ns
t_{ENA}	3-State Enable Time	—	20	–	20	–	25	–	30	–	30	–	35	ns
t_{DIS}	3-State Disable Time[1]	—	20	–	20	–	25	–	25	–	30	–	30	ns
t_S	Input Register Set-up Time	12	—	12	–	15	–	20	–	25	–	25	–	ns
t_H	Input Register Hold Time	3	—	3	–	3	–	3	–	3	–	3	–	ns
t_{PW}	Clock Pulse Width	10	—	10	–	15	–	20	–	25	–	25	–	ns
t_{HCL}	Relative Hold Time	0	—	0	–	0	–	0	–	0	–	0	–	ns

NOTES:

2577 tbl 07

1. Transition is measured ±500mV from steady state voltage.
2. Minimum delays guaranteed but not tested

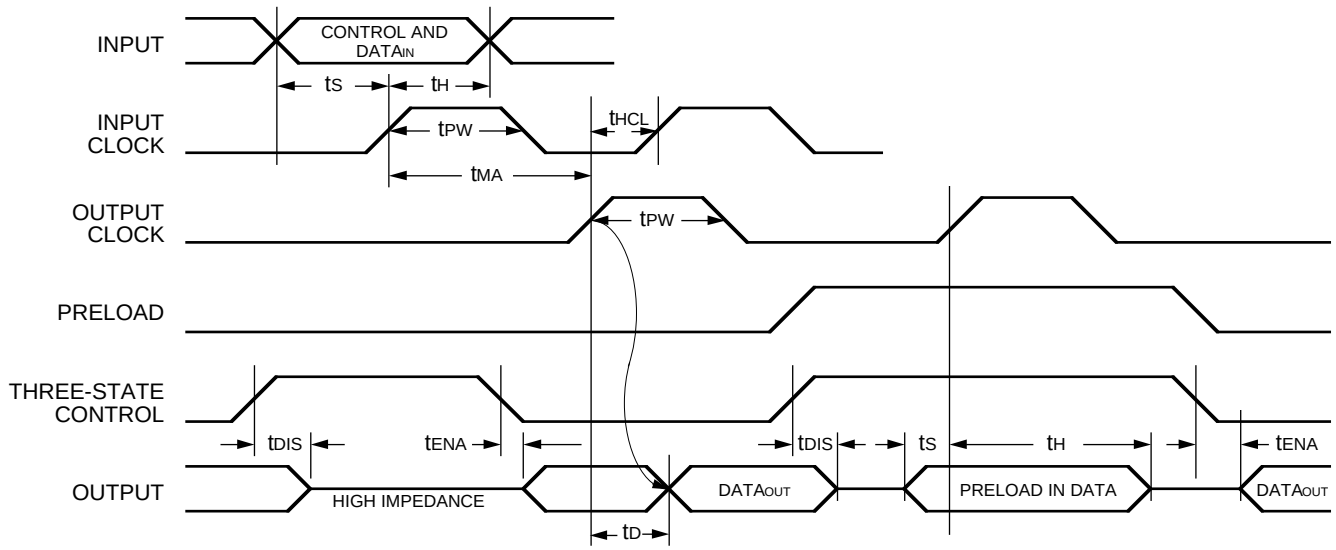


Figure 1. Timing Diagram

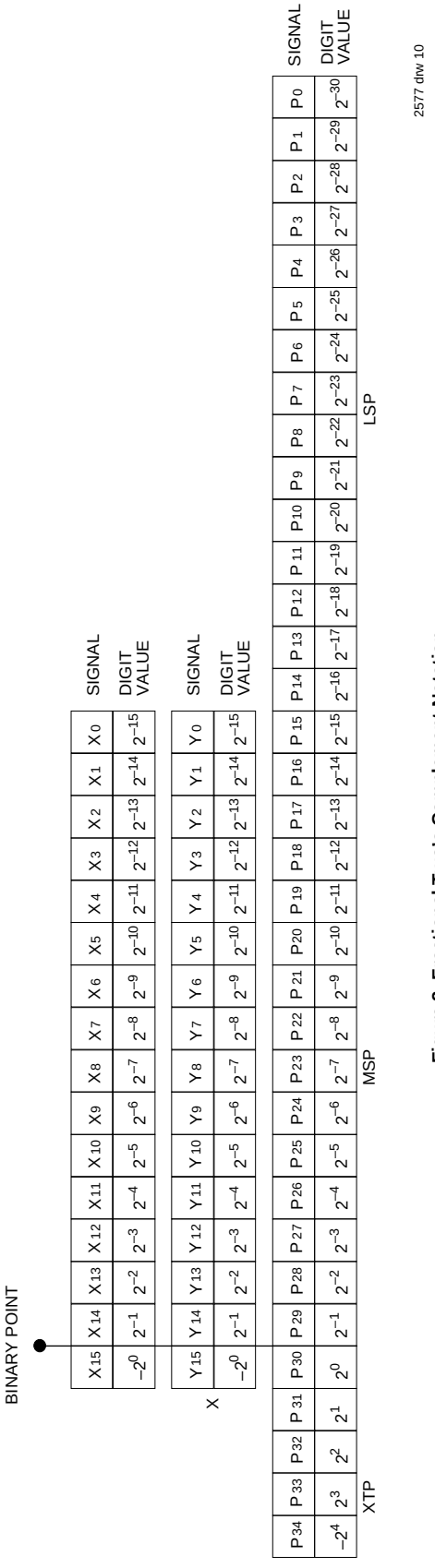


Figure 2. Fractional Two's Complement Notation.

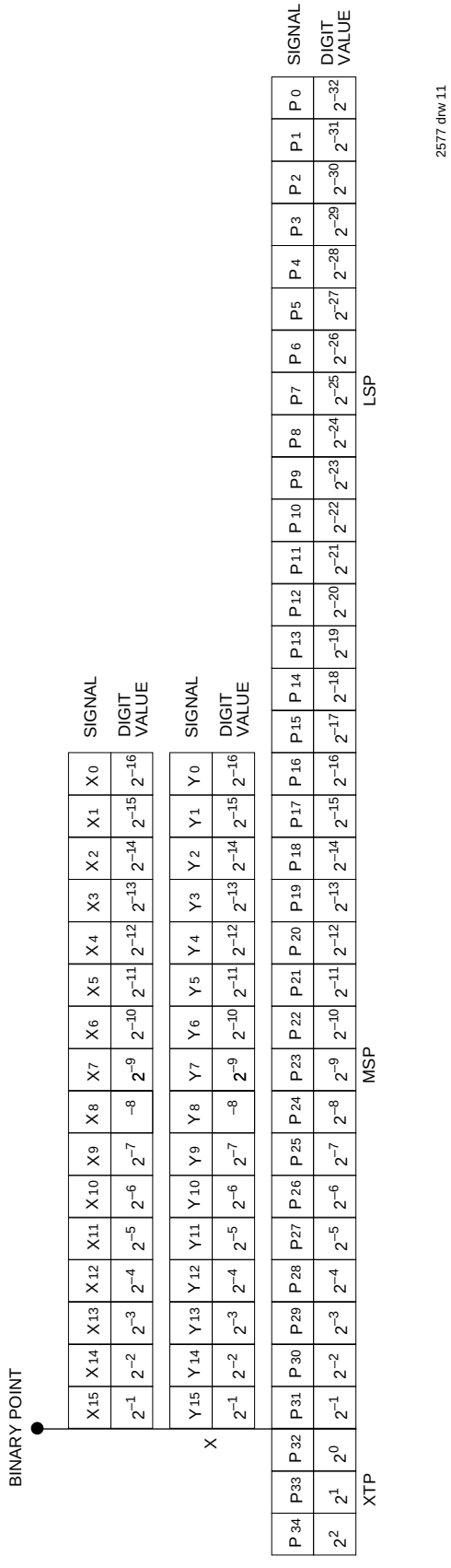


Figure 3. Fractional Unsigned Mgnitude Notation

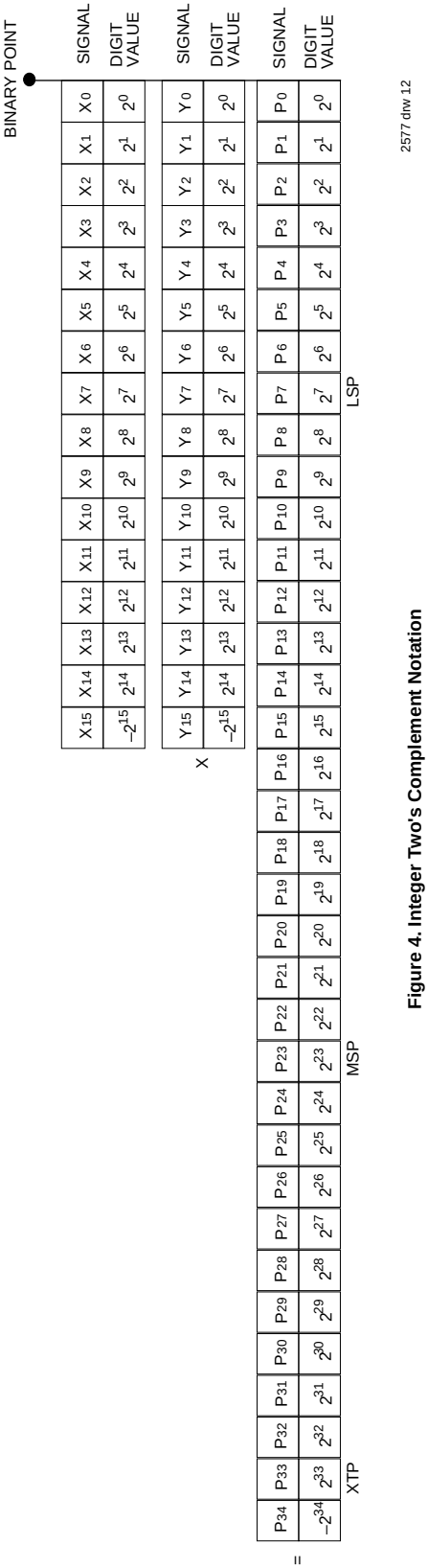


Figure 4. Integer Two's Complement Notation

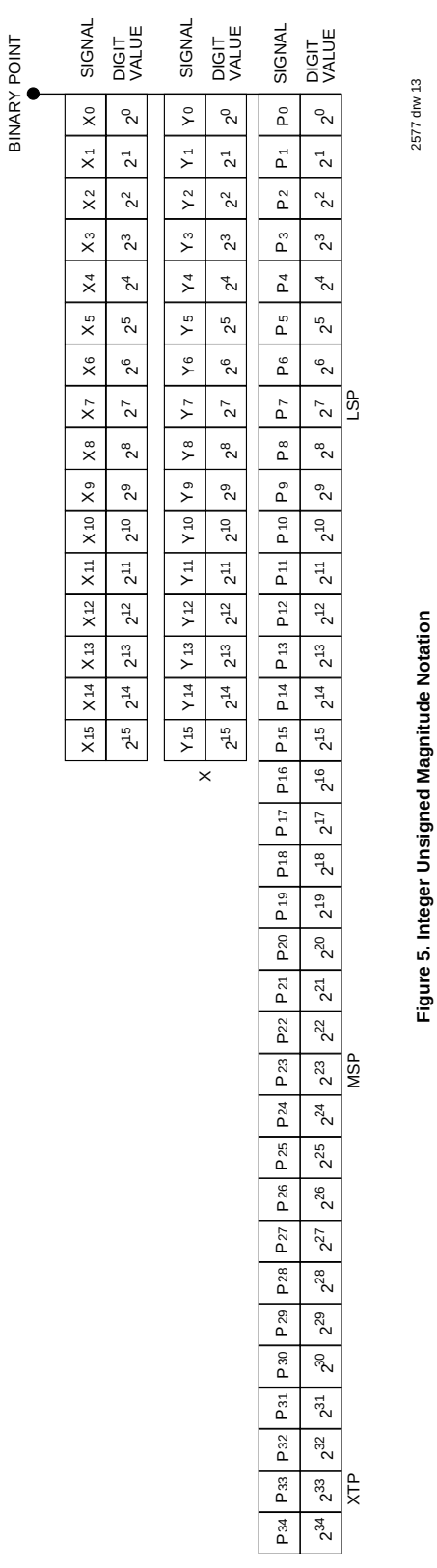
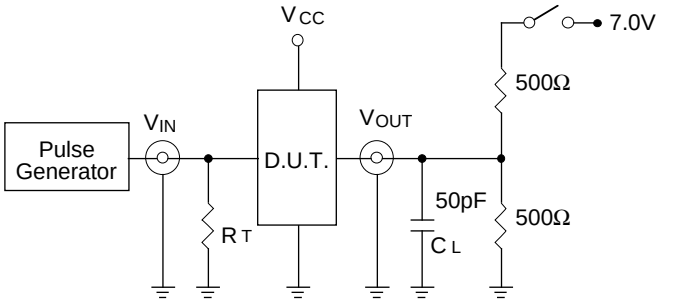


Figure 5. Integer Unsigned Magnitude Notation

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2577 drw 06

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

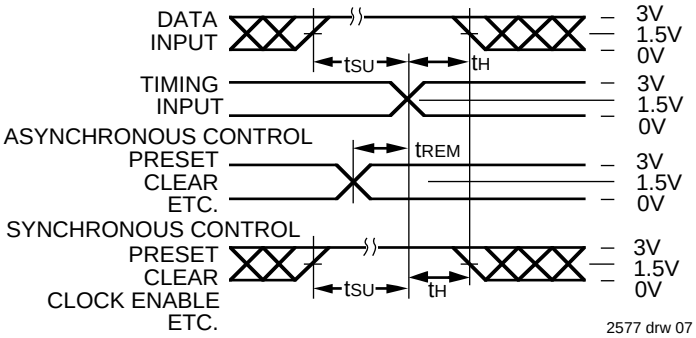
2577 lnk 09

DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.

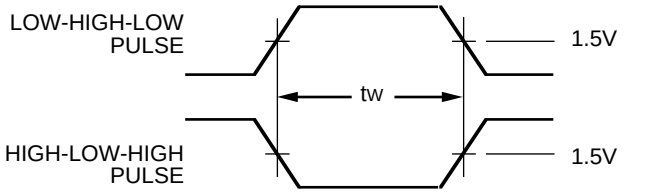
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



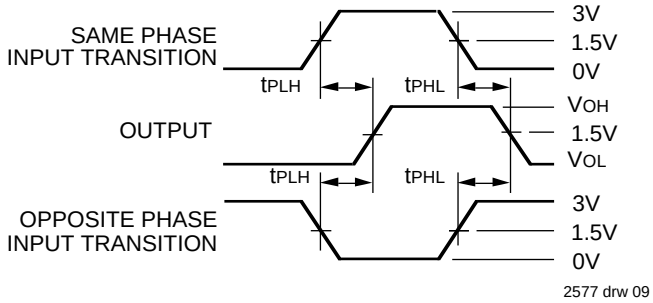
2577 drw 07

PULSE WIDTH



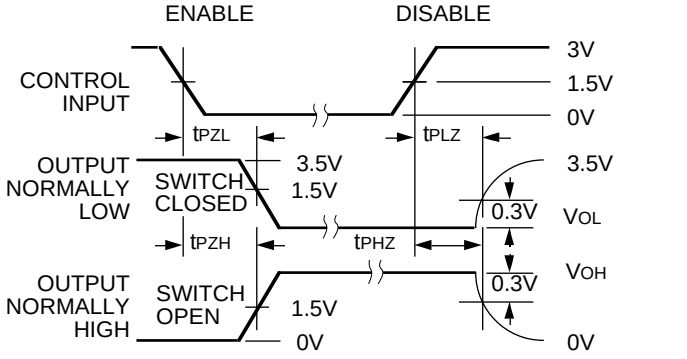
2577 drw 08

PROPAGATION DELAY



2577 drw 09

ENABLE AND DISABLE TIMES

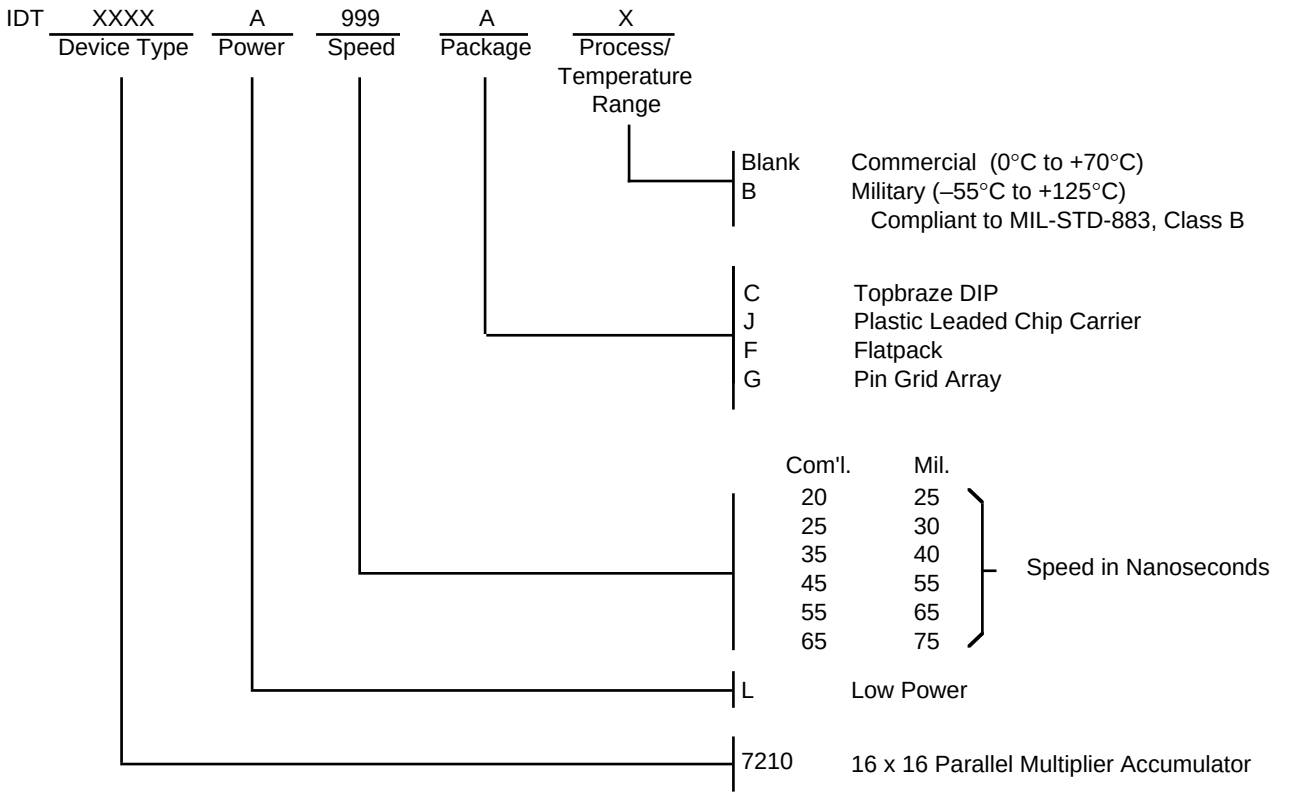


2577 drw 10

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2577 drw 11

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