RENESAS

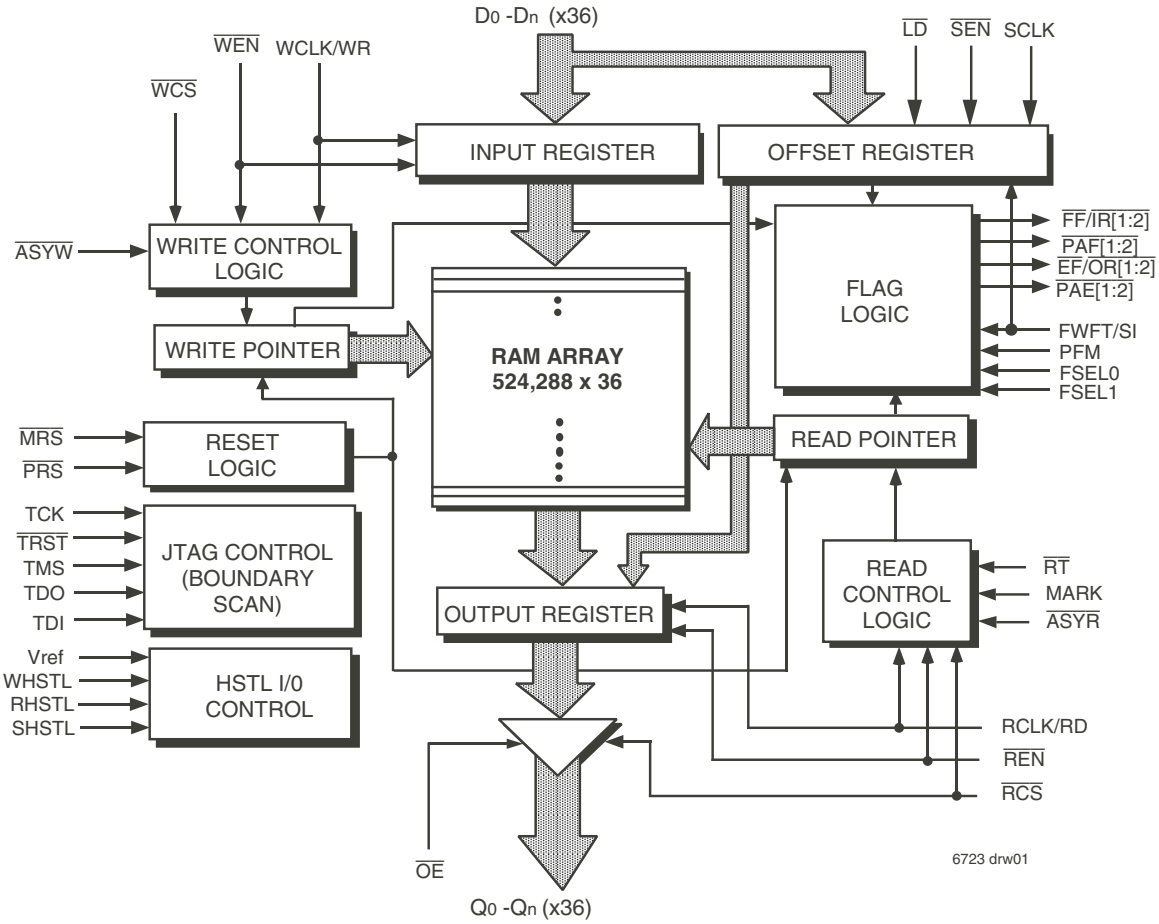
2.5V 18M-BIT HIGH-SPEED TeraSync™ FIFO 36-BIT CONFIGURATIONS 524,288 x 36

IDT72T36135M

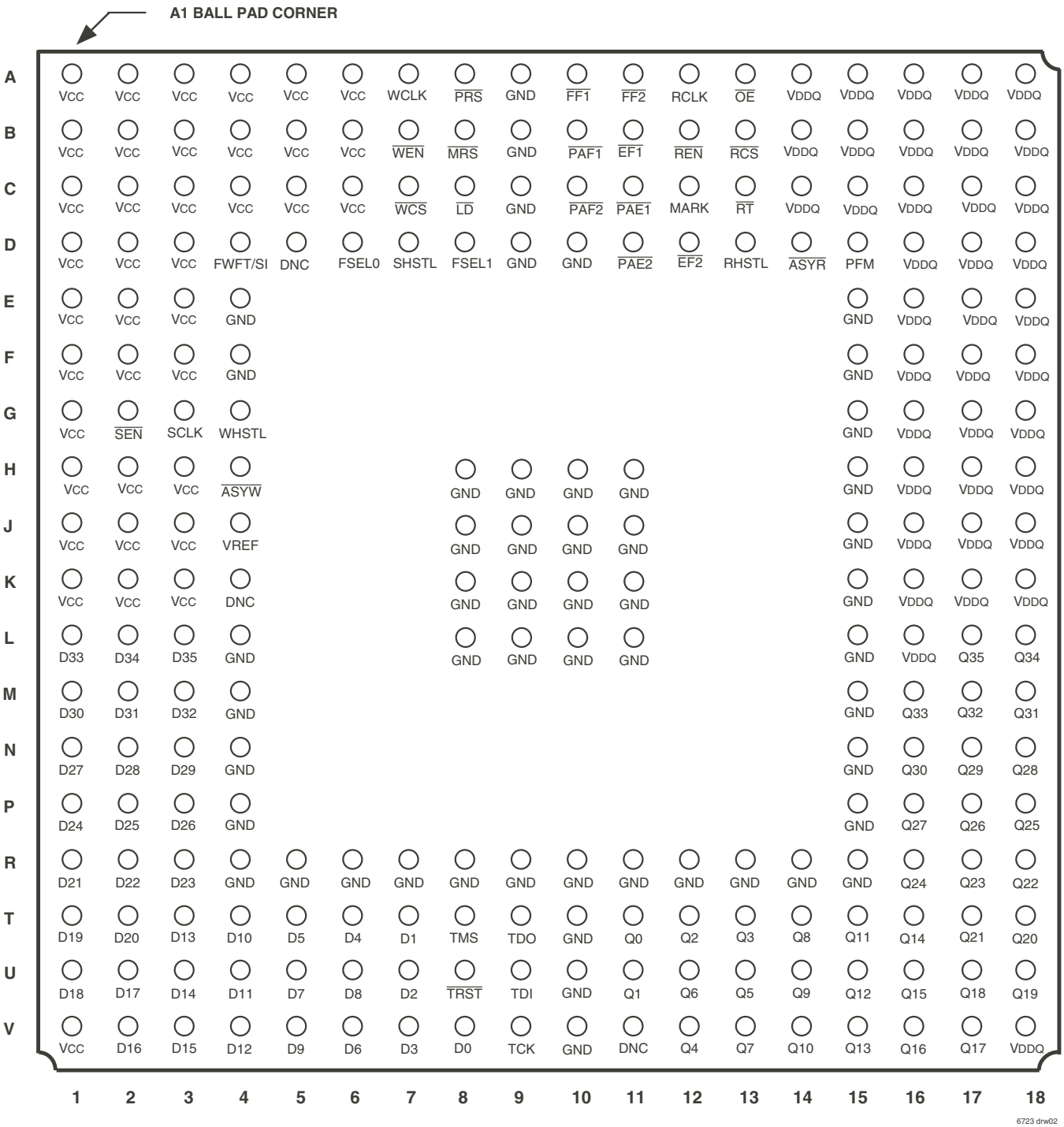
FEATURES:

- Industry's largest FIFO memory organization:
  IDT72T36135 — 524,288 x 36 - 18M-bits
- Up to 200 MHz Operation of Clocks
- Functionally and pin compatible to 9Mbit IDT72T36125 TeraSync devices
- User selectable HSTL/LVTTL Input and/or Output
- User selectable Asynchronous read and/or write port timing
- Mark & Retransmit, resets read pointer to user marked position
- Write Chip Select ($\overline{WCS}$) input disables Write Port
- Read Chip Select ($\overline{RCS}$) synchronous to RCLK
- Programmable Almost-Empty and Almost-Full flags, each flag can default to one of eight preselected offsets
- Program programmable flags by either serial or parallel means
- Selectable synchronous/asynchronous timing modes for Almost-Empty and Almost-Full flags
- Separate SCLK input for Serial programming of flag offsets
- Auto power down minimizes standby power consumption
- Master Reset clears entire FIFO
- Partial Reset clears data, but retains programmable settings
- Empty and Full flags signal FIFO status
- Select IDT Standard timing (using $\overline{EF}$[1:2] and $\overline{FF}$[1:2] flags) or First Word Fall Through timing (using $\overline{OR}$[1:2] and $\overline{IR}$[1:2] flags)
- Output enable puts data outputs into high impedance state
- JTAG port, provided for Boundary Scan function
- Available in 240-pin (19mm x 19mm)Plastic Ball Grid Array (PBGA) 50% more space saving than the leading 9M-bit FIFOs
- Independent Read and Write Clocks (permit reading and writing simultaneously)
- High-performance submicron CMOS technology
- Industrial temperature range (–40°C to +85°C) is available
- Green parts available, see ordering information

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



NOTE:
1. DNC - Do Not Connect.

PBGA: 1mm pitch, 19mm x 19mm (BB240, order code: BB)
TOP VIEW

DESCRIPTION:

The IDT72T36135M is an exceptionally deep, extremely high speed, CMOS First-In-First-Out (FIFO) memory with clocked read and write controls and a wide extended x36 bus to allow ample data flow. These FIFOs offer several key user benefits:

- High density offering of 18 Mbit
- 200MHz R/W Clocks supporting 7.2Gbps of data throughput
- User selectable MARK location for retransmit
- User selectable I/O structure for HSTL or LVTTL
- Asynchronous/Synchronous translation on the read or write ports
- The first word data latency period, from the time the first word is written to an empty FIFO to the time it can be read, is fixed and short.

TeraSync FIFOs are particularly appropriate for network, video, telecommunications, data communications and other applications that need to buffer large amounts of data at very high performance.

The input port can be selected as either a Synchronous (clocked) interface, or Asynchronous interface. During Synchronous operation the input port is controlled by a Write Clock (WCLK) input and a Write Enable ($\overline{WEN}$) input. Data present on the Dn data inputs is written into the FIFO on every rising edge of WCLK when $\overline{WEN}$ is asserted. During Asynchronous operation only the WR input is used to write data into the FIFO. Data is written on a rising edge of WR, the $\overline{WEN}$ input should be tied to its active state, (LOW).

The input port can be selected for either 2.5V LVTTL or HSTL operation, this operation is selected by the state of the WHSTL input during a master reset. A Write Chip Select input ($\overline{WCS}$) is provided for use when the write port is in both LVTTL and HSTL modes. During operation the $\overline{WCS}$ input can be used to disable write port inputs (data only).

The output port can be selected as either a Synchronous (clocked) interface, or Asynchronous interface. During Synchronous operation the output port is controlled by a Read Clock (RCLK) input and Read Enable ($\overline{REN}$) input. Data is read from the FIFO on every rising edge of RCLK when $\overline{REN}$ is asserted. During Asynchronous operation only the RD input is used to read data from the FIFO. Data is read on a rising edge of RD, the $\overline{REN}$ input should be tied to its active state, LOW. When Asynchronous operation is selected on the output port the FIFO must be configured for Standard IDT mode, also the $\overline{RCS}$ should be tied LOW and the $\overline{OE}$ input used to provide three-state control of the outputs, Qn.

The output port can be selected for either 2.5V LVTTL or HSTL operation, this operation is selected by the state of the RHSTL input during a master reset.

An Output Enable ($\overline{OE}$) input is provided for three-state control of the outputs. A Read Chip Select ($\overline{RCS}$) input is also provided, the $\overline{RCS}$ input is synchronized to the read clock, and also provides three-state control of the Qn data outputs. When $\overline{RCS}$ is disabled, the data outputs will be high impedance. During Asynchronous operation of the output port, $\overline{RCS}$ should be enabled, held LOW.

The frequencies of both the RCLK and the WCLK signals may vary from 0 to f_{MAX} with complete independence. There are no restrictions on the frequency of the one clock input with respect to the other.

There are two possible timing modes of operation with these devices: IDT Standard mode and First Word Fall Through (FWFT) mode.

In *IDT Standard mode,* the first word written to an empty FIFO will not appear on the data output lines unless a specific read operation is performed. A read operation, which consists of activating $\overline{REN}$ and enabling a rising RCLK edge, will shift the word from internal memory to the data output lines.

In *FWFT mode,* the first word written to an empty FIFO is clocked directly to the data output lines after three transitions of the RCLK signal. A $\overline{REN}$ does not have to be asserted for accessing the first word. However, subsequent words written to the FIFO do require a LOW on $\overline{REN}$ for access. The state of the FWFT/SI input during Master Reset determines the timing mode in use.

For applications requiring more data storage capacity than a single FIFO can provide, the FWFT timing mode permits depth expansion by chaining FIFOs in series (i.e. the data outputs of one FIFO are connected to the corresponding data inputs of the next). No external logic is required.

The 18M-bit TeraSync FIFO has 8 flag pins, $\overline{EF}$/$\overline{OR}$[1:2] (Empty Flag or Output Ready), $\overline{FF}$/$\overline{IR}$[1:2] (Full Flag or Input Ready), $\overline{PAE}$[1:2] (Programmable Almost-Empty flag) and $\overline{PAF}$[1:2] (Programmable Almost-Full flag). The $\overline{EF}$[1:2] and $\overline{FF}$[1:2] functions are selected in IDT Standard mode. The $\overline{IR}$[1:2] and $\overline{OR}$[1:2] functions are selected in FWFT mode. $\overline{PAE}$[1:2] and $\overline{PAF}$[1:2] are always available for use, irrespective of timing mode. Each flag has a double because the 18M FIFO was designed as a Multi-chip Module, so each set of flags supports its respective internal 9M FIFO. Some extra external gating logic will have to be used to accurately read each flag output. This will be covered in the flagging section of the datasheet.

$\overline{PAE}$[1:2] and $\overline{PAF}$[1:2] can be programmed independently to switch at any point in memory. Programmable offsets determine the flag switching threshold and can be loaded by two methods: parallel or serial. Eight default offset settings are also provided, so that $\overline{PAE}$[1:2] can be set to switch at a predefined number of locations from the empty boundary and the $\overline{PAF}$[1:2] threshold can also be set at similar predefined values from the full boundary. The default offset values are set during Master Reset by the state of the FSEL0, FSEL1, and $\overline{LD}$ pins.

For serial programming, $\overline{SEN}$ together with $\overline{LD}$ on each rising edge of SCLK, are used to load the offset registers via the Serial Input (SI). For parallel programming, $\overline{WEN}$ together with $\overline{LD}$ on each rising edge of WCLK, are used to load the offset registers via D_n. $\overline{REN}$ together with $\overline{LD}$ on each rising edge of RCLK can be used to read the offsets in parallel from Q_n regardless of whether serial or parallel offset loading has been selected.

During Master Reset ($\overline{MRS}$) the following events occur: the read and write pointers are set to the first location of the FIFO. The FWFT pin selects IDT Standard mode or FWFT mode.

The Partial Reset ($\overline{PRS}$) also sets the read and write pointers to the first location of the memory. However, the timing mode, programmable flag programming method, and default or programmed offset settings existing before Partial Reset remain unchanged. The flags are updated according to the timing mode and offsets in effect. $\overline{PRS}$ is useful for resetting a device in mid-operation, when reprogramming programmable flags would be undesirable.

It is also possible to select the timing mode of the $\overline{PAE}$[1:2] (Programmable Almost-Empty flag) and $\overline{PAF}$[1:2] (Programmable Almost-Full flag) outputs. The timing modes can be set to be either asynchronous or synchronous for the $\overline{PAE}$[1:2] and $\overline{PAF}$[1:2] flags.

If asynchronous $\overline{PAE}$/$\overline{PAF}$[1:2] configuration is selected, the $\overline{PAE}$[1:2] is asserted LOW on the LOW-to-HIGH transition of RCLK. $\overline{PAE}$[1:2] is reset to HIGH on the LOW-to-HIGH transition of WCLK. Similarly, the $\overline{PAF}$[1:2] is asserted LOW on the LOW-to-HIGH transition of WCLK and $\overline{PAF}$[1:2] is reset to HIGH on the LOW-to-HIGH transition of RCLK.

If synchronous $\overline{PAE}$/$\overline{PAF}$[1:2] configuration is selected , the $\overline{PAE}$[1:2] is asserted and updated on the rising edge of RCLK only and not WCLK. Similarly, $\overline{PAF}$[1:2] is asserted and updated on the rising edge of WCLK only and not RCLK. The mode desired is configured during MasterReset by the state of the Programmable Flag Mode (PFM) pin.

This device includes a Retransmit from Mark feature that utilizes two control inputs, MARK and , $\overline{RT}$ (Retransmit). If the MARK input is enabled with respect to the RCLK, the memory location being read at that point will be marked. Any subsequent retransmit operation, $\overline{RT}$ goes LOW, will reset the read pointer to this 'marked' location.

If, at any time, the FIFO is not actively performing an operation, the chip will automatically power down. Once in the power down state, the standby supply current consumption is minimized. Initiating any operation (by activating control

DESCRIPTION (CONTINUED)

inputs) will immediately take the device out of the power down state.

Both an Asynchronous Output Enable pin ($\overline{OE}$) and Synchronous Read Chip Select pin ($\overline{RCS}$) are provided on the FIFO. The Synchronous Read Chip Select is synchronized to the RCLK. Both the output enable and read chip select control the output buffer of the FIFO, causing the buffer to be either HIGH impedance or LOW impedance.

A JTAG test port is provided, here the FIFO has fully functional Boundary Scan feature, compliant with IEEE 1449.1 Standard Test Access Port and Boundary Scan Architecture. Special consideration should be taken into account for JTAG testing since the device is a MCM. Please see JTAG section for further details.

The TeraSync FIFO has the capability of operating its ports (write and/or read) in either LVTTL or HSTL mode, each ports selection independent of the other. The write port selection is made via WHSTL and the read port selection via RHSTL. An additional input HSTL is also provided, this allows the user to select HSTL operation for other pins on the device (not associated with the write or read ports).

The IDT72T36135M is fabricated using high speed submicron CMOS technology.

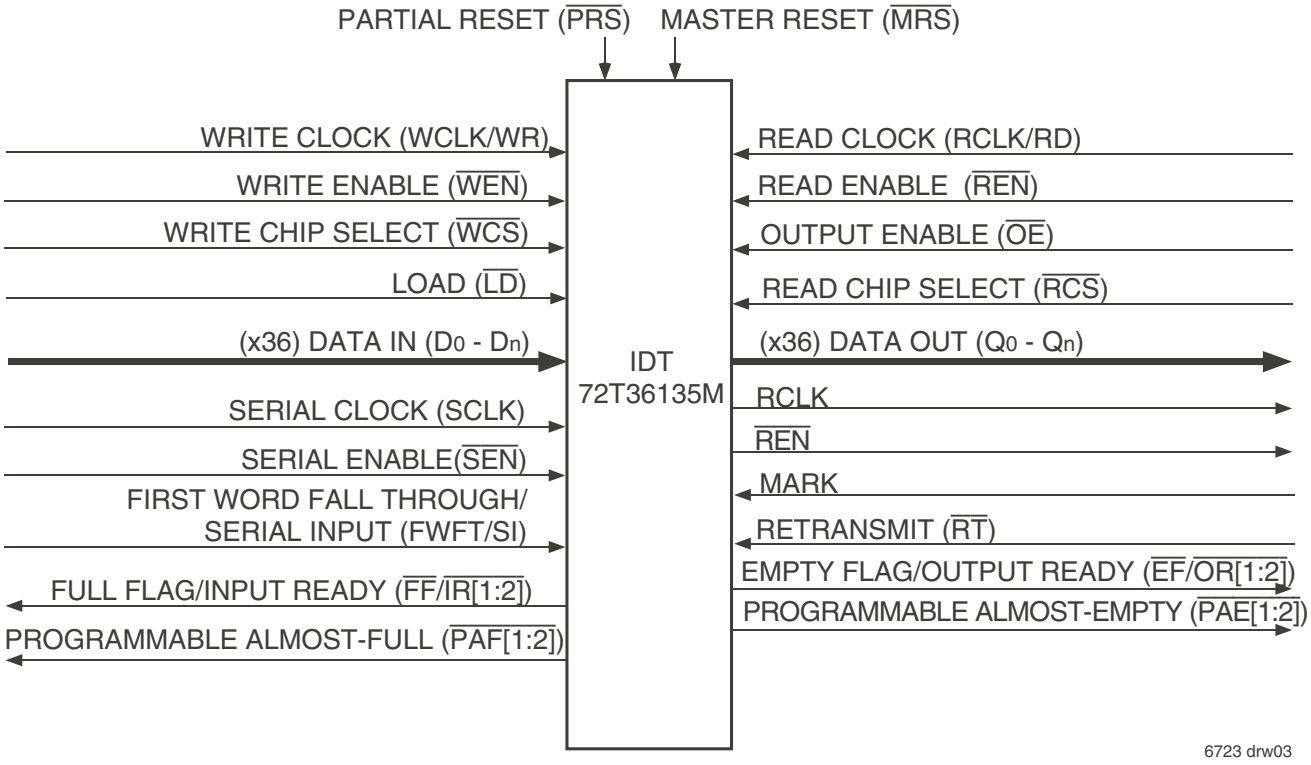


Figure 1. Single Device Configuration Signal Flow Diagram

PIN DESCRIPTION

Symbol	Name	I/O TYPE	Description
$\overline{ASYR}$[1]	Asynchronous Read Port	LVTTL INPUT	A HIGH on this input during Master Reset will select Synchronous read operation for the output port. A LOW will select Asynchronous operation. If Asynchronous is selected the FIFO must operate in IDT Standard mode.
$\overline{ASYW}$[1]	Asynchronous Write Port	LVTTL INPUT	A HIGH on this input during Master Reset will select Synchronous write operation for the input port. A LOW will select Asynchronous operation.
D0–D35	Data Inputs	HSTL-LVTTL INPUT	Data inputs for a 36-bit bus.
$\overline{EF}$/$\overline{OR}$ [1:2]	Empty Flag/ Output Ready	HSTL-LVTTL OUTPUT	In the IDT Standard mode, the $\overline{EF}$[1:2] function is selected. $\overline{EF}$[1:2] indicates whether or not the FIFO memory is empty. In FWFT mode, the $\overline{OR}$[1:2] function is selected. $\overline{OR}$[1:2] indicates whether or not there is valid data available at the outputs. **Please see Flagging section for external gating instructions of these flags.**
$\overline{FF}$/$\overline{IR}$ [1:2]	Full Flag/ Input Ready	HSTL-LVTTL OUTPUT	In the IDT Standard mode, the $\overline{FF}$[1:2] function is selected. $\overline{FF}$[1:2] indicates whether or not the FIFO memory is full. In the FWFT mode, the $\overline{IR}$[1:2] function is selected. $\overline{IR}$[1:2] indicates whether or not there is space available for writing to the FIFO memory. **Please see Flagging section for external gating instructions of these flags.**
FSEL0[1]	Flag Select Bit 0	LVTTL INPUT	During Master Reset, this input along with FSEL1 and the $\overline{LD}$ pin, will select the default offset values for the programmable flags $\overline{PAE}$[1:2] and $\overline{PAF}$[1:2]. There are up to eight possible settings available.
FSEL1[1]	Flag Select Bit 1	LVTTL INPUT	During Master Reset, this input along with FSEL0 and the $\overline{LD}$ pin will select the default offset values for the programmable flags $\overline{PAE}$[1:2] and $\overline{PAF}$[1:2]. There are up to eight possible settings available.
FWFT/ SI	First Word Fall Through/Serial In	HSTL-LVTTL INPUT	During Master Reset, selects First Word Fall Through or IDT Standard mode. After Master Reset, this pin functions as a serial input for loading offset registers. If Asynchronous operation of the read port has been selected then the FIFO must be set-up in IDT Standard mode.
$\overline{LD}$	Load	HSTL-LVTTL INPUT	This is a dual purpose pin. During Master Reset, the state of the $\overline{LD}$ input along with FSEL0 and FSEL1, determines one of eight default offset values for the $\overline{PAE}$[1:2] and $\overline{PAF}$[1:2] flags, along with the method by which these offset registers can be programmed, parallel or serial (see Table 1). After Master Reset, this pin enables writing to and reading from the offset registers.
MARK	Mark for Retransmit	HSTL-LVTTL INPUT	When this pin is asserted the current location of the read pointer will be marked. Any subsequent Retransmit operation will reset the read pointer to this position.
$\overline{MRS}$	Master Reset	HSTL-LVTTL INPUT	$\overline{MRS}$ initializes the read and write pointers to zero and sets the output register to all zeroes. During Master Reset, the FIFO is configured for either FWFT or IDT Standard mode, Synchronous/Asynchronous operation of the read or write port, one of eight programmable flag default settings, serial or parallel programming of the offset settings, zero latency timing mode, and synchronous versus asynchronous programmable flag timing modes.
$\overline{OE}$	Output Enable	HSTL-LVTTL INPUT	$\overline{OE}$ provides Asynchronous three-state control of the data outputs, Qn. During a Master or Partial Reset the $\overline{OE}$ input is the only input that provide High-Impedance control of the data outputs.
$\overline{PAE}$ [1:2]	Programmable Almost-Empty Flag	HSTL-LVTTL OUTPUT	$\overline{PAE}$[1:2] goes LOW if the number of words in the FIFO memory is less than offset n, which is stored in the Empty Offset register. $\overline{PAE}$[1:2] goes HIGH if the number of words in the FIFO memory is greater than or equal to offset n. **Please see Flagging section for external gating instructions of these flags.**
$\overline{PAF}$ [1:2]	Programmable Almost-Full Flag	HSTL-LVTTL OUTPUT	$\overline{PAF}$[1:2] goes HIGH if the number of free locations in the FIFO memory is more than offset m, which is stored in the Full Offset register. $\overline{PAF}$[1:2] goes LOW if the number of free locations in the FIFO memory is less than or equal to m. **Please see Flagging section for external gating instructions of these flags.**
PFM[1]	Programmable Flag Mode	LVTTL INPUT	During Master Reset, a LOW on PFM will select Asynchronous Programmable flag timing mode. A HIGH on PFM will select Synchronous Programmable flag timing mode.
$\overline{PRS}$	Partial Reset	HSTL-LVTTL INPUT	$\overline{PRS}$ initializes the read and write pointers to zero and sets the output register to all zeroes. During Partial Reset, the existing mode (IDT or FWFT), programming method (serial or parallel), and programmable flag settings are all retained.
Q0–Q35	Data Outputs	HSTL-LVTTL OUTPUT	Data outputs for an 36-bit bus.
RCLK/ RD	Read Clock/ Read Stobe	HSTL-LVTTL INPUT	If Synchronous operation of the read port has been selected, when enabled by $\overline{REN}$, the rising edge of RCLK reads data from the FIFO memory and offsets from the programmable registers. If $\overline{LD}$ is LOW, the values loaded into the offset registers is output on a rising edge of RCLK. If Asynchronous operation of the read

PIN DESCRIPTION (CONTINUED)

Symbol	Name	I/O TYPE	Description
RCLK/ $\overline{RD}$	Read Clock/ Read Strobe	HSTL-LVTTL INPUT	port has been selected, a rising edge on RD reads data from the FIFO in an Asynchronous manner. $\overline{REN}$ should be tied LOW.
$\overline{RCS}$	Read Chip Select	HSTL-LVTTL INPUT	$\overline{RCS}$ provides synchronous control of the read port and output impedance of Qn, synchronous to RCLK. During a Master Reset or Partial Reset the $\overline{RCS}$ input is don't care, if $\overline{OE}$ is LOW the data outputs will be Low-Impedance regardless of $\overline{RCS}$.
$\overline{REN}$	Read Enable	HSTL-LVTTL INPUT	If Synchronous operation of the read port has been selected, $\overline{REN}$ enablesRCLK for reading data from the FIFO memory and offset registers. If Asynchronous operation of the read port has been selected, the $\overline{REN}$ input should be tied LOW.
RHSTL[1]	Read Port HSTL Select	LVTTL INPUT	This pin is used to select HSTL or 2.5v LVTTL outputs for the FIFO. If HSTL inputs are required, this input must be tied HIGH. Otherwise it should be tied LOW.
$\overline{RT}$	Retransmit	HSTL-LVTTL INPUT	$\overline{RT}$ asserted on the rising edge of RCLK initializes the READ pointer to zero, sets the $\overline{EF}$[1:2] flag to LOW ($\overline{OR}$[1:2] to HIGH in FWFT mode) and doesn't disturb the write pointer, programming method, existing timing mode or programmable flag settings. If a mark has been set via the MARK input pin, then the read pointer will jump to the 'mark' location.
SCLK	Serial Clock	HSTL-LVTTL INPUT	A rising edge on SCLK will clock the serial data present on the SI input into the offset registers providing that $\overline{SEN}$ is enabled.
$\overline{SEN}$	Serial Enable	HSTL-LVTTL INPUT	$\overline{SEN}$ enables serial loading of programmable flag offsets.
SHSTL	System HSTL Select	LVTTL INPUT	All inputs not associated with the write or read port can be selected for HSTL operation via the SHSTL input.
TCK[2]	JTAG Clock	HSTL-LVTTL INPUT	Clock input for JTAG function. TMS and TDI are sampled on the rising edge of TCK. Data is output on TDO on the falling edge.
$\overline{TRST}$[2]	JTAG Reset	HSTL-LVTTL INPUT	$\overline{TRST}$ is an asynchronous reset pin for the JTAG controller.
TMS	JTAG Mode Select	HSTL-LVTTL INPUT	TMS is a serial input pin. Bits are serially loaded on the rising edge of TCK, which selects 1 of 5 modes of operation for the JTAG boundary scan.
TDI	Test Data Input	HSTL-LVTTL INPUT	During JTAG boundary scan operation test data is serially loaded via TDI on the rising edge of TCK. This is also the data for the Instruction Register, ID Register and Bypass Register.
TDO	Test Data Output	HSTL-LVTTL OUTPUT	During JTAG boundary scan operation test data is serially output via TDO on the falling edge of TCK. This output is in High-Z except when shifting, while in SHIFT-DR and SHIFT-IR controller states.
$\overline{WEN}$	Write Enable	HSTL-LVTTL INPUT	When Synchronous operation of the write port has been selected, $\overline{WEN}$ enables WCLK for writing data into theFIFO memory and offset registers. If Asynchronous operation of the write port has been selected, the $\overline{WEN}$ input should be tied LOW.
$\overline{WCS}$	Write Chip Select	HSTL-LVTTL INPUT	This pin disables the write port data inputs when the device write port is configured for HSTL mode. This provides added power savings.
WCLK/ WR	Write Clock/ Write Strobe	HSTL-LVTTL INPUT	If Synchronous operation of the write port has been selected, when enabled by $\overline{WEN}$, the rising edge of WCLK writes data into the FIFO. If Asynchronous operation of the write port has been selected, WR writes data into the FIFO on a rising edge in an Asynchronous manner, ($\overline{WEN}$ should be tied to its active state).
WHSTL[1]	Write Port HSTL Select	LVTTL INPUT	This pin is used to select HSTL or 2.5V LVTTL inputs for the FIFO. If HSTL inputs are required, this input must be tied HIGH. Otherwise it should be tied LOW.
Vcc	+2.5v Supply	Power	These are Vcc supply inputs and must be connected to the 2.5V supply rail.
GND	Ground Pin	GND	These are Ground pins and must be connected to the GND rail.
Vref	Reference Voltage	I	This is a Voltage Reference input and must be connected to a voltage level determined from the table, "Recommended DC Operating Conditions". This provides the reference voltage when using HSTL class inputs. If HSTL class inputs are not being used, this pin should be tied LOW.
VDDQ	O/P Rail Voltage	I	This pin should be tied to the desired voltage rail for providing power to the output drivers.

NOTES:
1. Inputs should not change state after Master Reset.
2. If the JTAG feature is not being used, TCK and $\overline{TRST}$ should be tied LOW.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with respect to GND	–0.5 to +3.6[2]	V
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–50 to +50	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Compliant with JEDEC JESD8-5. V_{CC} terminal only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}[2,3]	Input Capacitance	V_{IN} = 0V	15[3]	pF
C_{OUT}[1,2]	Output Capacitance	V_{OUT} = 0V	10.5	pF

NOTES:

1. With output deselected, ($\overline{OE} \geq V_{IH}$).
2. Characterized values, not currently tested.
3. C_{IN} for Vref is 40pF.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		2.375	2.5	2.625	V
GND	Supply Voltage		0	0	0	V
V_{IH}	Input High Voltage	— LVTTL	1.7	—	3.45	V
		— eHSTL	V_{REF}+0.2	—	V_{DDQ}+0.3	V
		— HSTL	V_{REF}+0.2	—	V_{DDQ}+0.3	V
V_{IL}	Input Low Voltage	— LVTTL	-0.3	—	0.7	V
		— eHSTL	-0.3	—	V_{REF}-0.2	V
		— HSTL	-0.3	—	V_{REF}-0.2	V
V_{REF}[1]	Voltage Reference Input	— eHSTL	0.8	0.9	1.0	V
		— HSTL	0.68	0.75	0.9	V
T_A	Operating Temperature Commercial		0	—	70	°C
T_A	Operating Temperature Industrial		-40	—	85	°C

NOTE:

1. V_{REF} is only required for HSTL or eHSTL inputs. V_{REF} should be tied LOW for LVTTL operation.
2. Outputs are not 3.3V tolerant.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 2.5V ± 0.125V, T_A = 0°C to +70°C;Industrial: V_{CC} = 2.5V ± 0.125V, T_A = -40°C to +85°C)

Symbol	Parameter			Min.	Max.	Unit
I_{LI}	Input Leakage Current			–10	10	µA
I_{LO}	Output Leakage Current			–10	10	µA
V_{OH}[5]	Output Logic "1" Voltage,	I_{OH} = –8 mA	@V_{DDQ} = 2.5V ± 0.125V (LVTTL)	V_{DDQ}-0.4	—	V
		I_{OH} = –8 mA	@V_{DDQ} = 1.8V ± 0.1V (eHSTL)	V_{DDQ}-0.4	—	V
		I_{OH} = –8 mA	@V_{DDQ} = 1.5V ± 0.1V (HSTL)	V_{DDQ}-0.4	—	V
V_{OL}	Output Logic "0" Voltage,	I_{OL} = 8 mA	@V_{DDQ} = 2.5V ± 0.125V (LVTTL)	—	0.4V	V
		I_{OL} = 8 mA	@V_{DDQ} = 1.8V ± 0.1V (eHSTL)	—	0.4V	V
		I_{OL} = 8 mA	@V_{DDQ} = 1.5V ± 0.1V (HSTL)	—	0.4V	V
I_{CC1}[1,2]	Active V_{CC} Current (V_{CC} = 2.5V)	I/O = LVTTL		—	120	mA
		I/O = HSTL		—	180	mA
		I/O = eHSTL		—	180	mA
I_{CC2}[1]	Standby V_{CC} Current (V_{CC} = 2.5V)	I/O = LVTTL		—	40	mA
		I/O = HSTL		—	140	mA
		I/O = eHSTL		—	140	mA

NOTES:

1. Both WCLK and RCLK toggling at 20MHz. Data inputs toggling at 10MHz. $\overline{WCS}$ = HIGH, $\overline{REN}$ or $\overline{RCS}$ = HIGH.
2. For the IDT72T36135M, typical I_{CC1} calculation (with data outputs in Low-Impedance):
3. For all devices, typical I_{DDQ} calculation: with data outputs in High-Impedance: I_{DDQ} (mA) = 0.15 x fs, fs = WCLK = RCLK frequency (in MHz)
   with data outputs in Low-Impedance: I_{DDQ} (mA) = (C_L x V_{DDQ} x fs x N)/2000
   fs = WCLK = RCLK frequency (in MHz), V_{DDQ} = 2.5V for LVTTL; 1.5V for HSTL; 1.8V for eHSTL, C_L = capacitive load (pf), t_A = 25°C, N = Number of outputs switching.
4. Total Power consumed: PT = (V_{CC} x I_{CC}) + V_{DDQ} x I_{DDQ}).
5. Outputs are not 3.3V tolerant.

AC ELECTRICAL CHARACTERISTICS[1] — SYNCHRONOUS TIMING

(Commercial: V_{CC} = 2.5V ± 5%, T_A = 0°C to +70°C;Industrial: V_{CC} = 2.5V ± 5%, T_A = -40°C to +85°C)

Symbol	Parameter	Commercial IDT72T36135ML5		Com'l & Ind'l IDT72T36135ML6		Unit
		Min.	Max.	Min.	Max.	
f_C	Clock Cycle Frequency (Synchronous)	—	200	—	166	MHz
t_A	Data Access Time	0.6	3.6	0.6	3.8	ns
t_{CLK}	Clock Cycle Time	5	—	6	—	ns
t_{CLKH}	Clock High Time	2.5	—	3.0	—	ns
t_{CLKL}	Clock Low Time	2.5	—	3.0	—	ns
t_{DS}	Data Setup Time	1.5	—	2.0	—	ns
t_{DH}	Data Hold Time	0.5	—	0.5	—	ns
t_{ENS}	Enable Setup Time	1.5	—	2.0	—	ns
t_{ENH}	Enable Hold Time	0.5	—	0.5	—	ns
t_{LDS}	Load Setup Time	1.5	—	2.0	—	ns
t_{LDH}	Load Hold Time	0.5	—	0.5	—	ns
t_{WCSS}	$\overline{WCS}$ setup time	1.5	—	2.0	—	ns
t_{WCSH}	$\overline{WCS}$ hold time	0.5	—	0.5	—	ns
f_S	Clock Cycle Frequency (SCLK)	—	10	—	10	MHz
t_{SCLK}	Serial Clock Cycle	100	—	100	—	ns
t_{SCKH}	Serial Clock High	45	—	45	—	ns
t_{SCKL}	Serial Clock Low	45	—	45	—	ns
t_{SDS}	Serial Data In Setup	15	—	15	—	ns
t_{SDH}	Serial Data In Hold	5	—	5	—	ns
t_{SENS}	Serial Enable Setup	5	—	5	—	ns
t_{SENH}	Serial Enable Hold	5	—	5	—	ns
t_{RS}	Reset Pulse Width[3]	10	—	10	—	ns
t_{RSS}	Reset Setup Time	15	—	15	—	ns
t_{HRSS}	HSTL Reset Setup Time	4	—	4	—	µs
t_{RSR}	Reset Recovery Time	10	—	10	—	ns
t_{RSF}	Reset to Flag and Output Time	—	15	—	15	ns
t_{WFF}	Write Clock to $\overline{FF}$[1:2] or $\overline{IR}$[1:2]	—	3.6	—	3.7	ns
t_{REF}	Read Clock to $\overline{EF}$[1:2] or $\overline{OR}$[1:2]	—	3.6	—	3.7	ns
t_{PAFS}	Write Clock to Synchronous $\overline{PAF}$[1:2]	—	3.6	—	3.7	ns
t_{PAES}	Read Clock to Synchronous $\overline{PAE}$[1:2]	—	3.6	—	3.7	ns
t_{RCSLZ}	RCLK to Active from High-Z[3]	—	3.6	—	3.7	ns
t_{RCSHZ}	RCLK to High-Z[3]	—	3.6	—	3.7	ns
t_{SKEW1}	Skew time between RCLK and WCLK for $\overline{EF}$[1:2] and $\overline{FF}$[1:2]	—	4	—	5	ns
t_{SKEW2}	Skew time between RCLK and WCLK for $\overline{PAE}$[1:2] and $\overline{PAF}$[1:2]	—	5	—	6	ns

NOTES:
1. All AC timings apply to both Standard IDT mode and First Word Fall Through mode.
2. Pulse widths less than minimum values are not allowed.
3. Values guaranteed by design, not currently tested.
4. Industrial temperature range product for 6ns speed grade is available as a standard device. All other speed grades are available by special order.

AC ELECTRICAL CHARACTERISTICS — ASYNCHRONOUS TIMING

(Commercial: V_{CC} = 2.5V ± 5%, T_A = 0°C to +70°C;Industrial: V_{CC} = 2.5V ± 5%, T_A = -40°C to +85°C)

Symbol	Parameter	Commercial IDT72T36135ML5		Com'l & Ind'l IDT72T36135ML6		Unit
		Min.	Max.	Min.	Max.	
f_A	Cycle Frequency (Asynchronous)	—	83	—	66	MHz
t_{AA}	Data Access Time	0.6	10	0.6	12	ns
t_{CYC}	Cycle Time	12	—	15	—	ns
t_{CYH}	Cycle HIGH Time	5	—	7	—	ns
t_{CYL}	Cycle LOW Time	5	—	7	—	ns
t_{RPE}	Read Pulse after $\overline{EF}$[1:2] HIGH	10	—	12	—	ns
t_{FFA}	Clock to Asynchronous $\overline{FF}$[1:2]	—	10	—	12	ns
t_{EFA}	Clock to Asynchronous $\overline{EF}$[1:2]	—	10	—	12	ns
t_{PAFA}	Clock to Asynchronous Programmable Almost-Full Flag	—	10	—	12	ns
t_{PAEA}	Clock to Asynchronous Programmable Almost-Empty Flag	—	10	—	12	ns
t_{OLZ}	Output Enable to Output in Low Z[3]	0	—	0	—	ns
t_{OE}	Output Enable to Output Valid	—	3.6	—	3.8	ns
t_{OHZ}	Output Enable to Output in High Z[3]	—	3.6	—	3.8	ns
t_{HF}	Clock to $\overline{HF}$	—	10	—	12	ns

NOTES:
1. All AC timings apply to both Standard IDT mode and First Word Fall Through mode.
2. Industrial temperature range product for 6ns speed grade is available as a standard device. All other speed grades are available by special order.
3. Values guaranteed by design, not currently tested.

HSTL
1.5V AC TEST CONDITIONS

Input Pulse Levels	0.25 to 1.25V
Input Rise/Fall Times	0.4ns
Input Timing Reference Levels	0.75
Output Reference Levels	VDDQ/2

NOTE:
1. VDDQ = 1.5V±.

AC TEST LOADS

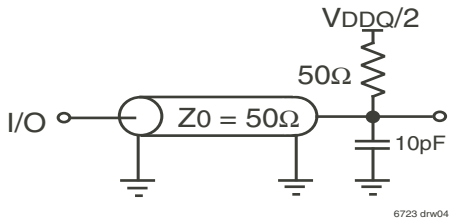


Figure 2a. AC Test Load

EXTENDED HSTL
1.8V AC TEST CONDITIONS

Input Pulse Levels	0.4 to 1.4V
Input Rise/Fall Times	0.4ns
Input Timing Reference Levels	0.9
Output Reference Levels	VDDQ/2

NOTE:
1. VDDQ = 1.8V±.

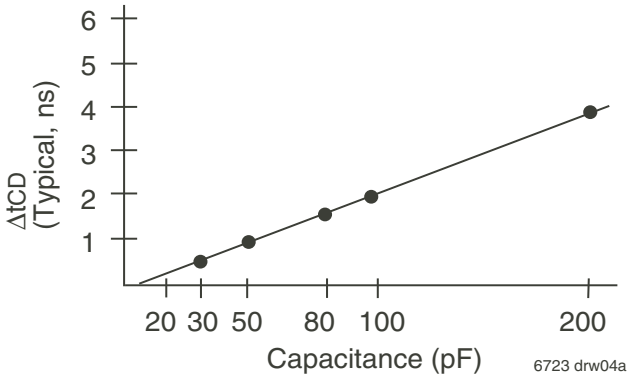


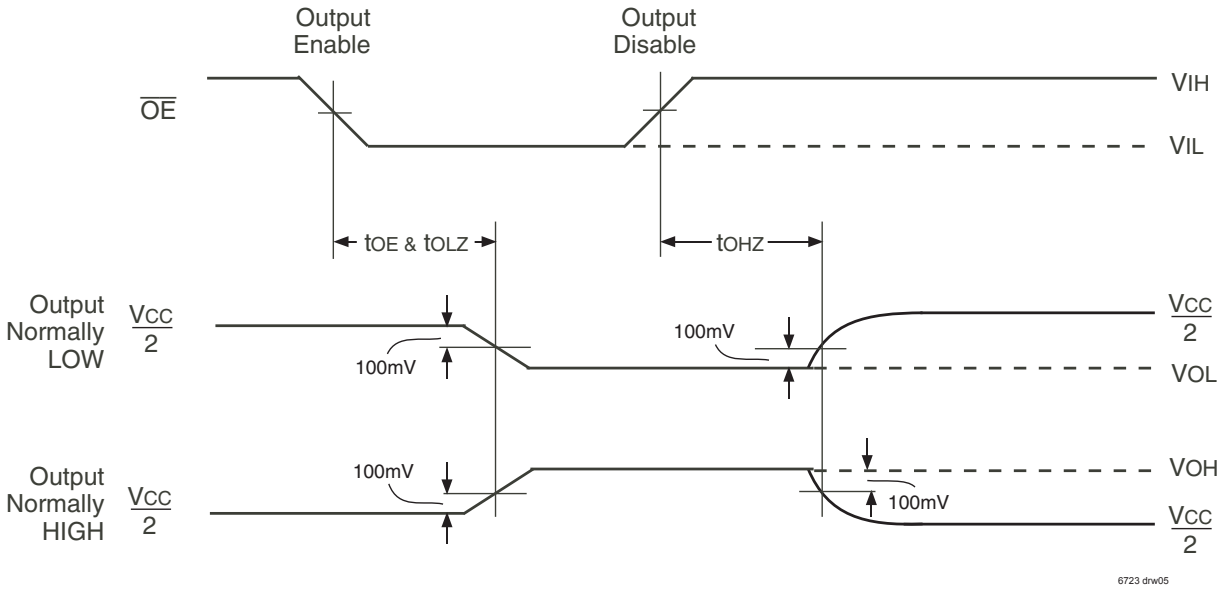
Figure 2b. Lumped Capacitive Load, Typical Derating

2.5V LVTTL
2.5V AC TEST CONDITIONS

Input Pulse Levels	GND to 2.5V
Input Rise/Fall Times	1ns
Input Timing Reference Levels	VCC/2
Output Reference Levels	VDDQ/2

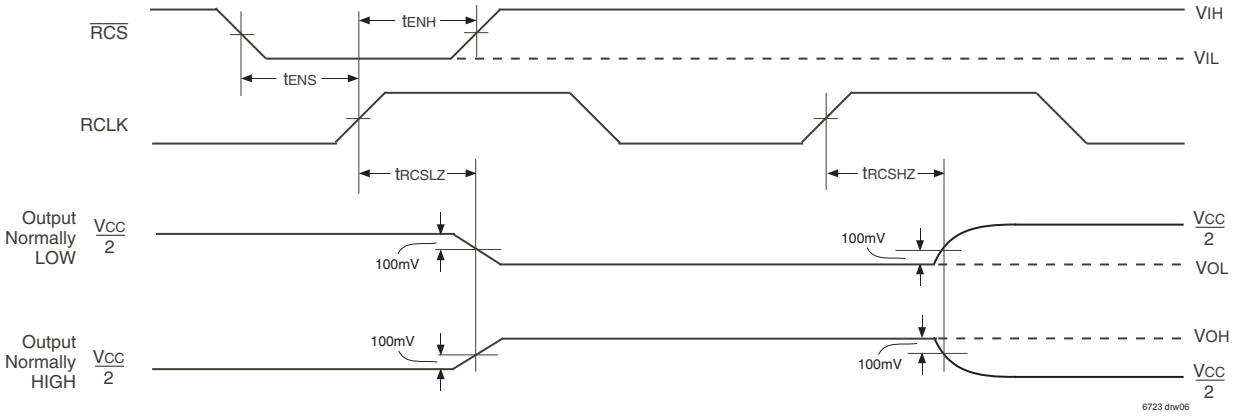
NOTE:
1. For LVTTL VCC = VDDQ.

OUTPUT ENABLE & DISABLE TIMING



NOTES:
1. $\overline{REN}$ is HIGH.
2. $\overline{RCS}$ is LOW.

READ CHIP SELECT ENABLE & DISABLE TIMING



NOTES:
1. $\overline{REN}$ is HIGH.
2. $\overline{OE}$ is LOW.

FUNCTIONAL DESCRIPTION

TIMING MODES: IDT STANDARD vs FIRST WORD FALL THROUGH (FWFT) MODE

The IDT72T36135M support two different timing modes of operation: IDT Standard mode or First Word Fall Through (FWFT) mode. The selection of which mode will operate is determined during Master Reset, by the state of the FWFT/SI input.

If, at the time of Master Reset, FWFT/SI is LOW, then IDT Standard mode will be selected. This mode uses the Empty Flag ($\overline{EF}$[1:2]) to indicate whether or not there are any words present in the FIFO. It also uses the Full Flag function ($\overline{FF}$[1:2]) to indicate whether or not the FIFO has any free space for writing. In IDT Standard mode, every word read from the FIFO, including the first, must be requested using the Read Enable ($\overline{REN}$) and RCLK.

If, at the time of Master Reset, FWFT/SI is HIGH, then FWFT mode will be selected. This mode uses Output Ready ($\overline{OR}$[1:2]) to indicate whether or not there is valid data at the data outputs (Q_n). It also uses Input Ready ($\overline{IR}$[1:2]) to indicate whether or not the FIFO has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to Q_n after three RCLK rising edges, $\overline{REN}$ = LOW is not necessary. Subsequent words must be accessed using the Read Enable ($\overline{REN}$) and RCLK.

Various signals, both input and output signals operate differently depending on which timing mode is in effect.

IDT STANDARD MODE

In this mode, the status flags, $\overline{FF}$[1:2], $\overline{PAF}$[1:2], $\overline{PAE}$[1:2], and $\overline{EF}$[1:2] operate in the manner outlined in Table 2. To write data into to the FIFO, Write Enable ($\overline{WEN}$) must be LOW. Data presented to the DATA IN lines will be clocked into the FIFO on subsequent transitions of the Write Clock (WCLK). After the first write is performed, the Empty Flag ($\overline{EF}$[1:2]) will go HIGH. Subsequent writes will continue to fill up the FIFO. The Programmable Almost-Empty flag ($\overline{PAE}$[1:2]) will go HIGH after n + 1 words have been loaded into the FIFO, where n is the empty offset value. The default setting for these values are stated in the footnote of Table 1. This parameter is also user programmable. See section on Programmable Flag Offset Loading.

Continuing to write data into the FIFO will cause the Programmable Almost-Full flag ($\overline{PAF}$[1:2]) to go LOW. Again, if no reads are performed, the $\overline{PAF}$[1:2] will go LOW. The offset "m" is the full offset value. The default setting for these values are stated in the footnote of Table 1. This parameter is also user programmable. See section on Programmable Flag Offset Loading.

When the FIFO is full, the Full Flag ($\overline{FF}$[1:2]) will go LOW, inhibiting further write operations. If no reads are performed after a reset, $\overline{FF}$[1:2] will go LOW after D writes to the FIFO.

If the FIFO is full, the first read operation will cause $\overline{FF}$[1:2] to go HIGH. Subsequent read operations will cause $\overline{PAF}$[1:2] to go HIGH at the conditions described in Table 2. If further read operations occur, without write operations, $\overline{PAE}$[1:2] will go LOW when there are n words in the FIFO, where n is the empty offset value. Continuing read operations will cause the FIFO to become empty. When the last word has been read from the FIFO, the $\overline{EF}$[1:2] will go LOW inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty.

When configured in IDT Standard mode, the $\overline{EF}$[1:2] and $\overline{FF}$[1:2] outputs are double register-buffered outputs.

Relevant timing diagrams for IDT Standard mode can be found in Figure 10, 11, 12 and 17.

FIRST WORD FALL THROUGH MODE (FWFT)

In this mode, the status flags, $\overline{IR}$[1:2], $\overline{PAF}$[1:2], $\overline{PAE}$[1:2], and $\overline{OR}$[1:2] operate in the manner outlined in Table 3. To write data into to the FIFO, $\overline{WEN}$ must be LOW. Data presented to the DATA IN lines will be clocked into the FIFO on subsequent transitions of WCLK. After the first write is performed, the Output Ready ($\overline{OR}$[1:2]) flag will go LOW. Subsequent writes will continue to fill up the FIFO. $\overline{PAE}$[1:2] will go HIGH after n + 2 words have been loaded into the FIFO, where n is the empty offset value. The default setting for these values are stated in the footnote of Table 1. This parameter is also user programmable. See section on Programmable Flag Offset Loading.

When the FIFO is full, the Input Ready ($\overline{IR}$[1:2]) flag will go HIGH, inhibiting further write operations. If no reads are performed after a reset, $\overline{IR}$[1:2] will go HIGH after D writes to the FIFO. Note that the additional word in FWFT mode is due to the capacity of the memory plus output register.

If the FIFO is full, the first read operation will cause the $\overline{IR}$[1:2] flag to go LOW. Subsequent read operations will cause the $\overline{PAF}$[1:2] to go HIGH at the conditions described in Table 3. If further read operations occur, without write operations, the $\overline{PAE}$[1:2] will go LOW when there are n + 1 words in the FIFO, where n is the empty offset value. Continuing read operations will cause the FIFO to become empty. When the last word has been read from the FIFO, $\overline{OR}$[1:2] will go HIGH inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty.

When configured in FWFT mode, the $\overline{OR}$[1:2] flag output is triple register-buffered, and the $\overline{IR}$[1:2] flag output is double register-buffered.

Relevant timing diagrams for FWFT mode can be found in Figure 13, 14, 15 and 18.

PROGRAMMING FLAG OFFSETS

Full and Empty Flag offset values are user programmable. The IDT72T36135M have internal registers for these offsets. There are eight default offset values selectable during Master Reset. These offset values are shown in Table 1. Offset values can also be programmed into the FIFO in one of two ways; serial or parallel loading method. The selection of the loading method is done using the $\overline{LD}$ (Load) pin. During Master Reset, the state of the $\overline{LD}$ input determines whether serial or parallel flag offset programming is enabled. A HIGH on $\overline{LD}$ during Master Reset selects serial loading of offset values. A LOW on $\overline{LD}$ during Master Reset selects parallel loading of offset values.

In addition to loading offset values into the FIFO, it is also possible to read the current offset values. Offset values can be read via the parallel output port Q_0-Qn, regardless of the programming mode selected (serial or parallel). It is not possible to read the offset values in serial fashion.

Figure 3, *Programmable Flag Offset Programming Sequence*, summaries the control pins and sequence for both serial and parallel programming modes. For a more detailed description, see discussion that follows.

The offset registers may be programmed (and reprogrammed) any time after Master Reset, regardless of whether serial or parallel programming has been selected. Valid programming ranges are from 0 to D-1.

SYNCHRONOUS vs ASYNCHRONOUS PROGRAMMABLE FLAG TIMING SELECTION

The IDT72T36135M can be configured during the Master Reset cycle with either synchronous or asynchronous timing for $\overline{PAF}[1:2]$ and $\overline{PAE}[1:2]$ flags by use of the PFM pin.

If synchronous $\overline{PAF}/\overline{PAE}[1:2]$ configuration is selected (PFM, HIGH during $\overline{MRS}$), the PAF is asserted and updated on the rising edge of WCLK only and not RCLK. Similarly, $\overline{PAE}[1:2]$ is asserted and updated on the rising edge of RCLK only and not WCLK. For detail timing diagrams, see Figure 22 for synchronous $\overline{PAF}[1:2]$ timing and Figure 23 for synchronous $\overline{PAE}[1:2]$ timing.

If asynchronous $\overline{PAF}/\overline{PAE}[1:2]$ configuration is selected (PFM, LOW during $\overline{MRS}$), the PAF is asserted LOW on the LOW-to-HIGH transition of WCLK and $\overline{PAF}[1:2]$ is reset to HIGH on the LOW-to-HIGH transition of RCLK. Similarly, $\overline{PAE}[1:2]$ is asserted LOW on the LOW-to-HIGH transition of RCLK. $\overline{PAE}[1:2]$ is reset to HIGH on the LOW-to-HIGH transition of WCLK. For detail timing diagrams, see Figure 24 for asynchronous $\overline{PAF}[1:2]$ timing and Figure 25 for asynchronous $\overline{PAE}[1:2]$ timing.

TABLE 1 — DEFAULT PROGRAMMABLE FLAG OFFSETS

IDT72T36135M			
*$\overline{LD}$	FSEL1	FSEL0	Offsets n,m
H	L	L	1,023
L	H	L	511
L	L	H	255
L	L	L	127
L	H	H	63
H	H	L	31
H	L	H	15
H	H	H	7
*$\overline{LD}$	FSEL1	FSEL0	Program Mode
H	X	X	Serial(3)
L	X	X	Parallel(4)

*THIS PIN MUST BE HIGH AFTER MASTER RESET TO WRITE OR READ DATA TO/FROM THE FIFO MEMORY.

NOTES:
1. n = empty offset for $\overline{PAE}[1:2]$.
2. m = full offset for $\overline{PAF}[1:2]$.
3. As well as selecting serial programming mode, one of the default values will also be loaded depending on the state of FSEL0 & FSEL1.
4. As well as selecting parallel programming mode, one of the default values will also be loaded depending on the state of FSEL0 & FSEL1.

TABLE 2 — STATUS FLAGS FOR IDT STANDARD MODE

	IDT72T36135M	$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
Number of Words in FIFO	0	H	H	L	L
	1 to n (1)	H	H	L	H
	n + 1 to (524,288-(m+1))	H	H	H	H
	(524,288-m) to 524,287	H	L	H	H
	524,288	L	L	H	H

NOTE:
1. See Table 1 for values for n, m.

TABLE 3 — STATUS FLAGS FOR FWFT MODE

	IDT72T36135M	$\overline{IR}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{OR}$
Number of Words in FIFO	0	L	H	L	H
	1 to n+1	L	H	L	L
	n + 1 to (524,289-(m+1))	L	H	H	L
	(524,289-m) to 524,288	L	L	H	L
	524,289	H	L	H	L

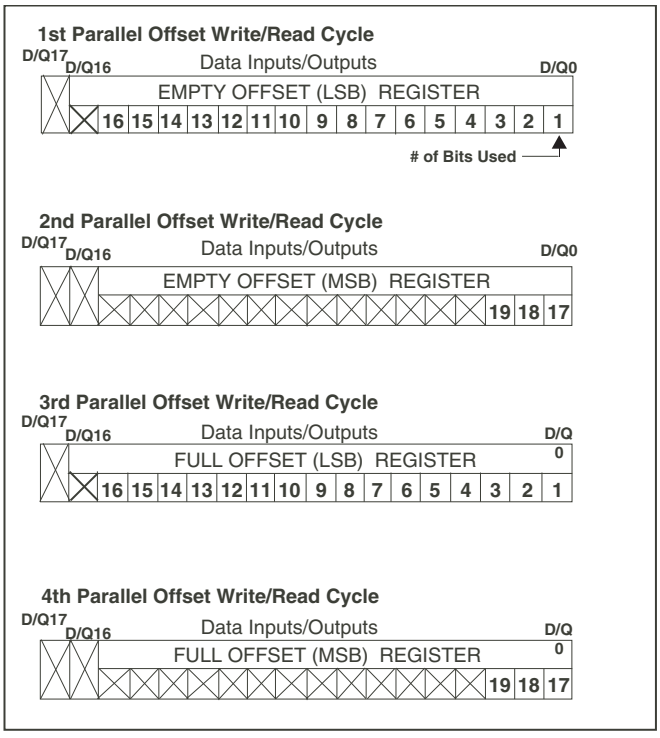
6723 drw07

NOTE:
1. See Table 1 for values for n, m.

$\overline{LD}$	$\overline{WEN}$	$\overline{REN}$	$\overline{SEN}$	WCLK	RCLK	SCLK	IDT72T36135M
0	0	1	1	↑	X	X	Parallel write to registers: Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1	0	1	X	↑	X	Parallel read from registers: Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1	1	0	X	X	↑	Serial shift into registers: 38 bits for the IDT72T36135M 1 bit for each rising SCLK edge Starting with Empty Offset (LSB) Ending with Full Offset (MSB)
X	1	1	1	X	X	X	No Operation
1	0	X	X	↑	X	X	Write Memory
1	X	0	X	X	↑	X	Read Memory
1	1	1	X	X	X	X	No Operation

6723 drw08

NOTES:
1. The programming method can only be selected at Master Reset.
2. Parallel reading of the offset registers is always permitted regardless of which programming method has been selected.
3. The programming sequence applies to both IDT Standard and FWFT modes.



6723 drw09

NOTE:
1. Consecutive reads of the offset registers is not permitted. The read operation must be disabled for a minimum of one RCLK cycle in between offset register accesses. (Please refer to Figure 21, *Parallel Read of Programmable Flag Registers (IDT Standard and FWFT Modes)* for more details).

Figure 3. Programmable Flag Offset Programming Sequence

SERIAL PROGRAMMING MODE

If Serial Programming mode has been selected, as described above, then programming of $\overline{PAE}[1:2]$ and $\overline{PAF}[1:2]$ values can be achieved by using a combination of the $\overline{LD}$, $\overline{SEN}$, SCLK and SI input pins. Programming $\overline{PAE}[1:2]$ and $\overline{PAF}[1:2]$ proceeds as follows: when $\overline{LD}$ and $\overline{SEN}$ are set LOW, data on the SI input are written, one bit for each SCLK rising edge, starting with the Empty Offset LSB and ending with the Full Offset MSB. 38 bits total required. See Figure 19, *Serial Loading of Programmable Flag Registers*, for the timing diagram for this mode.

Using the serial method, individual registers cannot be programmed selectively. $\overline{PAE}[1:2]$ and $\overline{PAF}[1:2]$ can show a valid status only after the complete set of bits (for all offset registers) has been entered. The registers can be reprogrammed as long as the complete set of new offset bits is entered. When $\overline{LD}$ is LOW and $\overline{SEN}$ is HIGH, no serial write to the registers can occur.

Write operations to the FIFO are allowed before and during the serial programming sequence. In this case, the programming of all offset bits does not have to occur at once. A select number of bits can be written to the SI input and then, by bringing $\overline{LD}$ and $\overline{SEN}$ HIGH, data can be written to FIFO memory via D_n by toggling $\overline{WEN}$. When $\overline{WEN}$ is brought HIGH with $\overline{LD}$ and $\overline{SEN}$ restored to a LOW, the next offset bit in sequence is written to the registers via SI. If an interruption of serial programming is desired, it is sufficient either to set $\overline{LD}$ LOW and deactivate $\overline{SEN}$ or to set $\overline{SEN}$ LOW and deactivate $\overline{LD}$. Once $\overline{LD}$ and $\overline{SEN}$ are both restored to a LOW level, serial offset programming continues.

From the time serial programming has begun, neither programmable flag will be valid until the full set of bits required to fill all the offset registers has been written. Measuring from the rising SCLK edge that achieves the above criteria; $\overline{PAF}[1:2]$ will be valid after three more rising WCLK edges plus t_{PAF}, $\overline{PAE}[1:2]$ will be valid after the next three rising RCLK edges plus t_{PAE}.

It is only possible to read the flag offset values via the parallel output port Qn.

PARALLEL MODE

If Parallel Programming mode has been selected, as described above, then programming of $\overline{PAE}[1:2]$ and $\overline{PAF}[1:2]$ values can be achieved by using a combination of the $\overline{LD}$, WCLK, $\overline{WEN}$ and D_n input pins. Programming $\overline{PAE}[1:2]$ and $\overline{PAF}[1:2]$ proceeds as follows: $\overline{LD}$ and $\overline{WEN}$ must be set LOW. When programming the Offset Registers of the TeraSync FIFO's the number of programming cycles will be based on the bus width, the following rules apply:

4 enabled write cycles are required to program the offset registers, (2 per offset). Data on the inputs Dn are written into the Empty Offset Register on the first two LOW-to-HIGH transition of WCLK. Upon the third and fourth LOW-to-HIGH transition of WCLK, data are written into the Full Offset Register. See Figure 3, *Programmable Flag Offset Programming Sequence* for more details.

RETRANSMIT FROM MARK OPERATION

The Retransmit from Mark feature allows FIFO data to be read repeatedly starting at a user-selected position. The FIFO is first put into retransmit mode that will 'mark' a beginning word and also set a pointer that will prevent ongoing FIFO write operations from over-writing retransmit data. The retransmit data can be read repeatedly any number of times from the 'marked' position. The FIFO can be taken out of retransmit mode at any time to allow normal device operation. The 'mark' position can be selected any number of times, each selection over-writing the previous mark location. Retransmit operation is available in both IDT standard and FWFT modes.

During IDT standard mode the FIFO is put into retransmit mode by a Low-to-High transition on RCLK when the 'MARK' input is HIGH and $\overline{EF}[1:2]$ is HIGH. The rising RCLK edge 'marks' the data present in the FIFO output register as the first retransmit data. The FIFO remains in retransmit mode until a rising edge on RCLK occurs while MARK is LOW.

Once a 'marked' location has been set (and the device is still in retransmit mode, MARK is HIGH), a retransmit can be initiated by a rising edge on RCLK while the retransmit input ($\overline{RT}$) is LOW. $\overline{REN}$ must be HIGH (reads disabled) before bringing $\overline{RT}$ LOW. The device indicates the start of retransmit setup by setting $\overline{EF}[1:2]$ LOW, also preventing reads. When $\overline{EF}[1:2]$ goes HIGH, retransmit setup is complete and read operations may begin starting with the first data at the MARK location. Since IDT standard mode is selected, every word read including the first 'marked' word following a retransmit setup requires a LOW on $\overline{REN}$ (read enabled).

Note, write operations may continue as normal during all retransmit functions, however write operations to the 'marked' location will be prevented. See Figure 17, *Retransmit from Mark (IDT standard mode)*, for the relevant timing diagram.

During FWFT mode the FIFO is put into retransmit mode by a rising RCLK edge when the 'MARK' input is HIGH and $\overline{OR}[1:2]$ is LOW. The rising RCLK edge 'marks' the data present in the FIFO output register as the first retransmit data. The FIFO remains in retransmit mode until a rising RCLK edge occurs while MARK is LOW.

Once a marked location has been set (and the device is still in retransmit mode, MARK is HIGH), a retransmit can be initiated by a rising RCLK edge while the retransmit input ($\overline{RT}$) is LOW. $\overline{REN}$ must be HIGH (reads disabled) before bringing $\overline{RT}$ LOW. The device indicates the start of retransmit setup by setting $\overline{OR}[1:2]$ HIGH.

When $\overline{OR}[1:2]$ goes LOW, retransmit setup is complete and on the next rising RCLK edge after retransmit setup is complete, ($\overline{RT}$ goes HIGH), the contents of the first retransmit location are loaded onto the output register. Since FWFT mode is selected, the first word appears on the outputs regardless of $\overline{REN}$, a LOW on $\overline{REN}$ is not required for the first word. Reading all subsequent words requires a LOW on $\overline{REN}$ to enable the rising RCLK edge. See Figure 18, *Retransmit from Mark timing (FWFT mode)*, for the relevant timing diagram.

Note, there must be a minimum of 128 words of data between the write pointer and read pointer when the MARK is asserted. Also, once the MARK is set, the write pointer will not increment past the "marked" location until the MARK is deasserted. This prevents "overwriting" of retransmit data.

HSTL/LVTTL I/O

Both the write port and read port are user selectable between HSTL or LVTTL I/O, via two select pins, WHSTL and RHSTL respectively. All other control pins are selectable via SHSTL, see Table 4 for details of groupings.

Note, that when the write port is selected for HSTL mode, the user can reduce the power consumption (in stand-by mode by utilizing the $\overline{WCS}$ input).

All "Static Pins" must be tied to V_{CC} or GND. These pins are LVTTL only, and are purely device configuration pins.

TABLE 4 — I/O CONFIGURATION

WHSTL SELECT	RHSTL SELECT		SHSTL SELECT		STATIC PINS	
WHSTL: HIGH = HSTL LOW = LVTTL	RHSTL: HIGH = HSTL LOW = LVTTL		SHSTL: HIGH = HSTL LOW = LVTTL		LVTTL ONLY	
Dn (I/P) WCLK/WR (I/P) $\overline{WEN}$ (I/P) $\overline{WCS}$ (I/P)	RCLK/RD (I/P) $\overline{RCS}$ (I/P) MARK (I/P) $\overline{REN}$ (I/P) $\overline{OE}$ (I/P) $\overline{RT}$ (I/P) Qn (O/P)	$\overline{EF}/\overline{OR}[1:2]$ (O/P) $\overline{PAF}[1:2]$ (O/P) $\overline{PAE}[1:2]$ (O/P) $\overline{FF}/\overline{IR}[1:2]$ (O/P) TDO (O/P)	SCLK (I/P) $\overline{LD}$ (I/P) $\overline{MRS}$ (I/P) TCK (I/P) TMS (I/P) $\overline{SEN}$ (I/P) FWFT/SI (I/P)	$\overline{PRS}$ (I/P) $\overline{TRST}$ (I/P) TDI (I/P)	$\overline{ASYR}$ (I/P) FSEL1 (I/P) SHSTL (I/P) RHSTL (I/P)	$\overline{ASYW}$ (I/P) FSEL0 (I/P) PFM (I/P) WHSTL (I/P)

SIGNAL DESCRIPTION
INPUTS:

DATA IN (D_0 - D_n)

Data inputs for 36-bit wide data (D_0 - D_{35}).

CONTROLS:

MASTER RESET ($\overline{MRS}$)

A Master Reset is accomplished whenever the $\overline{MRS}$ input is taken to a LOW state. This operation sets the internal read and write pointers to the first location of the RAM array. $\overline{PAE}$[1:2] will go LOW, $\overline{PAF}$[1:2] will go HIGH.

If FWFT/SI is LOW during Master Reset then the IDT Standard mode, along with $\overline{EF}$[1:2] and $\overline{FF}$[1:2] are selected. $\overline{EF}$[1:2] will go LOW and $\overline{FF}$[1:2] will go HIGH. If FWFT/SI is HIGH, then the First Word Fall Through mode (FWFT), along with $\overline{IR}$[1:2] and $\overline{OR}$[1:2], are selected. $\overline{OR}$[1:2] will go HIGH and $\overline{IR}$[1:2] will go LOW.

All control settings such as RM and PFM are defined during the Master Reset cycle.

During a Master Reset, the output register is initialized to all zeroes. A Master Reset is required after power up, before a write operation can take place. $\overline{MRS}$ is asynchronous.

See Figure 8, *Master Reset Timing*, for the relevant timing diagram.

PARTIAL RESET ($\overline{PRS}$)

A Partial Reset is accomplished whenever the $\overline{PRS}$ input is taken to a LOW state. As in the case of the Master Reset, the internal read and write pointers are set to the first location of the RAM array, $\overline{PAE}$[1:2] goes LOW, $\overline{PAF}$[1:2] goes HIGH.

Whichever mode is active at the time of Partial Reset, IDT Standard mode or First Word Fall Through, that mode will remain selected. If the IDT Standard mode is active, then $\overline{FF}$[1:2] will go HIGH and $\overline{EF}$[1:2] will go LOW. If the First Word Fall Through mode is active, then $\overline{OR}$[1:2] will go HIGH, and $\overline{IR}$[1:2] will go LOW.

Following Partial Reset, all values held in the offset registers remain unchanged. The programming method (parallel or serial) currently active at the time of Partial Reset is also retained. The output register is initialized to all zeroes. $\overline{PRS}$ is asynchronous.

A Partial Reset is useful for resetting the device during the course of operation, when reprogramming programmable flag offset settings may not be convenient.

See Figure 9, *Partial Reset Timing*, for the relevant timing diagram.

ASYNCHRONOUS WRITE ($\overline{ASYW}$)

The write port can be configured for either Synchronous or Asynchronous mode of operation. If during Master Reset the $\overline{ASYW}$ input is LOW, then Asynchronous operation of the write port will be selected. During Asynchronous operation of the write port the WCLK input becomes WR input, this is the Asynchronous write strobe input. A rising edge on WR will write data present on the Dn inputs into the FIFO. ($\overline{WEN}$ must be tied LOW when using the write port in Asynchronous mode).

When the write port is configured for Asynchronous operation the full flag ($\overline{FF}$[1:2]) operates in an asynchronous manner, that is, the full flag will be updated based in both a write operation and read operation. Note, if Asynchronous mode is selected, FWFT is not permissable. Refer to Figures 26, 27, 30 and 31 for relevant timing and operational waveforms.

ASYNCHRONOUS READ ($\overline{ASYR}$)

The read port can be configured for either Synchronous or Asynchronous mode of operation. If during a Master Reset the $\overline{ASYR}$ input is LOW, then Asynchronous operation of the read port will be selected. During Asynchronous operation of the read port the RCLK input becomes RD input, this is the Asynchronous read strobe input. A rising edge on RD will read data from the FIFO via the output register and Qn port. ($\overline{REN}$ must be tied LOW during Asynchronous operation of the read port).

The $\overline{OE}$ input provides three-state control of the Qn output bus, in an asynchronous manner. ($\overline{RCS}$, provides three-state control of the read port in Synchronous mode).

When the read port is configured for Asynchronous operation the device must be operating on IDT standard mode, FWFT mode is not permissible if the read port is Asynchronous. The Empty Flag ($\overline{EF}$[1:2]) operates in an Asynchronous manner, that is, the empty flag will be updated based on both a read operation and a write operation. Refer to figures 28, 29, 30 and 31 for relevant timing and operational waveforms.

RETRANSMIT ($\overline{RT}$)

The Retransmit ($\overline{RT}$) input is used in conjunction with the MARK input, together they provide a means by which data previously read out of the FIFO can be reread any number of times. If retransmit operation has been selected (i.e. the MARK input is HIGH), a rising edge on RCLK while $\overline{RT}$ is LOW will reset the read pointer back to the memory location set by the user via the MARK input.

If IDT standard mode has been selected the $\overline{EF}$[1:2] flag will go LOW and remain LOW for the time that $\overline{RT}$ is held LOW. $\overline{RT}$ can be held LOW for any number of RCLK cycles, the read pointer being reset to the marked location. The next rising edge of RCLK after $\overline{RT}$ has returned HIGH, will cause $\overline{EF}$[1:2] to go HIGH, allowing read operations to be performed on the FIFO. The next read operation will access data from the 'marked' memory location.

Subsequent retransmit operations may be performed, each time the read pointer returning to the 'marked' location. See Figure 17, *Retransmit from Mark (IDT Standard mode)* for the relevant timing diagram.

If FWFT mode has been selected the $\overline{OR}$[1:2] flag will go HIGH and remain HIGH for the time that $\overline{RT}$ is held LOW. $\overline{RT}$ can be held LOW for any number of RCLK cycles, the read pointer being reset to the 'marked' location. The next RCLK rising edge after $\overline{RT}$ has returned HIGH, will cause $\overline{OR}$[1:2] to go LOW and due to FWFT operation, the contents of the marked memory location will be loaded onto the output register, a read operation being required for all subsequent data reads.

Subsequent retransmit operations may be performed each time the read pointer returning to the 'marked' location. See Figure 18, *Retransmit from Mark (FWFT mode)* for the relevant timing diagram.

MARK

The MARK input is used to select Retransmit mode of operation. An RCLK rising edge while MARK is HIGH will mark the memory location of the data currently present on the output register, the device will also be placed into retransmit mode. For the IDT72T36135M a minimum of 128 words (x36). Also, once the MARK is set, the write pointer will not increment past the "marked" location until the MARK is deasserted. This prevents "overwriting" of retransmit data.

The MARK input must remain HIGH during the whole period of retransmit mode, a falling edge of RCLK while MARK is LOW will take the device out of retransmit mode and into normal mode. Any number of MARK locations can be set during FIFO operation, only the last marked location taking effect. Once a

mark location has been set the write pointer cannot be incremented past this marked location. During retransmit mode write operations to the device may continue without hindrance.

FIRST WORD FALL THROUGH/SERIAL IN (FWFT/SI)

This is a dual purpose pin. During Master Reset, the state of the FWFT/SI input determines whether the device will operate in IDT Standard mode or First Word Fall Through (FWFT) mode.

If, at the time of Master Reset, FWFT/SI is LOW, then IDT Standard mode will be selected. This mode uses the Empty Flag ($\overline{EF}$[1:2]) to indicate whether or not there are any words present in the FIFO memory. It also uses the Full Flag function ($\overline{FF}$[1:2]) to indicate whether or not the FIFO memory has any free space for writing. In IDT Standard mode, every word read from the FIFO, including the first, must be requested using the Read Enable ($\overline{REN}$) and RCLK.

If, at the time of Master Reset, FWFT/SI is HIGH, then FWFT mode will be selected. This mode uses Output Ready ($\overline{OR}$[1:2]) to indicate whether or not there is valid data at the data outputs (Q_n). It also uses Input Ready ($\overline{IR}$[1:2]) to indicate whether or not the FIFO memory has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to Q_n after three RCLK rising edges, $\overline{REN}$ = LOW is not necessary. Subsequent words must be accessed using the Read Enable ($\overline{REN}$) and RCLK.

After Master Reset, FWFT/SI acts as a serial input for loading $\overline{PAE}$[1:2] and $\overline{PAF}$[1:2] offsets into the programmable registers. The serial input function can only be used when the serial loading method has been selected during Master Reset. Serial programming using the FWFT/SI pin functions the same way in both IDT Standard and FWFT modes.

WRITE STROBE & WRITE CLOCK (WR/WCLK)

If Synchronous operation of the write port has been selected via $\overline{ASYW}$, this input behaves as WCLK.

A write cycle is initiated on the rising edge of the WCLK input. Data setup and hold times must be met with respect to the LOW-to-HIGH transition of the WCLK. It is permissible to stop the WCLK. Note that while WCLK is idle, the $\overline{FF}$/$\overline{IR}$[1:2], and $\overline{PAF}$[1:2] flags will not be updated. The Write and Read Clocks can either be independent or coincident.

If Asynchronous operation has been selected this input is WR (write strobe). Data is Asynchronously written into the FIFO via the Dn inputs whenever there is a rising edge on WR. In this mode the WEN input must be tied LOW.

WRITE ENABLE ($\overline{WEN}$)

When the $\overline{WEN}$ input is LOW, data may be loaded into the FIFO RAM array on the rising edge of every WCLK cycle if the device is not full. Data is stored in the RAM array sequentially and independently of any ongoing read operation.

When $\overline{WEN}$ is HIGH, no new data is written in the RAM array on each WCLK cycle.

To prevent data overflow in the IDT Standard mode, $\overline{FF}$[1:2] will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, $\overline{FF}$[1:2] will go HIGH allowing a write to occur. The $\overline{FF}$[1:2] is updated by two WCLK cycles + t_{SKEW} after the RCLK cycle.

To prevent data overflow in the FWFT mode, $\overline{IR}$[1:2] will go HIGH, inhibiting further write operations. Upon the completion of a valid read cycle, $\overline{IR}$[1:2] will go LOW allowing a write to occur. The $\overline{IR}$[1:2] flag is updated by two WCLK cycles + t_{SKEW} after the valid RCLK cycle.

$\overline{WEN}$ is ignored when the FIFO is full in either FWFT or IDT Standard mode.

If Asynchronous operation of the write port has been selected, then WEN must be held active, (tied LOW).

READ STROBE & READ CLOCK (RD/RCLK)

If Synchronous operation of the read port has been selected via $\overline{ASYR}$, this input behaves as RCLK. A read cycle is initiated on the rising edge of the RCLK input. Data can be read on the outputs, on the rising edge of the RCLK input. It is permissible to stop the RCLK. Note that while RCLK is idle, the $\overline{EF}$/$\overline{OR}$[1:2], and $\overline{PAE}$[1:2] flags will not be updated. The Write and Read Clocks can be independent or coincident.

If Asynchronous operation has been selected this input is RD (Read Strobe) . Data is Asynchronously read from the FIFO via the output register whenever there is a rising edge on RD. In this mode the $\overline{REN}$ and $\overline{RCS}$ inputs must be tied LOW. The $\overline{OE}$ input is used to provide Asynchronous control of the three-state Qn outputs.

WRITE CHIP SELECT ($\overline{WCS}$)

The $\overline{WCS}$ disables all Write Port inputs (data only) if it is held HIGH. To perform normal operations on the write port, the $\overline{WCS}$ must be enabled, held LOW.

READ ENABLE ($\overline{REN}$)

When Read Enable is LOW, data is loaded from the RAM array into the output register on the rising edge of every RCLK cycle if the device is not empty.

When the $\overline{REN}$ input is HIGH, the output register holds the previous data and no new data is loaded into the output register. The data outputs Q_0-Q_n maintain the previous data value.

In the IDT Standard mode, every word accessed at Q_n, including the first word written to an empty FIFO, must be requested using $\overline{REN}$ provided that $\overline{RCS}$ is LOW. When the last word has been read from the FIFO, the Empty Flag ($\overline{EF}$[1:2]) will go LOW, inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty. Once a write is performed, $\overline{EF}$[1:2] will go HIGH allowing a read to occur. The $\overline{EF}$[1:2] flag is updated by two RCLK cycles + t_{SKEW} after the valid WCLK cycle. Both $\overline{RCS}$ and $\overline{REN}$ must be active, LOW for data to be read out on the rising edge of RCLK.

In the FWFT mode, the first word written to an empty FIFO automatically goes to the outputs Q_n, on the third valid LOW-to-HIGH transition of RCLK + t_{SKEW} after the first write. $\overline{REN}$ and $\overline{RCS}$ do not need to be asserted LOW for the First Word to fall through to the output register. In order to access all other words, a read must be executed using $\overline{REN}$ and $\overline{RCS}$. The RCLK LOW-to-HIGH transition after the last word has been read from the FIFO, Output Ready ($\overline{OR}$[1:2]) will go HIGH with a true read (RCLK with $\overline{REN}$ = LOW; $\overline{RCS}$ = LOW), inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty.

If Asynchronous operation of the Read port has been selected, then $\overline{REN}$ must be held active, (tied LOW).

SERIAL ENABLE ($\overline{SEN}$)

The $\overline{SEN}$ input is an enable used only for serial programming of the offset registers. The serial programming method must be selected during Master Reset. $\overline{SEN}$ is always used in conjunction with $\overline{LD}$. When these lines are both LOW, data at the SI input can be loaded into the program register one bit for each LOW-to-HIGH transition of SCLK.

When $\overline{SEN}$ is HIGH, the programmable registers retains the previous settings and no offsets are loaded. $\overline{SEN}$ functions the same way in both IDT Standard and FWFT modes.

OUTPUT ENABLE ($\overline{OE}$)

When Output Enable is enabled (LOW), the parallel output buffers receive data from the output register. When $\overline{OE}$ is HIGH, the output data bus (Q_n) goes into a high impedance state. During Master or a Partial Reset the $\overline{OE}$ is the only input that can place the output bus Qn, into High-Impedance. During Reset the $\overline{RCS}$ input can be HIGH or LOW, it has no effect on the Qn outputs.

READ CHIP SELECT ($\overline{RCS}$)

The Read Chip Select input provides synchronous control of the Read output port. When $\overline{RCS}$ goes LOW, the next rising edge of RCLK causes the Qn outputs to go to the Low-Impedance state. When $\overline{RCS}$ goes HIGH, the next RCLK rising edge causes the Qn outputs to return to HIGH Z. During a Master or Partial Reset the $\overline{RCS}$ input has no effect on the Qn output bus, $\overline{OE}$ is the only input that provides High-Impedance control of the Qn outputs. If $\overline{OE}$ is LOW the Qn data outputs will be Low-Impedance regardless of $\overline{RCS}$ until the first rising edge of RCLK after a Reset is complete. Then if $\overline{RCS}$ is HIGH the data outputs will go to High-Impedance.

The $\overline{RCS}$ input does not effect the operation of the flags. For example, when the first word is written to an empty FIFO, the $\overline{EF}$[1:2] will still go from LOW to HIGH based on a rising edge of RCLK, regardless of the state of the $\overline{RCS}$ input.

Also, when operating the FIFO in FWFT mode the first word written to an empty FIFO will still be clocked through to the output register based on RCLK, regardless of the state of $\overline{RCS}$. For this reason the user must take care when a data word is written to an empty FIFO in FWFT mode. If $\overline{RCS}$ is disabled when an empty FIFO is written into, the first word will fall through to the output register, but will not be available on the Qn outputs which are in HIGH-Z. The user must take $\overline{RCS}$ active LOW to access this first word, place the output bus in LOW-Z. $\overline{REN}$ must remain disabled HIGH for at least one cycle after $\overline{RCS}$ has gone LOW. A rising edge of RCLK with $\overline{RCS}$ and $\overline{REN}$ active LOW, will read out the next word. Care must be taken so as not to lose the first word written to an empty FIFO when $\overline{RCS}$ is HIGH. Refer to Figure 16, ***$\overline{RCS}$ and $\overline{REN}$*** *Read Operation (FWFT Mode).* The $\overline{RCS}$ pin must also be active (LOW) in order to perform a Retransmit. See Figure 12 for *Read Cycle and Read Chip Select Timing (IDT Standard Mode).* See Figure 15 for *Read Cycle and Read Chip Select Timing (First Word Fall Through Mode).*

If Asynchronous operation of the Read port has been selected, then $\overline{RCS}$ must be held active, (tied LOW). $\overline{OE}$ provides three-state control of Qn.

WRITE PORT HSTL SELECT (WHSTL)

The control inputs, data inputs and flag outputs associated with the write port can be setup to be either HSTL or LVTTL. If WHSTL is HIGH during the Master Reset, then HSTL operation of the write port will be selected. If WHSTL is LOW at Master Reset, then LVTTL will be selected.

The inputs and outputs associated with the write port are listed in Table 4, I/O Configuration.

READ PORT HSTL SELECT (RHSTL)

The control inputs, data inputs and flag outputs associated with the read port can be setup to be either HSTL or LVTTL. If RHSTL is HIGH during the Master Reset, then HSTL operation of the read port will be selected. If RHSTL is LOW at Master Reset, then LVTTL will be selected for the read port.

The inputs and outputs associated with the read port are listed in Table 4, I/O Configuration.

SYSTEM HSTL SELECT (SHSTL)

All inputs not associated with the write and read port can be setup to be either HSTL or LVTTL. If SHSTL is HIGH during Master Reset, then HSTL operation of all the inputs not associated with the write and read port will be selected. If SHSTL is LOW at Master Reset, then LVTTL will be selected. The inputs associated with SHSTL are listed in Table 4, I/O Configuration.

LOAD ($\overline{LD}$)

This is a dual purpose pin. During Master Reset, the state of the $\overline{LD}$ input, along with FSEL0 and FSEL1, determines one of eight default offset values for the $\overline{PAE}$[1:2] and $\overline{PAF}$[1:2] flags, along with the method by which these offset registers can be programmed, parallel or serial (see Table 1). After Master Reset, $\overline{LD}$ enables write operations to and read operations from the offset registers. Only the offset loading method currently selected can be used to write to the registers. Offset registers can be read only in parallel.

After Master Reset, the $\overline{LD}$ pin is used to activate the programming process of the flag offset values $\overline{PAE}$[1:2] and $\overline{PAF}$[1:2]. Pulling $\overline{LD}$ LOW will begin a serial loading or parallel load or read of these offset values. THIS PIN MUST BE HIGH AFTER MASTER RESET TO WRITE OR READ DATA TO/FROM THE FIFO MEMORY.

PROGRAMMABLE FLAG MODE (PFM)

During Master Reset, a LOW on PFM will select Asynchronous Programmable flag timing mode. A HIGH on PFM will select Synchronous Programmable flag timing mode. If asynchronous $\overline{PAF}$/$\overline{PAE}$[1:2] configuration is selected (PFM, LOW during $\overline{MRS}$), the $\overline{PAE}$[1:2] is asserted LOW on the LOW-to-HIGH transition of RCLK. $\overline{PAE}$[1:2] is reset to HIGH on the LOW-to-HIGH transition of WCLK. Similarly, the $\overline{PAF}$[1:2] is asserted LOW on the LOW-to-HIGH transition of WCLK and $\overline{PAF}$[1:2] is reset to HIGH on the LOW-to-HIGH transition of RCLK.

If synchronous $\overline{PAE}$/$\overline{PAF}$[1:2] configuration is selected (PFM, HIGH during MRS) , the $\overline{PAE}$[1:2] is asserted and updated on the rising edge of RCLK only and not WCLK. Similarly, $\overline{PAF}$[1:2] is asserted and updated on the rising edge of WCLK only and not RCLK. The mode desired is configured during master reset by the state of the Programmable Flag Mode (PFM) pin.

OUTPUTS:

FULL FLAG ($\overline{FF}$/$\overline{IR}$[1:2])

This is a dual purpose pin. In IDT Standard mode, the Full Flag ($\overline{FF}$[1:2]) function is selected. When the FIFO is full, $\overline{FF}$[1:2] will go LOW, inhibiting further write operations. When $\overline{FF}$[1:2] is HIGH, the FIFO is not full. If no reads are performed after a reset (either $\overline{MRS}$ or $\overline{PRS}$), $\overline{FF}$[1:2] will go LOW after D writes to the FIFO (D = 524,288 for the IDT72T36135M). See Figure 10, *Write Cycle and Full Flag Timing (IDT Standard Mode)*, for the relevant timing information. Please see Flagging section for external gating instructions of these flags.

In FWFT mode, the Input Ready ($\overline{IR}$[1:2]) function is selected. $\overline{IR}$[1:2] goes LOW when memory space is available for writing in data. When there is no longer any free space left, $\overline{IR}$[1:2] goes HIGH, inhibiting further write operations. If no reads are performed after a reset (either $\overline{MRS}$ or $\overline{PRS}$), $\overline{IR}$[1:2] will go HIGH after D writes to the FIFO (D = 524,288 for the IDT72T36135M). See Figure 13, *Write Timing (FWFT Mode)*, for the relevant timing information.

The $\overline{IR}$[1:2] status not only measures the contents of the FIFO memory, but also counts the presence of a word in the output register. Thus, in FWFT mode, the total number of writes necessary to deassert $\overline{IR}$[1:2] is one greater than needed to assert $\overline{FF}$[1:2] in IDT Standard mode.

$\overline{FF}$/$\overline{IR}$[1:2] is synchronous and updated on the rising edge of WCLK. $\overline{FF}$/$\overline{IR}$[1:2] are double register-buffered outputs.

Note, when the device is in Retransmit mode, this flag is a comparison of the write pointer to the 'marked' location. This differs from normal mode where this flag is a comparison of the write pointer to the read pointer.

EMPTY FLAG ($\overline{EF}$/$\overline{OR}$[1:2])

This is a dual purpose pin. In the IDT Standard mode, the Empty Flag ($\overline{EF}$[1:2]) function is selected. When the FIFO is empty, $\overline{EF}$[1:2] will go LOW, inhibiting further read operations. When $\overline{EF}$[1:2] is HIGH, the FIFO is not empty. See Figure 11, *Read Cycle, Empty Flag and First Word Latency Timing (IDT Standard Mode)*, for the relevant timing information. Please see Flagging section for external gating instructions of these flags.

In FWFT mode, the Output Ready ($\overline{OR}$[1:2]) function is selected. $\overline{OR}$[1:2] goes LOW at the same time that the first word written to an empty FIFO appears valid on the outputs. $\overline{OR}$[1:2] stays LOW after the RCLK LOW to HIGH transition that shifts the last word from the FIFO memory to the outputs. $\overline{OR}$[1:2] goes HIGH only with a true read (RCLK with $\overline{REN}$ = LOW). The previous data stays at the outputs, indicating the last word was read. Further data reads are inhibited until $\overline{OR}$[1:2] goes LOW again. See Figure 14, *Read Timing (FWFT Mode)*, for the relevant timing information.

$\overline{EF}$/$\overline{OR}$[1:2] is synchronous and updated on the rising edge of RCLK.

In IDT Standard mode, $\overline{EF}$[1:2] is a double register-buffered output. In FWFT mode, $\overline{OR}$[1:2] is a triple register-buffered output.

PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAF[1:2]}$)

The Programmable Almost-Full flag ($\overline{PAF}$[1:2]) will go LOW when the FIFO reaches the almost-full condition. In IDT Standard mode, if no reads are performed after reset ($\overline{MRS}$), $\overline{PAF}$[1:2] will go LOW after (D - m) words are written to the FIFO. The $\overline{PAF}$[1:2] will go LOW after (524,288-m) writes for the IDT72T36135M. The offset "m" is the full offset value. The default setting for this value is stated in the footnote of Table 2, Status Flags for IDT Standard Mode. Please see Flagging section for external gating instructions of these flags.

In FWFT mode, the $\overline{PAF}$[1:2] will go LOW after (524,289-m) writes for the IDT72T36135M, where m is the full offset value. The default setting for this value is stated in Table 3, Status Flags for FWFT Mode.

See Figure 22, *Synchronous Programmable Almost-Full Flag Timing (IDT Standard and FWFT Mode)*, for the relevant timing information.

If asynchronous $\overline{PAF}$[1:2] configuration is selected, the $\overline{PAF}$[1:2] is asserted LOW on the LOW-to-HIGH transition of the Write Clock (WCLK). $\overline{PAF}$[1:2] is reset to HIGH on the LOW-to-HIGH transition of the Read Clock (RCLK). If synchronous $\overline{PAF}$[1:2] configuration is selected, the $\overline{PAF}$[1:2] is updated on the rising edge of WCLK. See Figure 24, *Asynchronous Almost-Full Flag Timing (IDT Standard and FWFT Mode)*.

Note, when the device is in Retransmit mode, this flag is a comparison of the write pointer to the 'marked' location. This differs from normal mode where this flag is a comparison of the write pointer to the read pointer.

PROGRAMMABLE ALMOST-EMPTY FLAG ($\overline{PAE[1:2]}$)

The Programmable Almost-Empty flag ($\overline{PAE}$[1:2]) will go LOW when the FIFO reaches the almost-empty condition. In IDT Standard mode, $\overline{PAE}$[1:2] will go LOW when there are n words or less in the FIFO. The offset "n" is the empty offset value. The default setting for this value is stated in the footnote of Table 1. Please see Flagging section for external gating instructions of these flags.

In FWFT mode, the $\overline{PAE}$[1:2] will go LOW when there are n+1 words or less in the FIFO. The default setting for this value is stated in Table 1.

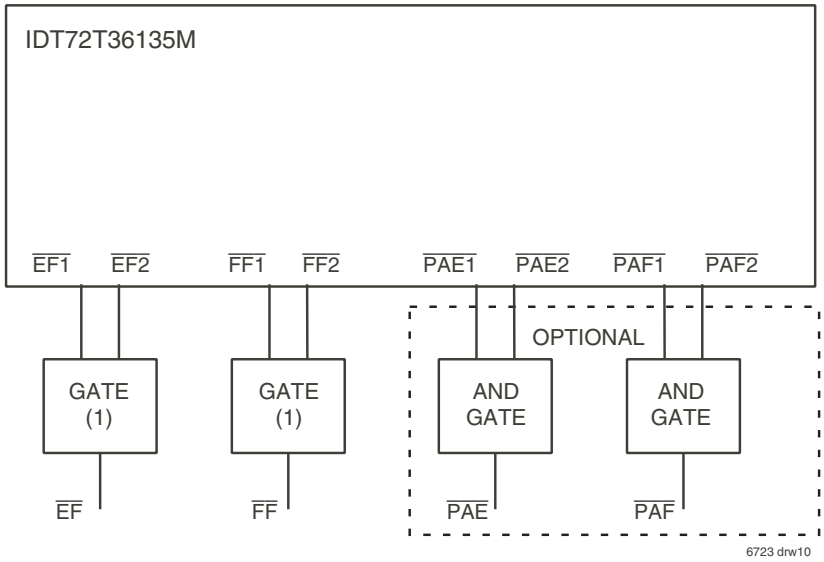
See Figure 23, *Synchronous Programmable Almost-Empty Flag Timing (IDT Standard and FWFT Mode)*, for the relevant timing information.

If asynchronous $\overline{PAE}$[1:2] configuration is selected, the $\overline{PAE}$[1:2] is asserted LOW on the LOW-to-HIGH transition of the Read Clock (RCLK). $\overline{PAE}$[1:2] is reset to HIGH on the LOW-to-HIGH transition of the Write Clock (WCLK). If synchronous $\overline{PAE}$[1:2] configuration is selected, the $\overline{PAE}$[1:2] is updated on the rising edge of RCLK. See Figure 25, *Asynchronous Programmable Almost-Empty Flag Timing (IDT Standard and FWFT Mode)*.

CONSIDERATIONS FOR READING FLAG OUTPUTS

On this device, there are two sets of flagging outputs for the empty flag ($\overline{EF1}$ & $\overline{EF2}$), full flag ($\overline{FF1}$ & $\overline{FF2}$), Programmable Almost Empty Flag ($\overline{PAE1}$ & $\overline{PAE2}$), and Programmable Almost Full Flag ($\overline{PAF1}$ & $\overline{PAF2}$) the user must work with in order to be able to correctly read the status of each flag. Since this device is a multi-chip module (MCM), both die's flags must be read accordingly to avoid skewing problems between the two internal die.

To remedy this function, the user must tie together $\overline{FF1}$ & $\overline{FF2}$, and $\overline{EF1}$ & $\overline{EF2}$ flag outputs to an external gate from a neighboring programmable device such as an FPGA or PLD and read from the output of the logical gate. An OR gate is used for FWFT mode and an AND gate is used for IDT mode. This must be done to avoid timing skew problems between the two sets of flags. For the $\overline{PAE}[1:2]$ and $\overline{PAF}[1:2]$ active low output flags, the user has the option to leave the $\overline{PAE}[1:2]$ and $\overline{PAF}[1:2]$ as is and use both pins at different programmable water marks for measuring buffer status. Please see the section on Parallel Programming Mode to understand how to program these two sets of flags as different water marks in Functional Description section of the datasheet. This gives added flexibility for queue management. Below is an example diagram for how this is accomplished.



NOTE:
1. An "OR" Gate is used for FWFT mode, and an "AND" Gate is used for IDT Standard mode.

Figure 4. Output Flag Gating Considerations

PIN COMPATIBILITY WITH 9M TERASYNC (IDT72T36125) CONSIDERATIONS

The IDT72T36135M can be a drop and replacement for the 9M TeraSync (IDT72T36125) if specific pin changes are made to the 18M FIFO. Since the 18M TeraSync is a Multi-Chip Module (MCM), containing two 9M TeraSyncs (IDT72T18125) in width expansion mode, certain functionality can not be offered in the 18M TeraSync such as bus matching, single flag outputs and interspersed parity. From these changes, the 18M FIFO has removed specific inputs such as IW, OW, BM, BE, IP, while also gaining another set of output flags as specified in **Considerations for Reading Flag Outputs** which are $\overline{EF2}$, $\overline{FF2}$, $\overline{PAE2}$, and $\overline{PAF2}$.

To maintain drop-in replacement compatibility for the 18M TeraSync, the pin changes on the pin diagram for the 18M TeraSync FIFO from the 9M TeraSync FIFO have been identified, and listed in the table below.

TABLE 5 — PIN CHANGES BETWEEN 9M TERASYNC AND 18M TERASYNC

9M TeraSync FIFO (IDT72T36125) pins changed	18M TeraSync FIFO (IDT72T36135M) new pins
BM	$\overline{EF2}$
IP	$\overline{PAE2}$
IW	NC (No Connect)
OW	NC (No Connect)
HF	$\overline{PAF2}$
EREN	$\overline{FF2}$
ERCLK	NC (No Connect)
BE	GND

NOTES:
1. Internally, the 9M pins on the left side of the table will be tied to the GND or VDD plane, respectively in the 18M device.
2. Please see IDT72T36125 TeraSync FIFO datasheet for additional features listed.

JTAG FUNCTIONALITY AND CONFIGURATION

The IDT72T36135M is composed of two independent memory arrays, and thus cannot be treated as a single JTAG device in the scan chain. The two arrays (A and B) each have identical characteristics and commands but must be treated as separate entities in JTAG operations. Please refer to Figure 5, *JTAG Configuration for IDT72T36135M*.

JTAG signaling must be provided serially to each array and utilize the information provided in the Scan Register Descriptions, JTAG Instruction Description. Specifically, commands for Array B must precede those Array A in any JTAG operations sent to the IDT72T36135M. Please reference Application Note AN-411, "JTAG Testing of Multichip Modules" for specific instructions on performing JTAG testing on the IDT72T36135M. AN-411 is available at www.idt.com.

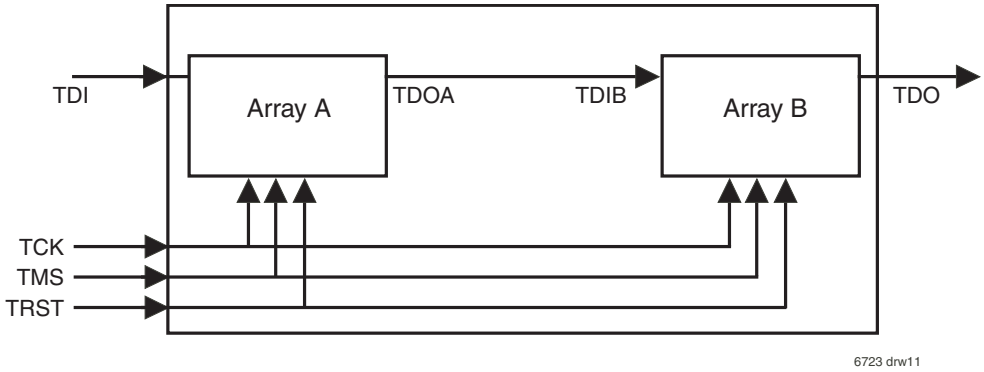
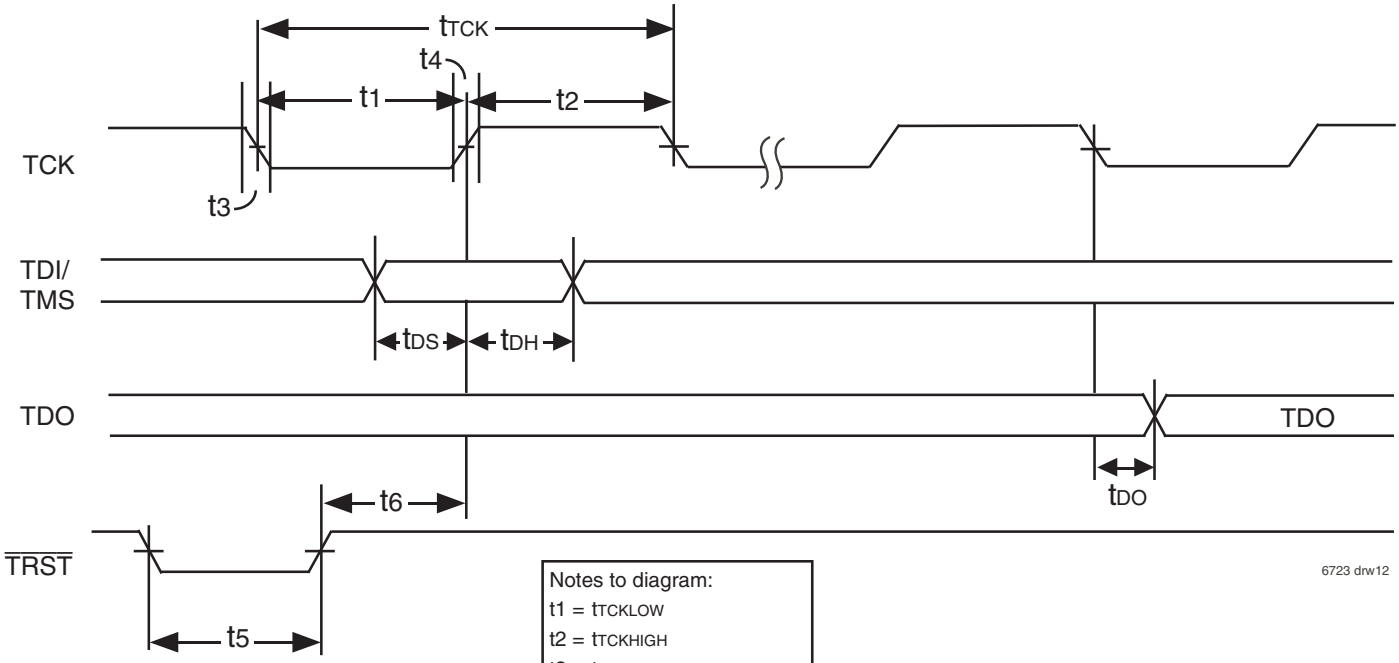


Figure 5. JTAG Configuration for IDT72T36135M

JTAG TIMING SPECIFICATION



Notes to diagram:
t1 = tTCKLOW
t2 = tTCKHIGH
t3 = tTCKFALL
t4 = tTCKRISE
t5 = tRST (reset pulse width)
t6 = tRSR (reset recovery)

SYSTEM INTERFACE PARAMETERS

Parameter	Symbol	Test Conditions	IDT72T36135M		
			Min.	Max.	Units
Data Output	t_{DO}[1]		-	20	ns
Data Output Hold	t_{DOH}[1]		0	-	ns
Data Input	t_{DS}	trise=3ns	10	-	ns
	t_{DH}	tfall=3ns	10	-	

NOTE:
1. 50pf loading on external output signals.

JTAG AC ELECTRICAL CHARACTERISTICS

(Vcc = 2.5V ± 5%; Tcase = 0°C to +85°C)

Parameter	Symbol	Test Conditions	IDT72T36135M		
			Min.	Max.	Units
JTAG Clock Input Period	tTCK	-	100	-	ns
JTAG Clock HIGH	tTCKHIGH	-	40	-	ns
JTAG Clock Low	tTCKLOW	-	40	-	ns
JTAG Clock Rise Time	tTCKRISE	-	-	5[1]	ns
JTAG Clock Fall Time	tTCKFALL	-	-	5[1]	ns
JTAG Reset	tRST	-	50	-	ns
JTAG Reset Recovery	tRSR	-	50	-	ns

NOTE:
1. Guaranteed by design.

JTAG INTERFACE

Five additional pins (TDI, TDO, TMS, TCK and $\overline{TRST}$) are provided to support the JTAG boundary scan interface. The IDT72T36135M incorporates the necessary tap controller and modified pad cells to implement the JTAG facility.

Note that IDT provides appropriate Boundary Scan Description Language program files for these devices.

The Standard JTAG interface consists of four basic elements:

- *Test Access Port (TAP)*
- *TAP controller*
- *Instruction Register (IR)*
- *Data Register Port (DR)*

The following sections provide a brief description of each element. For a complete description refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

The Figure below shows the standard Boundary-Scan Architecture

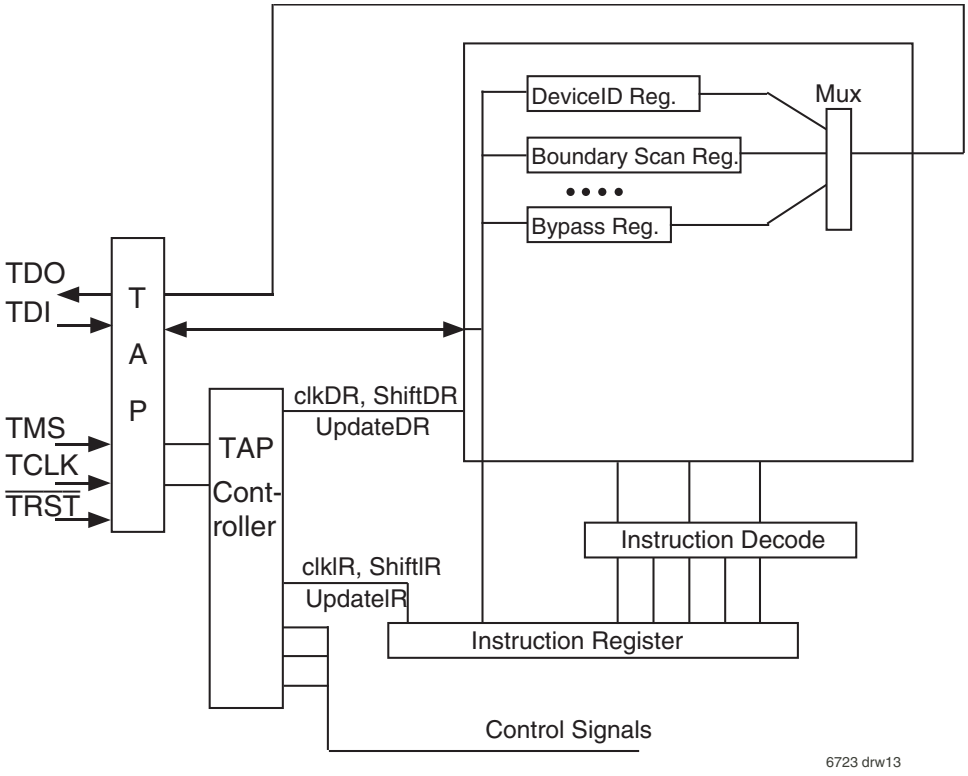


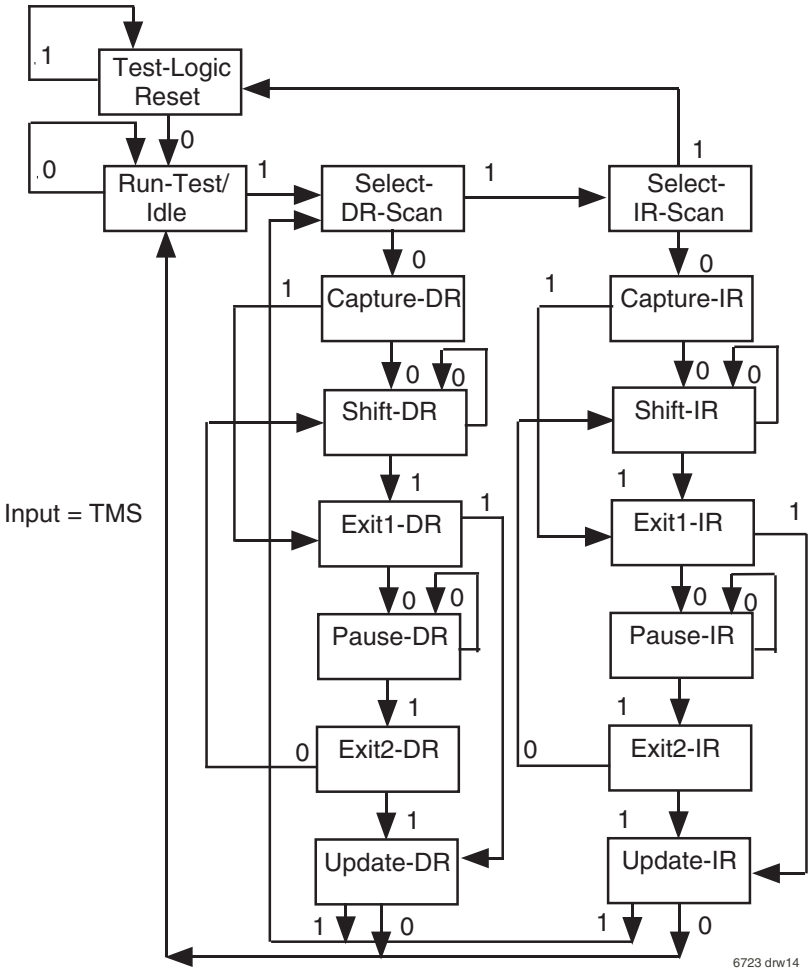
Figure 6. Boundary Scan Architecture

TEST ACCESS PORT (TAP)

The Tap interface is a general-purpose port that provides access to the internal of the processor. It consists of four input ports (TCLK, TMS, TDI, $\overline{TRST}$) and one output port (TDO).

THE TAP CONTROLLER

The Tap controller is a synchronous finite state machine that responds to TMS and TCLK signals to generate clock and control signals to the Instruction and Data Registers for capture and update of data.



NOTES:
1. Five consecutive TCK cycles with TMS = 1 will reset the TAP.
2. TAP controller does not automatically reset upon power-up. The user must provide a reset to the TAP controller (either by $\overline{TRST}$ or TMS).
3. TAP controller must be reset before normal FIFO operations can begin.

Figure 7. TAP Controller State Diagram

Refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1) for the full state diagram

All state transitions within the TAP controller occur at the rising edge of the TCLK pulse. The TMS signal level (0 or 1) determines the state progression that occurs on each TCLK rising edge. The TAP controller takes precedence over the FIFO memory and must be reset after power up of the device. See $\overline{TRST}$ description for more details on TAP controller reset.

Test-Logic-Reset All test logic is disabled in this controller state enabling the normal operation of the IC. The TAP controller state machine is designed in such a way that, no matter what the initial state of the controller is, the Test-Logic-Reset state can be entered by holding TMS at high and pulsing TCK five times. This is the reason why the Test Reset ($\overline{TRST}$) pin is optional.

Run-Test-Idle In this controller state, the test logic in the IC is active only if certain instructions are present. For example, if an instruction activates the self test, then it will be executed when the controller enters this state. The test logic in the IC is idles otherwise.

Select-DR-Scan This is a controller state where the decision to enter the Data Path or the Select-IR-Scan state is made.

Select-IR-Scan This is a controller state where the decision to enter the Instruction Path is made. The Controller can return to the Test-Logic-Reset state other wise.

Capture-IR In this controller state, the shift register bank in the Instruction Register parallel loads a pattern of fixed values on the rising edge of TCK. The last two significant bits are always required to be “01”.

Shift-IR In this controller state, the instruction register gets connected between TDI and TDO, and the captured pattern gets shifted on each rising edge of TCK. The instruction available on the TDI pin is also shifted in to the instruction register.

Exit1-IR This is a controller state where a decision to enter either the Pause-IR state or Update-IR state is made.

Pause-IR This state is provided in order to allow the shifting of instruction register to be temporarily halted.

Exit2-DR This is a controller state where a decision to enter either the Shift-IR state or Update-IR state is made.

Update-IR In this controller state, the instruction in the instruction register is latched in to the latch bank of the Instruction Register on every falling edge of TCK. This instruction also becomes the current instruction once it is latched.

Capture-DR In this controller state, the data is parallel loaded in to the data registers selected by the current instruction on the rising edge of TCK.

Shift-DR, Exit1-DR, Pause-DR, Exit2-DR and Update-DR These controller states are similar to the Shift-IR, Exit1-IR, Pause-IR, Exit2-IR and Update-IR states in the Instruction path.

SCAN REGISTER DESCRIPTIONS

THE INSTRUCTION REGISTER

The Instruction register allows an instruction to be shifted in serially into the processor at the rising edge of TCLK.

The Instruction is used to select the test to be performed, or the test data register to be accessed, or both. The instruction shifted into the register is latched at the completion of the shifting process when the TAP controller is at Update-IR state.

The instruction register must contain 8 bit instruction register-based cells which can hold instruction data. These mandatory cells are located nearest the serial outputs they are the least significant bits.

TEST DATA REGISTER

The Test Data register contains three test data registers: the Bypass, the Boundary Scan register and Device ID register.

These registers are connected in parallel between a common serial input and a common serial data output.

The following sections provide a brief description of each element. For a complete description, refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

TEST BYPASS REGISTER

The register is used to allow test data to flow through the device from TDI to TDO. It contains a single stage shift register for a minimum length in serial path. When the bypass register is selected by an instruction, the shift register stage is set to a logic zero on the rising edge of TCLK when the TAP controller is in the Capture-DR state.

The operation of the bypass register should not have any effect on the operation of the device in response to the BYPASS instruction.

THE BOUNDARY-SCAN REGISTER

The Boundary Scan Register allows serial data TDI be loaded in to or read out of the processor input/output ports. The Boundary Scan Register is a part of the IEEE 1149.1-1990 Standard JTAG Implementation.

THE DEVICE IDENTIFICATION REGISTER

The Device Identification Register is a Read Only 64-bit register used to specify the manufacturer, part number and version of the processor to be determined through the TAP in response to the IDCODE instruction.

IDT JEDEC ID number is 0xB3. This translates to 0x33 when the parity is dropped in the 11-bit Manufacturer ID field.

For the IDT72T36135M, the Part Number field contains the following values:

Device	Part# Field
IDT72T36135M	0417

31(MSB) 28	27 12	11 1	0(LSB)
Version (4 bits) 0X0	Part Number (16-bit)	Manufacturer ID (11-bit) 0X33	1

IDT72T36135M JTAG Device Identification Register

Please note:

The IDT72T36135M device is a two die MCM which means 64 bits will be shifted out of the device when the user is in IDCODE. Since the JTAG device identification register is 32 bits per die.

JTAG INSTRUCTION REGISTER

The Instruction register allows instruction to be serially input into the device when the TAP controller is in the Shift-IR state. The instruction is decoded to perform the following:

- Select test data registers that may operate while the instruction is current. The other test data registers should not interfere with chip operation and the selected data register.
- Define the serial test data register path that is used to shift data between TDI and TDO during data register scanning.

The Instruction Register is a 8 bit field (i.e. IR3, IR2, IR1, IR0 per die) to decode 32 different possible instructions. Instructions are decoded as follows.

Please note:

Again, since this device is a two die MCM, the JTAG instructions must be shifted in twice during JTAG testing. To account for each dies 4bit instruction registers for a total of 8 bits altogether.

JTAG INSTRUCTION DESCRIPTION

Hex Value	Instruction	Function
0x00	EXTEST	Select Boundary Scan Register
0x22	IDCODE	Select Chip Identification data register
0x11	SAMPLE/PRELOAD	Select Boundary Scan Register
0x33	HIGH-IMPEDANCE	JTAG
0xFF	BYPASS	Select Bypass Register

JTAG Instruction Register Decoding

The following sections provide a brief description of each instruction. For a complete description refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

EXTEST

The required EXTEST instruction places the IC into an external boundary-test mode and selects the boundary-scan register to be connected between TDI and TDO. During this instruction, the boundary-scan register is accessed to drive test data off-chip via the boundary outputs and receive test data off-chip via the boundary inputs. As such, the EXTEST instruction is the workhorse of IEEE. Std 1149.1, providing for probe-less testing of solder-joint opens/shorts and of logic cluster function.

IDCODE

The optional IDCODE instruction allows the IC to remain in its functional mode and selects the optional device identification register to be connected between TDI and TDO. The device identification register is a 64-bit shift register containing information regarding the IC manufacturer, device type, and version code. Accessing the device identification register does not interfere with the operation of the IC. Also, access to the device identification register should be immediately available, via a TAP data-scan operation, after power-up of the IC or after the TAP has been reset using the optional $\overline{\text{TRST}}$ pin or by otherwise moving to the Test-Logic-Reset state.

SAMPLE/PRELOAD

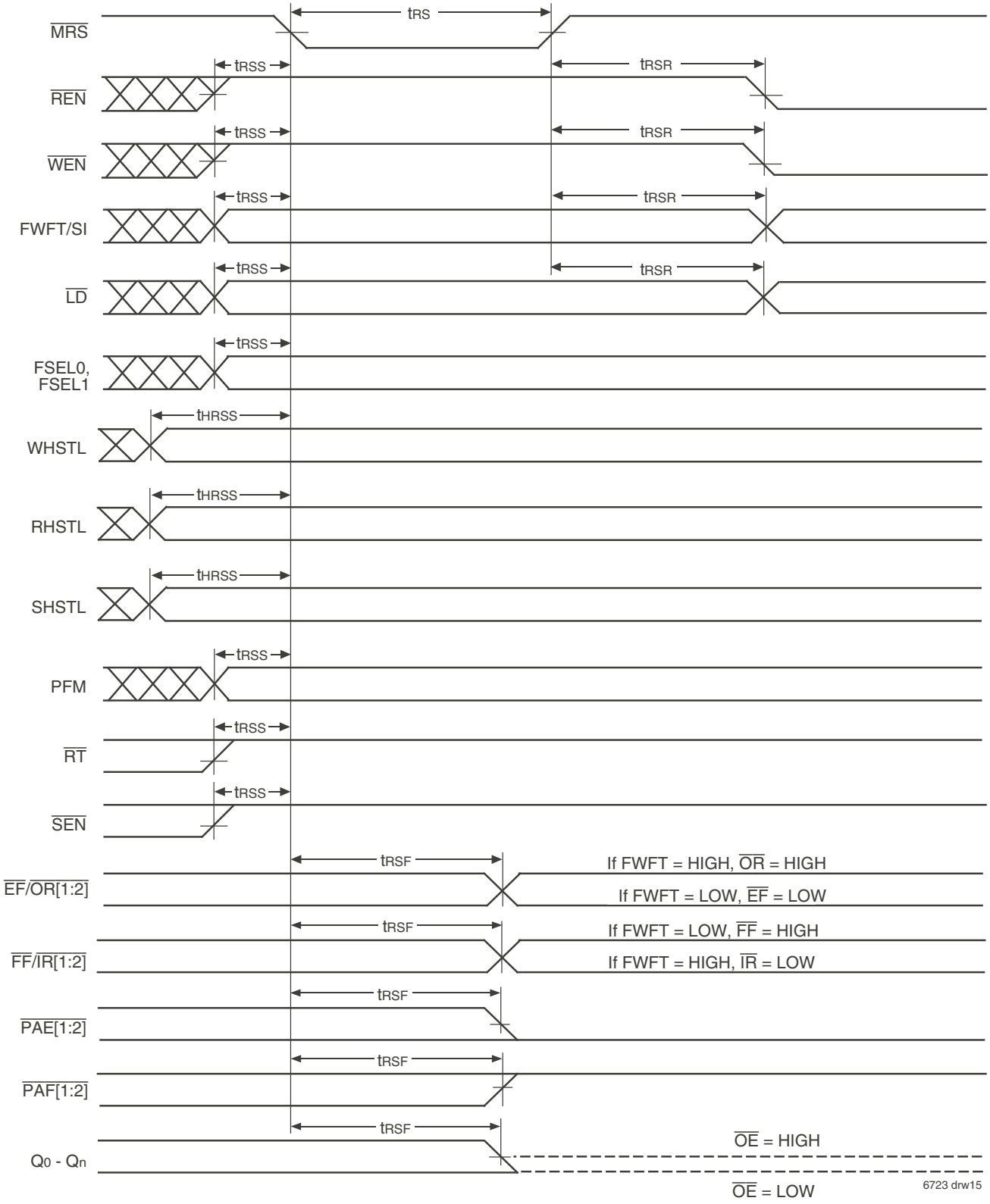
The required SAMPLE/PRELOAD instruction allows the IC to remain in a normal functional mode and selects the boundary-scan register to be connected between TDI and TDO. During this instruction, the boundary-scan register can be accessed via a date scan operation, to take a sample of the functional data entering and leaving the IC. This instruction is also used to preload test data into the boundary-scan register before loading an EXTEST instruction.

HIGH-IMPEDANCE

The optional High-Impedance instruction sets all outputs (including two-state as well as three-state types) of an IC to a disabled (high-impedance) state and selects the one-bit bypass register to be connected between TDI and TDO. During this instruction, data can be shifted through the bypass register from TDI to TDO without affecting the condition of the IC outputs.

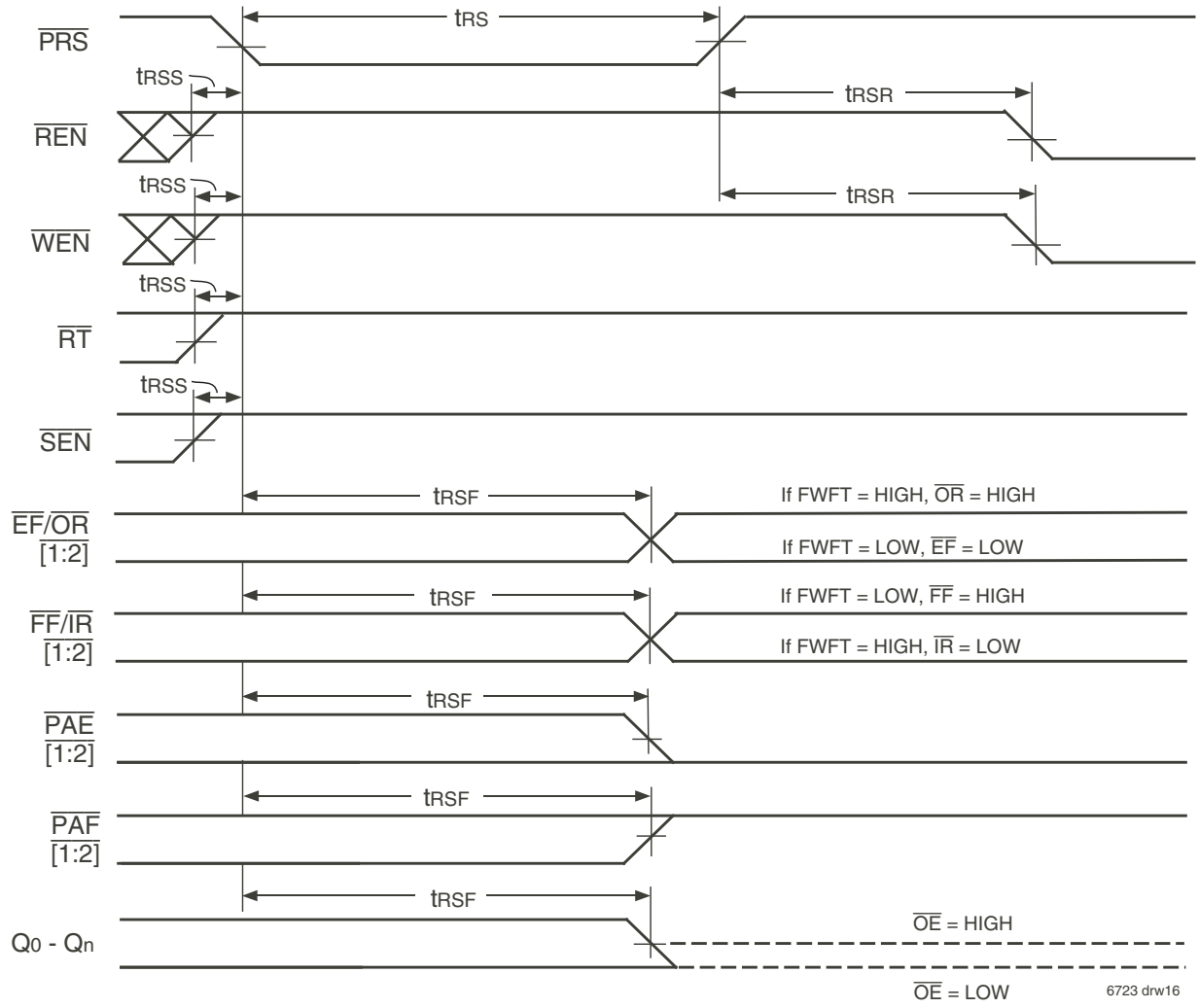
BYPASS

The required BYPASS instruction allows the IC to remain in a normal functional mode and selects the one-bit bypass register to be connected between TDI and TDO. The BYPASS instruction allows serial data to be transferred through the IC from TDI to TDO without affecting the operation of the IC.



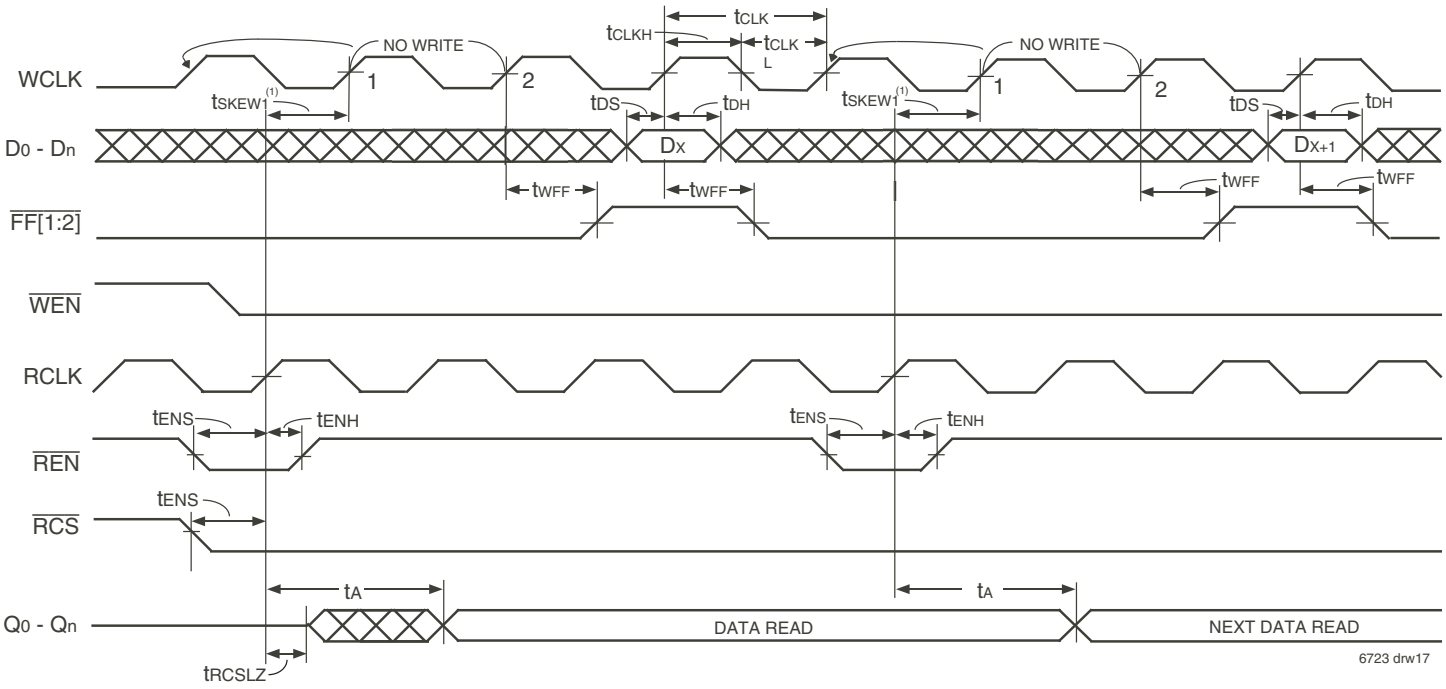
NOTE:
1. During Master Reset the High-Impedance control of the Qn data outputs is provided by $\overline{OE}$ only, $\overline{RCS}$ can be HIGH or LOW until the first rising edge of RCLK after Master Reset is complete.

Figure 8. Master Reset Timing



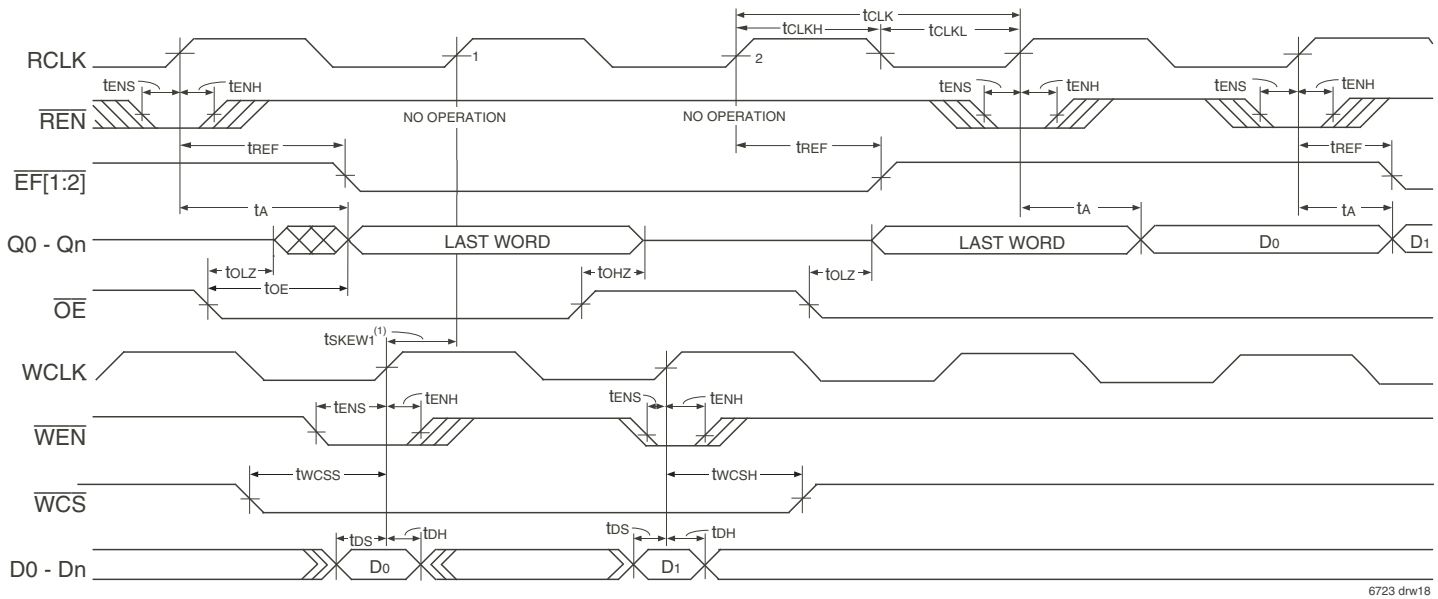
NOTE:
1. During Partial Reset the High-Impedance control of the Qn data outputs is provided by $\overline{OE}$ only, $\overline{RCS}$ can be HIGH or LOW until the first rising edge of RCLK after Master Reset is complete.

Figure 9. Partial Reset Timing



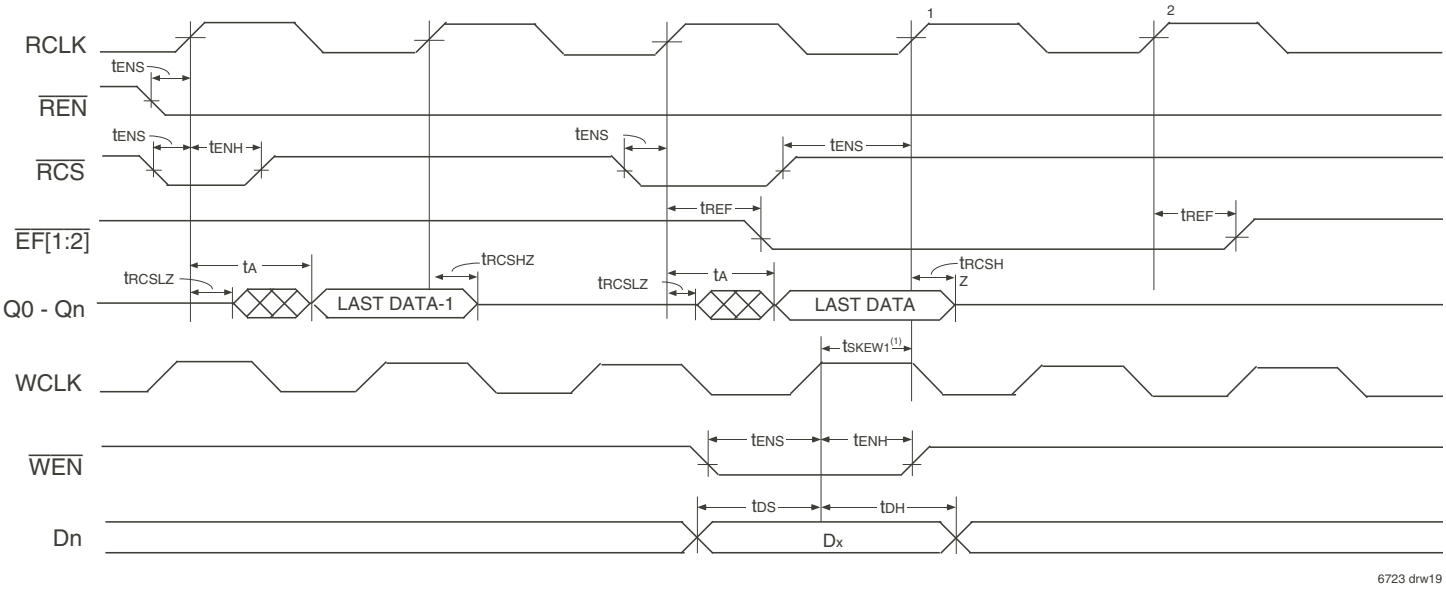
NOTES:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}[1:2]$ will go HIGH (after one WCLK cycle pus t_{WFF}). If the time between the rising edge of the RCLK and the rising edge of the WCLK is less than t_{SKEW1}, then the $\overline{FF}[1:2]$ deassertion may be delayed one extra WCLK cycle.
2. $\overline{LD}$ = HIGH, $\overline{OE}$ = LOW, $\overline{EF}[1:2]$ = HIGH.
3. $\overline{WCS}$ = LOW.

Figure 10. Write Cycle and Full Flag Timing (IDT Standard Mode)



NOTES:
1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}[1:2]$ will go HIGH (after one RCLK cycle plus t_{REF}). If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}, then $\overline{EF}[1:2]$ deassertion may be delayed one extra RCLK cycle.
2. $\overline{LD}$ = HIGH.
3. First data word latency = t_{SKEW1} + 1*T_{RCLK} + t_{REF}.
4. $\overline{RCS}$ is LOW.

Figure 11. Read Cycle, Output Enable, Empty Flag and First Data Word Latency (IDT Standard Mode)



NOTES:
1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}[1:2]$ will go HIGH (after one RCLK cycle plus t_{REF}). If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}, then $\overline{EF}[1:2]$ deassertion may be delayed one extra RCLK cycle.
2. $\overline{LD}$ = HIGH.
3. First data word latency = t_{SKEW1} + 1*T_{RCLK} + t_{REF}.
4. $\overline{OE}$ is LOW.

Figure 12. Read Cycle and Read Chip Select (IDT Standard Mode)

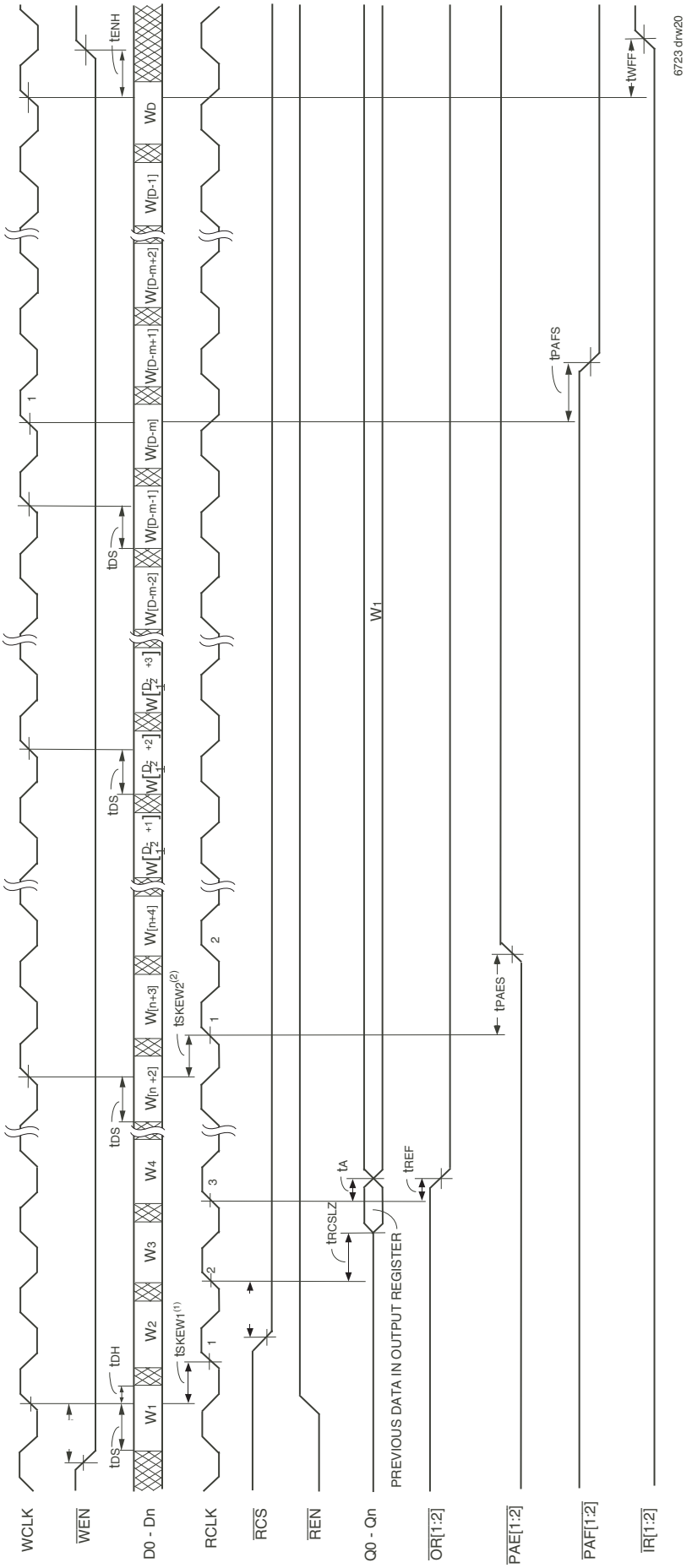


Figure 13. Write Timing (First Word Fall Through Mode)

NOTES:
1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{OR}[1:2]$ will go LOW after two RCLK cycles plus t_{REF}. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}, then $\overline{OR}[1:2]$ assertion may be delayed one extra RCLK cycle.
2. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{PAE}[1:2]$ will go HIGH after one RCLK cycle plus t_{PAES}. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then the $\overline{PAE}[1:2]$ deassertion may be delayed one extra RCLK cycle.
3. $\overline{LD}$ = HIGH, $\overline{OE}$ = LOW
4. n = $\overline{PAF}[1:2]$ offset, m = $\overline{PAF}[1:2]$ offset and D = maximum FIFO depth.
5. D = 524,289 for the IDT72T36135M.
6. First data word latency = t_{SKEW1} + 2*T_{RCLK} + t_{REF}.

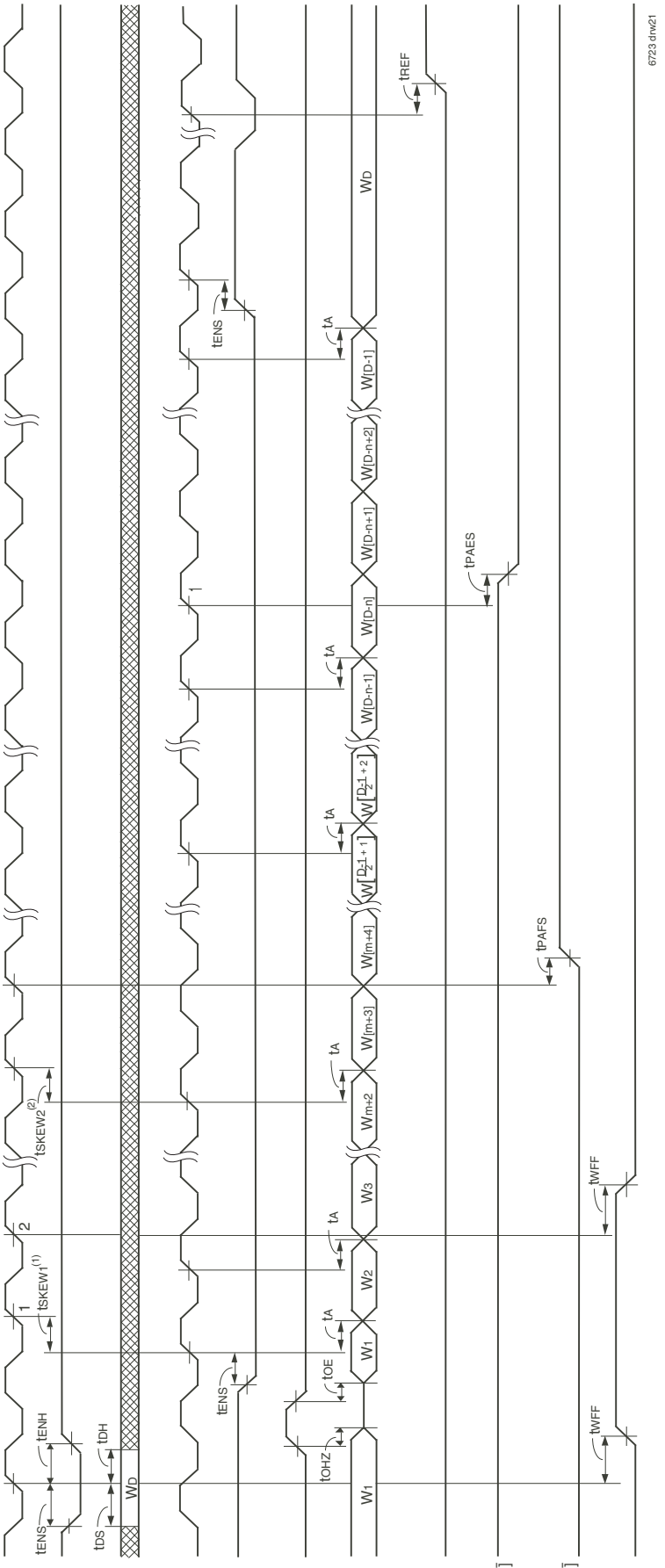
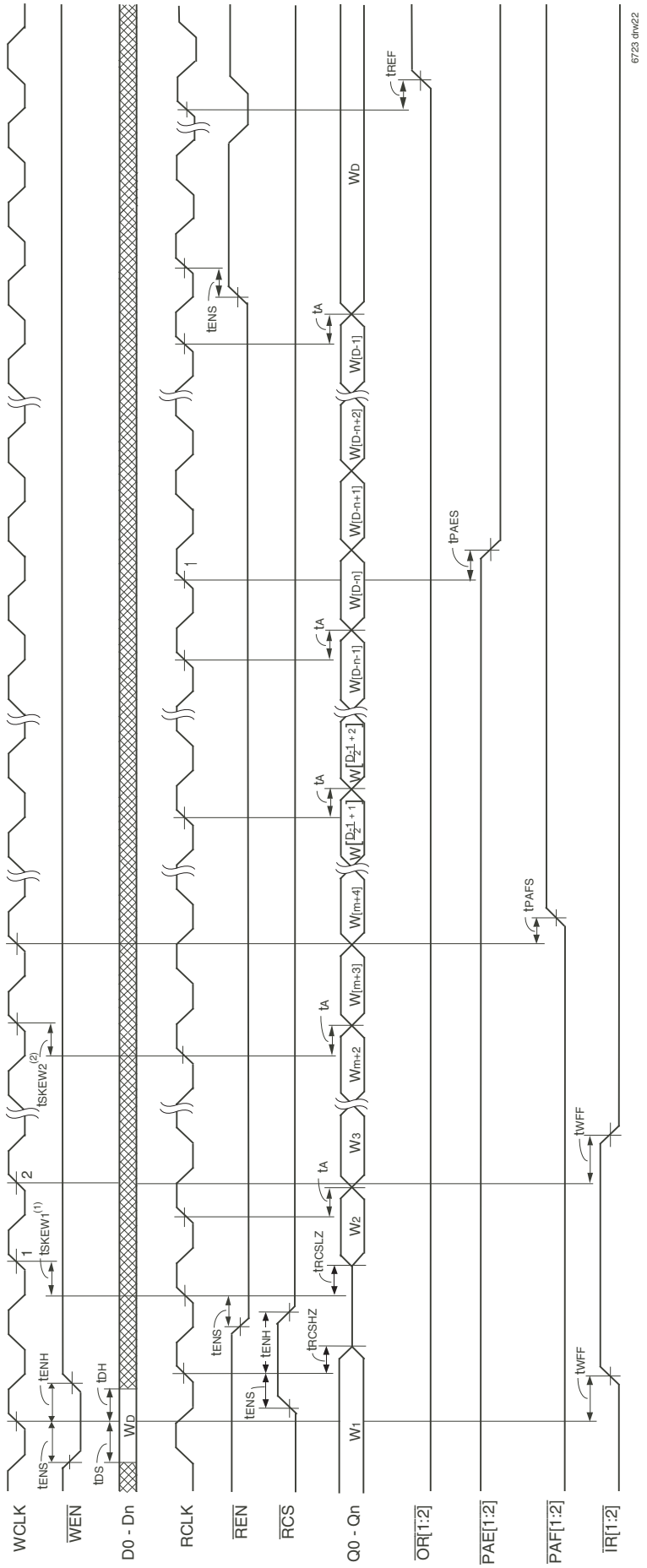


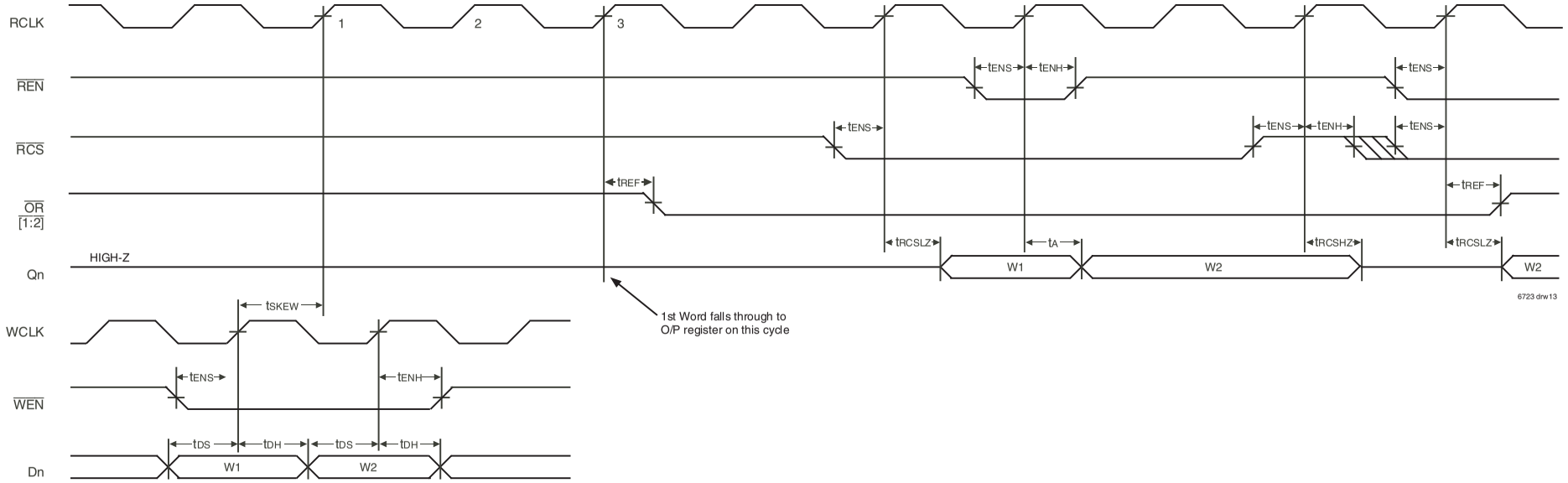
Figure 14. Read Timing (First Word Fall Through Mode)

NOTES:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{IR}[1:2]$ will go LOW after one WCLK cycle plus t_{WFF}. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then the $\overline{IR}[1:2]$ assertion may be delayed one extra WCLK cycle.
2. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{PAF}[1:2]$ will go HIGH after one WCLK cycle plus t_{PAFS}. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then the $\overline{PAF}[1:2]$ deassertion may be delayed one extra WCLK cycle.
3. $\overline{LD}$ = HIGH.
4. n = $\overline{PAE}[1:2]$ Offset, m = $\overline{PAF}[1:2]$ offset and D = maximum FIFO depth.
5. D = 524,289 for the IDT72T36135M.
6. $\overline{RCS}$ = LOW.



NOTES:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{IR}[1:2]$ will go LOW after one WCLK cycle plus t_{WFF}. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then the $\overline{IR}[1:2]$ assertion may be delayed one extra WCLK cycle.
2. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{PAF}[1:2]$ will go HIGH after one WCLK cycle plus t_{PAFS}. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then the $\overline{PAF}[1:2]$ deassertion may be delayed one extra WCLK cycle.
3. $\overline{LD}$ = HIGH.
4. n = $\overline{PAE}[1:2]$ Offset, m = $\overline{PAF}[1:2]$ offset and D = maximum FIFO depth.
5. D = 524,289 for the IDT72T36135M.
6. $\overline{OE}$ = LOW.

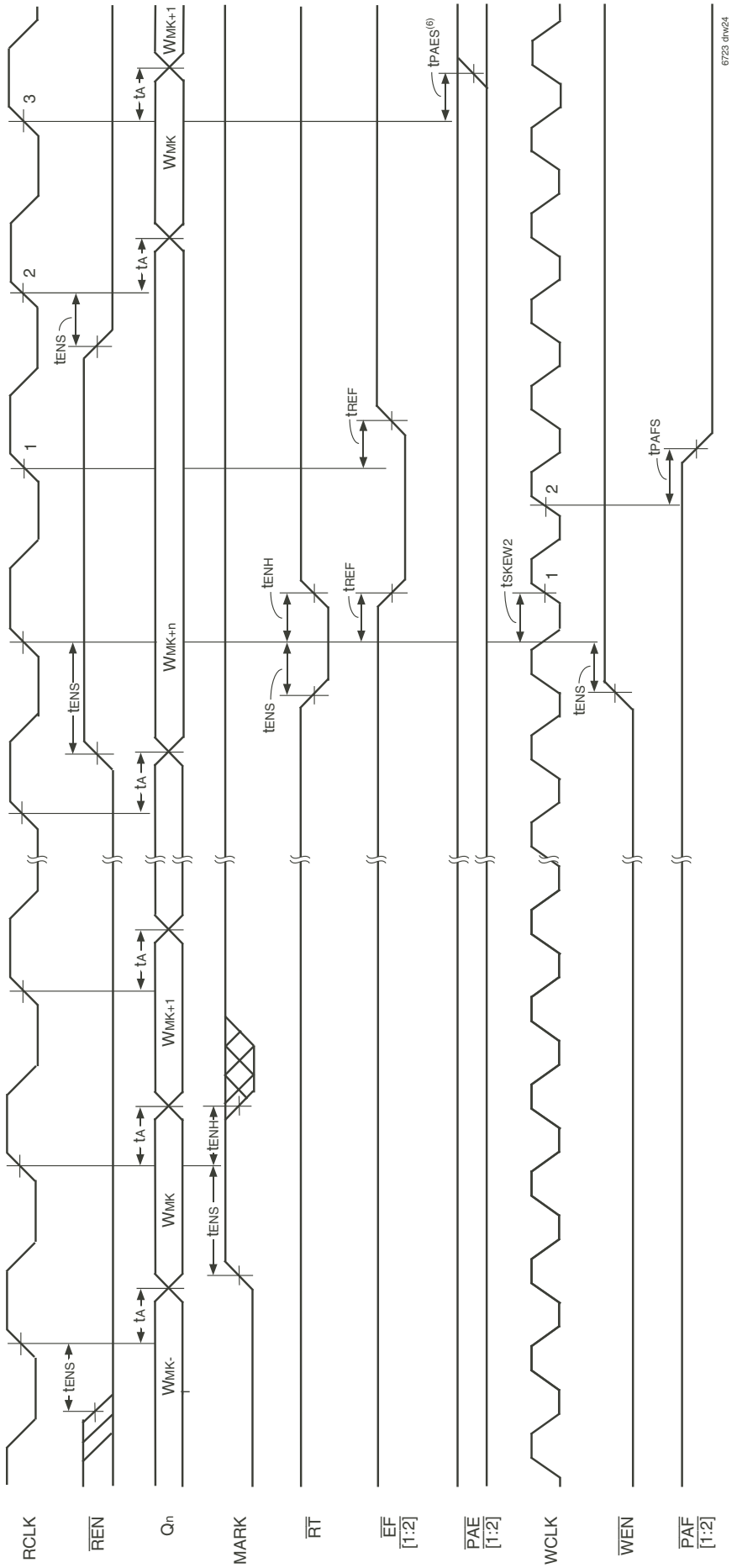
Figure 15. Read Cycle and Read Chip Select Timing (First Word Fall Through Mode)



NOTES:

1. It is very important that the $\overline{REN}$ be held HIGH for at least one cycle after $\overline{RCS}$ has gone LOW. If $\overline{REN}$ goes LOW on the same cycle as $\overline{RCS}$ or earlier, then Word, W1 will be lost, Word, W2 will be read on the output when the bus goes to LOW-Z.
2. The 1st Word will fall through to the output register regardless of $\overline{REN}$ and $\overline{RCS}$. However, subsequent reads require that both $\overline{REN}$ and $\overline{RCS}$ be active, LOW.

Figure 16 . $\overline{RCS}$ and $\overline{REN}$ Read Operation (FWFT Mode)



NOTES:
1. Retransmit setup is complete when $\overline{EF}[1:2]$ returns HIGH.
2. $\overline{OE}$ = LOW;$\overline{RCS}$ = LOW.
3. $\overline{RT}$ must be HIGH when reading from FIFO.
4. Once MARK is set, the write pointer will not increment past the 'marked' location, preventing overwrites of Retransmit data.
5. Before a "MARK" can be set there must be at least 64 number of words of data between the Write Pointer and Read Pointer locations.
6. A transition in the $\overline{PAE}[1:2]$ flag may occur one RCLK cycle earlier than shown, (on cycle 2).

Figure 17. Retransmit from Mark (IDT Standard Mode)

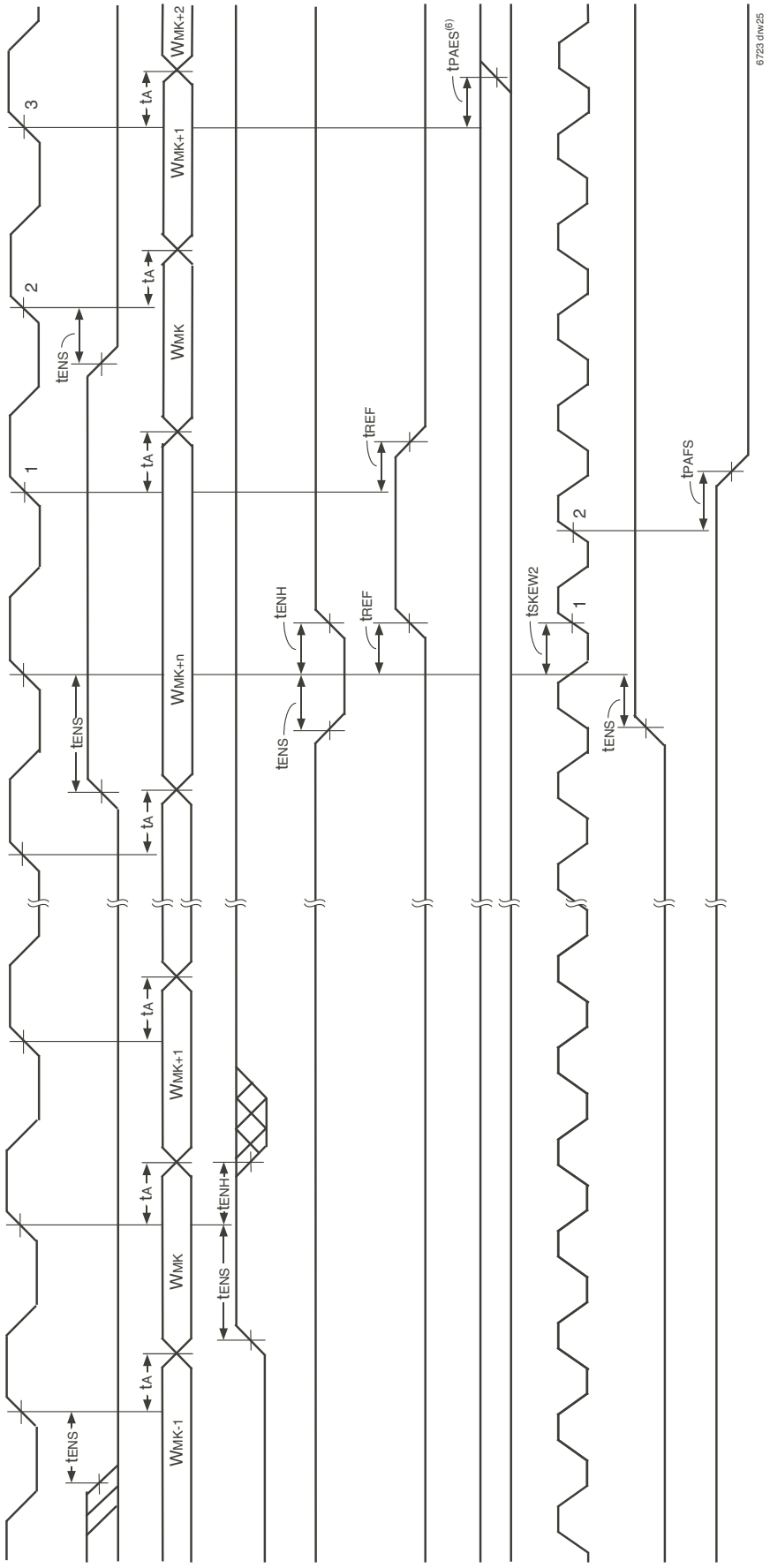


Figure 18. Retransmit from Mark (First Word Fall Through Mode)

NOTES:
1. Retransmit setup is complete when $\overline{OR}$[1:2] returns LOW.
2. $\overline{OE}$ = LOW;$\overline{RCS}$ = LOW.
3. $\overline{RT}$ must be HIGH when reading from FIFO.
4. Once MARK is set, the write pointer will not increment past the 'marked' location, preventing overwrites of Retransmit data.
5. Before a "MARK" can be set there must be at least 64 number of words of data between the Write Pointer and Read Pointer locations.
6. A transition in the $\overline{PAE}$[1:2] flag may occur one RCLK cycle earlier than shown, (on cycle 2).

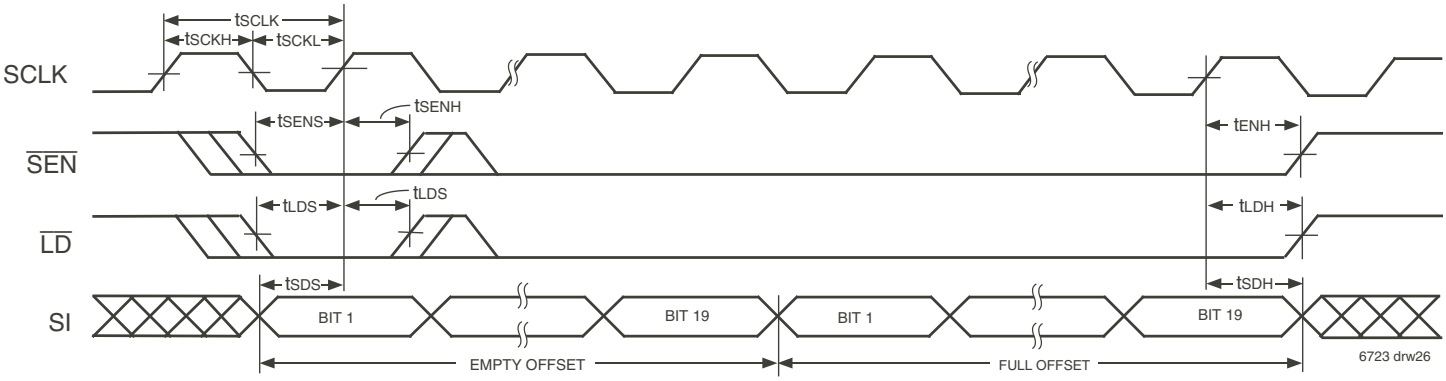


Figure 19. Serial Loading of Programmable Flag Registers (IDT Standard and FWFT Modes)

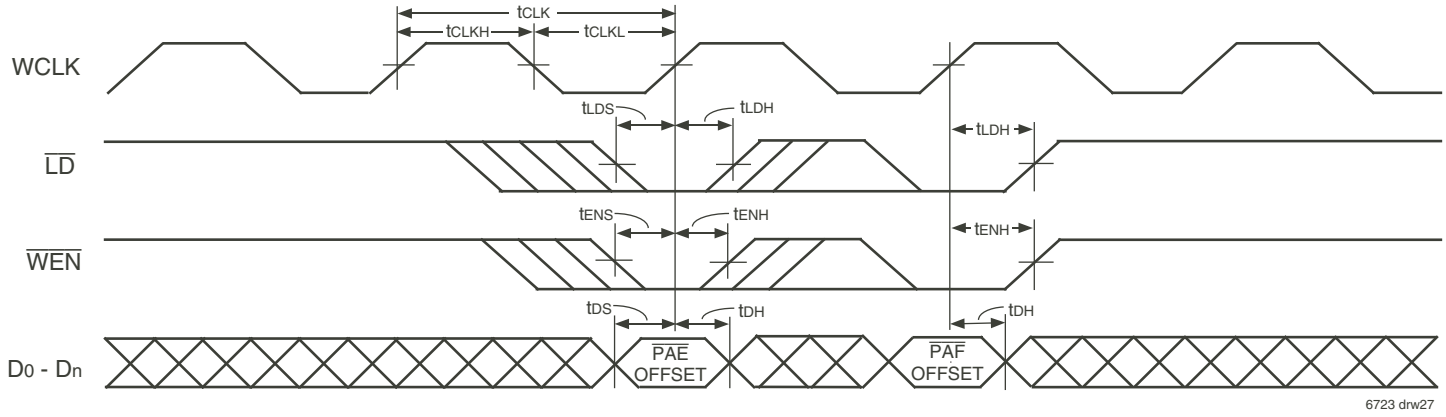
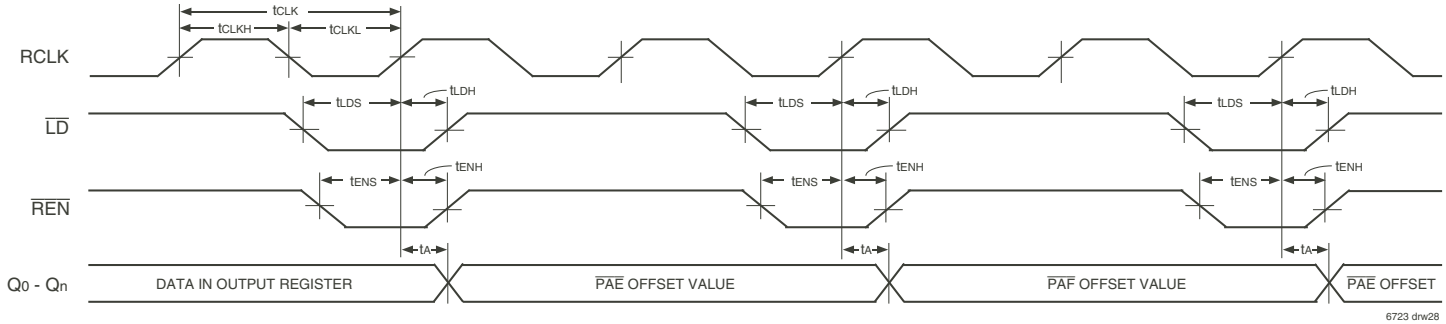
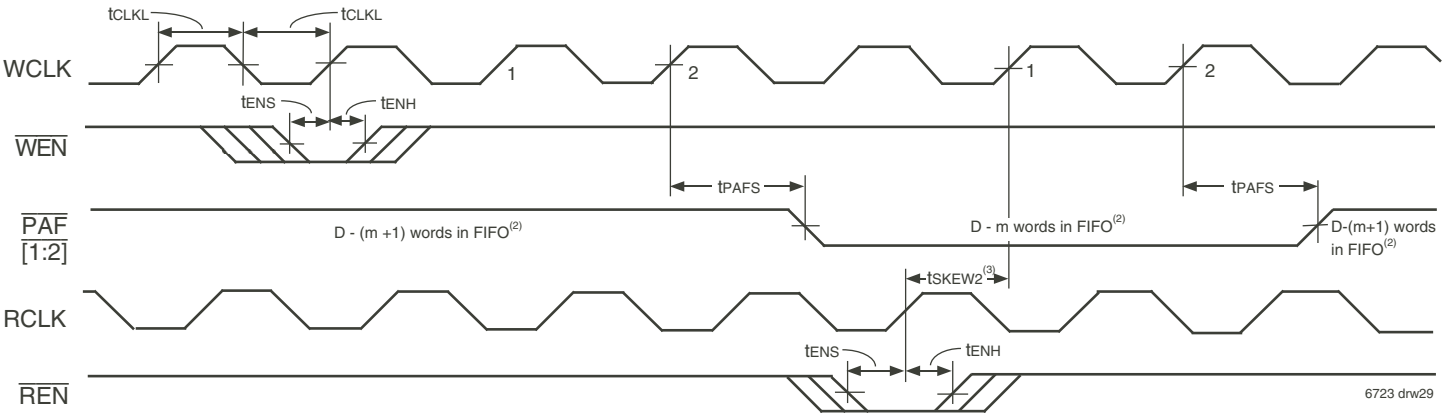


Figure 20. Parallel Loading of Programmable Flag Registers (IDT Standard and FWFT Modes)



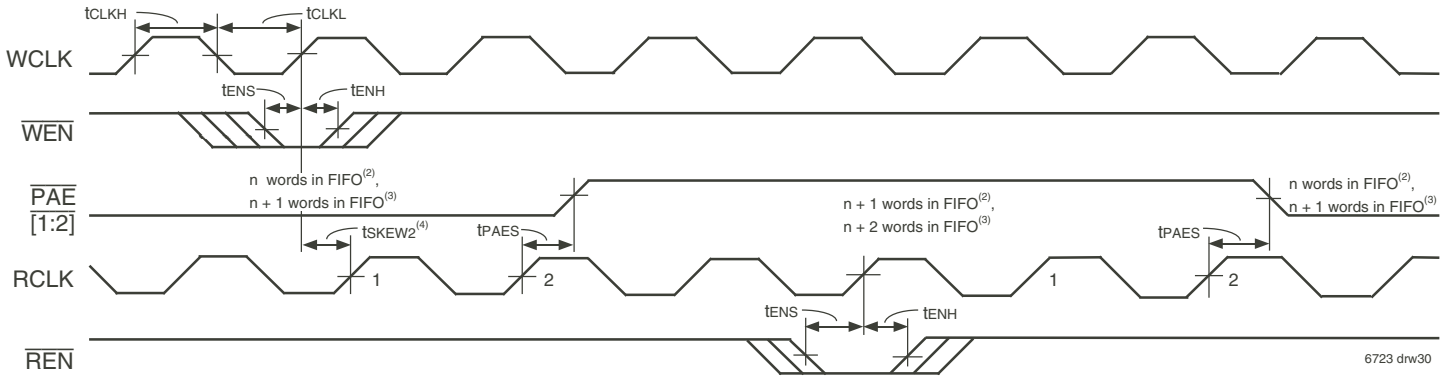
NOTES:
1. $\overline{OE}$ = LOW.
2. The offset registers cannot be read on consecutive RCLK cycles. The read must be disabled ($\overline{REN}$ = HIGH) for a minimum of one RCLK cycle in between register accesses.

Figure 21. Parallel Read of Programmable Flag Registers (IDT Standard and FWFT Modes)



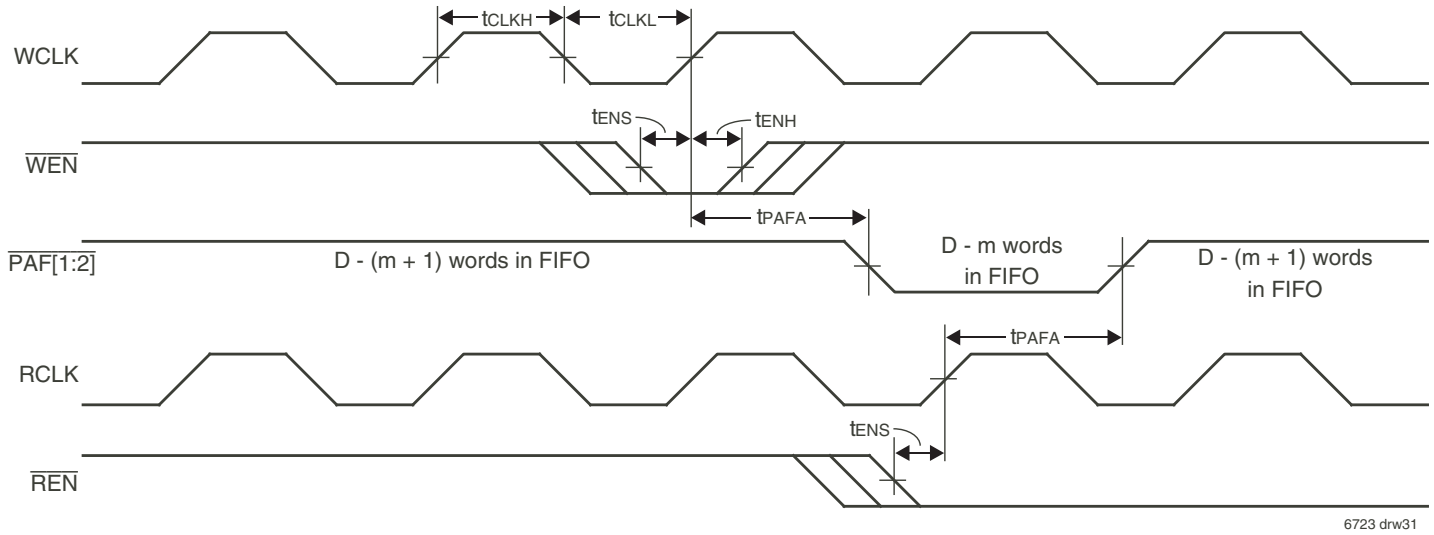
NOTES:
1. m = PAF[1:2] offset.
2. D = maximum FIFO depth.
   In IDT Standard mode: D = 524,288 for the IDT72T36135M.
   In FWFT mode: D = 524,289 for the IDT72T36135M.
3. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that PAF[1:2] will go HIGH (after one WCLK cycle plus t_{PAFS}). If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then the PAF[1:2] deassertion time may be delayed one extra WCLK cycle.
4. PAF[1:2] is asserted and updated on the rising edge of WCLK only.
5. Select this mode by setting PFM HIGH during Master Reset.

Figure 22. Synchronous Programmable Almost-Full Flag Timing (IDT Standard and FWFT Modes)



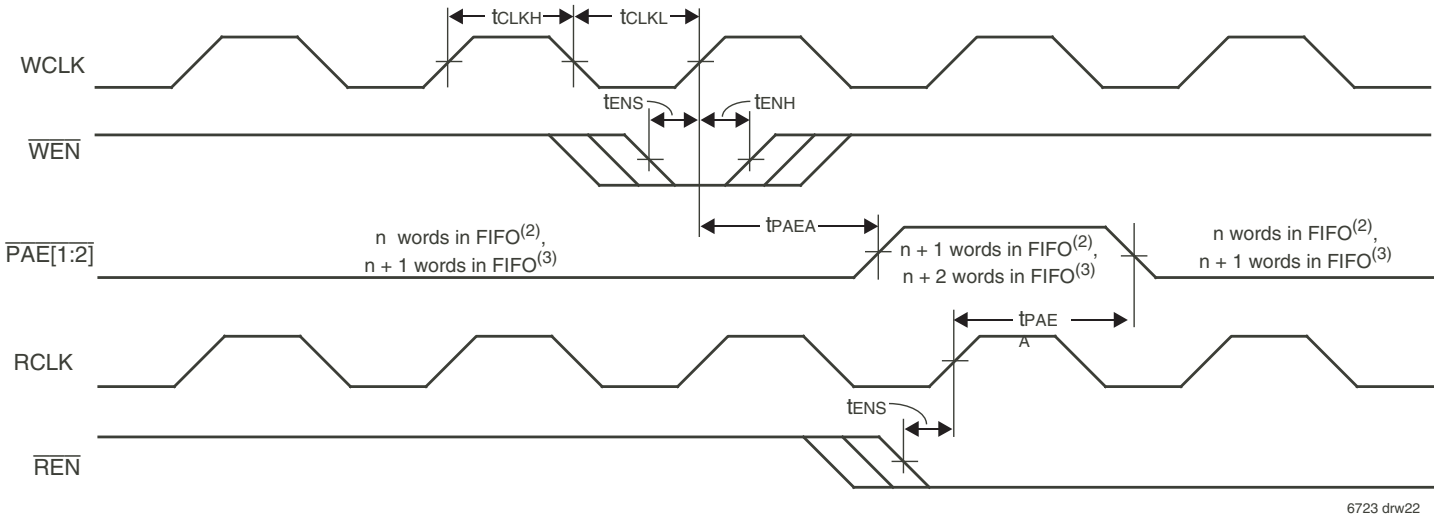
NOTES:
1. n = PAE[1:2] offset.
2. For IDT Standard mode
3. For FWFT mode.
4. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that PAE[1:2] will go HIGH (after one RCLK cycle plus t_{PAES}). If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then the PAE[1:2] deassertion may be delayed one extra RCLK cycle.
5. PAE[1:2] is asserted and updated on the rising edge of WCLK only.
6. Select this mode by setting PFM HIGH during Master Reset.
7. RCS = LOW.

Figure 23. Synchronous Programmable Almost-Empty Flag Timing (IDT Standard and FWFT Modes)



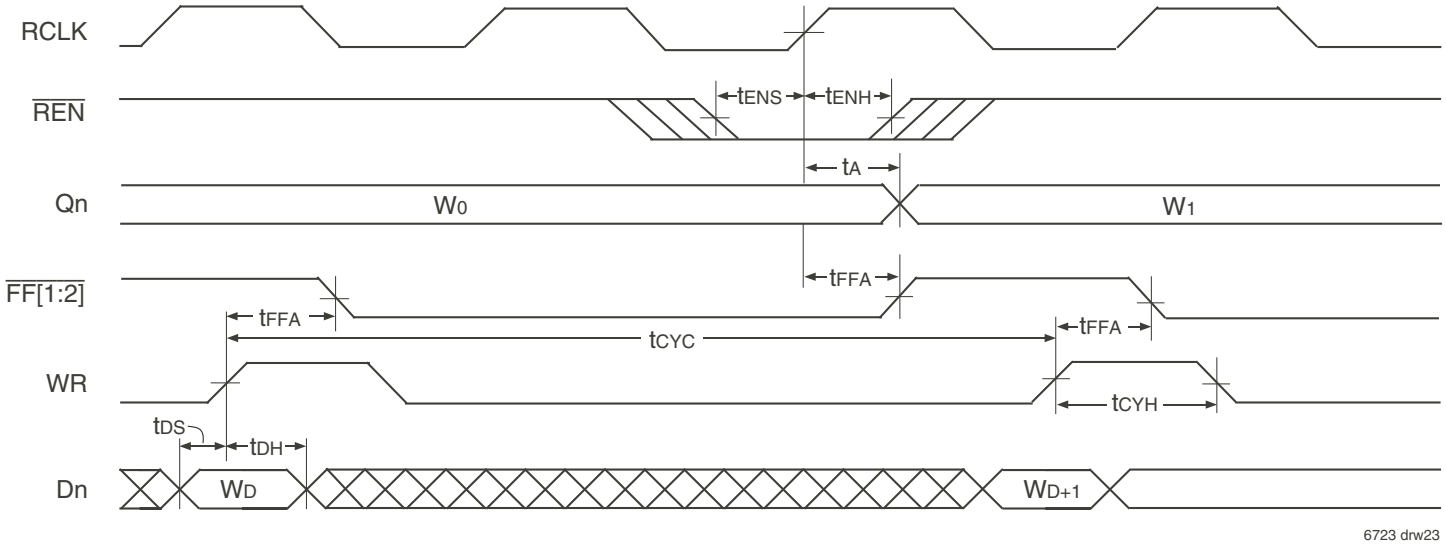
NOTES:
1. m = PAF[1:2] offset.
2. D = maximum FIFO Depth.
   In IDT Standard Mode: D = 524,288 for the IDT72T36135M.
   In FWFT Mode: D = 524,289 for the IDT72T36135M.
3. PAF[1:2] is asserted to LOW on WCLK transition and reset to HIGH on RCLK transition.
4. Select this mode by setting PFM LOW during Master Reset.
5. RCS = LOW.

Figure 24. Asynchronous Programmable Almost-Full Flag Timing (IDT Standard and FWFT Modes)



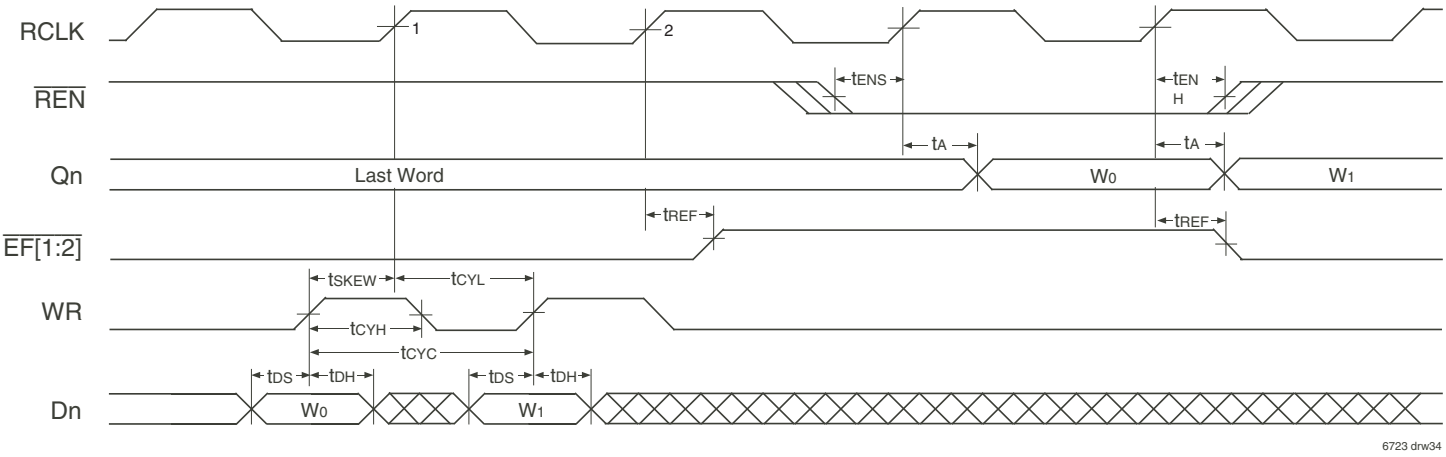
NOTES:
1. n = PAE[1:2] offset.
2. For IDT Standard Mode.
3. For FWFT Mode.
4. PAE[1:2] is asserted LOW on RCLK transition and reset to HIGH on WCLK transition.
5. Select this mode by setting PFM LOW during Master Reset.
6. RCS = LOW.

Figure 25. Asynchronous Programmable Almost-Empty Flag Timing (IDT Standard and FWFT Modes)



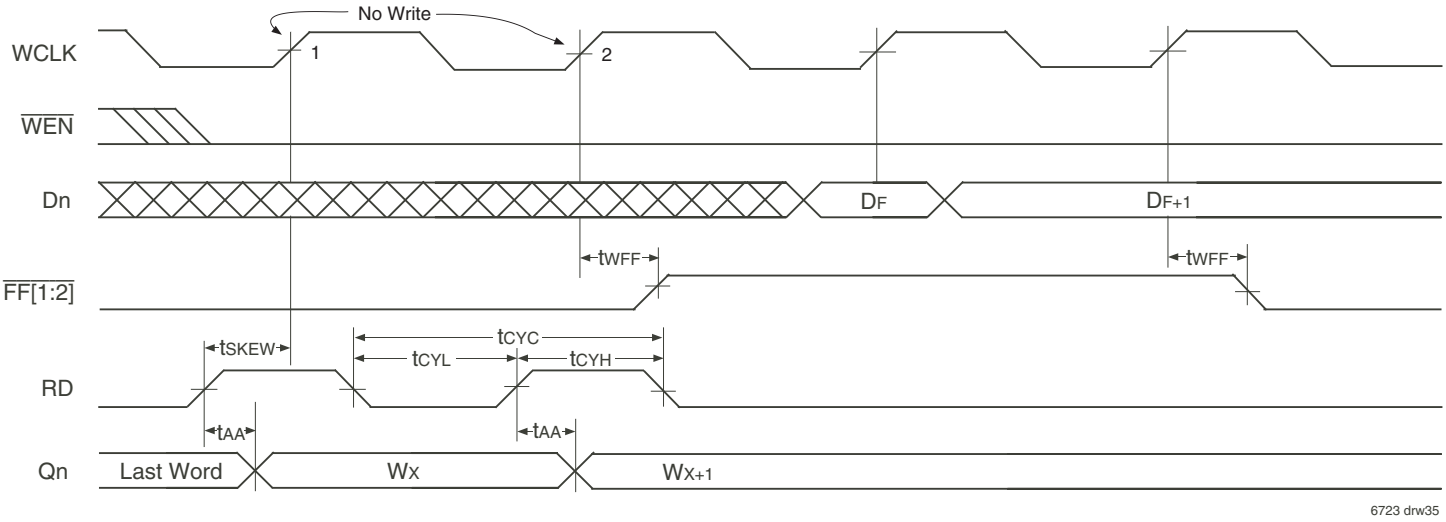
NOTE:
1. $\overline{OE}$ = LOW, $\overline{WEN}$ = LOW and $\overline{RCS}$ = LOW.

Figure 26. Asynchronous Write, Synchronous Read, Full Flag Operation (IDT Standard Mode)



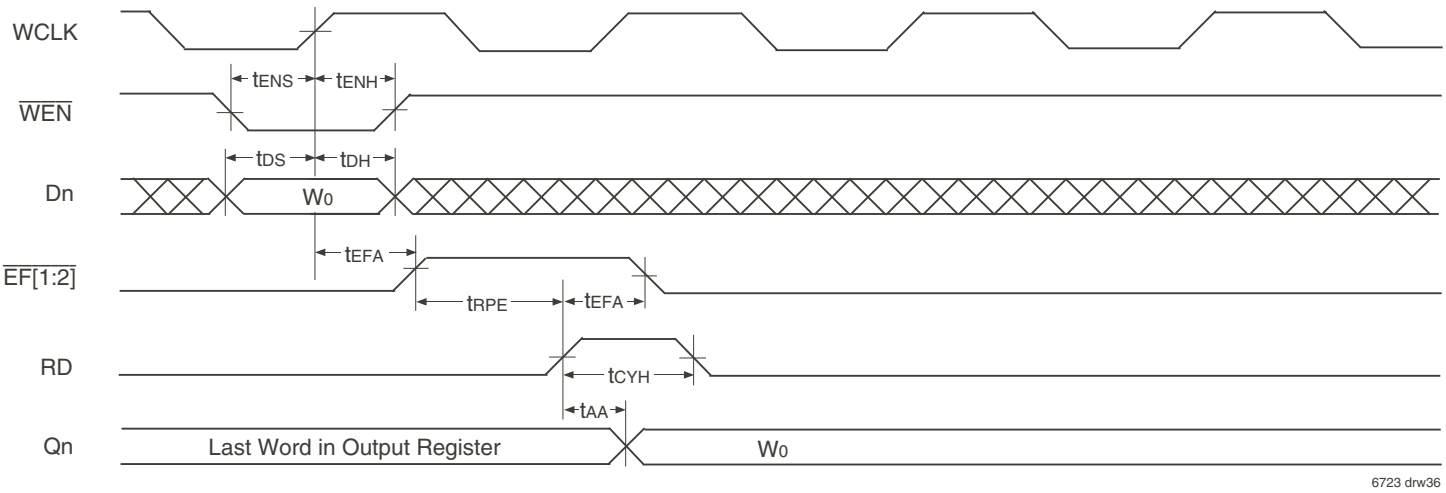
NOTE:
1. $\overline{OE}$ = LOW, $\overline{WEN}$ = LOW and $\overline{RCS}$ = LOW.

Figure 27. Asynchronous Write, Synchronous Read, Empty Flag Operation (IDT Standard Mode)



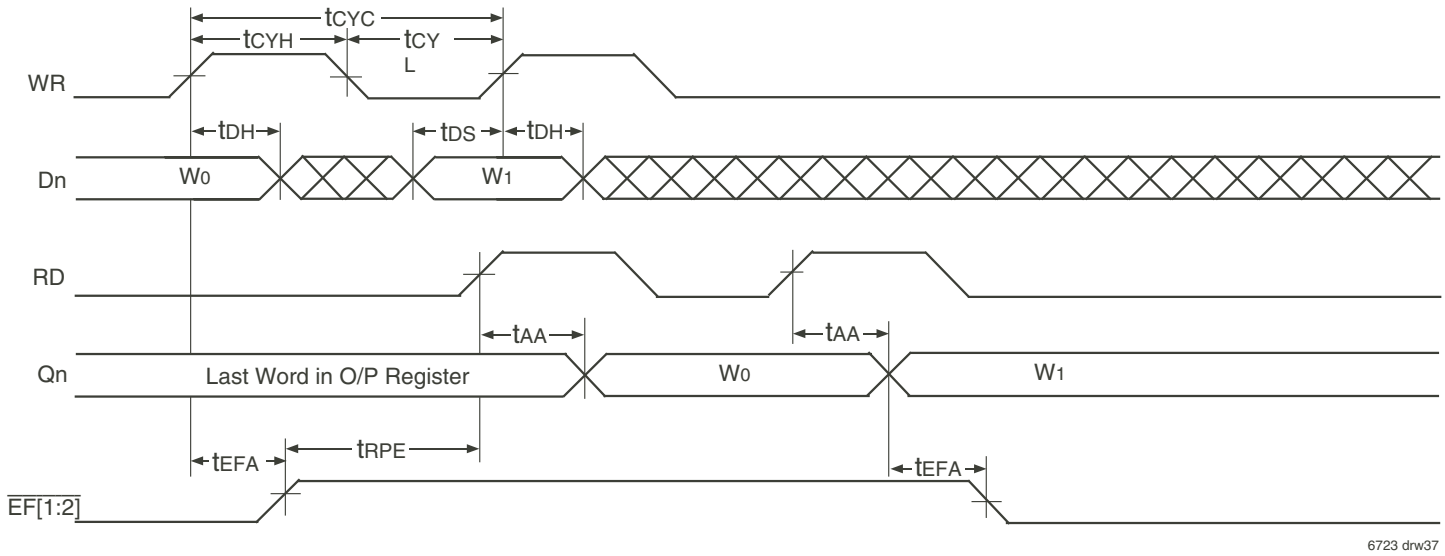
NOTE:
1. $\overline{OE}$ = LOW, $\overline{RCS}$ = LOW and $\overline{REN}$ = LOW.
2. Asynchronous Read is available in IDT Standard Mode only.

Figure 28. Synchronous Write, Asynchronous Read, Full Flag Operation (IDT Standard Mode)



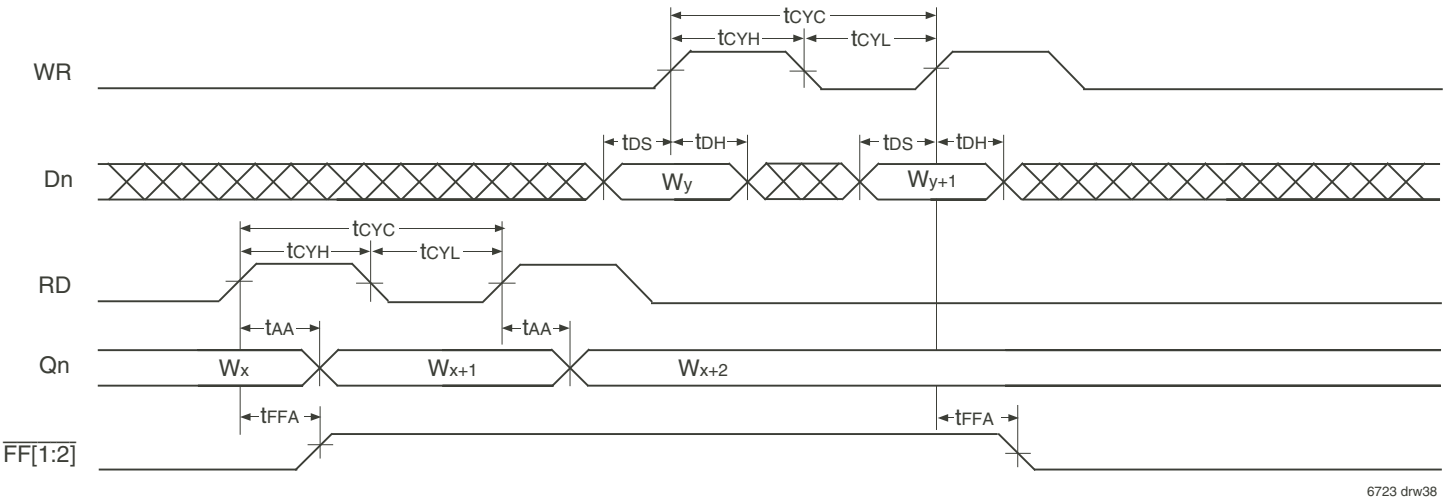
NOTE:
1. $\overline{OE}$ = LOW, $\overline{REN}$ = LOW and $\overline{RCS}$ = LOW.
2. Asynchronous Read is available in IDT Standard Mode only.

Figure 29. Synchronous Write, Asynchronous Read, Empty Flag Operation (IDT Standard Mode)



NOTES:
1. $\overline{OE}$ = LOW, $\overline{WEN}$ = LOW, $\overline{REN}$ = LOW and $\overline{RCS}$ = LOW
2. Asynchronous Read is available in IDT Standard Mode only.

Figure 30. Asynchronous Write, Asynchronous Read, Empty Flag Operation (IDT Standard Mode)



NOTES:
1. $\overline{OE}$ = LOW, $\overline{WEN}$ = LOW, $\overline{REN}$ = LOW and $\overline{RCS}$ = LOW.
2. Asynchronous Read is available in IDT Standard Mode only.

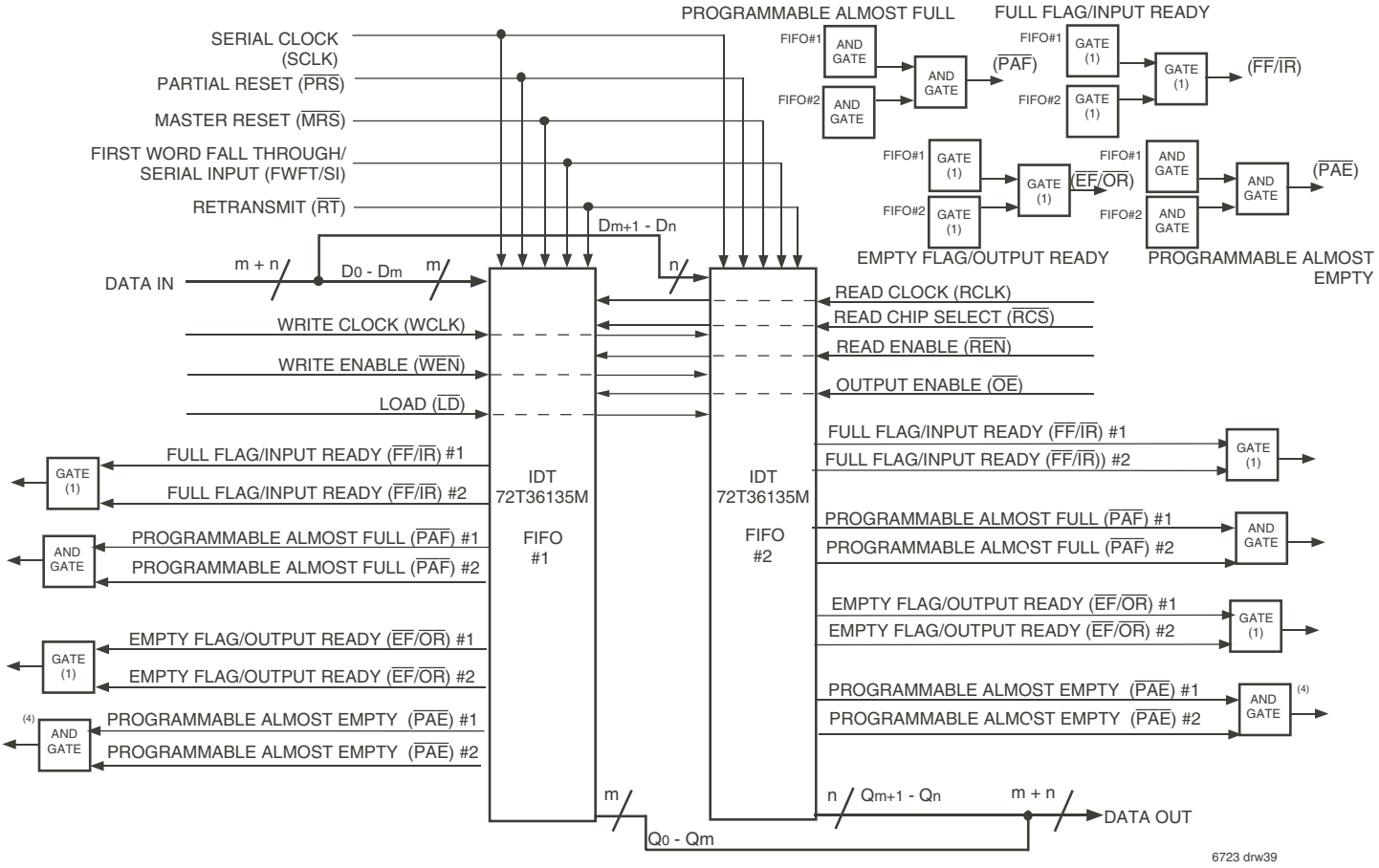
Figure 31. Asynchronous Write, Asynchronous Read, Full Flag Operation (IDT Standard Mode)

OPTIONAL CONFIGURATIONS

WIDTH EXPANSION CONFIGURATION

Word width may be increased by connecting together the control signals of multiple devices plus using external gating logic. Status flags can be gated and detected from the gate output. The $\overline{EF}$[1:2], $\overline{FF}$[1:2], $\overline{PAE}$[1:2], and $\overline{PAF}$[1:2] flags should be gated using logical gates to remove the possibility of clock skew between the two device(s) outputs.

Figure 32 demonstrates a width expansion using two IDT72T36135M devices. D_0 - D_{35} from each device form a 72-bit wide input bus and Q_0-Q_{35} from each device form a 72-bit wide output bus. Any word width can be attained by adding additional IDT72T36135M devices.



NOTES:
1. An OR gate is used for FWFT mode, AND gate for IDT mode.
2. Do not connect any output control signals directly together.
3. FIFO #1 and FIFO #2 must be the same depth, but may be different word widths.
4. $\overline{PAE}$/$\overline{PAF}$[1:2] optional, see section of external gating of output flags.

Figure 32. Block Diagram of 524,288 x 72 Width Expansion

DEPTH EXPANSION CONFIGURATION (FWFT MODE ONLY)

The IDT72T36135M can easily be adapted to applications requiring depths greater than and 524,288 with an 36-bit bus width. In FWFT mode, the FIFOs can be connected in series (the data outputs of one FIFO connected to the data inputs of the next) with no external logic necessary. The resulting configuration provides a total depth equivalent to the sum of the depths associated with each single FIFO. Figure 33 shows a depth expansion using two IDT72T36135M devices.

For depth expansion mode option #1, "logical OR gates" need to be used to drive the active low input $\overline{WEN}$ and $\overline{REN}$ pins respectively from the active low output $\overline{OR}$[1:2] and $\overline{IR}$[1:2] pins. Two sets of OR gates are used in this mode to derive a feedback loop to the $\overline{REN}$ and $\overline{WEN}$ pins to avoid writing or reading to/from a device when the device is not ready to accept data. The 2nd row of OR gates take in the $\overline{IR}$ or $\overline{OR}$ pin's status and allow for data to be written/read to the next FIFO in the chain. If the $\overline{IR}$ or $\overline{OR}$ pins are low, this will enable the device to accept writes or reads from the next device in line. To use this mode, the FIFO device's clock speed depends on the added prop delay of the "OR" gates and setup time between the two FIFO devices. Example, if the "OR" gates being used have a combined 10ns propagation delay, a 1ns jitter budget, and 1ns clock skew margin, 12ns must be taken into account during each clock cycle. For instance, a 25MHz clock has around a 40ns clock cycle. For a 45% - 55% clock duty cycle, 18ns account for 45% of the duty cycle when the clock is high. This means, 18ns – 12ns = 6ns of setup time for data to be available at the 2nd IDT FIFO which is fine considering the setup time for this FIFO is around 1.5ns.

Designers must leave an adequate timing window to allow data to be captured by the 2nd IDT FIFO. Please take this into consideration when using this depth expansion mode to avoid data meta-stability issues.

Care should be taken to select FWFT mode during Master Reset for all FIFOs in the depth expansion configuration. The first word written to an empty configuration will pass from one FIFO to the next ("ripple down") until it finally appears at the outputs of the last FIFO in the chain – no read operation is necessary but the RCLK of each FIFO must be free-running. Each time the data word appears at the outputs of one FIFO, that device's $\overline{OR}$[1:2] line goes LOW, enabling a write to the next FIFO in line. OR gates are used to take in the considerations of the next FIFO in the chains $\overline{IR}$ pin status. If the $\overline{IR}$ pins are Low, this will enable the device to accept writes from upstream devices.

For an empty expansion configuration, the amount of time it takes for $\overline{OR}$[1:2] of the last FIFO in the chain to go LOW (i.e. valid data to appear on the last FIFO's outputs) after a word has been written to the first FIFO is the sum of the delays for each individual FIFO and the sum of the OR gate prop delays:

$$(N - 1)*(4*\text{transfer clock}) + 3*T_{RCLK} + 2*\text{OR prop delay}$$

where N is the number of FIFOs in the expansion and T_{RCLK} is the RCLK period. Note that extra cycles should be added for the possibility that the t_{SKEW1} specification is not met between WCLK and transfer clock, or RCLK and transfer clock, for the $\overline{OR}$[1:2] flag.

The "ripple down" delay is only noticeable for the first word written to an empty depth expansion configuration. There will be no delay evident for subsequent words written to the configuration.

The first free location created by reading from a full depth expansion configuration will "bubble up" from the last FIFO to the previous one until it finally moves into the first FIFO of the chain. Each time a free location is created in one FIFO of the chain, that FIFO's $\overline{IR}$[1:2] line goes LOW, enabling the preceding FIFO to write a word to fill it.

For a full expansion configuration, the amount of time it takes for $\overline{IR}$[1:2] of the first FIFO in the chain to go LOW after a word has been read from the last FIFO is the sum of the delays for each individual FIFO and the sum of the OR gate prop delays:

$$(N - 1)*(3*\text{transfer clock}) + 2\,T_{WCLK} + 2*\text{OR prop delay}$$

where N is the number of FIFOs in the expansion and T_{WCLK} is the WCLK period. Note that extra cycles should be added for the possibility that the t_{SKEW1} specification is not met between RCLK and transfer clock, or WCLK and transfer clock, for the $\overline{IR}$[1:2] flag.

The Transfer Clock line should be tied to either WCLK or RCLK, whichever is faster. Both these actions result in data moving, as quickly as possible, to the end of the chain and free locations to the beginning of the chain.

Depth Expansion Option #2 is depicted in Figure 34, *Depth Expansion Option#2*. One device will be active at a time by toggling the WCS pins. Data will be written into FIFO in Ping Pong fashion. First data is written into FIFO#1, second data is written into FIFO#2, third data is written into FIFO#1, fourth data is written into FIFO#2, and so on. Data can then be read out in the same manner on the read side by toggling the $\overline{RCS}$1 and $\overline{RCS}$2.

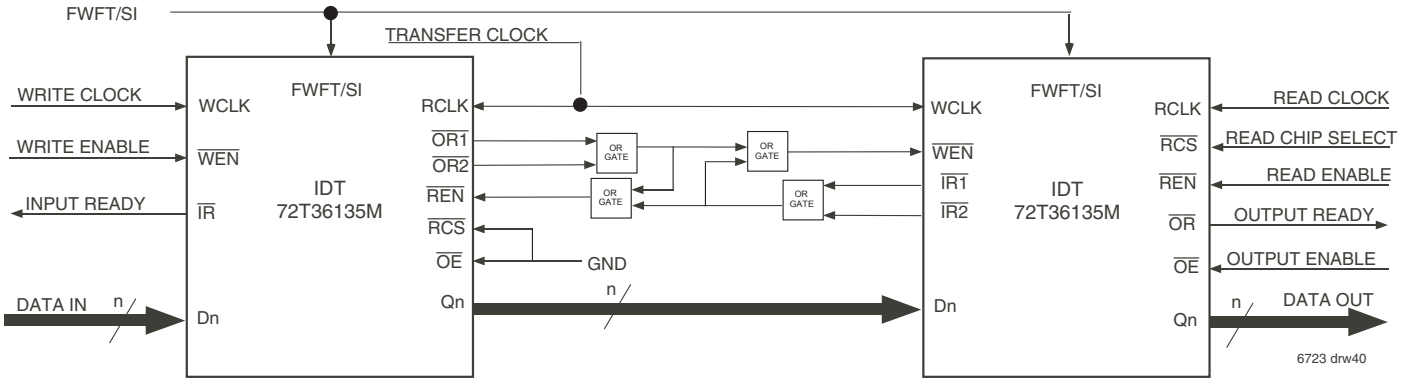


Figure 33. Depth Expansion Option #1

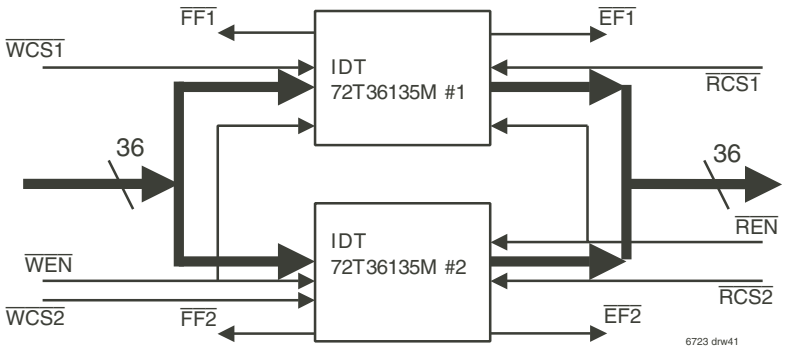
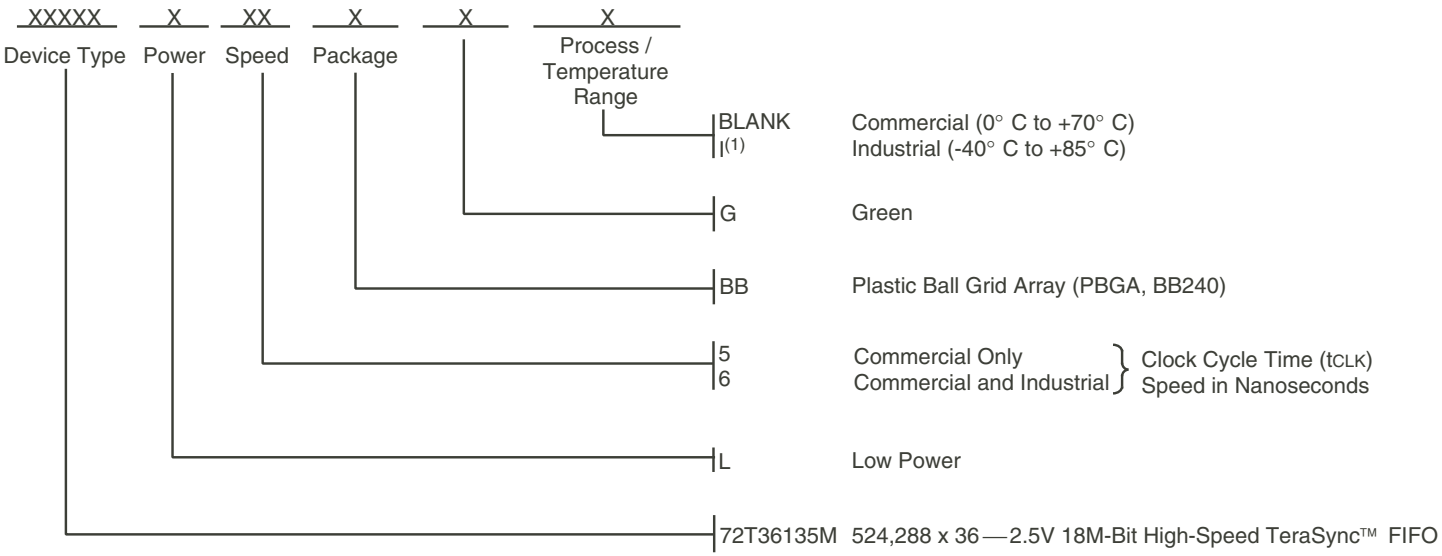


Figure 34. Depth Expansion Option #2

ORDERING INFORMATION



6723 drw42

NOTES:
1. Industrial temperature range product for 6ns speed grade is available as a standard device. All other speed grades are available by special order.
2. Green parts are available. For specific speeds and packages please contact your sales office.

DATASHEET DOCUMENT HISTORY

09/01/2005	pg. 1.
02/28/2006	pg. 10.
05/29/2006	pgs. 10, 21, and 23.
02/04/2009	pg. 48.
05/10/2016	pgs. 2, 3, 4, 7, 9, 19, 24, 46, 47, and 48

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