

FEATURES:

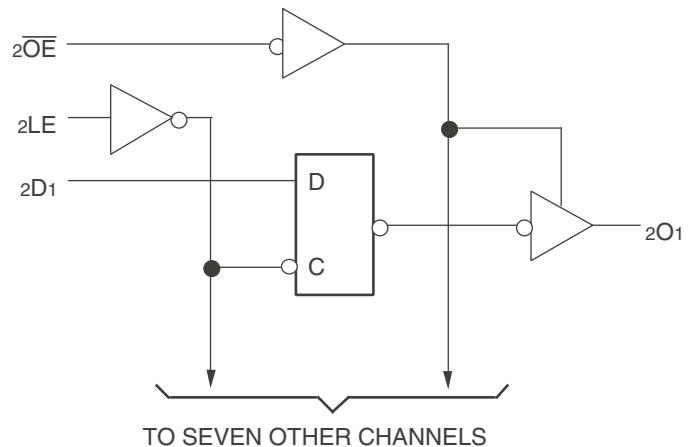
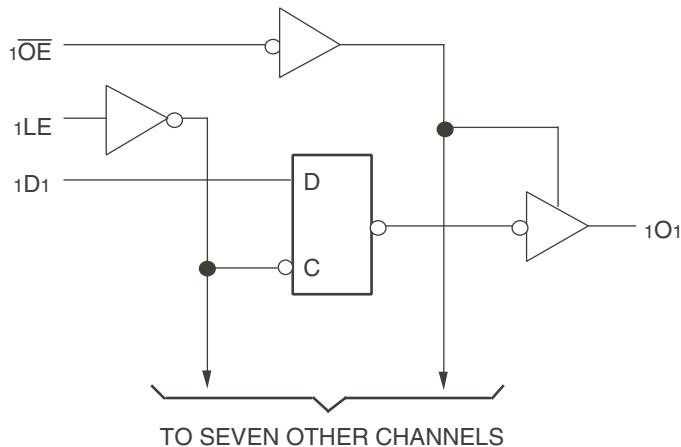
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- $V_{CC} = 5V \pm 10\%$
- Balanced Output Drivers: $\pm 24\text{mA}$
- Reduced system switching noise
- Typical VOLP (Output Ground Bounce) < 0.6V at $V_{CC} = 5V$, $TA = 25^\circ\text{C}$
- Available in SSOP and TSSOP packages

DESCRIPTION:

The FCT162373T 16-bit transparent D-type latch is built using advanced dual metal CMOS technology. This high-speed, low-power latch is ideal for temporary storage of data. It can be used for implementing memory address latches, I/O ports, and bus drivers. The Output Enable and Latch Enable controls are organized to operate each device as two 8-bit latches, or one 16-bit latch. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT162373T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors. The FCT162373T is a plug-in replacement for the FCT16373T and ABT16373 for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

1OE	1	48	1LE
1O1	2	47	1D1
1O2	3	46	1D2
GND	4	45	GND
1O3	5	44	1D3
1O4	6	43	1D4
Vcc	7	42	Vcc
1O5	8	41	1D5
1O6	9	40	1D6
GND	10	39	GND
1O7	11	38	1D7
1O8	12	37	1D8
2O1	13	36	2D1
2O2	14	35	2D2
GND	15	34	GND
2O3	16	33	2D3
2O4	17	32	2D4
Vcc	18	31	Vcc
2O5	19	30	2D5
2O6	20	29	2D6
GND	21	28	GND
2O7	22	27	2D7
2O8	23	26	2D8
2OE	24	25	2LE

SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +120	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXX Output and I/O terminals.
- Output and I/O terminals terminals for FCT162XXX.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6	pF
COUT	Output Capacitance	VOUT = 0V	3.5	8	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xLE	Latch Enable Input (Active HIGH)
xOE	Outputs Enable Input (Active LOW)
xOx	3-State Outputs

FUNCTION TABLE⁽¹⁾

Inputs			Outputs
xDx	xLE	xOE	xOx
H	H	L	H
L	H	L	L
X	X	H	Z

NOTE:

- H = HIGH Voltage Level
- X = Don't Care
- L = LOW Voltage Level
- Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $TA = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	± 1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{IL}	Input LOW Current (Input pins) ⁽⁵⁾		$V_I = \text{GND}$	—	—	± 1	μA
	Input LOW Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{OZH}	High Impedance Output Current	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}	(3-State Output pins) ⁽⁵⁾		$V_O = 0.5\text{V}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}$, $V_O = \text{GND}$ ⁽³⁾		-80	-140	-250	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND or } V_{CC}$		—	5	500	μA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_O = 1.5\text{V}$ ⁽³⁾		60	115	200	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_O = 1.5\text{V}$ ⁽³⁾		-60	-115	-200	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -24\text{mA}$	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 24\text{mA}$	—	0.3	0.55	V

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is $\pm 5\mu\text{A}$ at $TA = -55^{\circ}\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open $x\bar{O}E$ = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	60	100	$\mu A/$ MHz
I_C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $x\bar{O}E$ = GND xLE = V _{CC} One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND	—	0.6	1.5	mA
		V _{IN} = 3.4V V _{IN} = GND	—	0.9	2.3		
		V _{IN} = V _{CC} V _{IN} = GND	—	2.4	4.5 ⁽⁵⁾		
		V _{IN} = 3.4V V _{IN} = GND	—	6.4	16.5 ⁽⁵⁾		

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at V_{CC} = 5.0V, +25°C ambient.

3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.

6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$$I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current (I_{CC1}, I_{CC2} and I_{CC3})

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

N_{CP} = Number of Clock Inputs at f_{CP}

f_i = Input Frequency

N_i = Number of Inputs at f_i

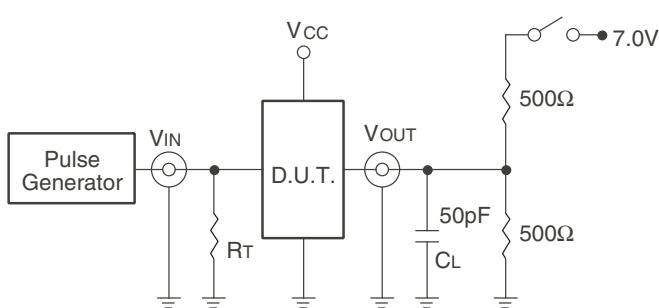
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	74FCT162373AT		74FCT162373CT		74FCT162373ET		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t_{PLH}	Propagation Delay xDx to xOx	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	5.2	1.5	4.2	1.5	3.4	ns
t_{PHL}	Propagation Delay xLE to xOx		2	8.5	2	5.5	1.5	3.7	ns
t_{PZL}	Output Enable Time		1.5	6.5	1.5	5.5	1.5	4.4	ns
t_{PZH}	Output Disable Time		1.5	5.5	1.5	5	1.5	3.6	ns
t_{SU}	Set-up Time HIGH or LOW, xDx to xLE		2	—	2	—	1	—	ns
t_H	Hold Time HIGH or LOW, xDx to xLE		1.5	—	1.5	—	1	—	ns
t_W	xLE Pulse Width HIGH		5	—	5	—	3 ⁽⁴⁾	—	ns
$t_{SK(o)}$	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	ns

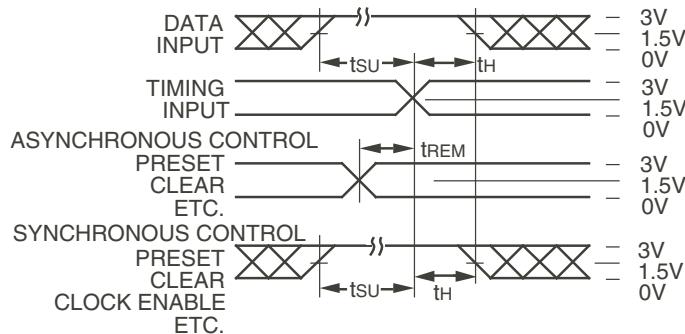
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.

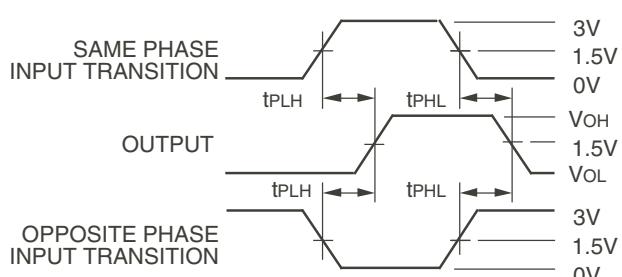
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-up, Hold, and Release Times



Propagation Delay

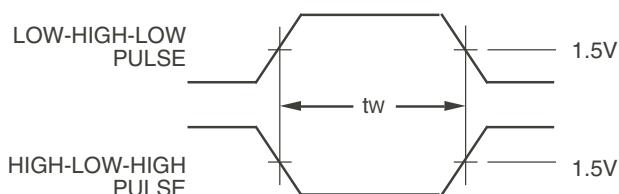
SWITCH POSITION

Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

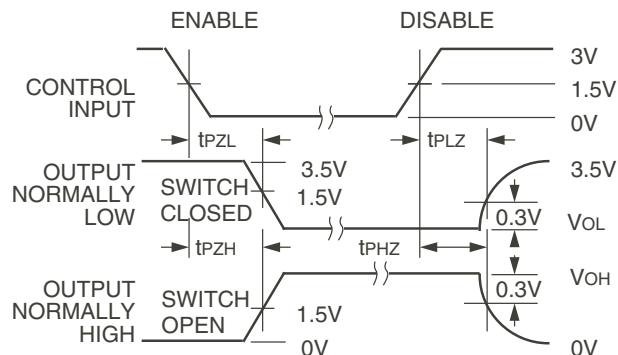
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

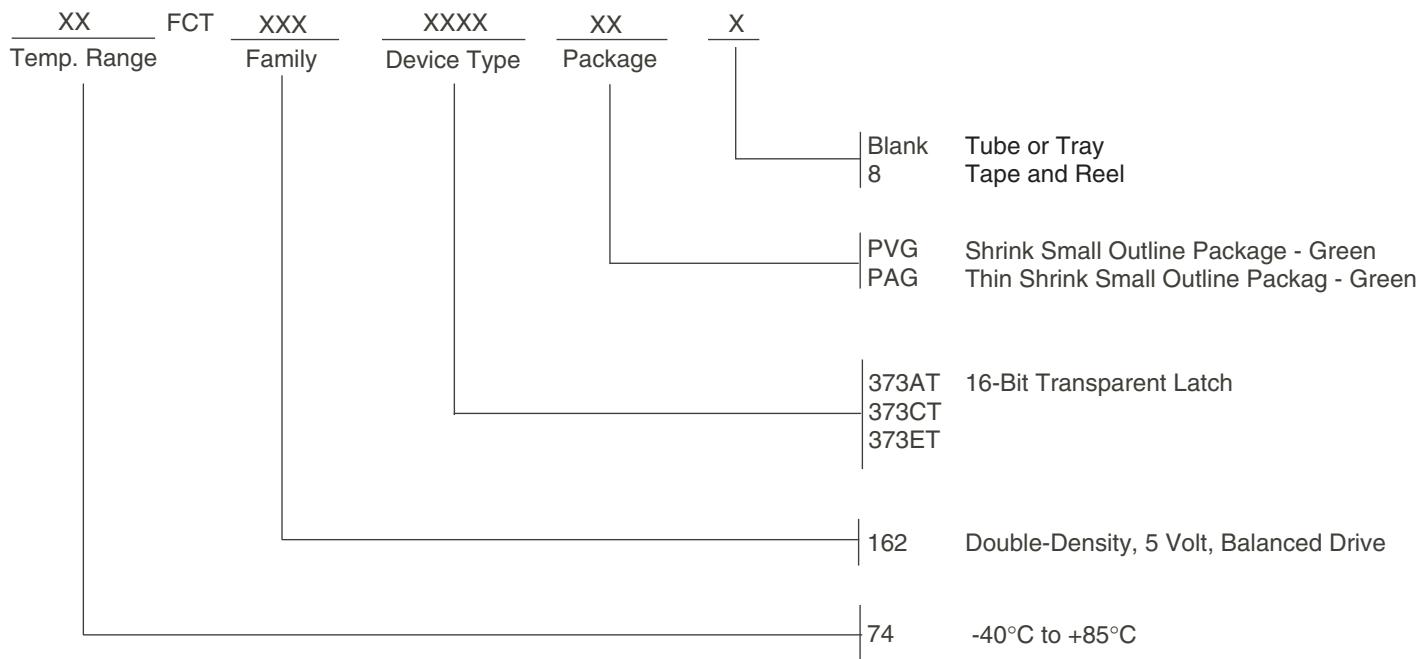


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate \leq 1.0MHz; $t_f \leq 2.5$ ns; $t_r \leq 2.5$ ns.

ORDERING INFORMATION



Datasheet Document History

09/06/2009	Pg. 7	Updated the ordering information by removing the "IDT" notation and non RoHS part.
03/19/2015	Pg. 7	Added Tape & Reel to the ordering information.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.