

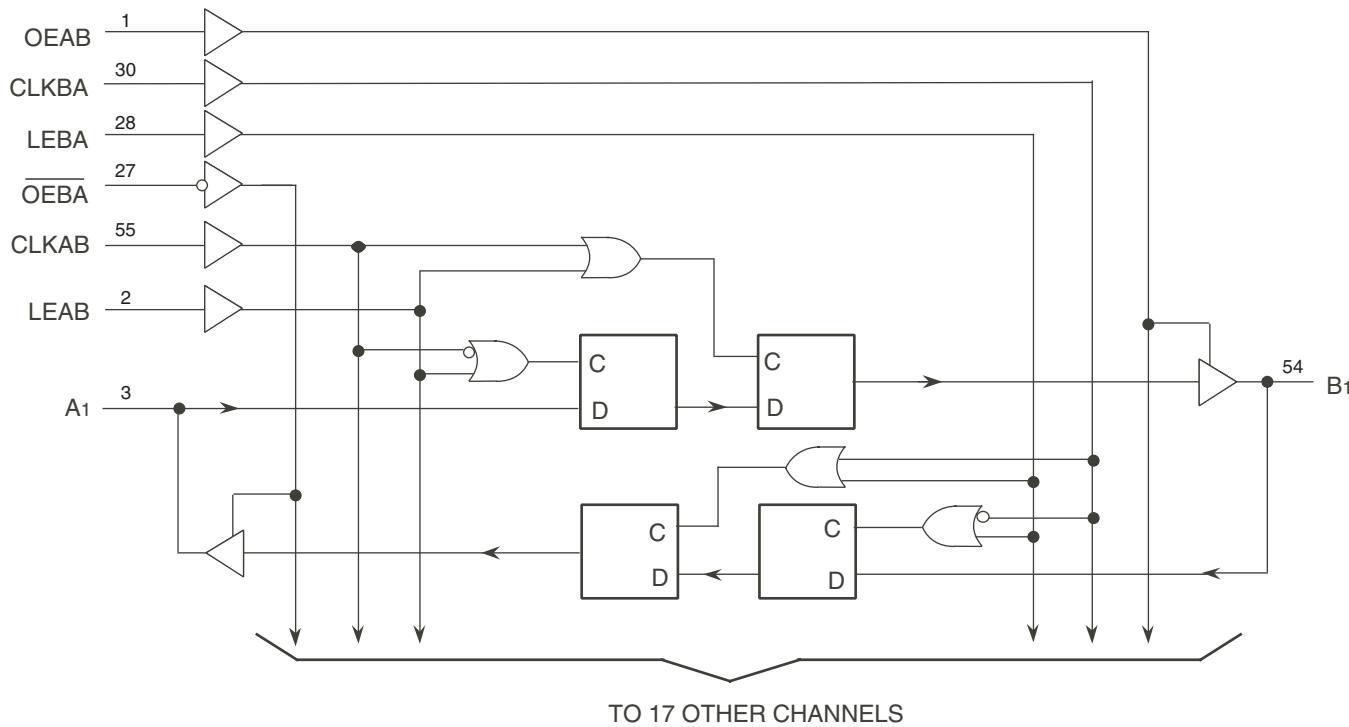
FEATURES:

- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Balanced Output Drivers ($\pm 24\text{mA}$)
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) < 0.6V at $\text{V}_{CC} = 5\text{V}$, $\text{TA} = 25^\circ\text{C}$
- Available in SSOP and TSSOP packages

DESCRIPTION:

The FCT162501T 18-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power 18-bit registered bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes. Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch enable (LEAB and LEBA) and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in transparent mode when LEAB is high. When LEAB is low, the A bus data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB . OEAB is the output enable for the B port. Data flow from the B port to the A port is similar but requires using $\overline{\text{OEBA}}$, LEBA and CLKBA . Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT162501T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors. The FCT162501T is a plug-in replacement for the FCT16501T and ABT16501 for on-board bus interface applications.

FUNCTIONAL BLOCK DIAGRAM

PIN CONFIGURATION

OEAB	1	56	GND
LEAB	2	55	CLKAB
A1	3	54	B1
GND	4	53	GND
A2	5	52	B2
A3	6	51	B3
Vcc	7	50	VCC
A4	8	49	B4
A5	9	48	B5
A6	10	47	B6
GND	11	46	GND
A7	12	45	B7
A8	13	44	B8
A9	14	43	B9
A10	15	42	B10
A11	16	41	B11
A12	17	40	B12
GND	18	39	GND
A13	19	38	B13
A14	20	37	B14
A15	21	36	B15
Vcc	22	35	VCC
A16	23	34	B16
A17	24	33	B17
GND	25	32	GND
A18	26	31	B18
OEBA	27	30	CLKBA
LEBA	28	29	GND

SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to 7	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	V
TSTG	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXX Output and I/O terminals.
3. Output and I/O terminals for FCT162XXX.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	3.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	3.5	8	pF

NOTE:

1. This parameter is measured at characterization but not tested.

FUNCTION TABLE^(1,4)

Inputs				Outputs
OEAB	LEAB	CLKAB	A _x	B _x
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B ⁽²⁾
H	L	H	X	B ⁽³⁾

NOTES:

1. A-to-B data flow is shown. B-to-A data flow is similar but uses \overline{OEBA} , \overline{LEBA} , and \overline{CLKBA} .
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
4. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-impedance
↑ = LOW-to-HIGH Transition

PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input
\overline{OEBA}	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A _x	A-to-B Data Inputs or B-to-A 3-State Outputs
B _x	B-to-A Data Inputs or A-to-B 3-State Outputs

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $TA = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	± 1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{IL}	Input LOW Current (Input pins) ⁽⁵⁾		$V_I = \text{GND}$	—	—	± 1	μA
	Input LOW Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{OZH}	High Impedance Output Current	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}	(3-State Output pins) ⁽⁵⁾		$V_O = 0.5\text{V}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}$, $V_O = \text{GND}$ ⁽³⁾		-80	-140	-250	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND or } V_{CC}$		—	5	500	μA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit	
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_O = 1.5\text{V}$ ⁽³⁾		60	115	200	mA	
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_O = 1.5\text{V}$ ⁽³⁾		-60	-115	-200	mA	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -24\text{mA}$		2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 24\text{mA}$		—	0.3	0.55	V

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is $\pm 5\mu\text{A}$ at $TA = -55^{\circ}\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open OEAB = \overline{OEBA} = V _{CC} or GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	75	120	$\mu A/$ MHz
I_C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open $f_{CP} = 10MHz$ (CLKAB) 50% Duty Cycle OEAB = \overline{OEBA} = V _{CC}	V _{IN} = V _{CC} V _{IN} = GND	—	0.8	1.7	mA
		LEAB = GND One Bit Toggling $f_i = 5MHz$ 50% Duty Cycle	V _{IN} = 3.4V V _{IN} = GND	—	1.3	3.2	
		V _{CC} = Max. Outputs Open $f_{CP} = 10MHz$ (CLKAB) 50% Duty Cycle OEAB = \overline{OEBA} = V _{CC}	V _{IN} = V _{CC} V _{IN} = GND	—	3.8	6.5 ⁽⁵⁾	
		LEAB = GND Eighteen Bit Toggling $f_i = 2.5MHz$ 50% Duty Cycle	V _{IN} = 3.4V V _{IN} = GND	—	8.5	20.8 ⁽⁵⁾	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at V_{CC} = 5.0V, +25°C ambient.

3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.

6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$$I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current (I_{CC1}, I_{CC2} and I_{CC3})

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V).

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

N_{CP} = Number of Clock Inputs at f_{CP}

f_i = Input Frequency

N_i = Number of Inputs at f_i

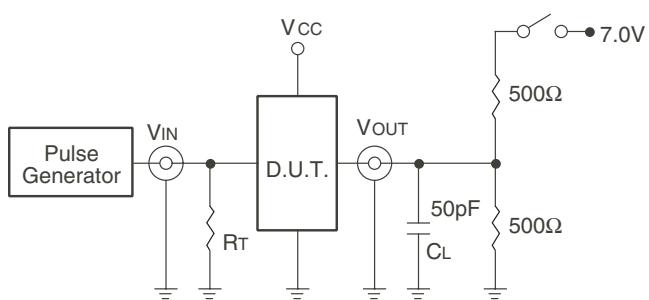
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	74FCT162501AT		74FCT162501CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t_{MAX}	CLKAB or CLKBA frequency ⁽⁴⁾	CL = 50pF RL = 500Ω	—	150	—	150	MHz
t_{PLH}	Propagation Delay Ax to Bx or Bx to Ax		1.5	5.1	1.5	4.3	ns
t_{PHL}	Propagation Delay LEBA to Ax, LEAB to Bx		1.5	5.6	1.5	4.4	ns
t_{PLH}	Propagation Delay CLKBA to Ax, CLKAB to Bx		1.5	5.6	1.5	4.4	ns
t_{PZH}	Output Enable Time OEBA to Ax, OEAB to Bx		1.5	6	1.5	4.8	ns
t_{PLZ}	Output Disable Time OEBA to Ax, OEAB to Bx		1.5	5.6	1.5	5.2	ns
t_{SU}	Set-up Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA		3	—	2.4	—	ns
t_H	Hold Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA		0	—	0	—	ns
t_{SU}	Set-up Time, HIGH or LOW Ax to LEAB, Bx to LEBA	Clock LOW Clock HIGH	3	—	2	—	ns
t_H	Hold Time, HIGH or LOW Ax to LEAB, Bx to LEBA		1.5	—	1.5	—	ns
t_W	LEAB or LEBA Pulse Width HIGH ⁽⁴⁾		1.5	—	0.5	—	ns
t_W	CLKAB or CLKBA Pulse Width HIGH or LOW ⁽⁴⁾		3	—	3	—	ns
$t_{SK(0)}$	Output Skew ⁽³⁾		—	0.5	—	0.5	ns

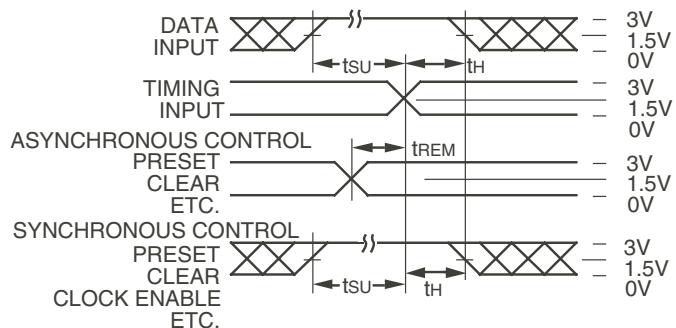
NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.

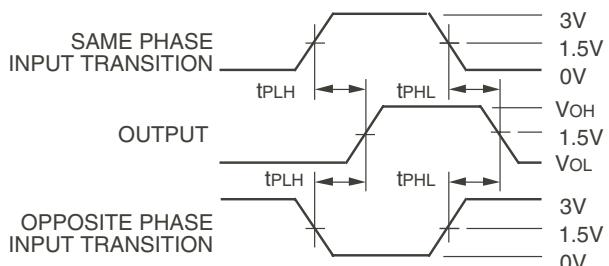
TEST CIRCUITS AND WAVEFORMS



Test Circuits For all Outputs



Set-up, Hold, and Release Times



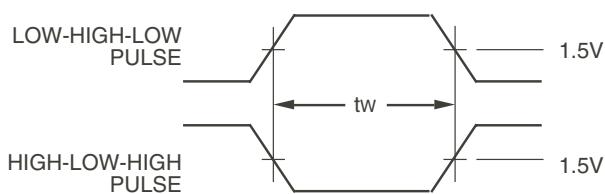
Propagation Delay

SWITCH POSITION

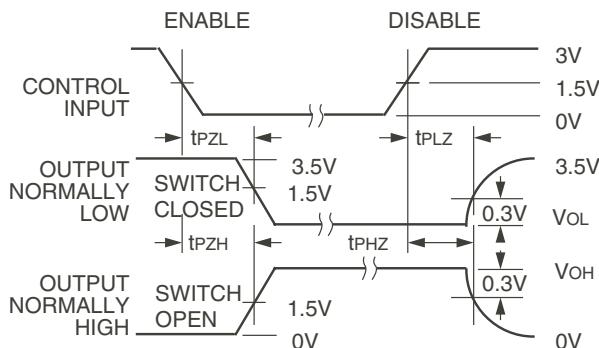
Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width



Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$.

ORDERING INFORMATION

XX	FCT	XXX	XXXX	XX	
Temp. Range		Family	Device Type	Package	
				PVG PAG	Shrink Small Outline Package - Green Thin Shrink Small Outline Package - Green
				501AT 501CT	18-Bit Registered Transceiver
			162		Double-Density, 5 Volt, Balanced Drive
			74		40 C to +85 C

Datasheet Document History

09/06/09 Pg.6 Updated the ordering information by removing the "IDT" notation and non RoHS part.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.