74FCT38072S

DATASHEET

Description

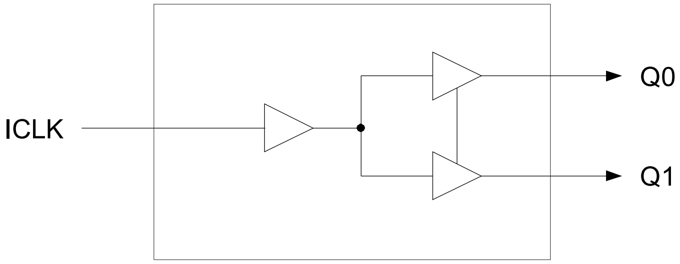
The 74FCT38072S is a low skew, single input to two output, clock buffer. The 74FCT38072S has best in class additive phase Jitter of sub 50 fsec.

Renesas makes many non-PLL and PLL based low skew output devices as well as Zero Delay Buffers to synchronize clocks. Contact us for all of your clocking needs.

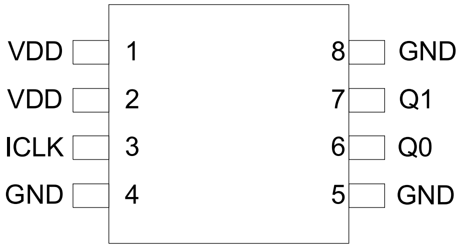
Features

- Low additive phase jitter RMS: 50fs
- Extremely low skew outputs (50ps)
- Low cost clock buffer
- Packaged in 8-pin SOIC and 8-pin DFN, Pb-free
- Input/Output clock frequency up to 200 MHz
- Low power CMOS technology
- Operating voltages of 1.8V to 3.3V
- Extended temperature range (-40° to +105°C)

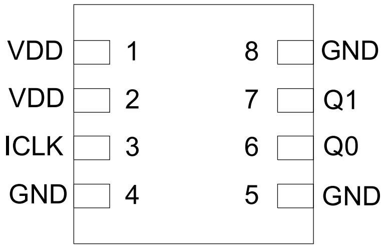
Block Diagram



Pin Assignments



8-pin SOIC



8-pin DFN

Pin Descriptions

Pin Number[1]	Pin Name	Pin Type	Pin Description
1	VDD	Power	Connect to +1.8V, +2.5 V, or +3.3 V.
2	VDD	Power	Connect to +1.8V, +2.5 V, or +3.3 V.
3	ICLK	Input	Clock input.
4	GND	Power	Connect to ground.
5	GND	Power	Connect to ground.
6	Q0	Output	Clock output 0.
7	Q1	Output	Clock output 1.
8	GND	Power	Connect to ground.

[1] VDD on pin 1 and 2 is the same internal signal and must be connected to the same power rail on the PCB.

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01 µF should be connected between VDD pin and GND pin, as close to the device as possible. A 33 Ω series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

To achieve the low output skew that the 74FCT38072S is capable of, careful attention must be paid to board layout. Essentially, both outputs must have identical terminations, identical loads and identical trace geometries. If they do not, the output skew will be degraded. For example, using a 30Ω series termination on one output (with 33Ω on the others) will cause at least 15 ps of skew.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 74FCT38072S. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	3.465V
Outputs	-0.5 V to VDD+0.5 V
ICLK	3.465V
Ambient Operating Temperature (extended)	-40 to +105°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Unit
Ambient Operating Temperature (extended)	-40		+105	°C
Power Supply Voltage (measured in respect to GND)	+1.71		+3.465	V

DC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD=1.8V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Voltage	VDD		1.71		1.89	V
Input High Voltage, ICLK	V_{IH}	Note 1	0.7xVDD		VDD	V
Input Low Voltage, ICLK	V_{IL}	Note 1			0.3xVDD	V
Output High Voltage	V_{OH}	I_{OH} = -10 mA	1.3			V
Output Low Voltage	V_{OL}	I_{OL} = 10mA			0.35	V
Operating Supply Current	IDD	No load, 135 MHz		15		mA
Nominal Output Impedance	Z_O			17		Ω
Input Capacitance	C_{IN}	ICLK		5		pF

Notes: 1. Nominal switching threshold is VDD/2

VDD=2.5 V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Voltage	VDD		2.375		2.625	V
Input High Voltage, ICLK	V_{IH}	Note 1	0.7xVDD		VDD	V
Input Low Voltage, ICLK	V_{IL}	Note 1			0.3xVDD	V
Output High Voltage	V_{OH}	I_{OH} = -16 mA	1.8			V
Output Low Voltage	V_{OL}	I_{OL} = 16 mA			0.5	V
Operating Supply Current	IDD	No load, 135 MHz		18		mA
Nominal Output Impedance	Z_O			17		Ω
Input Capacitance	C_{IN}	ICLK		5		pF

VDD=3.3 V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Voltage	VDD		3.15		3.45	V
Input High Voltage, ICLK	V_{IH}	Note 1	0.7xVDD		VDD	V
Input Low Voltage, ICLK	V_{IL}	Note 1			0.3xVDD	V
Output High Voltage	V_{OH}	I_{OH} = -25 mA	2.2			V
Output Low Voltage	V_{OL}	I_{OL} = 25 mA			0.7	V
Operating Supply Current	IDD	No load, 135 MHz		22		mA
Nominal Output Impedance	Z_O			17		Ω
Input Capacitance	C_{IN}	ICLK		5		pF

AC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD = 1.8V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.36 to 1.44 V, C_L=5 pF		0.6	1.0	ns
Output Fall Time	t_{OF}	1.44 to 0.36 V, C_L=5 pF		0.6	1.0	ns
Start-up Time	$t_{START\text{-}UP}$	Part start-up time for valid outputs after VDD ramp-up			2	ms
Propagation Delay		Note 1	1.5	2.5	4	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew		Rising edges at VDD/2, Note 2		50	65	ps
Device to Device Skew		Rising edges at VDD/2			200	ps

VDD = 2.5 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

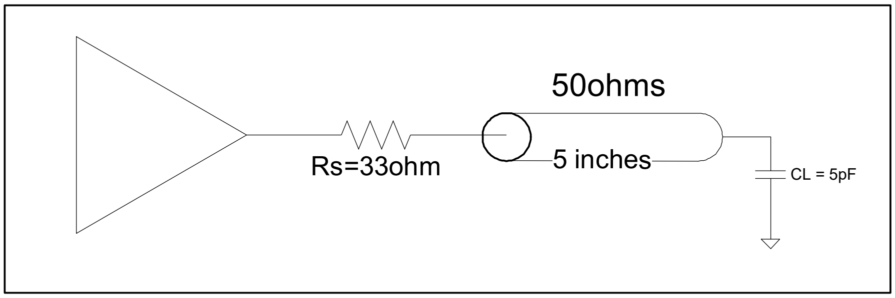
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.5 to 2.0 V, C_L=5 pF		0.6	1.0	ns
Output Fall Time	t_{OF}	2.0 to 0.5 V, C_L=5 pF		0.6	1.0	ns
Start-up Time	$t_{START\text{-}UP}$	Part start-up time for valid outputs after VDD ramp-up			2	ms
Propagation Delay		Note 1	1.8	2.5	4.5	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew		Rising edges at VDD/2, Note 2		50	65	ps
Device to Device Skew		Rising edges at VDD/2			200	ps

VDD = 3.3 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.66 to 2.64 V, C_L=5 pF		0.6	1.0	ns
Output Fall Time	t_{OF}	2.64 to 0.66 V, C_L=5 pF		0.6	1.0	ns
Start-up Time	$t_{START\text{-}UP}$	Part start-up time for valid outputs after VDD ramp-up			2	ms
Propagation Delay		Note 1	1.5	2.5	4	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew		Rising edges at VDD/2, Note 2		50	65	ps
Device to Device Skew		Rising edges at VDD/2			200	ps

Notes:
1. With rail to rail input clock
2. Between any 2 outputs with equal loading.
3. Duty cycle on outputs will match incoming clock duty cycle. Consult Renesas for tight duty cycle clock generators.

Test Load and Circuit



Thermal Characteristics

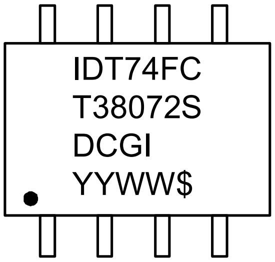
8SOIC

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

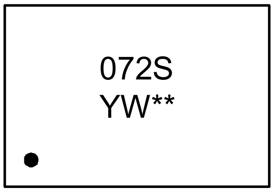
8DFN

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		140.7		°C/W
	θ_{JA}	1 m/s air flow		136.5		°C/W
	θ_{JA}	2 m/s air flow		133.3		°C/W
	θ_{JA}	3 m/s air flow		131.4		°C/W
Thermal Resistance Junction to Board	θ_{JB}			93.8		°C/W
Thermal Resistance Junction to Case	θ_{JC}			64.5		°C/W

Marking Diagrams



8-pin SOIC



8-pin DFN

Notes:
1. “**” is the lot number.
2. “YYWW” or “YW” are the last digits of the year and week that the part was assembled.
3 “G” denotes RoHS compliant package.
4. “$” denotes the mark code.
5. “I” denotes extended temperature range device.

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the links in the Ordering section. The package information is the most current data available.

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
74FCT38072SDCGI	see page 6	Tubes	8-pin SOIC (8-SOIC)	-40 to +105 °C
74FCT38072SDCGI8		Tape and Reel	8-pin SOIC (8-SOIC)	-40 to +105 °C
74FCT38072SCMGI		Cut Tape	8-pin DFN (8-DFN)	-40 to +105 °C
74FCT38072SCMGI8		Tape and Reel	8-pin DFN (8-DFN)	-40 to +105 °C

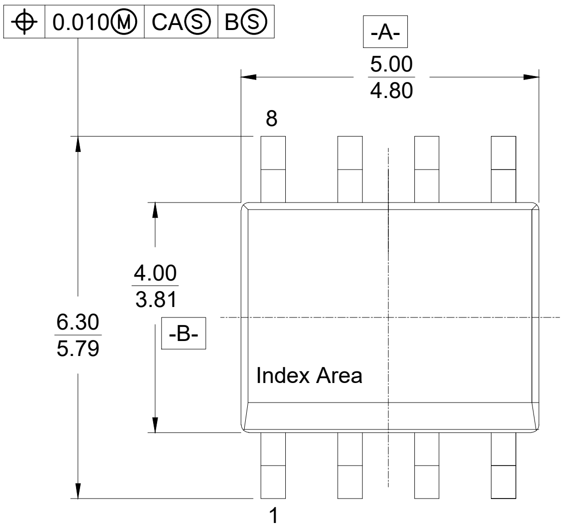
“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Revision History

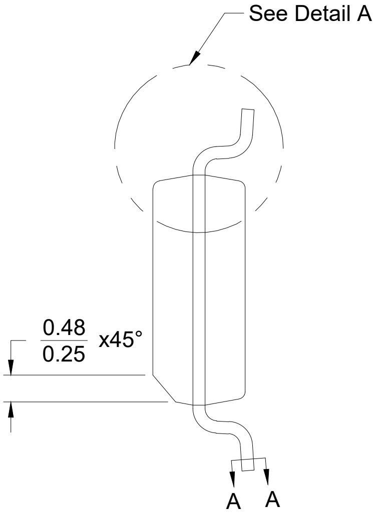
Revision Date	Description of Change
Jun 5, 2025	• Added Thermal Characteristics for the 8-DFN package. • Added a link to the 8-DFN package in Ordering Information.
February 3, 2023	Updated POD link in Package Outline Drawings.
May 4, 2020	• Added a footnote to Pin Descriptions • Updated the Package Outline Drawings; however, no technical changes were made
March 18, 2015	Initial release.

Package Outline Drawing

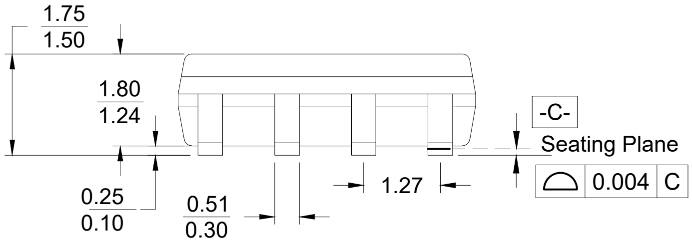
Package Code: DCG8D1
8-SOIC 4.82 x 3.81 x 1.72 mm Body, 1.27mm Pitch
PSC-4068-01, Revision: 02, Date Created: Jun 21, 2022



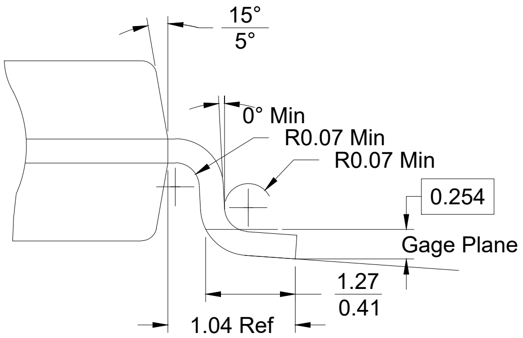
Top View



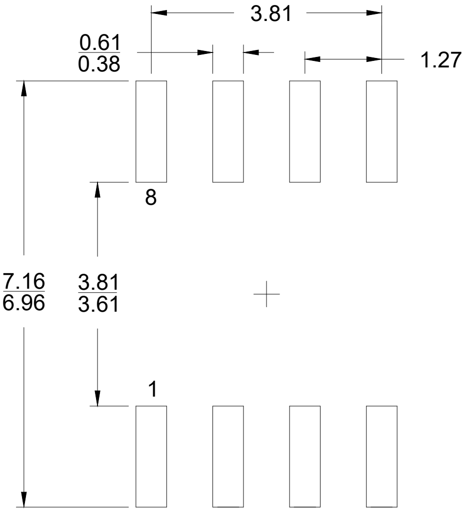
Side View



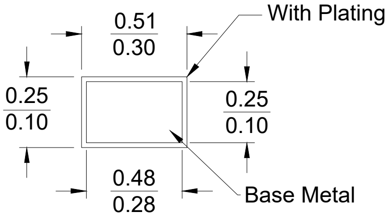
Side View



Detail A
(Rotated 90° CW)



RECOMMENDED LAND PATTERN
(PCB Top View, SMD Design)



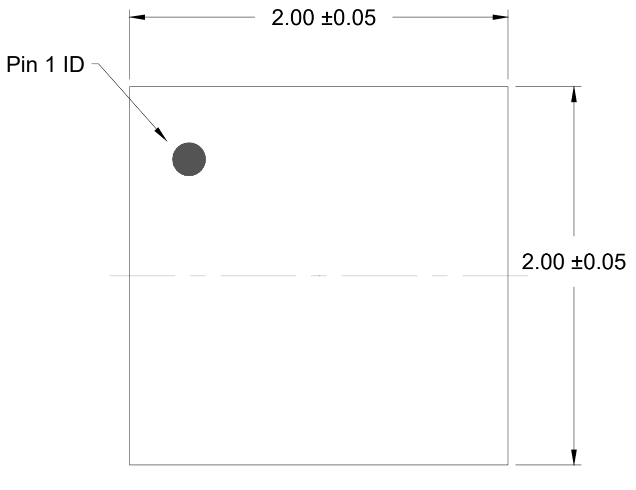
Section A-A

NOTES:

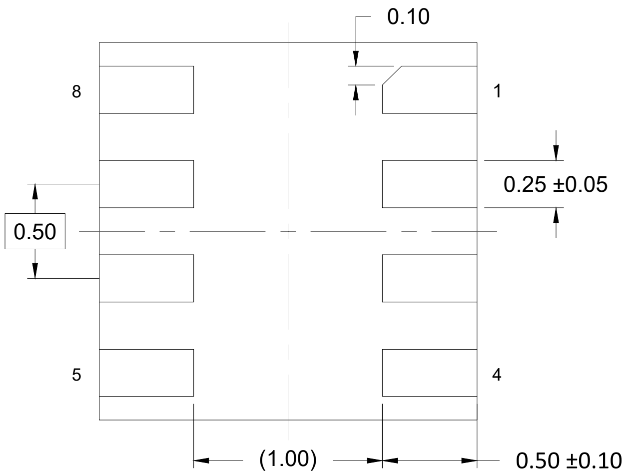
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Foot length is measured at gauge plane 0.25 mm above seating plane.

Package Outline Drawing

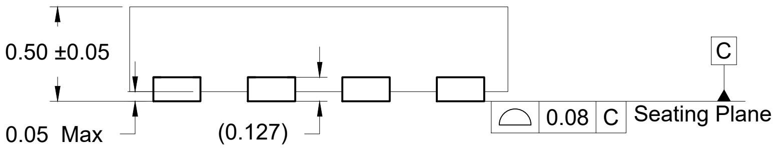
Package Code:CMG8D1
8-DFN 2.0 x 2.0 x 0.5 mm Body, 0.5mm Pitch
PSC-4490-01, Revision: 00, Date Created: Oct 05, 2023



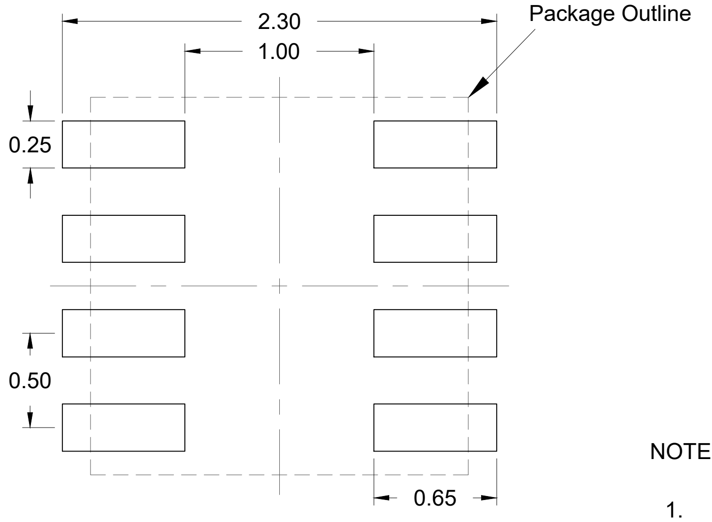
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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